19-3289; Rev 1; 6/05

EVALUATION KIT AVAILABLE

3V to 28V Input, Low-Cost, Hysteretic Synchronous Step-Down Controllers

General Description

The MAX8576–MAX8579 synchronous PWM buck controllers use a hysteretic voltage-mode control algorithm to achieve a fast transient response without requiring loop compensation. The MAX8576/MAX8577 contain an internal LDO regulator allowing the controllers to function from only one 3V to 28V input supply. The MAX8578/MAX8579 do not contain the internal LDO and require a separate supply to power the IC when the input supply is higher than 5.5V. The MAX8576–MAX8579 output voltages are adjustable from 0.6V to 0.9 x V_{IN} at loads up to 15A.

Nominal switching frequency is programmable over the 200kHz to 500kHz range. High-side MOSFET sensing is used for adjustable hiccup current-limit and short-circuit protection. The MAX8576/MAX8578 can start up into a precharged output without pulling the output voltage down. The MAX8577/MAX8579 have startup output overvoltage protection (OVP), and will pull down a precharged output.

Applications

Motherboard Power Supplies

AGP and PCI-Express Power Supplies

Graphic-Card Power Supplies

Set-Top Boxes

Point-of-Load Power Supplies

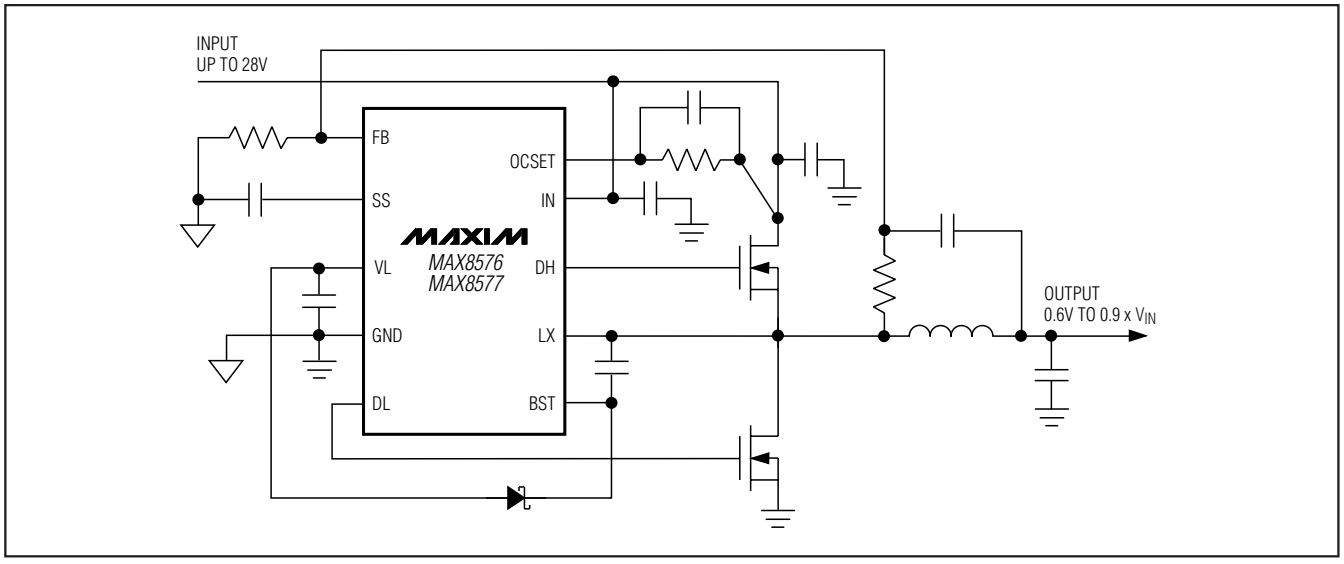
Features

- **3V to 28V Supply Voltage Range**
- **1.2% Accurate Over Temperature**
- **Adjustable Output Voltage Down to 0.6V**
- **200kHz to 500kHz Switching Frequency**
- **Adjustable Temperature-Compensated Hiccup Current Limit**
- **Lossless Peak Current Sensing**
- **Monotonic Startup into Prebias Output (MAX8576/MAX8578)**
- **Startup Overvoltage Protection (MAX8577/MAX8579)**
- **Enable/Shutdown**
- **Adjustable Soft-Start**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8576EUB	-40°C to +85°C	10 µMAX®
MAX8577EUB	-40°C to +85°C	10 µMAX
MAX8578EUB	-40°C to +85°C	10 µMAX
MAX8579EUB	-40°C to +85°C	10 µMAX

Typical Operating Circuit



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Pin Configurations appear at end of data sheet.

3V to 28V Input, Low-Cost, Hysteretic Synchronous Step-Down Controllers

ABSOLUTE MAXIMUM RATINGS

IN to GND (MAX8576/MAX8577) .....-0.3V to +30V
VL to GND (MAX8576/MAX8577).....-0.3V to +6V
IN to VL (MAX8576/MAX8577) .....-0.3V to +30V
V_{CC} to GND (MAX8578/MAX8579) .....-0.3V to +6V
SS to GND (MAX8576/MAX8577) .....-0.3V to (V_{VL} + 0.3)V
SS to GND (MAX8578/MAX8579).....-0.3V to (V_{CC} + 0.3)V
DL to GND (MAX8576/MAX8577) .....-0.3V to (V_{VL} + 0.3)V
DL to GND (MAX8578/MAX8579) .....-0.3V to (V_{CC} + 0.3)V
BST to GND.....-0.3V to +36V
BST to LX.....-0.3V to +6V
LX to GND .....-1V (-2.5V for <50ns Transient) to +30V
DH to LX.....-0.3V to +(V_{BST} + 0.3)V
FB to GND .....-0.3V to +6V
EN to GND (MAX8578/MAX8679EUB).....-0.3V to +6V
OCSET to GND (MAX8576/MAX8677) .....-0.3V to (V_{IN} + 0.3)V
OCSET to GND (MAX8578/MAX8679) .....-0.3V to +30V
OCSET to LX (MAX8576/MAX8677) .....-0.6V to (V_{IN} + 0.3)V
OCSET to LX (MAX8578/MAX8679).....-0.6V to +30V
DH and DL Continuous Current .....±250mA RMS
Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C).....444mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V (MAX8576/MAX8577 only), 4.7µF capacitor from VL (MAX8576/MAX8577 only) or V_{CC} (MAX8578/MAX8579 only) to GND; V_{CC} = V_{EN} = 5V (MAX8578/MAX8579 only); 0.01µF capacitor from SS to GND; V_{FB} = 0.65V; V_{BST} = 5V; V_{LX} = V_{GND} = 0V; V_{OCSET} = 11.5V; DH = unconnected; DL = unconnected; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY VOLTAGES						
IN Supply Voltage	MAX8576/MAX8577		5.5		28.0	V
	IN = VL (MAX8576/MAX8577)		3.0		5.5	
V_{CC} Input Voltage	MAX8576/MAX8577		3.0		5.5	V
VL Output Voltage	I_{VL} = 10mA (MAX8576/MAX8577)		4.75	5.0	5.25	V
VL Maximum Output Current	MAX8576/MAX8577		20			mA
VL or V_{CC} Undervoltage Lockout (UVLO)	Rising		2.75	2.8	2.90	V
	Falling		2.4	2.45	2.5	
	Hysteresis			350		mV
Supply Current	No switching, V_{FB} = 0.65V (MAX8576/MAX8577)	V_{IN} = 12V		0.6	2	mA
		V_{IN} = V_{VL} = 5V		1.1	3	
		V_{IN} = V_{VL} = 3.3V		0.6	2	
	V_{EN} = 0V or V_{FB} = 0.65V, no switching (MAX8578/MAX8579)	V_{CC} = 5V		0.6	2	
		V_{CC} = 3.3V		0.6	2	
REGULATOR						
Output Regulation Accuracy	V_{FB} peak		0.593	0.6	0.607	V
Output Regulation Hysteresis	(Note 1)		12.5	20	28.0	mV
FB Propagation Delay	FB falling to DL falling			50		ns
	FB rising to DH falling			70		
Overvoltage-Protection (OVP) Threshold			0.70	0.75	0.80	V
High-Side Current-Sense Program Current (Note 2)	T_A = +85°C			60		µA
	T_A = +25°C		42.5	50	57.5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V (MAX8576/MAX8577 only), 4.7µF capacitor from VL (MAX8576/MAX8577 only) or V_{CC} (MAX8578/MAX8579 only) to GND; V_{CC} = V_{EN} = 5V (MAX8578/MAX8579 only); 0.01µF capacitor from SS to GND; V_{FB} = 0.65V; V_{BST} = 5V; V_{LX} = V_{GND} = 0V; V_{OCSET} = 11.5V; DH = unconnected; DL = unconnected; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High-Side Current-Sense Overcurrent Trip Adjustment Range	V_{IN} - V_{OCSET}	0.05		0.40	V
Soft-Start Internal Resistance		45	80	125	kΩ
Fault Hiccup Internal SS Pulldown Current	V_{LX} < V_{OCSET} and V_{FB} < V_{SS}		250		nA
DRIVER SPECIFICATIONS					
DH Driver Resistance	Sourcing current		2.6	4.0	Ω
	Sinking current		1.9	3.0	
DL Driver Resistance	Sourcing current		2.6	4.0	Ω
	Sinking current		1.1	2.0	
Dead Time	DH low to DL high and DL low to DH high (adaptive)		40		ns
DH Minimum On-Time			140	245	ns
DL Minimum On-Time	Normal operation		120	220	ns
	Current fault		580		
BST Current	V_{BST} - V_{LX} = 5.5V, V_{LX} = 28V, V_{FB} < V_{SS}		1.65		mA
EN					
Input Voltage Low	V_{CC} = 3V (MAX8578/MAX8579)			0.7	V
Input Voltage High	V_{CC} = 5.5V (MAX8578/MAX8579)	1.5			V
THERMAL SHUTDOWN					
Thermal Shutdown	Rising temperature, hysteresis = 20°C (typ)		+160		°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V (MAX8576/MAX8577 only), 4.7µF capacitor from VL (MAX8576/MAX8577 only) or V_{CC} (MAX8578/MAX8579 only) to GND; V_{CC} = V_{EN} = 5V (MAX8578/MAX8579 only); 0.01µF capacitor from SS to GND; V_{FB} = 0.65V; V_{BST} = 5V; V_{LX} = V_{GND} = 0V; V_{OCSET} = 11.5V; DH = unconnected; DL = unconnected; **T_A = -40°C to +85°C**, unless otherwise noted. Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGES					
IN Supply Voltage	MAX8576/MAX8577	5.5		28.0	V
	IN = VL, MAX8576/MAX8577	3.0		5.5	
V_{CC} Input Voltage	MAX8576/MAX8577	3.0		5.5	V
VL Output Voltage	I_{VL} = 10mA, MAX8576/MAX8577	4.75		5.25	V
VL Maximum Output Current	MAX8576/MAX8577	20			mA

3V to 28V Input, Low-Cost, Hysteretic Synchronous Step-Down Controllers

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V (MAX8576/MAX8577 only), 4.7µF capacitor from VL (MAX8576/MAX8577 only) or V_{CC} (MAX8578/MAX8579 only) to GND; V_{CC} = V_{EN} = 5V (MAX8578/MAX8579 only); 0.01µF capacitor from SS to GND; V_{FB} = 0.65V; V_{BST} = 5V; V_{LX} = V_{GND} = 0V; V_{OCSET} = 11.5V; DH = unconnected; DL = unconnected; **T_A = -40°C to +85°C**, unless otherwise noted. Note 3)

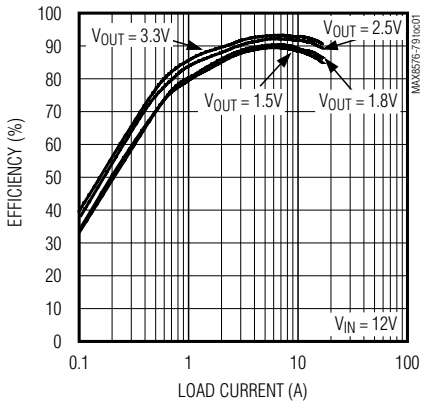
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
VL or V_{CC} Undervoltage Lockout (UVLO)	Rising		2.75		2.90	V
	Falling		2.40		2.55	
Supply Current	No switching, V_{FB} = 0.65V (MAX8576/MAX8577)	V_{IN} = 12V			2	mA
		V_{IN} = V_{VL} = 5V			3.5	
		V_{IN} = V_{VL} = 3.3V			2	
	V_{EN} = 0V or V_{FB} = 0.65V, no switching (MAX8578/MAX8579)	V_{CC} = 5V			2	
		V_{CC} = 3.3V			2	
REGULATOR						
Output Regulation Accuracy	V_{FB} peak		0.591		0.607	V
Overvoltage-Protection (OVP) Threshold			0.70		0.80	V
High-Side Current-Sense Over-Current Trip Adjustment Range	V_{IN} - V_{OCSET}		0.05		0.40	V
DRIVER SPECIFICATIONS						
DH Driver Resistance	Sourcing current				4	Ω
	Sinking current				3.0	
DL Driver Resistance	Sourcing current				4.0	Ω
	Sinking current				2.0	
DH Minimum On-Time					245	ns
DL Minimum On-Time	Normal operation				220	ns
EN						
Input Voltage Low	V_{CC} = 3V, MAX8578/MAX8579				0.7	V
Input Voltage High	V_{CC} = 5.5V, MAX8578/MAX8579		1.5			V

Note 1: Guaranteed by design.
Note 2: This current linearly compensates for the MOSFET temperature coefficient.
Note 3: Specifications to -40°C are guaranteed by design and not production tested.

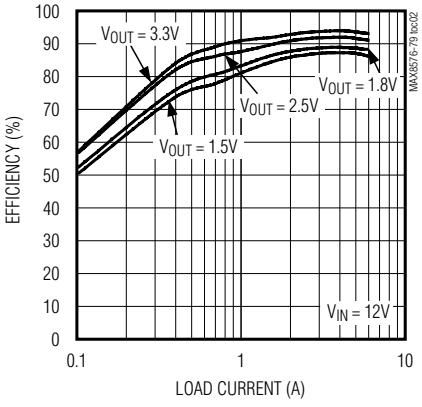
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

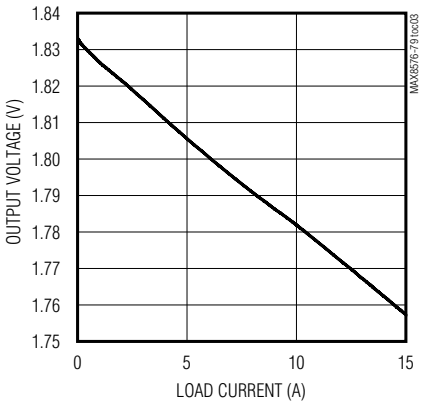
EFFICIENCY vs. LOAD CURRENT (CIRCUIT OF FIGURE 2)



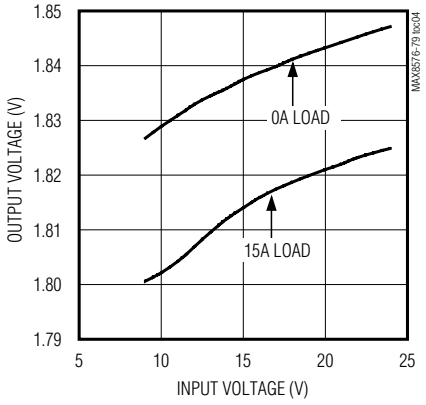
EFFICIENCY vs. LOAD CURRENT (CIRCUIT OF FIGURE 3)



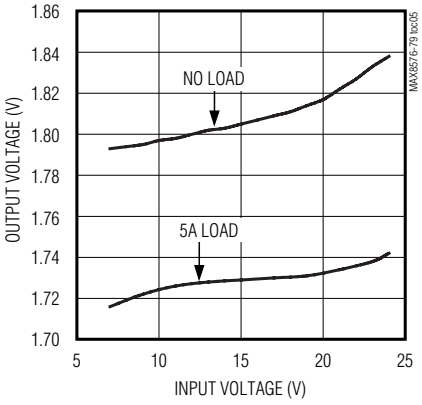
LOAD REGULATION (CIRCUIT OF FIGURE 2)



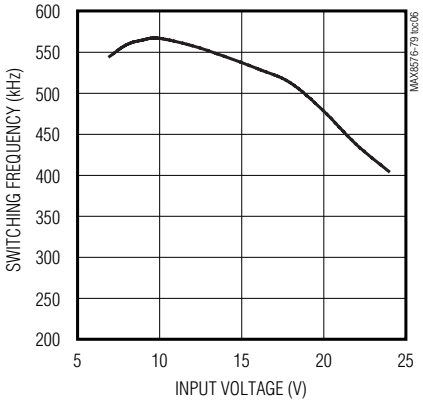
LINE REGULATION (CIRCUIT OF FIGURE 2)



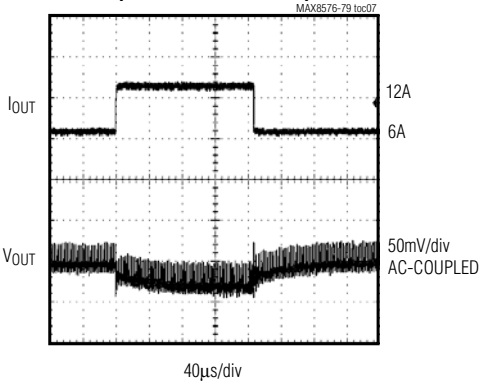
LINE REGULATION (CIRCUIT OF FIGURE 3)



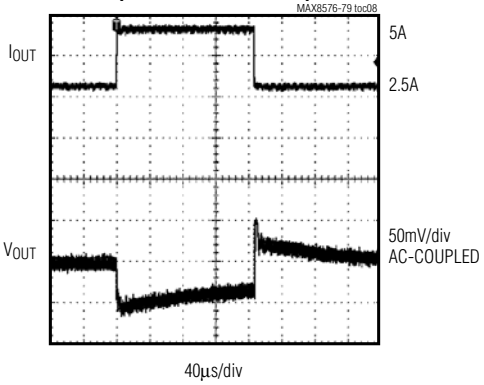
SWITCHING FREQUENCY vs. INPUT VOLTAGE (CIRCUIT OF FIGURE 3)



LOAD TRANSIENT (CIRCUIT OF FIGURE 2)



LOAD TRANSIENT (CIRCUIT OF FIGURE 3)

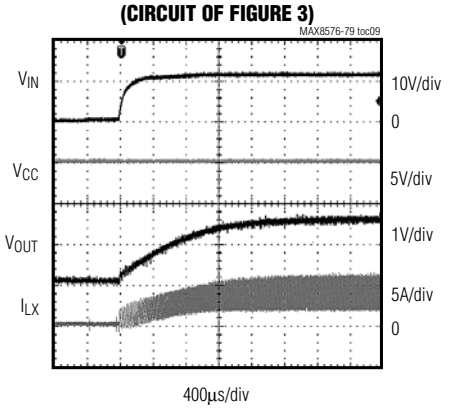


3V to 28V Input, Low-Cost, Hysteretic Synchronous Step-Down Controllers

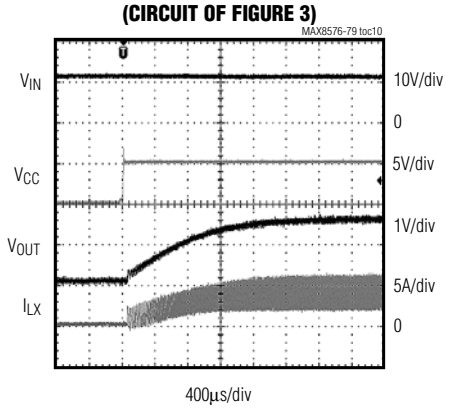
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

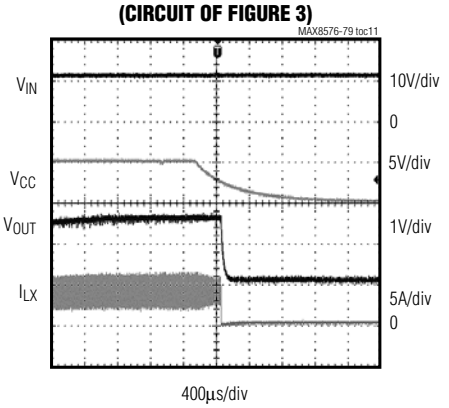
POWER-UP V_{IN} (CIRCUIT OF FIGURE 3)



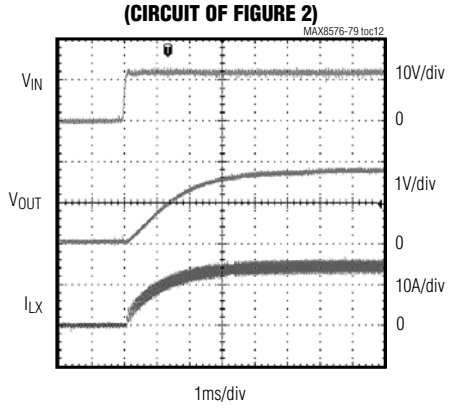
POWER-UP V_{CC} (CIRCUIT OF FIGURE 3)



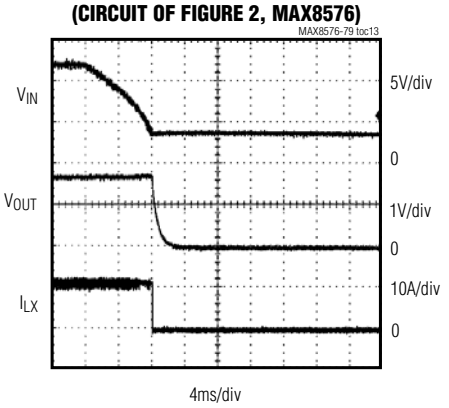
POWER-DOWN V_{CC} (CIRCUIT OF FIGURE 3)



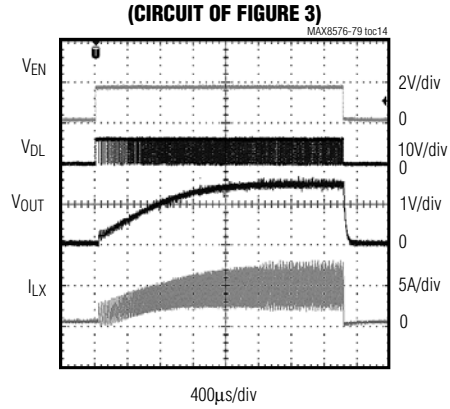
POWER-UP (CIRCUIT OF FIGURE 2)



POWER-DOWN (CIRCUIT OF FIGURE 2, MAX8576)



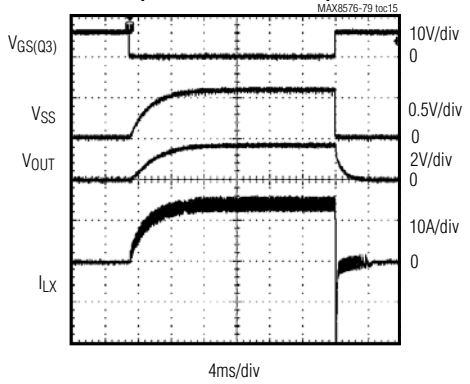
STARTUP AND SHUTDOWN (CIRCUIT OF FIGURE 3)



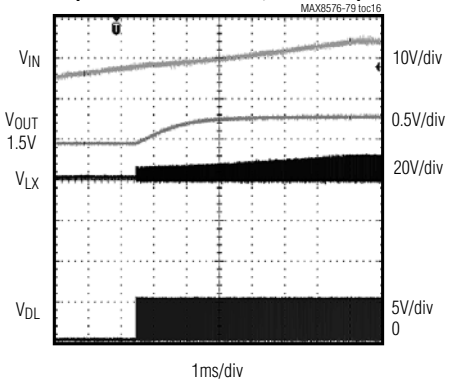
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

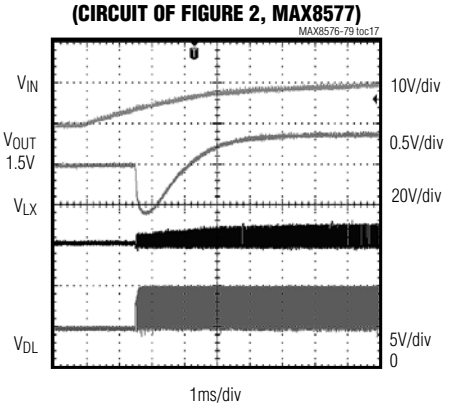
STARTUP AND SHUTDOWN (CIRCUIT OF FIGURE 2)



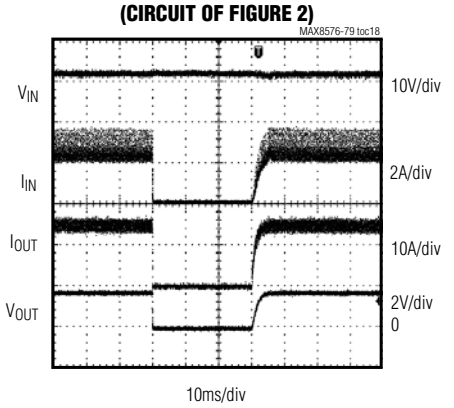
MONOTONIC OUTPUT-VOLTAGE RISE (CIRCUIT OF FIGURE 2, MAX8576)



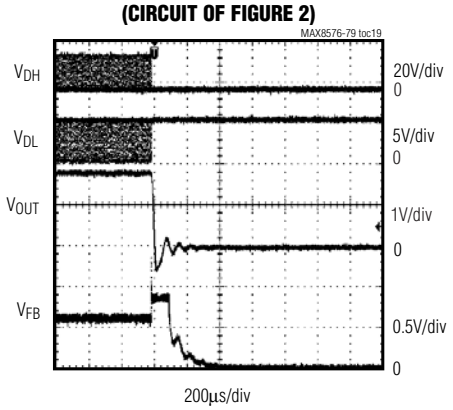
NONMONOTONIC OUTPUT-VOLTAGE RISE (CIRCUIT OF FIGURE 2, MAX8577)



SHORT CIRCUIT AND RECOVERY (CIRCUIT OF FIGURE 2)



OUTPUT OVERVOLTAGE PROTECTION (CIRCUIT OF FIGURE 2)



3V to 28V Input, Low-Cost, Hysteretic Synchronous Step-Down Controllers

Pin Description

PIN		NAME	FUNCTION
MAX8576/ MAX8577	MAX8578/ MAX8579		
1	1	FB	Feedback Input. Regulates at V_{FB} = 0.59V. Connect FB to a resistor-divider to set the output voltage. See the *Setting the Output Voltage* section.
2	2	SS	Soft-Start. Use an external capacitor (C_{SS}) to adjust the soft-start time. An internal 80kΩ resistor gives approximately 4ms soft-start time for a 0.01µF external capacitor. An internal 250nA current sink in hiccup mode gives approximately 10% duty cycle during fault conditions.
3	—	VL	Internal 5V Linear-Regulator Output. Bypass with a 4.7µF or larger ceramic capacitor. Must be connected to IN for operation from a 3.3V to 5.5V input.
—	3	V_{CC}	Supply Input (3V to 5.5V). Bypass with a 4.7µF or larger ceramic capacitor to GND.
4	4	GND	Ground
5	5	DL	Low-Side Gate-Drive Output. Drives the synchronous-rectifier MOSFET.
6	6	BST	Boost-Capacitor Connection for High-Side Gate-Drive Output. Connect a 0.1µF ceramic capacitor from BST to LX and a Schottky or switching diode and a 4.7Ω series resistor from BST to VL (MAX8576/MAX8577) or V_{CC} (MAX8578/MAX8579). See Figure 4.
7	7	LX	External Inductor Connection. Connect LX to the junctions of the MOSFETs and inductor.
8	8	DH	High-Side Gate-Drive Output. Drives the high-side MOSFET.
9	—	IN	Supply Voltage Input of the Internal Linear Regulator (3V to 28V). Connect to VL for operation from 3V to 5.5V input. Connect a 0.47µF or larger ceramic capacitor from IN to GND.
—	9	EN	Enable Input. A logic low on EN shuts down the converter and discharges the soft-start capacitor. Drive high or connect to V_{CC} for normal operation.
10	10	OCSET	Overcurrent-Limit Set. Programs the high-side peak current-limit threshold by setting the maximum-allowed V_{DS} voltage drop across the high-side MOSFET. Connect a resistor from IN to OCSET; an internal 50µA current sink sets the maximum voltage drop relative to V_{IN}. See the *Setting the Current Limit* section.

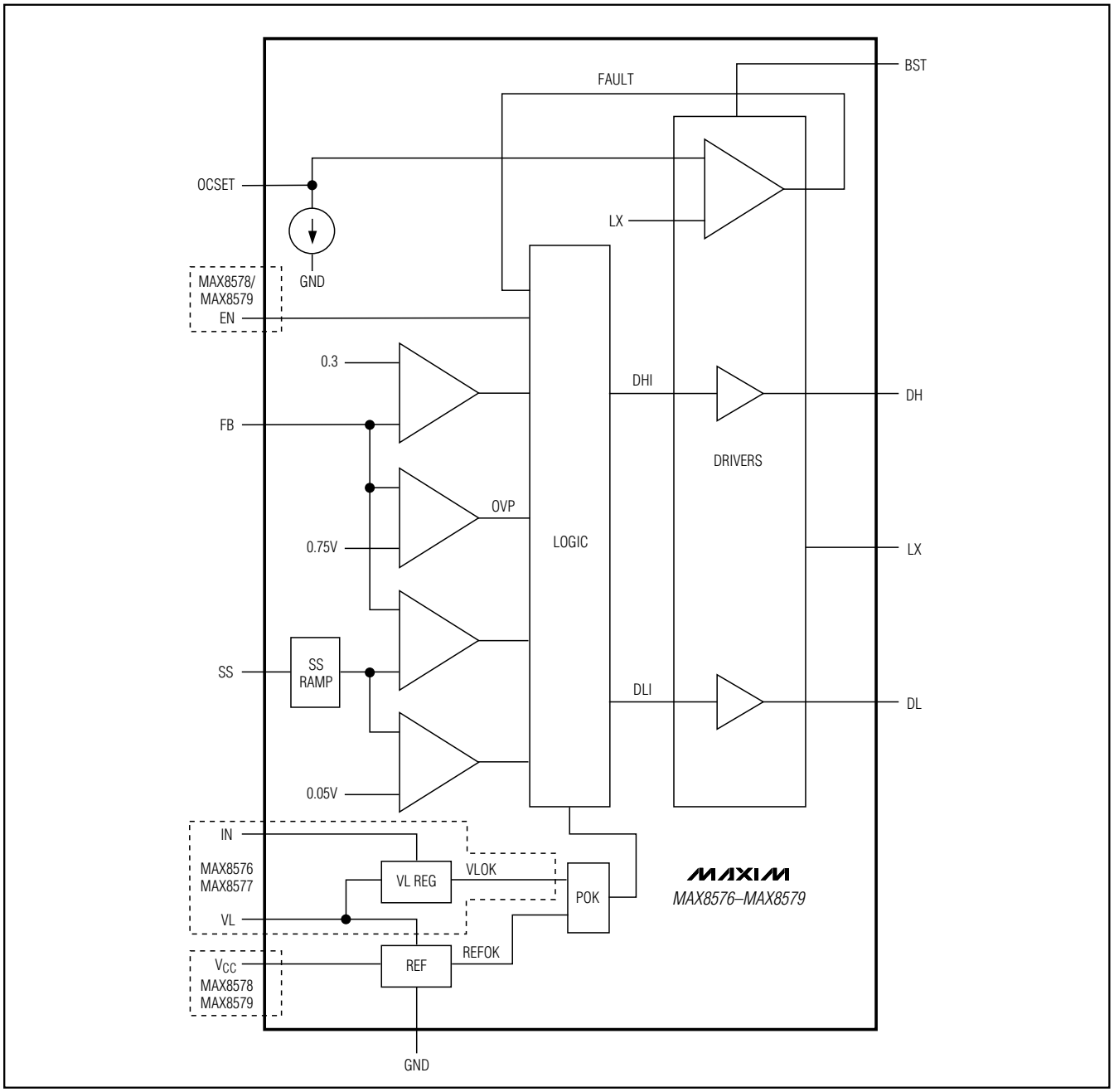
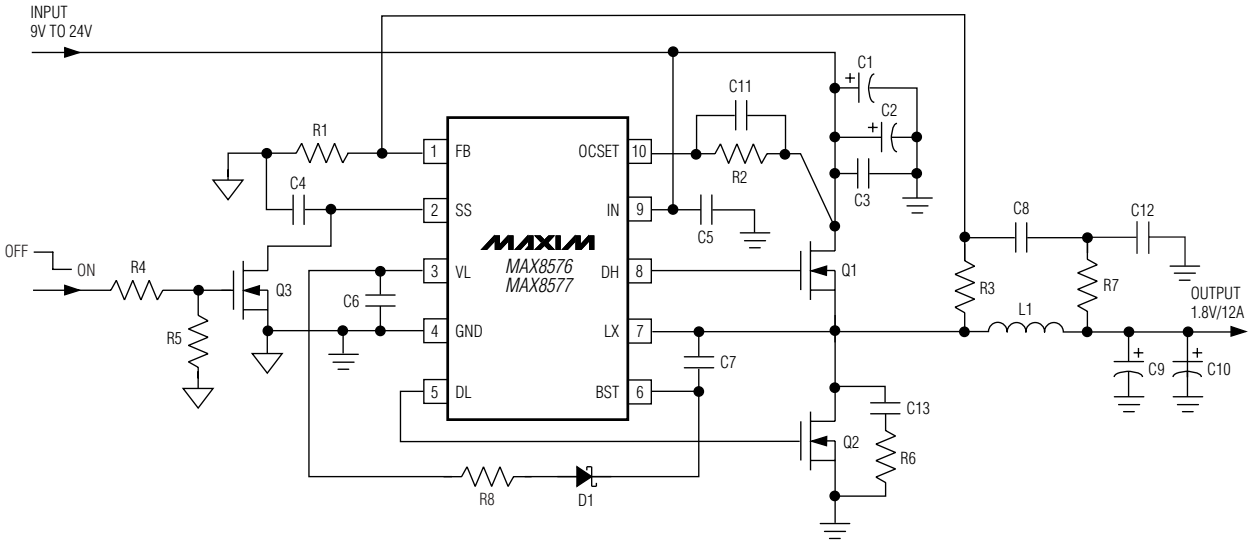


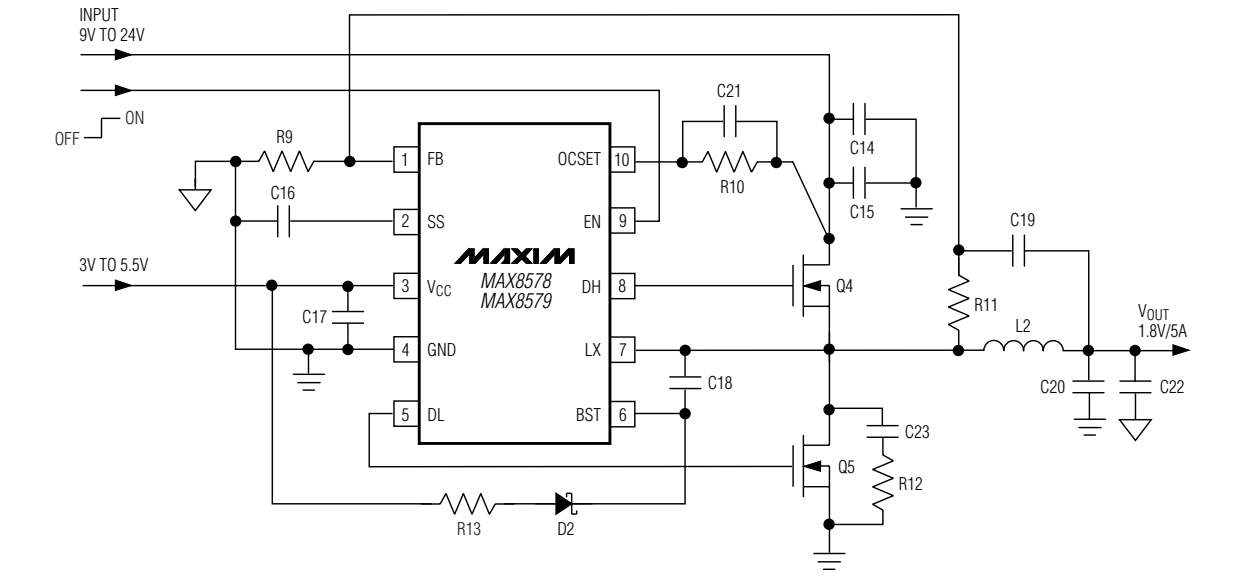
Figure 1. Functional Diagram

3V to 28V Input, Low-Cost, Hysteretic Synchronous Step-Down Controllers



12V INPUT, 1.8V/12A OUTPUT (f_S = 300kHz)
CIRCUIT IS TARGETED FOR 10.8V TO 13.2V INPUT. HOWEVER, INPUT RANGE OF 9V TO 24V IS POSSIBLE FOR IC EVALUATION. 30V RATED MOSFET MUST BE INSTALLED IF INPUT IS RAISED ABOVE 16V. ALL OTHER COMPONENTS CAN REMAIN UNCHANGED.

Figure 2. MAX8576/MAX8577 Typical Application Circuit



12V INPUT, 1.8V/5A OUTPUT (f_S = 500kHz, ALL CERAMIC)
CIRCUIT IS TARGETED FOR 10.8V TO 13.2V INPUT. HOWEVER, INPUT RANGE OF 9V TO 24V IS POSSIBLE FOR IC EVALUATION. 30V RATED MOSFET MUST BE INSTALLED IF INPUT IS RAISED ABOVE 16V. ALL OTHER COMPONENTS CAN REMAIN UNCHANGED.

Figure 3. MAX8578/MAX8579 Typical Application Circuit

MAX8576/MAX8577 External Component List

COMPONENTS	QTY	DESCRIPTION/VENDOR PART NUMBER
C1, C2	2	470µF, 35V aluminum electrolytic capacitors Sanyo 35MV470WX
C3	1	10µF, 25V X7R ceramic capacitor
C4	1	0.01µF, 10V X7R ceramic capacitor
C5	1	1µF, 35V X7R ceramic capacitor
C6	1	4.7µF, 6.3V X5R ceramic capacitor
C7, C12	2	0.1µF, 10V X7R ceramic capacitors
C8	1	0.027µF, 25V X7R ceramic capacitor
C9, C10	2	2200µF, 6.3V aluminum electrolytic capacitors Rubycon 6.3MBZ2200M10X20
C11	1	0.01µF, 25V X5R ceramic capacitor
C13	1	3300pF, 6.3V X5R ceramic capacitor
D1	1	High-speed diode, 100V, 250mA Philips BAS316 (SOD-323)
L1	1	1.8µH, 14A, 3.48mΩ Panasonic ETQP2H1R8BFA
Q1	1	30V, 12.5mΩ (max), SO-8 International Rectifier IRF7821
Q2	1	30V, 3.7mΩ, SO-8 International Rectifier IRF7832
Q3	1	2N7002 SOT-23
R1	1	6.04kΩ ±1% resistor
R2	1	5.11 kΩ ±1% resistor
R3	1	12.4kΩ ±1% resistor
R4	1	1kΩ ±5% resistor
R5	1	20kΩ ±5% resistor
R6	1	2Ω ±5% resistor
R7	1	10Ω ±5% resistor
R8	1	4.7Ω ±5% resistor

MAX8578/MAX8579 External Component List

COMPONENT	QTY	DESCRIPTION/VENDOR PART NUMBER
C14	1	10µF, 25V X5R ceramic capacitor
C15	1	1µF, 25V X5R ceramic capacitor
C16	1	4700pF, 10V X7R ceramic capacitor
C17	1	4.7µF, 6.3V X5R ceramic capacitor
C18	1	0.1µF, 10V X7R ceramic capacitor
C19	1	0.01µF, 25V X7R ceramic capacitor
C20	1	47µF, 6.3V, ESR = 5mΩ, ceramic capacitor Taiyo Yuden JMK432476MM
C21	1	0.01µF, 25V X5R ceramic capacitor
C22	0	Optional (47µF, 6.3V, ESR = 5mΩ ceramic capacitor Taiyo Yuden JMK432476MM)
C23	1	1000pF, 25V X5R ceramic capacitor
D2	1	High-speed diode, 100V, 250mA Philips BAS316 (SOD-323)
L2	1	2.2µH, 7.3A, 9.8mΩ Sumida CDEP104L-2R2
Q4	1	30V, 18mΩ (max), SO-8 International Rectifier IRF7807Z
Q5	1	30V, 9.5mΩ, SO-8 International Rectifier IRF7821
R9	1	6.04kΩ ±1% resistor
R10	1	2.49kΩ ±1% resistor
R11	1	12.4kΩ ±1% resistor
R12	1	2Ω ±5% resistor
R13	1	4.7Ω ±5% resistor

Detailed Description

The MAX8576–MAX8579 synchronous PWM buck controllers use Maxim's proprietary hysteretic voltage-mode control algorithm to achieve fast transient response without any loop-compensation requirement. The controller drives a pair of external n-channel power MOSFETs to improve efficiency and cost. The MAX8576/MAX8577 contain an internal linear low-dropout (LDO) regulator allowing the controller to operate from a single 3V to 28V input supply. The MAX8578/MAX8579 do not contain the internal LDO and require a separate supply to power the IC when the input supply is higher than 5.5V. The MAX8576–MAX8579 output voltages are adjustable from 0.6V to 0.9 x V_{IN} at loads up to 15A.

3V to 28V Input, Low-Cost, Hysteretic Synchronous Step-Down Controllers

Nominal switching frequency is programmable over the 200kHz to 500kHz range. High-side MOSFET sensing is used for adjustable hiccup current-limit and short-circuit protection. The MAX8576/MAX8578 can start up into a precharged output without pulling the output voltage down. The MAX8577/MAX8579 have startup output overvoltage protection (OVP).

The MAX8578/MAX8579 have a logic-enable input to turn on and off the output. The MAX8576/MAX8577 are turned off by pulling SS low with an external small n-channel MOSFET (see Figure 2).

DC-DC Converter Control Architecture

A proprietary hysteretic-PWM control scheme ensures high efficiency, fast switching, and fast transient response. This control scheme is simple: when the output voltage falls below the regulation threshold, the error comparator begins a switching cycle by turning on the high-side switch. This switch remains on until the minimum on-time expires and the output voltage is in regulation or the current-limit threshold is exceeded. Once off, the high-side switch remains off until the minimum off-time expires and the output voltage falls below the regulation threshold. During this period, the low-side synchronous rectifier turns on and remains on until the voltage at FB drops below its regulation threshold. The internal synchronous rectifier eliminates the need for an external Schottky diode.

Voltage-Positioning Load Regulation

As seen in Figures 2 and 3, the MAX8576–MAX8579 use a unique feedback network. By taking feedback from the LX node through R3 (R11 for the MAX8578/MAX8579), the usual phase lag due to the output capacitor does not exist, making the loop stable for either electrolytic or ceramic output capacitors. This configuration causes the output voltage to shift by the inductor DC resistance multiplied by the load current. This voltage-positioning load regulation greatly reduces overshoot during load transients, which effectively halves the peak-to-peak output-voltage excursions compared to traditional step-down converters. See the Load Transient graphs in the *Typical Operating Characteristics*.

Internal 5V Linear Regulator

All MAX8576/MAX8577 functions are powered from the on-chip, low-dropout 5V regulator with the input connected to IN. Bypass the regulator's output (VL) with a 1µF or greater ceramic capacitor. The capacitor must have an equivalent series resistance (ESR) of no greater than 10mΩ. When V_{IN} is less than 5.5V, short VL to IN. The MAX8578/MAX8579 do not have the on-chip 5V regulator and must use a separate external supply from 3V to 5.5V connected to V_{CC} if the input voltage is greater than 5.5V.

Undervoltage Lockout

If VL (MAX8576/MAX8577) or V_{CC} (MAX8578/MAX8579) drops below 2.45V (typ), the MAX8576–MAX8579 assume that the supply voltage is too low for proper circuit operation, so the UVLO circuitry inhibits switching and forces the DL and DH gate drivers low for the MAX8576/MAX8578, and DH low and DL high for the MAX8577/MAX8579. After V_{IN} rises above 2.8V (typ), the controller goes into the startup sequence and resumes normal operation.

Output Overvoltage Protection

The MAX8576–MAX8579 output overvoltage protection is provided by a glitch-resistant comparator on FB with a trip threshold of 750mV (typ). The overvoltage-protection circuit is latched by an OVP fault, terminating the run cycle and setting DH low and DL high. The fault is cleared by toggling EN or UVLO. Output OVP is active whenever the internal reference is in regulation.

Startup and Soft-Start

The soft-start sequence is initiated upon initial power-up, recovering from UVLO, or driving EN (MAX8578/MAX8579) high from a low state, or releasing SS (MAX8576/MAX8577) from a low state. The external soft-start capacitor (C_{SS}) is connected to an internal resistor-divider that exponentially charges the capacitor to 0.6V, with an SS ramp interval of 5 x RC or 4ms per 0.01µF. SS is one input to the internal voltage error comparator, while FB is the other input. The output voltage fed back to FB tracks the rising SS voltage. Switching commences immediately if V_{FB} is initially less than V_{SS}; if V_{FB} is greater than V_{SS}, DH remains low until V_{FB} is less than V_{SS}. DL remains low in the MAX8576/MAX8578. This prevents the converter from operating in reverse. However, DL is high before startup in the MAX8577/MAX8579 to enable OVP protection in case the high-side MOSFET is shorted.

Enable

Connecting EN to GND or logic low places the MAX8578/MAX8579 in shutdown mode. In shutdown, DH and DL are forced low, and the voltage at SS is discharged with a 250nA current, resulting in a ramp-down interval of approximately 10x the soft-start ramp-up interval. V_{SS} must fall to within 50mV of GND before another cycle can commence. SS (MAX8576/MAX8577) or EN (MAX8578/MAX8579) do not need to be cycled after an overcurrent event. Connect EN to V_{CC} or logic high for normal operation. To shut down the MAX8576/MAX8577, use an external circuit connected

to SS. See Figure 2 for details. The maximum on-resistance of the small external n-channel MOSFET should be less than 40Ω so that the SS voltage is below 10mV.

Synchronous-Rectifier Driver (DL)

Synchronous rectification reduces conduction losses in the rectifier by replacing the normal Schottky catch diode with a low-resistance MOSFET switch. The MAX8576–MAX8579 also use the synchronous rectifier to ensure proper startup of the boost gate-driver circuit. The DL low-side waveform is always the complement of the DH high-side drive waveform (with controlled dead time to prevent cross-conduction or shoot-through). A dead-time circuit monitors the DL output and prevents the high-side MOSFET from turning on until DL is fully off. For the dead-time circuit to work properly, there must be a low-resistance, low-inductance path from the DL driver to the MOSFET gate. Otherwise, the sense circuitry in the MAX8576–MAX8579 may interpret the MOSFET gate as off when gate charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the device). The dead time at the other edge (DH turning off) is also determined through gate sensing.

High-Side Gate-Drive Supply (BST)

Gate-drive voltage for the high-side n-channel switch is generated by a flying-capacitor boost circuit (Figure 4). The capacitor between BST and LX is charged from the IN supply up to V_{IN} minus the diode drop while the low-side MOSFET is on. When the low-side MOSFET is switched off, the stored voltage of the capacitor is stacked above LX to provide the necessary turn-on voltage (V_{GS}) for the high-side MOSFET. The controller then closes an internal switch between BST and DH to turn the high-side MOSFET on.

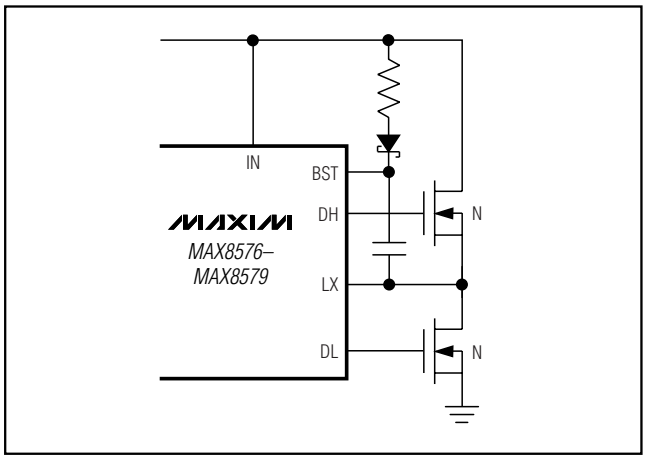


Figure 4. DH Boost Circuit

Current-Limit Circuit

Current limit is set externally with a resistor from OCSET to the drain of the high-side n-channel MOSFET that is normally connected to the input supply. The resistor programs the high-side peak current limit by setting the maximum-allowed $V_{DS(ON)}$ voltage drop across the high-side MOSFET. An internal 50µA current sink sets the maximum voltage drop relative to V_{IN}. If V_{FB} < 300mV, any overcurrent event (V_{DS} of the high-side n-channel MOSFET is larger than the limit programmed at OCSET) immediately sets DH low and terminates the run cycle. If V_{FB} > 300mV and an overcurrent event is detected, DH is immediately set low and four sequential overcurrent events terminate the run cycle. Once the run cycle is terminated, the SS capacitor is slowly discharged through the internal 250nA current sink to provide a hiccup current-limit effect. Choosing the proper value resistor is discussed in the *Setting the Current Limit* section.

Switching Frequency

Nominal switching frequency is programmable over the 200kHz to 500kHz range. This allows tradeoffs in efficiency, switching frequency, inductor value, and component size. Faster switching frequency allows for smaller inductor values but does result in some efficiency loss. Inductor-value calculations are provided in the *Inductor Value* section. The switching frequency is tuned by the selection of the feed-forward capacitor (C_{FF}). See the *Feed-Forward Capacitor* section.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX8576–MAX8579. When the junction temperature exceeds T_J = +160°C, an internal thermal sensor shuts down the IC, allowing the IC to cool. The thermal sensor turns the IC on again after the junction temperature cools to +140°C, resulting in a pulsed output during continuous thermal-overload conditions.

Design Procedures

Setting the Output Voltage

Select an output voltage between 0.6V and 0.9 x V_{IN} by connecting FB to a resistive voltage-divider between LX and GND (see Figures 2 and 3). Choose R1 for approximately 50µA to 150µA bias current in the resistive divider. A wide range of resistor values is acceptable, but a good starting point is to choose R1 as 6.04kΩ. Then, R3 is given by:

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$$R3 = R1 \times \left(\frac{V_{OUT} + 0.01V + (R_{DC} \times 0.5 \times I_{OUTMAX})}{V_{FB}} - 1 \right)$$

where V_{FB} = 0.590V, R_{DC} is the DC resistance of the output inductor, I_{OUTMAX} is the maximum output current. The term 0.01V is to reflect 1/2 of the feedback-threshold hysteresis.

Inductor Value

The inductor value is bounded by two operating parameters: the switching frequency and the inductor peak-to-peak ripple current. The peak-to-peak ripple current is typically in the range of 20% to 40% of the maximum output current. The equation below defines the inductance value:

$$L = \left(\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_S \times I_{LOAD(MAX)} \times LIR} \right)$$

where LIR is the ratio of inductor current ripple to DC load current and f_S is the switching frequency. A good compromise between size, efficiency, and cost is an LIR of 30%. The selected inductor must have a saturated current rating above the sum of the maximum output current and half of the peak-to-peak ripple current. The DC current rating of the inductor must be above the maximum output current to keep the temperature rise within the desired range. In addition, the DC resistance of the inductor must meet the requirement below:

$$R_{DC} \le \frac{\Delta V_{OUT}}{I_{OUTMAX}}$$

where ΔV_{OUT} is the maximum-allowed output-voltage drop from no load to full load (I_{OUTMAX}).

Setting the Current Limit

Resistor R2 (R7 for the MAX8577/MAX8579) of Figure 2 (Figure 3 for the MAX8577/MAX8579) sets the current limit and is connected between OCSET and the drain of the high-side n-channel MOSFET. An internal 50µA current sink sets the maximum voltage drop across the high-side n-channel MOSFET relative to V_{IN}. The maximum V_{DS} drop needs to be determined. This is calculated by:

$$V_{DS(ON)MAX} = I_{DS(MAX)} \times R_{DS(ON)MAX}$$

$I_{DS(MAX)}$ must be equal or greater than the maximum peak inductor current at the maximum output current. Use $R_{DS(ON)MAX}$ at the junction temperature of +25°C. The current limit is temperature compensated.

R_{OCSET} is calculated using the $V_{DS(ON)MAX}$ with the following formula:

$$R_{OCSET} = \frac{V_{DS(ON)MAX}}{50\mu A}$$

A 0.01µF ceramic capacitor is required in parallel with R_{OCSET} to decouple high-frequency noise.

MOSFET Selection

The MAX8576–MAX8579 drive two external, logic-level, n-channel MOSFETs as the circuit switching elements. The key selection parameters are:

1) On-resistance ($R_{DS(ON)}$): the lower, the better.
2) Maximum drain-to-source voltage (V_{DSS}): should be at least 20% higher than the input supply rail at the high-side MOSFET's drain.
3) Gate charges (Q_g, Q_{gd}, Q_{gs}): the lower, the better.

For a 3.3V input application, choose a MOSFET with a rated $R_{DS(ON)}$ at V_{GS} = 2.5V. For a 5V input application, choose the MOSFETs with rated $R_{DS(ON)}$ at V_{GS} ≤ 4.5V. For a good compromise between efficiency and cost, choose the high-side MOSFET (N1) that has conduction losses equal to switching loss at nominal input voltage and output current. The selected high-side MOSFET (N1) must have $R_{DS(ON)}$ that satisfies the current-limit-setting condition above. For N2, make sure that it does not spuriously turn on due to dV/dt caused by N1 turning on as this results in shoot-through current degrading the efficiency. MOSFETs with a lower Q_{gd} / Q_{gs} ratio have higher immunity to dV/dt.

For proper thermal-management design, the power dissipation must be calculated at the desired maximum operating junction temperature, maximum output current, and worst-case input voltage (for the low-side MOSFET, worst case is at $V_{IN(MAX)}$; for the high-side MOSFET, it could be either at $V_{IN(MAX)}$ or $V_{IN(MIN)}$). N1 and N2 have different loss components due to the circuit operation. N2 operates as a zero-voltage switch; therefore, major losses are: the channel-conduction loss (P_{N2CC}) and the body-diode conduction loss (P_{N2DC}).

$$P_{N2CC} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times I_{LOAD}^2 \times R_{DS(ON)}$$

Use $R_{DS(ON)}$ at $T_{J(MAX)}$.

$$P_{N2DC} = 2 \times I_{LOAD} \times V_F \times t_{dt} \times f_S$$

where V_F is the body-diode forward-voltage drop, t_{DT} is the dead time between N1 and N2 switching transitions (40ns typ), and f_S is the switching frequency.

N1 operates as a duty-cycle control switch and has the following major losses: the channel-conduction loss (P_{N1CC}), the VL overlapping switching loss (P_{N1SW}), and the drive loss (P_{N1DR}). N1 does not have body-diode conduction loss because the diode never conducts current.

$$P_{N1CC} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{LOAD}^2 \times R_{DS(ON)}$$

Use $R_{DS(ON)}$ at $T_{J(MAX)}$.

$$P_{N1SW} = V_{IN} \times I_{LOAD} \times \left(\frac{Q_{gs} + Q_{gd}}{I_{GATE}}\right) \times f_S$$

where I_{GATE} is the average DH driver output-current capability determined by:

$$I_{GATE} \cong 0.5 \times \frac{V_L}{R_{DH} + R_{GATE}}$$

where R_{DH} is the high-side MOSFET driver's on-resistance (2Ω typ) and R_{GATE} is the internal gate resistance of the MOSFET (approximately 2Ω).

$$P_{N1DR} = Q_g \times V_{GS} \times f_S \times \frac{R_{GATE}}{R_{GATE} + R_{DH}}$$

where V_{GS} is approximately equal to V_L.

In addition to the losses above, allow about 20% more for additional losses due to MOSFET output capacitances and N2 body-diode reverse-recovery charge dissipated in N1 that exists, but is not well defined in the MOSFET data sheet. Refer to the MOSFET data sheet for thermal-resistance specification to calculate the PC board area needed to maintain the desired maximum operating junction temperature with the above calculated power dissipations.

To reduce EMI caused by switching noise, add 0.1µF ceramic capacitor from the high-side switch drain to the low-side switch source or add resistors in series with DH and DL to slow down the switching transitions. However, adding series resistors increases the power dissipation of the MOSFET, so be sure this does not overheat the MOSFET.

The minimum load current must exceed the high-side MOSFET's maximum leakage current over temperature if fault conditions are expected.

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor must meet the ripple-current requirement (I_{RMS}) imposed by the switching currents defined by the following equation:

$$I_{RMS} = \frac{I_{LOAD} \times \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so $I_{RMS(MAX)}$ = I_{LOAD} / 2. Ceramic capacitors are recommended due to their low ESR and ESL at high frequency, with relatively lower cost. Choose a capacitor that exhibits less than 10°C temperature rise at the maximum operating RMS current for optimum long-term reliability.

Output Capacitor

The key selection parameters for the output capacitor are the actual capacitance value, the ESR, the equivalent series inductance (ESL), and the voltage-rating requirements. These parameters affect the overall stability, output voltage ripple, and transient response. The output ripple has three components: variations in the charge stored in the output capacitor, the voltage drop across the capacitor's ESR, and the ESL caused by the current into and out of the capacitor. The maximum output ripple voltage can be estimated by:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)} + V_{RIPPLE(ESL)}$$

The output voltage ripple as a consequence of the ESR and output capacitance is:

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{C_{OUT} \times f_S}$$

$$V_{RIPPLE(ESL)} = \left(\frac{V_{IN}}{L}\right) \times ESL$$

$$I_{P-P} = \left(\frac{V_{IN} - V_{OUT}}{f_S \times L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right)$$

where I_{P-P} is the peak-to-peak inductor current (see the *Inductor Value* section). These equations are suitable for initial capacitor selection, but final values should be

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chosen based on a prototype or evaluation circuit. As a general rule, a smaller current ripple results in less output voltage ripple. Since the inductor ripple current is a factor of the inductor value and input voltage, the output voltage ripple decreases with larger inductance and increases with higher input voltages. For reliable and safe operation, ensure that the capacitor's voltage and ripple-current ratings exceed the calculated values.

The response of the MAX8576–MAX8579 to a load 1transient depends on the selected output capacitors. After a load transient, the output voltage instantly changes by ESR times ΔI_{LOAD}. Before the controller can respond, the output voltage deviates further depending on the inductor and output capacitor values. The controller responds immediately as the output voltage deviates from its regulation limit (see the *Typical Operating Characteristics*).

The MAX8576–MAX8579 are compatible with both aluminum electrolytic and ceramic output capacitors. Due to the limited capacitance of a ceramic capacitor, it is typically used for a higher switching frequency and lower output current. Aluminum electrolytic is more applicable to frequencies up to 300kHz and can support higher output current with its much higher capacitance value.

Due to the much higher ESL and ESR of the aluminum electrolytic capacitor, an RC filter (R7 and C12 of Figure 2) is required to prevent excessive ESL and ESR ripple from tripping the feedback threshold prematurely.

MOSFET Snubber Circuit

Fast-switching transitions cause ringing because of resonating circuit parasitic inductance and capacitance at the switching nodes. This high-frequency ringing occurs at LX's rising and falling transitions and can interfere with circuit performance and generate EMI. To dampen this ringing, a series RC snubber circuit is added across each switch. Below is the procedure for selecting the value of the series RC circuit:

1) Connect a scope probe to measure V_{LX} to GND, and observe the ringing frequency, f_R.
2) Find the capacitor value (connected from LX to GND) that reduces the ringing frequency by half.

The circuit parasitic (C_{PAR}) at LX is then equal to 1/3 the value of the added capacitance above. The circuit parasitic inductance (L_{PAR}) is calculated by:

$$L_{PAR} = \frac{1}{(2\pi f_R)^2 \times C_{PAR}}$$

The resistor for critical dampening (R_{SNUB}) is equal to $2\pi \times f_R \times L_{PAR}$. Adjust the resistor value up or down to tailor the desired damping and the peak voltage excursion.

The capacitor (C_{SNUB}) should be at least 2 to 4 times the value of C_{PAR} to be effective. The power loss of the snubber circuit is dissipated in the resistor (P_{RSNUB}) and can be calculated as:

$$P_{RSNUB} = C_{SNUB} \times (V_{IN})^2 \times f_{SW}$$

where V_{IN} is the input voltage and f_{SW} is the switching frequency. Choose an R_{SNUB} power rating that meets the specific application's derating rule for the power dissipation calculated.

Feed-Forward Capacitor

The feed-forward capacitor, C8 (Figure 2, MAX8576/MAX8577 with aluminum electrolytic output capacitor), or C19 (Figure 3, MAX8578/MAX8579 with ceramic output capacitor), dominantly affects the switching frequency. Choose a ceramic X7R capacitor with a value given by:

$$C8 = \frac{1}{R_{FB}} \times \left(\frac{1}{F_S} - 120ns \times \frac{V_{IN}}{V_{OUT}} \right) \times 49.5 \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

or

$$C19 = \frac{1}{R_{FB}} \times \left(\frac{1}{F_S} - 120ns \times \frac{V_{IN}}{V_{OUT}} \right) \times 39.5 \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

where F_S is the desired switching frequency, and R_{FB} is the parallel combination of the two feedback divider-resistors (R1 and R3 of Figure 2, and R9 and R11 of Figure 3).

Select the closest standard value to C8 and C19 as possible.

The output inductor and output capacitor also affect the switching frequency, but to a much lesser extent.

The equations for C8 and C19 above should yield within ±30% of the desired switching frequency for most applications. The values of C8 and C19 can be increased to lower the frequency, or decreased to raise the frequency for better accuracy.

Application Information

PC Board Layout Guidelines

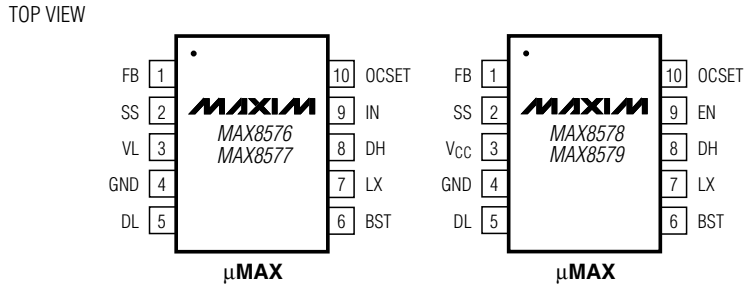
Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. Follow these guidelines for good PC board layout:

1) Place IC decoupling capacitors as close to IC pins as possible. Place the input ceramic decoupling capacitor directly across and as close as possible to the high-side MOSFET's drain and the low-side MOSFET's source. This is to help contain the high switching current within this small loop.
2) For output current > 10A, a four-layer PC board is recommended. Pour a ground plane in the second layer underneath the IC to minimize noise coupling.
3) Input, output, and VL capacitors are connected to the power ground plane with the exception of C12 and C22. These capacitors and all other capacitors are connected to the analog ground plane.
4) Make the connection from the current-limit setting resistor directly to the high-side MOSFET's drain to minimize the effect of PC board trace resistance and inductance.
5) Place the MOSFET as close as possible to the IC to minimize trace inductance. If parallel MOSFETs are used, keep the gate connection to both gates equal.
6) Connect the drain leads of the power MOSFET to a large copper area to help cool the device. Refer to the power MOSFET data sheet for the recommended copper area.
7) Place the feedback components as close to the IC pins as possible. The feedback divider-resistor from FB to the output inductor should be connected directly to the inductor and not sharing with other connections to this node.
8) Refer to the EV kit for further guidelines.

Suggested External Component Manufacturers

MANUFACTURER	COMPONENT	WEBSITE	PHONE
Central Semiconductor	Diodes	www.centralsemi.com	631-435-1110
Panasonic	Inductors	www.panasonic.com	402-564-3131
Sumida	Inductors	www.sumida.com	847-956-0666
International Rectifier	MOSFETs	www.irf.com	800-341-0392
Kemet	Capacitors	www.kemet.com	864-963-6300
Taiyo Yuden	Capacitors	www.t-yuden.com	408-573-4150
TDK	Capacitors	www.component.tdk.com	888-835-6646
Rubycon	Capacitors	www.rubycon.com	408-467-3864

Pin Configurations



Chip Information

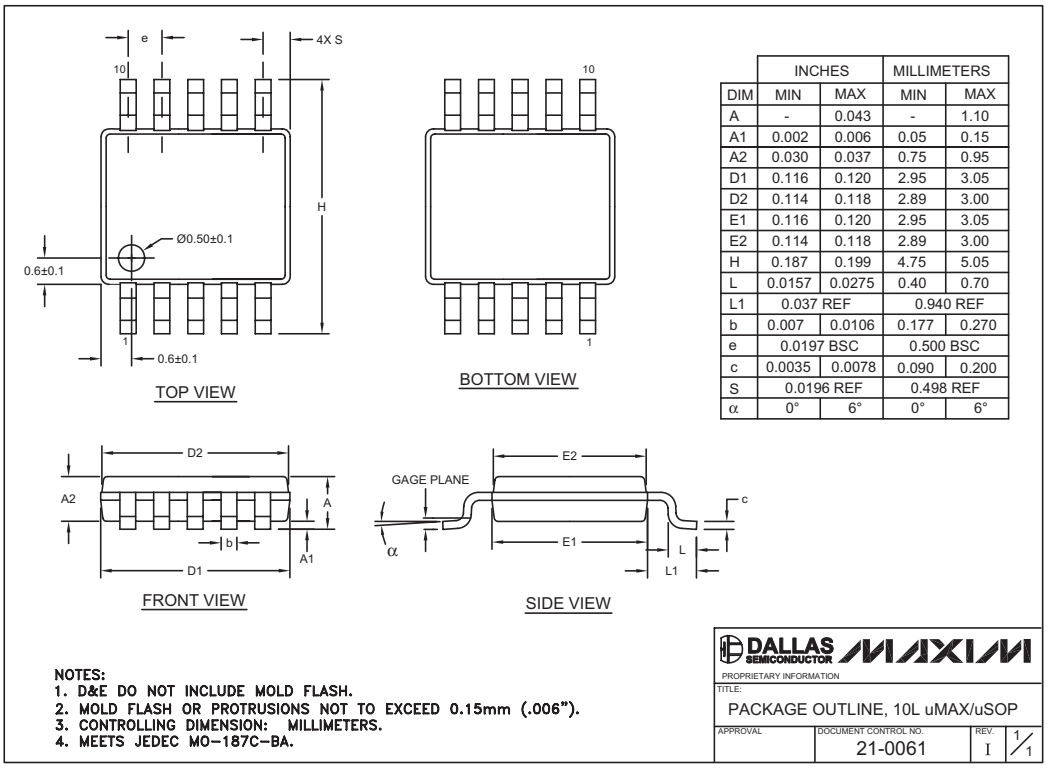
TRANSISTOR COUNT: 2087

PROCESSS: BICMOS

3V to 28V Input, Low-Cost, Hysteretic Synchronous Step-Down Controllers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°

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