19-3942; Rev 0; 1/06

Factory-Programmable, Single PLL Clock Generator

General Description

The MAX9491 multipurpose clock generator is ideal for communication applications. It offers a factory-programmable PLL output that can be set to almost any frequency, ranging from 4MHz to 200MHz. The MAX9491 uses a one-time-programmable (OTP) ROM to program the PLL output. The MAX9491 also features an integrated voltage-controlled crystal oscillator (VCXO) that is tuned by a DC voltage. The VCXO output is used as the PLL input. The VCXO has a wide ±200ppm (typ) tuning range. The OTP on the MAX9491 is factory preset, based upon the customer request. Contact the factory for samples with preferred frequencies.

The device operates from a 3.3V supply and is specified over the -40°C to +85°C extended temperature range. The MAX9491 is available in 14-pin TSSOP and 20-pin TQFN (5mm x 5mm) packages.

Features

- **5MHz to 35MHz for Crystal-Clock Reference**
- **5MHz to 50MHz for a Driver Clock Reference**
- **One Fractional-N PLL with Buffered Output**
- **4MHz to 200MHz Output Frequency Range**
- **Low RMS Jitter PLL (< 13ps) at 197 MHz**
- **Integrated VCXO with ±200ppm Tuning Range**
- **Available in 14-Pin TSSOP and 20-Pin TQFN Packages**
- **+3.3V Supply**
- **-40°C to +85°C Temperature Range**

Applications

Telecommunications

Data Networking Systems

Home Entertainment Centers

SOHO

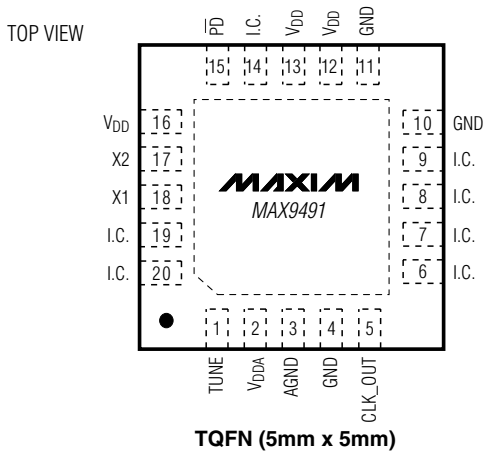
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9491ETP	-40°C to +85°C	20 TQFN-EP**	T2055-5
MAX9491EUD*	-40°C to +85°C	14 TSSOP	U14-2

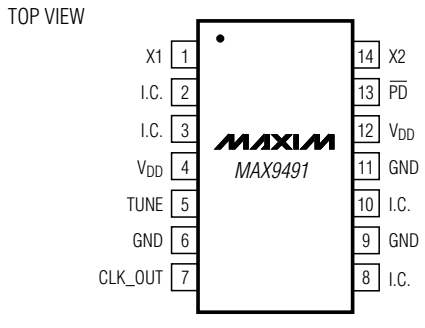
*Future product—contact factory for availability.

**EP = Exposed pad.

Pin Configurations



TQFN (5mm x 5mm)



TSSOP

Factory Programmable Single PLL Clock Generator

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +4.0V
V_{DDA} to AGND .....-0.3V to +4.0V
All Other Pins to GND .....-0.3V to V_{DD} + 0.3V
Short-Circuit Duration
(all LVCMOS outputs).....Continuous
ESD Protection (Human Body Model).....±2kV

Continuous Power Dissipation (T_A = +70°C)
20-Lead TQFN (derate 21.3mW/°C above +70°C) 2758mW
14-Pin TSSOP (derate 9.1mW/°C above +70°C) 796.8mW
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{DDA} = +3.0V to +3.6V and T_A = -40°C to +85°C. Typical values at V_{DD} = V_{DDA} = 3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVCMOS INPUTS ($\overline{PD}$, X1 as a reference INPUT CLK)						
Input High Level	V_{IH}		2.0		V_{DD}	V
Input Low Level	V_{IL}		0		0.8	V
High-Level Input Current	I_{IH}	V_{IN} = V_{DD}			20	µA
Low-Level Input Current	I_{IL}	V_{IN} = 0	-20			µA
CLOCK OUTPUT (CLK_OUT)						
Output High Level	V_{OH}	I_{OH} = -4mA	V_{DD} - 0.6			V
Output Low Level	V_{OL}	I_{OL} = 4mA			0.4	V
POWER SUPPLIES						
Digital Power-Supply Voltage	V_{DD}		3.0		3.6	V
Analog Power-Supply Voltage	V_{DDA}		3.0		3.6	V
Total Current for Digital and Analog Supplies	I_{DC}	f_{OUT} = 45MHz, no load f_{IN} = 13MHz		10		mA
Power-Down Current	$I_{DC}2$	$\overline{PD}$ = low		60		µA

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{DDA} = +3.0V to +3.6V, C_L = 10pF and T_A = -40°C to +85°C. Typical values are at V_{DD} = V_{DDA} = 3.3V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT CLOCK (CLK_OUT)						
Minimum Frequency Range	f_{OUT}	f_{IN} = 5MHz to 50MHz	4			MHz
Maximum Frequency Range		C_L < 5pF	133	200		
Clock Rise Time	t_R	20% to 80% of V_{DD}, f_{OUT} = 80MHz, f_{IN} = 13MHz		1.5		ns
Clock Fall Time	t_F	80% to 20% of V_{DD}, f_{OUT} = 80MHz, f_{IN} = 13MHz		1.3		ns
Duty Cycle		f_{OUT} = 45MHz, f_{IN} = 13MHz	44	50	56	%
Output Period Jitter	J_P	f_{OUT} = 45MHz, f_{IN} = 13MHz		14		ps RMS
		f_{OUT} = 80MHz, f_{IN} = 13MHz		22		
		f_{OUT} = 197MHz, f_{IN} = 13MHz		13		
Soft Power-On Time	t_{PO2}	$\overline{PD}$ from low to high, f_{OUT} = 45MHz, f_{IN} = 13MHz, see Figure 2		1		ms
Hard Power-On Time	t_{PO1}	See Figure 2		15		ms
VCXO CLOCK						
Crystal Frequency	f_{XTL}			27		MHz
Crystal Accuracy				±30		ppm
Tuning Voltage Range	V_{TUNE}		0		3	V
VCXO Tuning Range		V_{TUNE} = 0 to 3V, C_1 = C_2 = 4pF	±150	±200		ppm
TUNE Input Impedance	Z_{TUNE}			95		kΩ
Output CLK Accuracy		V_{TUNE} = 1.5V, C_1 = C_2 = 4pF		±50		ppm

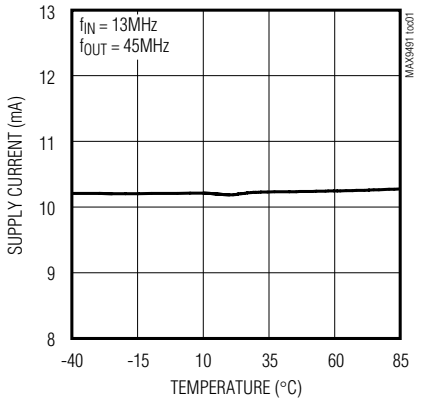
Note 1: All parameters are tested at T_A = +25°C. Specifications over temperature are guaranteed by design and characterization.
Note 2: Guaranteed by design and characterization; limits are set at ±6 sigma.

Factory Programmable Single PLL Clock Generator

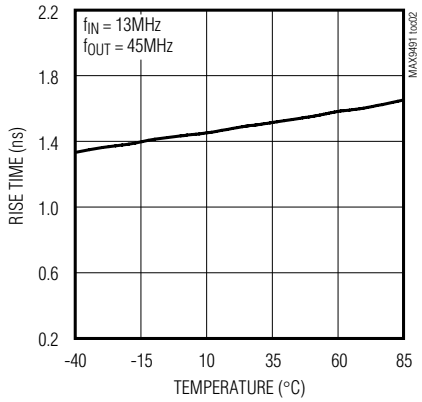
Typical Operating Characteristics

(V_{DD} = V_{DDA} = +3.3V, T_A = +25°C, f_{IN} = 13MHz clock, C_L = 10pF, 27MHz, unless otherwise noted.)

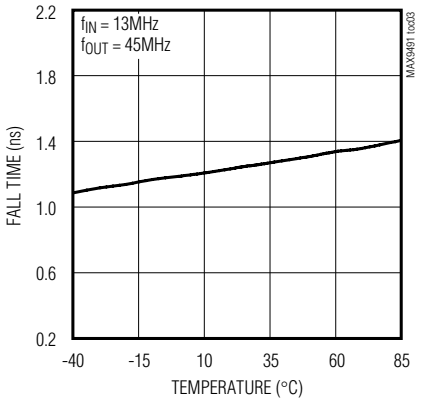
SUPPLY CURRENT vs. TEMPERATURE



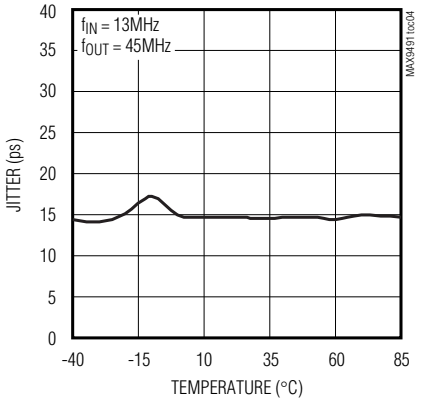
RISE TIME vs. TEMPERATURE



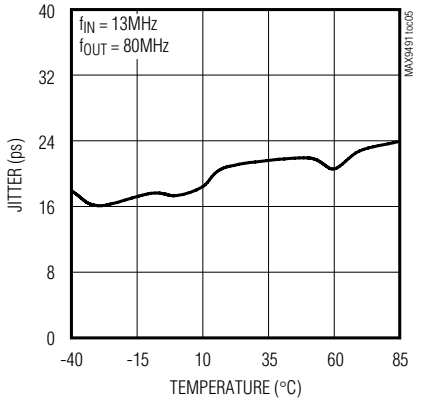
FALL TIME vs. TEMPERATURE



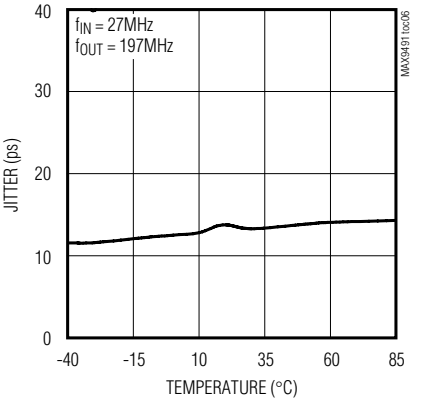
JITTER vs. TEMPERATURE



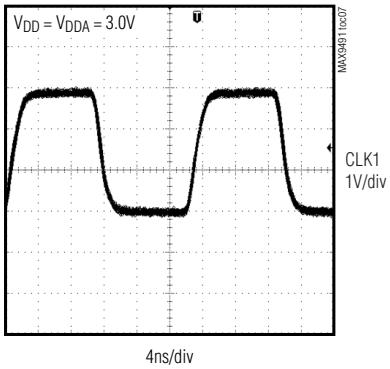
JITTER vs. TEMPERATURE



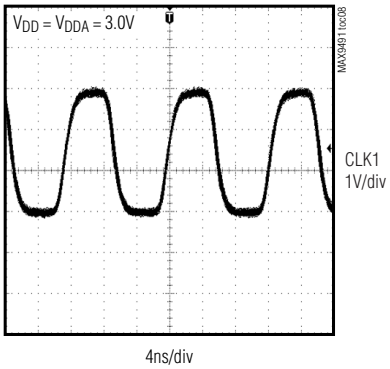
JITTER vs. TEMPERATURE



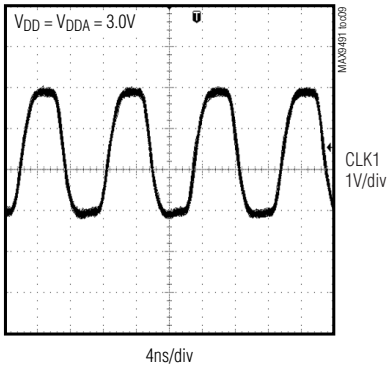
TYPICAL CLK_OUT WAVEFORM AT 45MHz



TYPICAL CLK_OUT WAVEFORM AT 80MHz



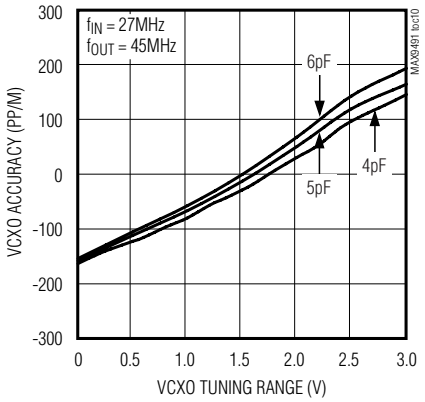
TYPICAL CLK_OUT WAVEFORM AT 197MHz



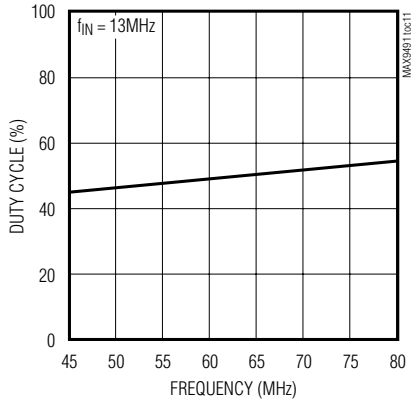
Typical Operating Characteristics (continued)

(V_{DD} = V_{DDA} = +3.3V, T_A = +25°C, f_{IN} = 13MHz clock, C_L = 10pF, 27MHz, unless otherwise noted.)

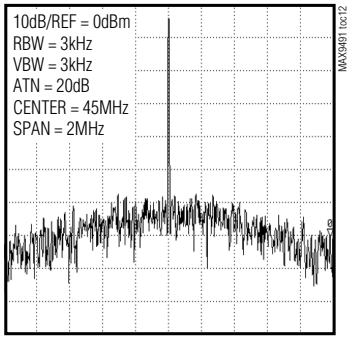
VCXO ACCURACY vs. VCXO TUNING RANGE



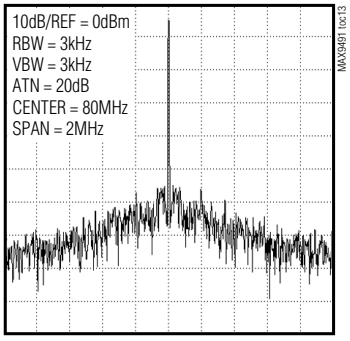
DUTY CYCLE vs. OUTPUT FREQUENCY



45MHz OUTPUT

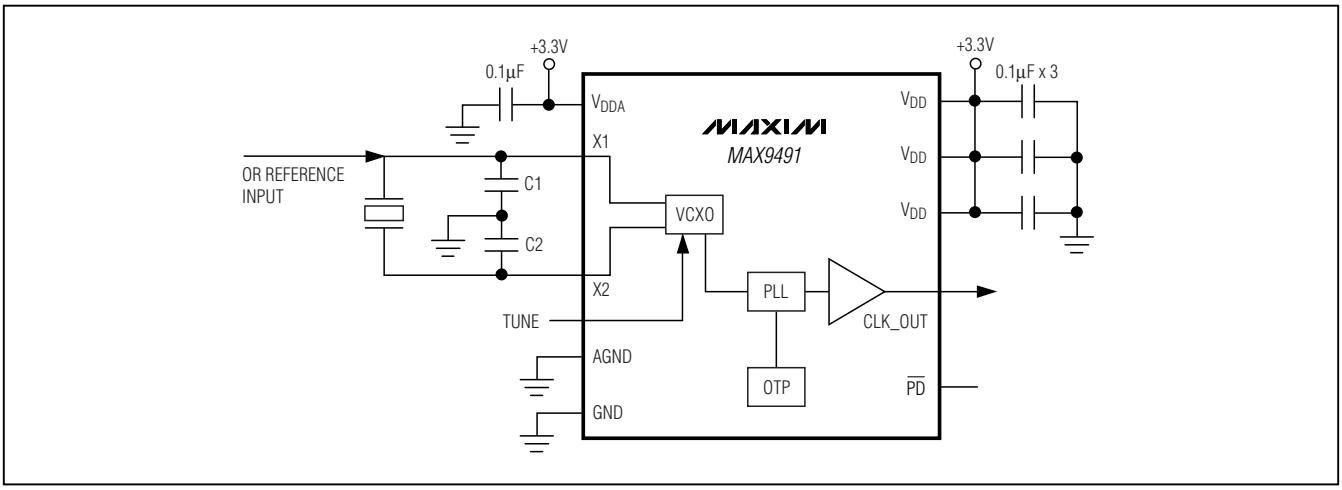


80MHz OUTPUT



Factory Programmable Single PLL Clock Generator

Typical Operating Circuit/Block Diagram



Pin Description

PIN		NAME	FUNCTION
TQFN	TSSOP		
1	5	TUNE	VCXO Tune Voltage Input. If using a reference clock input or VCXO is not used, connect TUNE to V_{DD}.
2	—	V_{DDA}	Analog Power Supply. Bypass to GND with a 0.1µF capacitor.
3	—	AGND	Analog Ground
4, 10, 11	6, 9, 11	GND	Ground
5	7	CLK_OUT	Output Clock. Internally pulled down.
6–9, 14, 19, 20	2, 3, 8, 10	I.C.	Internally Connected. Leave unconnected for normal operation.
12, 13, 16	4, 12	V_{DD}	Power Supply. Bypass to GND with a 0.1µF capacitor.
15	13	$\overline{PD}$	Active-Low Power-Down Input. Pull high for normal operation. Drive $\overline{PD}$ low to place MAX9491 in power-down mode. Internally pulled down.
17	14	X2	Crystal Connection 2. Leave unconnected if using a reference clock.
18	1	X1	Crystal Connection 1 or Reference Clock Input
EP	—	EP	Exposed Paddle (TQFN Only). Connect EP to GND or leave unconnected.

Detailed Description

The MAX9491 features a programmable fractional-N PLL, so frequencies between 4MHz to 200MHz can be generated. The device provides a buffered PLL clock output. The crystal input frequency can be between 5MHz and 35MHz, and the clock input between 5MHz and 50MHz. The internal VCXO has a fine-tuning range of ±200ppm.

Power-Down

Driving $\overline{PD}$ low places the MAX9491 in power-down mode. $\overline{PD}$ then sets CLK_OUT to high impedance and shuts down the PLL. CLK_OUT has an 80kΩ (typ) internal pulldown resistor.

Voltage-Controlled Crystal Oscillator (VCXO)

The MAX9491's internal VCXO produces a reference clock for the PLL used to generate the CLK_OUT. The oscillator uses a crystal as the base frequency reference and has a voltage-controlled tuning input for micro adjustment in a ±200ppm range. The tuning voltage, V_{TUNE}, can vary from 0 to 3V as shown in Figure 1. The crystal should be AT-cut and oscillate on its fundamental mode with ±30ppm. The crystal shunt capacitor

should be less than 10pF, including board parasitic capacitance. To achieve up to ±200ppm pullability, make sure the crystal-loading capacitance is less than 14pF. The VCXO is a free-running oscillator. It starts oscillating with an internal POR signal and can be disabled by $\overline{PD}$. When VCXO is not used, connect TUNE to V_{DD}.

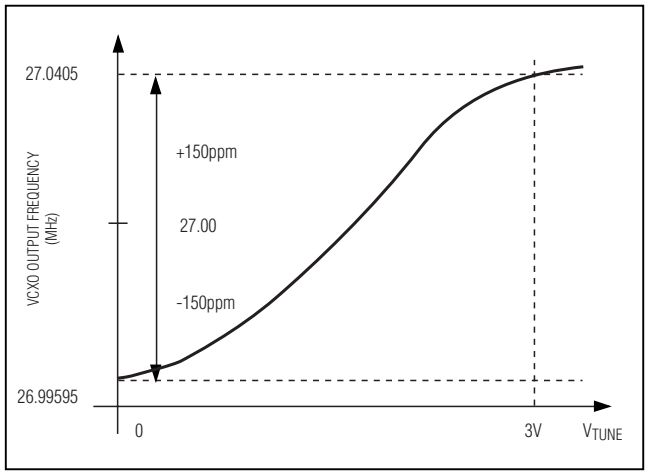


Figure 1. VCXO Tuning Range for a 27MHz Crystal

Applications Information

Using an Input Clock as the Reference

When an input clock is used as the reference, connect the input clock to X1, leave X2 unconnected, and connect TUNE to V_{DD}.

Crystal Selection

When using a crystal with the MAX9491's internal oscillator, connect the crystal to X1 and X2. Choose an AT-cut crystal that oscillates on its fundamental mode with ±30ppm and loading capacitance less than 14pF. To achieve a wide VCXO tuning range, select a crystal with motional capacitance greater than 7fF and connect 6pF or less shunt capacitors at both X1 and X2 to ground. When the VCXO is used as an oscillator, select both shunt capacitors to approximately 13pF. The optimal shunt capacitors for achieving minimum frequency offset can be determined experimentally.

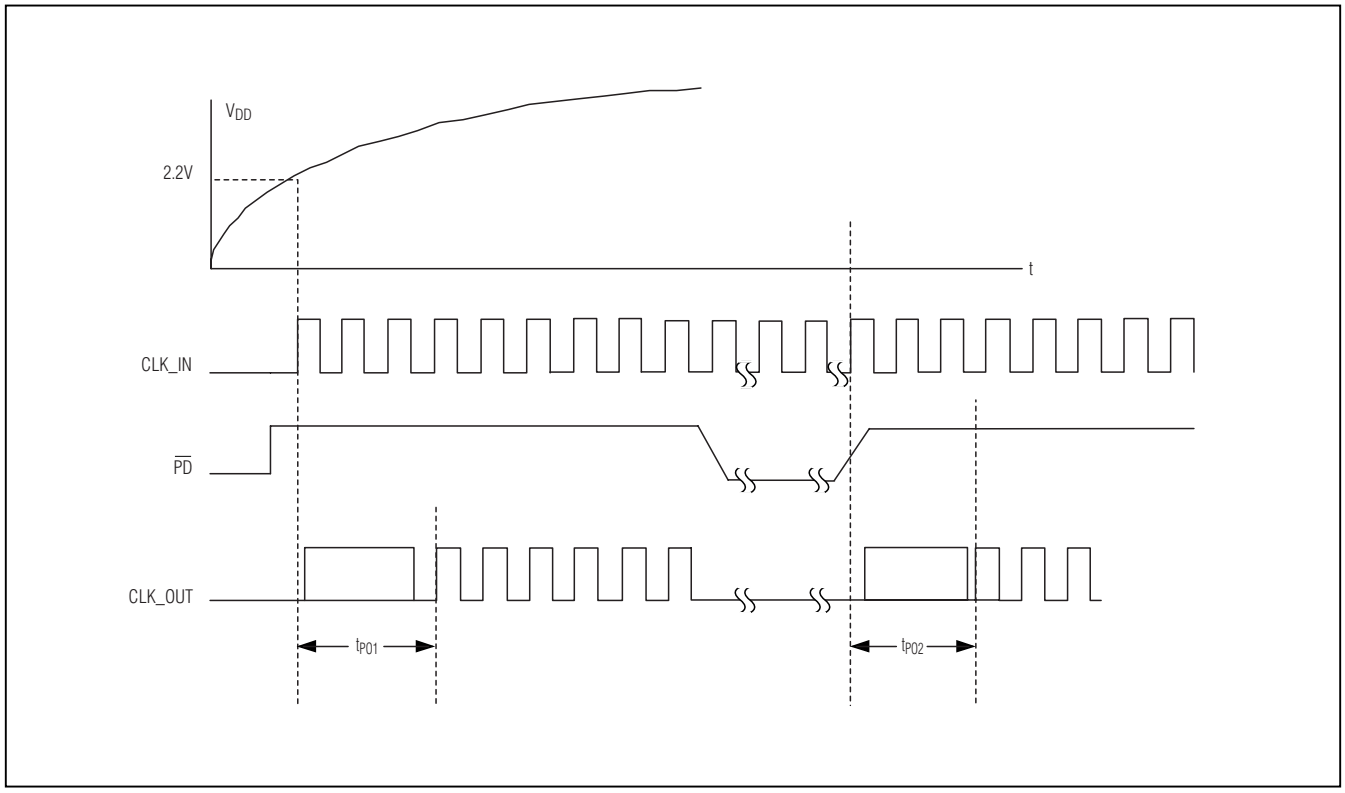


Figure 2. PLL Settling Time

Factory Programmable Single PLL Clock Generator

Board Layout Considerations and Bypassing

The MAX9491's high-frequency oscillator requires proper layout to ensure stability. For best performance, place components as close as possible to the device.

Digital or AC transient signals on GND can create noise at the clock output. Return GND to the highest quality ground available. Bypass each V_{DD} and V_{DDA} with a 0.1µF capacitor, placed as close as possible to the device. Careful PC board ground layout minimizes crosstalk between the output and digital inputs.

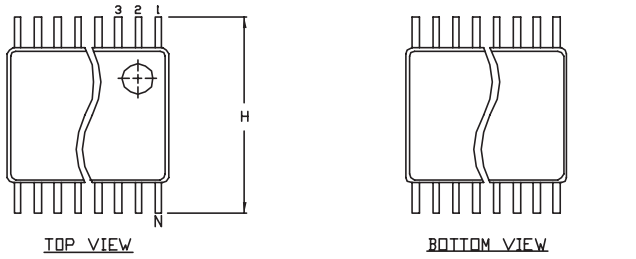
Chip Information

PROCESS: CMOS

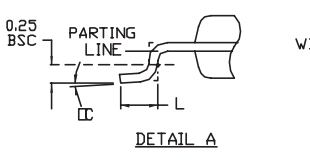
Package Information

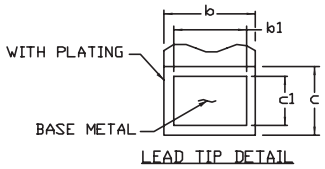
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_e	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°





JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

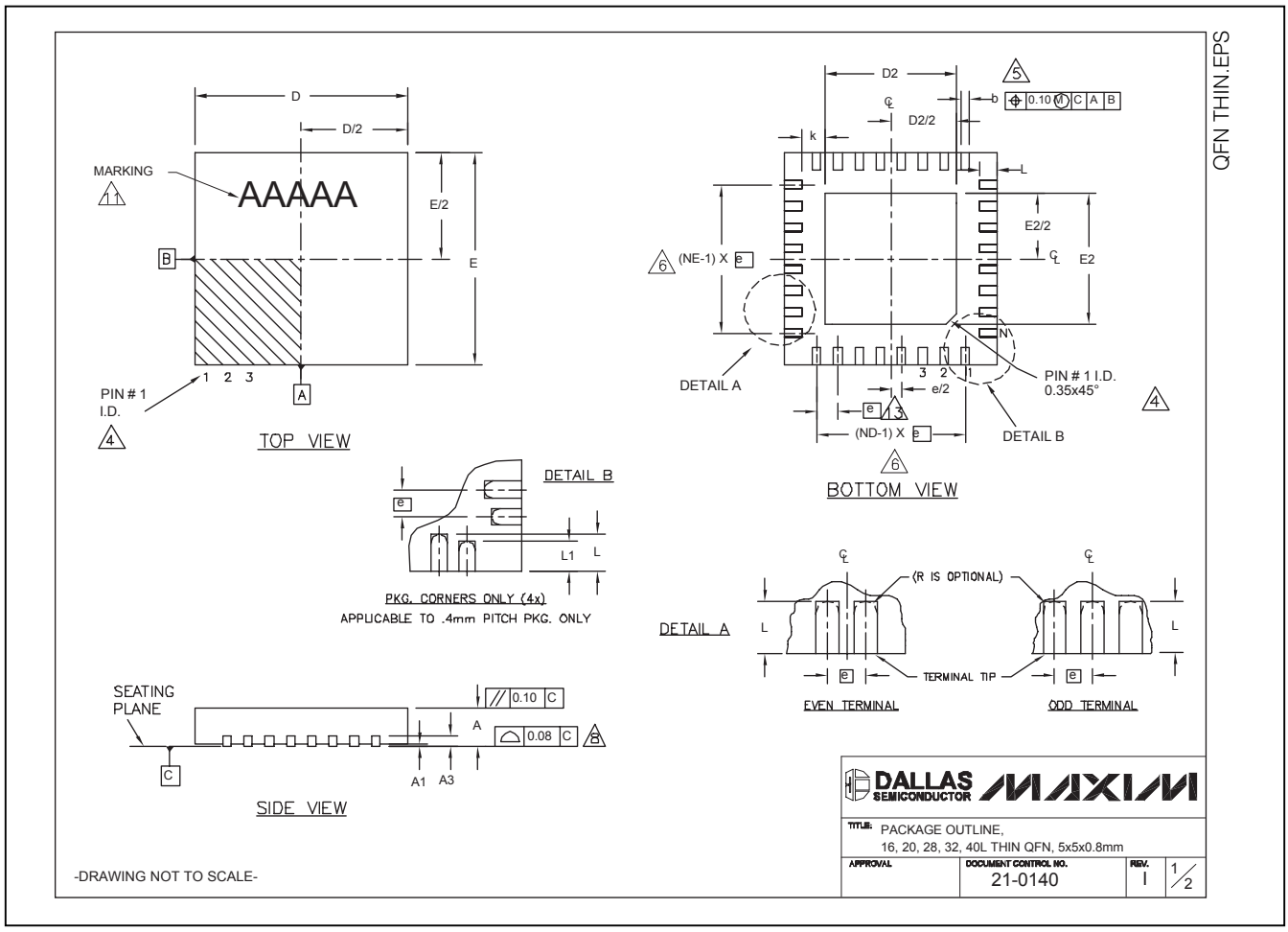
TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	G	1/1

Factory Programmable Single PLL Clock Generator

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			L (exceptions)	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	±0.15	
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	**	YES

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

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