19-1789; Rev 2; 1/12

Single/Dual, Ultra-Fast, ECL-Output Comparators with Latch Enable

General Description

The MAX9691/MAX9692/MAX9693 are ultra-fast ECL comparators capable of very short propagation delays. Their design maintains the excellent DC matching characteristics normally found only in slower comparators.

The MAX9691/MAX9692/MAX9693 have differential inputs and complementary outputs that are fully compatible with ECL-logic levels. Output current levels are capable of driving 50Ω terminated transmission lines. The ultra-fast operation makes signal processing possible at frequencies in excess of 600MHz.

The MAX9692/MAX9693 feature a latch-enable (LE) function that allows the comparator to be used in a sample-hold mode. When LE is ECL high, the comparator functions normally. When LE is driven ECL low, the outputs are forced to an unambiguous ECL-logic state, dependent on the input conditions at the time of the latch input transition. If the latch-enable function is not used on either of the two comparators, the appropriate LE input must be connected to ground; the companion $\overline{LE}$ input must be connected to a high ECL logic level.

These devices are available in SO, QSOP, and tiny µMAX® packages for added space savings.

Applications

High-Speed Line Receivers

Peak Detectors

Threshold Detectors

High-Speed Triggers

µMAX is a registered trademark of Maxim Integrated Products, Inc.

Features

- **1.2ns Propagation Delay**
- **100ps Propagation Delay Skew**
- **150ps Dispersion**
- **0.5ns Latch Setup Time**
- **0.5ns Latch-Enable Pulse Width**
- **Available in µMAX and QSOP Packages**
- **+5V, -5.2V Power Supplies**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9691EUA	-40°C to +85°C	8 µMAX
MAX9691ESA	-40°C to +85°C	8 SO
MAX9691EPA	-40°C to +85°C	8 PDIP

Note: *Devices are also available in lead(Pb)-free/RoHS-compliant packages. Specify lead-free by adding a "+" after the part number.*

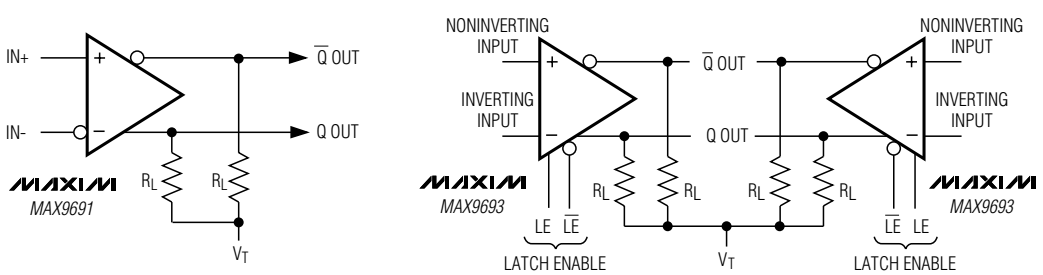
Ordering Information continued at the end of data sheet.

Selector Guide

PART	COMPARATORS PER PACKAGE	LATCH ENABLE	PIN-PACKAGE
MAX9691	1	No	8 µMAX, 8 SO, 8 PDIP
MAX9692	1	Yes	10 µMAX, 16 SO, 16 PDIP
MAX9693	2	Yes	16 QSOP, 16 SO, 16 PDIP

Pin Configurations appear at end of data sheet.

Functional Diagrams



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULLDOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω TO 200Ω CONNECTED TO -2.0V, OR 240Ω TO 2000Ω CONNECTED TO -5.2V.

Single/Dual, Ultra-Fast, ECL-Output Comparators with Latch Enable

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) .....-0.3V to +6V
Supply Voltage (V_{EE}) .....-6V to +0.3V
Input Voltage .....(V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Output Short-Circuit Duration .....Continuous
Differential Input Voltage .....±5V
Latch Enable .....(V_{EE} - 0.3V) to +0.3V
Output Current 50mA
Input Current .....±25mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX (derate 4.8mW/°C above 70°C).....387.8mW
8-Pin SO (derate 7.4mW/°C above +70°C).....588.2mW
8-Pin PDIP (derate 9.1mW/°C above +70°C).....727.3mW
10-Pin µMAX (derate 8.8mW/°C above +70°C).....707.3mW
16-Pin QSOP (derate 9.6mW/°C above +70°C) 771.5mW
16-Pin SO (derate 13.3mW/°C above +70°C) 1066.7mW
16-Pin PDIP (derate 10.5mW/°C above +70°C).....842.1mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5.2V, R_L = 50Ω to V_T, V_T = -2V, LE = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	T_A = +25°C	-6.5		6.5	mV
		T_A = T_{MIN} to T_{MAX}	-11.5		+11.5	
Temperature Coefficient	$\Delta V_{OS}/\Delta T$			10		µV/°C
Input Offset Current	I_{OS}	T_A = +25°C		0.2	5	µA
		T_A = T_{MIN} to T_{MAX}			8	
Input Bias Current	I_B	T_A = +25°C		6	20	µA
		T_A = T_{MIN} to T_{MAX}			30	
Input Voltage Range	V_{CM}	Note 1	-2.5		+3.0	V
Common-Mode Rejection Ratio	CMRR	-2.5V ≤ V_{CM} ≤ +3.0V (Note 1)	60	80		dB
Positive Power-Supply Rejection Ratio	+PSRR	4.5V ≤ V_{CC} ≤ 5.5V		60		dB
Negative Power-Supply Rejection Ratio	-PSRR	-5.7V ≤ V_{EE} ≤ -4.7V		60		dB
Open-Loop Gain	AOL	V_{CM} = 0V		70		dB
Differential Input Resistance	R_{IN}	-10mV < V_{IN} < 10mV		60		kΩ
Differential Input Clamp Voltage				1.7		V
Input Capacitance	C_{IN}			3		pF
Latch Enable Input Current High	$I_{IH(LE)}$	$V_{IH(LE)}$ = 1.1V		60	120	µA
Latch Enable Input Current Low	$I_{IL(LE)}$	$V_{IL(LE)}$ = 1.5V		0.2	10	µA
Latch Enable Logic High Voltage	$V_{IH(LE)}$		-1.1			V
Latch Enable Logic Low Voltage	$V_{IL(LE)}$				-1.5	V
Logic Output High Voltage	V_{OH}	T_A = T_{MIN}	-1.2		-0.87	V
		T_A = T_{MAX}	-0.99		-0.70	
		T_A = +25°C	-1.06		-0.76	
Logic Output Low Voltage	V_{OL}	T_A = T_{MIN}	-1.93		-1.57	V
		T_A = T_{MAX}	-1.89		-1.51	
		T_A = +25°C	-1.89		-1.55	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = -5.2V, R_L = 50Ω to V_T, V_T = -2V, LE = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	MAX9693	T_A = +25°C		34	46	mA
			T_A = T_{MIN} to T_{MAX}			50	
		MAX9691/ MAX9692	T_A = +25°C		18	26	
			T_A = T_{MIN} to T_{MAX}			36	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{EE} = -5.2V, R_L = 50Ω to V_T, V_T = -2V, LE = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MAX9691/MAX9692/MAX9693						
Propagation Delay (Notes 1, 2)	t_{pd+}, t_{pd-}	T_A = +25°C		1.2	1.8	ns
		T_A = T_{MIN} to T_{MAX}			2.0	
Rise/Fall Time	t_r, t_f	10% to 90%		500		ps
Propagation Delay Skew	Δ_{PD}			100		ps
Dispersion	P_{DSP}	V_{OD} from 10mV to 100mV		150		ps
MAX9692/MAX9693						
Latch-Enable Time (Note 1)	$T_{LE(\pm)}$	T_A = +25°C		1.0	1.8	ns
		T_A = T_{MIN} to T_{MAX}			2.0	
Latch-Enable Pulse Width (Note 1)	$t_{pw(LE)}$			0.5	1.0	ns
Setup Time (Note 1)	t_s			0.5	1.0	ns
Hold Time (Note 1)	t_h			0.5	1.0	ns
Channel-to-Channel Propagation Match	t_{PDM}	Note 2 (MAX9693 only)		100		ps

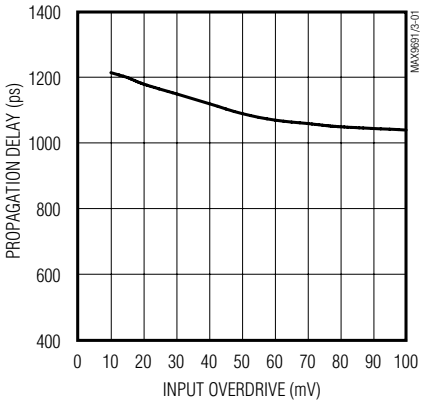
Note 1: Guaranteed by design.
Note 2: V_{IN} = 100mV, V_{OD} = 10mV.

Single/Dual, Ultra-Fast, ECL-Output Comparators with Latch Enable

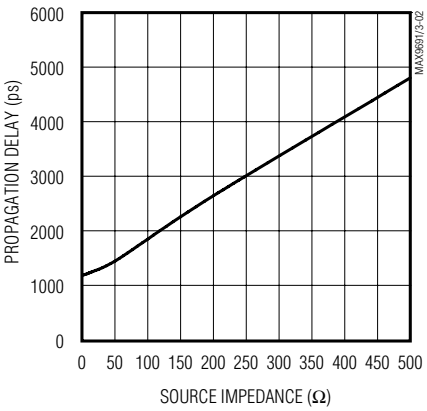
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5.2V, R_L = 50Ω to V_T, V_T = -2V, V_{OD} = 10mV, T_A = +25°C, unless otherwise noted.)

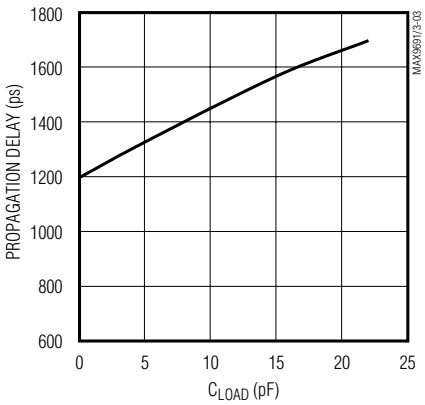
WORST-CASE PROPAGATION DELAY vs. INPUT OVERDRIVE



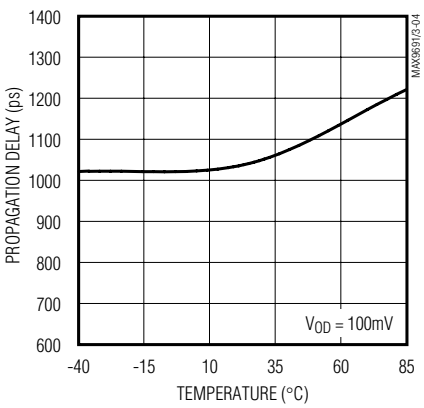
WORST-CASE PROPAGATION DELAY vs. SOURCE IMPEDANCE



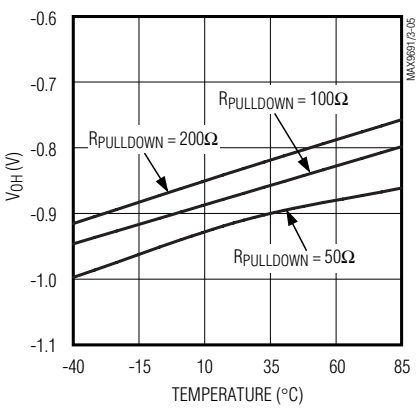
WORST-CASE PROPAGATION DELAY vs. C_{LOAD}



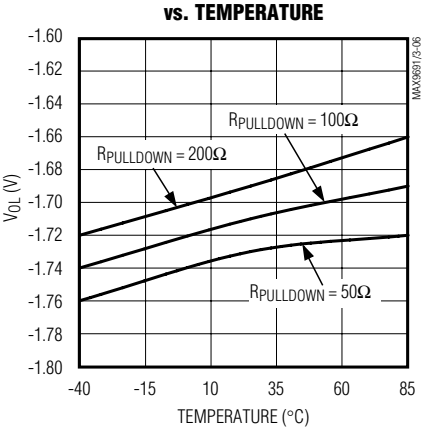
WORST-CASE PROPAGATION DELAY vs. TEMPERATURE



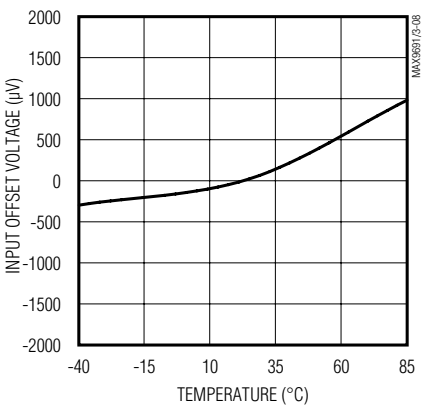
OUTPUT HIGH VOLTAGE vs. TEMPERATURE



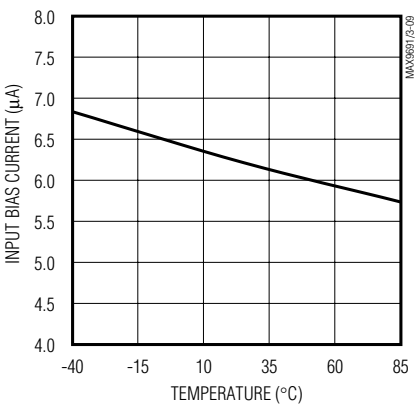
OUTPUT LOW VOLTAGE vs. TEMPERATURE



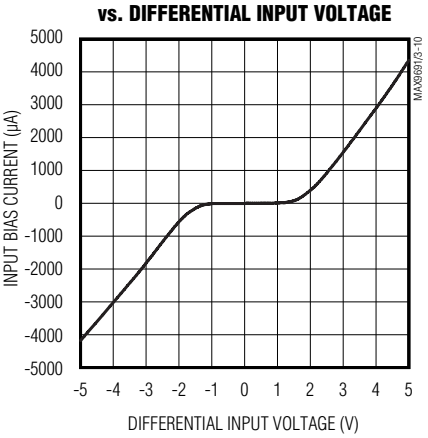
INPUT OFFSET VOLTAGE vs. TEMPERATURE



INPUT BIAS CURRENT vs. TEMPERATURE



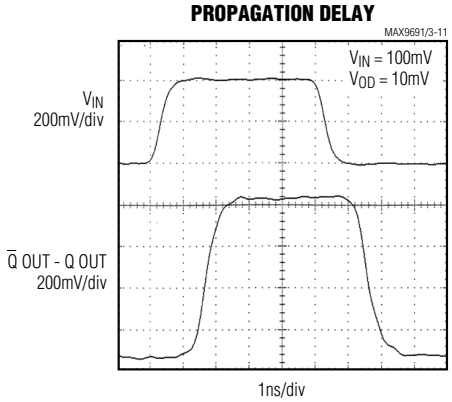
INPUT BIAS CURRENT vs. DIFFERENTIAL INPUT VOLTAGE



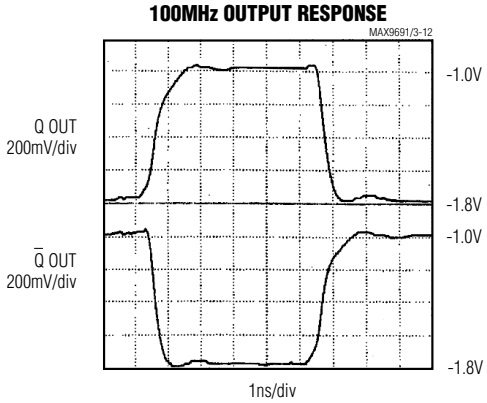
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5.2V, R_L = 50Ω to V_T, V_T = -2V, V_{OD} = 10mV, T_A = +25°C, unless otherwise noted.)

PROPAGATION DELAY



100MHz OUTPUT RESPONSE



Pin Description

PIN				NAME	FUNCTION
MAX9691	MAX9692 µMAX	MAX9692 PDIP/SO	MAX9693		
1	1	2	11	V_{CC}	Positive Supply. Bypass to GND with a 0.1µF capacitor.
2	2	3	—	IN+	Positive Input
3	3	4	—	IN-	Negative Input
4	6	8	6	V_{EE}	Negative Supply. Bypass to GND with a 0.1µF capacitor.
5	7	11	—	Q OUT	Output
6	8	12	—	$\overline{Q}$ OUT	Complimentary Output
7	9	16	—	GND2	Device Ground
8	10	1	—	GND1	Device Ground
—	4	5, 7, 9, 10, 13, 14, 15	—	N.C.	No Connection. Not internally connected.
—	5	6	—	LE	Latch Enable Input
—	—	—	1	Q OUTA	Channel A Output
—	—	—	2	$\overline{Q}$ OUTA	Channel A Complementary Output
—	—	—	3, 14	GND	Device Ground
—	—	—	4	LEA	Channel A Latch Enable Input
—	—	—	5	$\overline{LEA}$	Channel A Latch Enable Complementary Input
—	—	—	7	INA-	Channel A Negative Input
—	—	—	8	INA+	Channel A Positive Input
—	—	—	9	INB+	Channel B Positive Input
—	—	—	10	INB-	Channel B Negative Input
—	—	—	12	$\overline{LEB}$	Channel B Latch Enable Complementary Input
—	—	—	13	LEB	Channel B Latch Enable Input
—	—	—	15	$\overline{Q}$ OUTB	Channel B Complementary Output
—	—	—	16	Q OUTB	Channel B Output

Single/Dual, Ultra-Fast, ECL-Output Comparators with Latch Enable

Applications Information

Layout

Because of the MAX9691/MAX9692/MAX9693s' large gain-bandwidth characteristic, special precautions must be taken to use them. A PC board with a ground plane is mandatory. Mount 0.01µF ceramic decoupling capacitors as close to the power-supply pins as possible, and process the ECL outputs in microstrip fashion, consistent with the load termination of 50Ω to 200Ω (for V_T = -2V). For low-impedance applications, microstrip layout and terminations at the input may also be helpful. Pay close attention to the bandwidth of the decoupling and terminating components. Chip components can be used to minimize lead inductance. Connect GND1 and GND2 together to a solid copper ground plane for the MAX9691/MAX9692. GND1 biases the input gain stages, while GND2 biases the ECL output stage. If the LE function is not used, connect the LE pin to GND (MAX9692/MAX9693) and the complementary $\overline{LE}$ to ECL logic high level (MAX9693 only). Do not leave the inputs of an unused comparator floating for the MAX9693.

Input Slew-Rate Requirements

As with all high-speed comparators, the high gain-bandwidth product of these devices creates oscillation problems when the input goes through the linear region. For clean switching without oscillation or steps in the output waveform, the input must meet certain minimum slew-rate requirements. The tendency of the part to oscillate is a function of the layout and source impedance of the circuit employed. Poor layout and larger source impedance will increase the minimum slew-rate requirement.

Figure 1 shows a high-speed receiver application with 50Ω input and output termination. With this configuration, in which a ground plane and microstrip PC board are used, the minimum slew rate for clean output switching is 1V/µs.

In many applications, adding regenerative feedback will assist the input signal through the linear region, which will lower the minimum slew-rate requirement considerably. For example, with the addition of positive feedback components, R_f = 1kΩ and C_f = 10pF, the minimum slew-rate requirement can be reduced by a factor of four.

As high-speed receivers, the MAX9691/MAX9692/MAX9693 are capable of processing signals in excess of 600MHz. Figure 2 is a 100MHz example with an input signal level of 14mV_{RMS}.

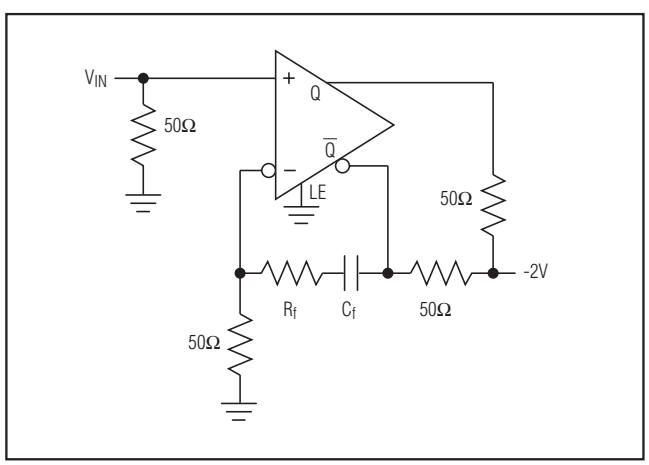


Figure 1. Regenerative Feedback—High-Speed Receiver with 50Ω Input and Output Termination

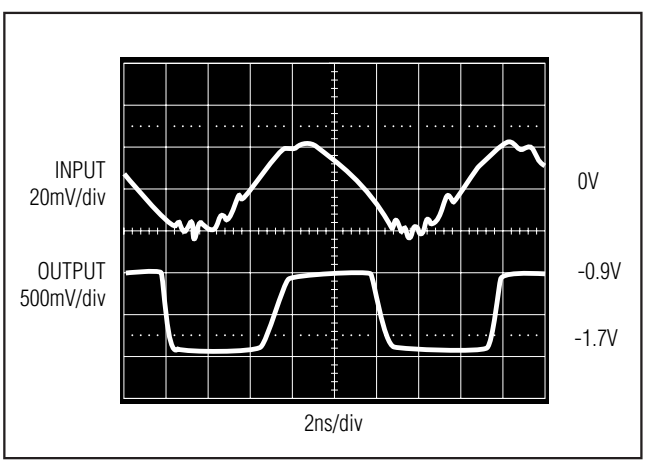


Figure 2. Signal Processed at 100MHz with Input Signal Level of 14mV_{RMS}

The timing diagram (Figure 3) illustrates the series of events that complete the compare function, under worst-case conditions. The top line of the diagram illustrates two latch-enable pulses. Each pulse is high for the compare function and low for the latch function. The first pulse demonstrates the compare function; part of the input action takes place during the compare mode. The second pulse demonstrates a compare function interval during which there is no change in the input.

The leading edge of the input signal (illustrated as a large-amplitude, small-overdrive pulse) switches the comparator after time interval t_{pd}. Output Q and $\overline{Q}$ transistors are similar in timing. The input signal must occur at time t_S before the latch falling edge, and must be maintained for time t_h after the edge to be acquired. After t_h, the output is no longer affected by the input status until the latch is again strobed. A minimum latch pulse width of $t_{pw(LE)}$ is needed for the strobe operation, and the output transitions occur after a time $t_{LE(\pm)}$.

The MAX9691/MAX9692/MAX9693 will not false trip (i.e., output invert) if one of the inputs is in the valid common-mode range while the other input is outside the common-mode range.

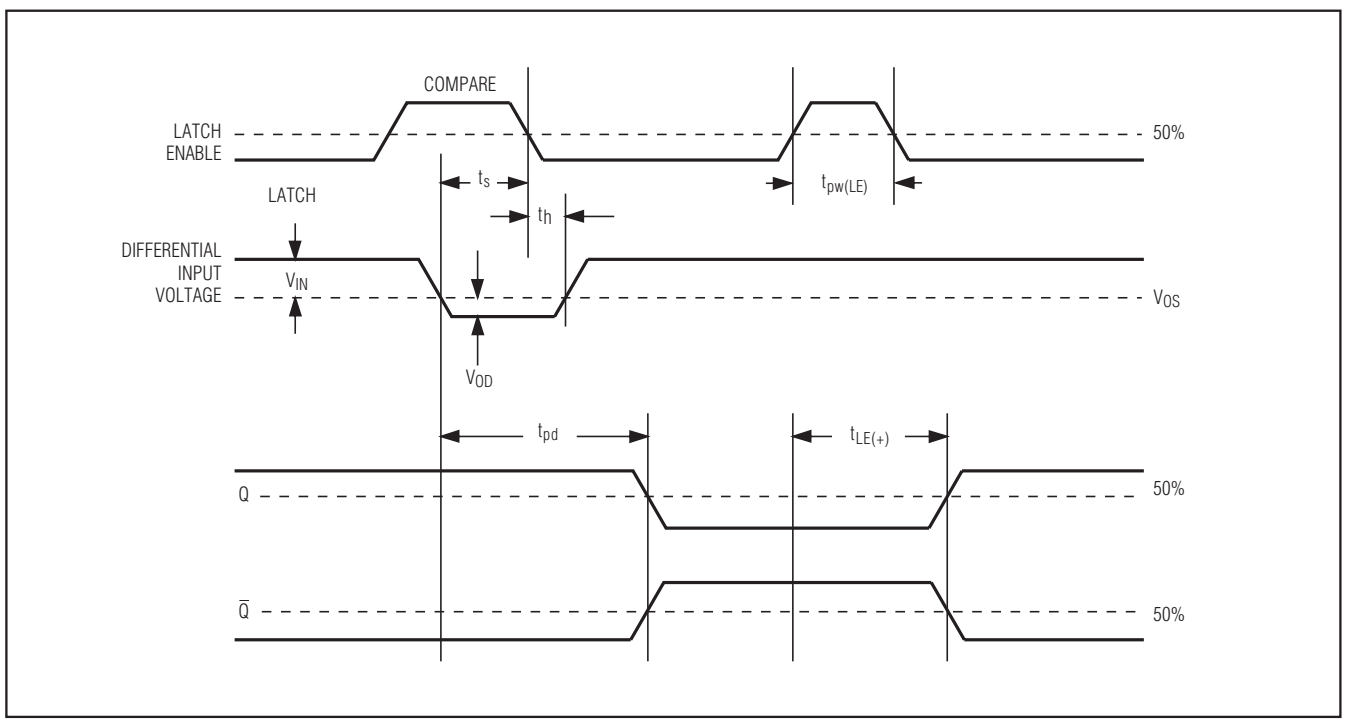


Figure 3. Timing Diagram

Single/Dual, Ultra-Fast, ECL-Output Comparators with Latch Enable

Definition of Terms

V_{OS} Input Offset Voltage. The voltage required between the input terminals to obtain 0V differential at the output.

V_{IN} Input Voltage Pulse Amplitude

V_{OD} Input Voltage Overdrive

t_{pd+} Input to Output High Delay. The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output low-to-high transition.

t_{pd-} Input to Output Low Delay. The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output high-to-low transition.

$t_{LE(+)}$ Latch-Enable to Output High Delay. The propagation delay measured from the 50% point of the latch-enable signal low-to-high transition to the 50% point of an output low-to-high transition.

$t_{LE(-)}$ Latch-Enable to Output Low Delay. The propagation delay measured from the 50% point of the latch-enable signal low-to-high transition to the 50% point of an output high-to-low transition.

$t_{pw(LE)}$ Latch-Enable Pulse Width. The minimum time the latch-enable signal must be high to acquire and hold an input signal.

t_s Setup Time. The minimum time before the negative transition of the latch-enable pulse that an input signal must be present to be acquired and held at the outputs.

t_h Hold Time. The minimum time after the negative transition of the latch-enable signal that an input signal must remain unchanged to be acquired and held at the output.

Δ_{pd} Propagation Delay Skew. The difference in propagation delay between the Q and $\overline{Q}$ outputs crossing each other in both directions.

P_{DSP} Propagation Delay Dispersion. The change in propagation delay as a result of the overdrive of the input signal varying.

t_{pdm} Propagation Delay Match (MAX9693 only). The difference in propagation delay between two separate channels.

Chip Information

PROCESS: BiCMOS

Ordering Information (continued)

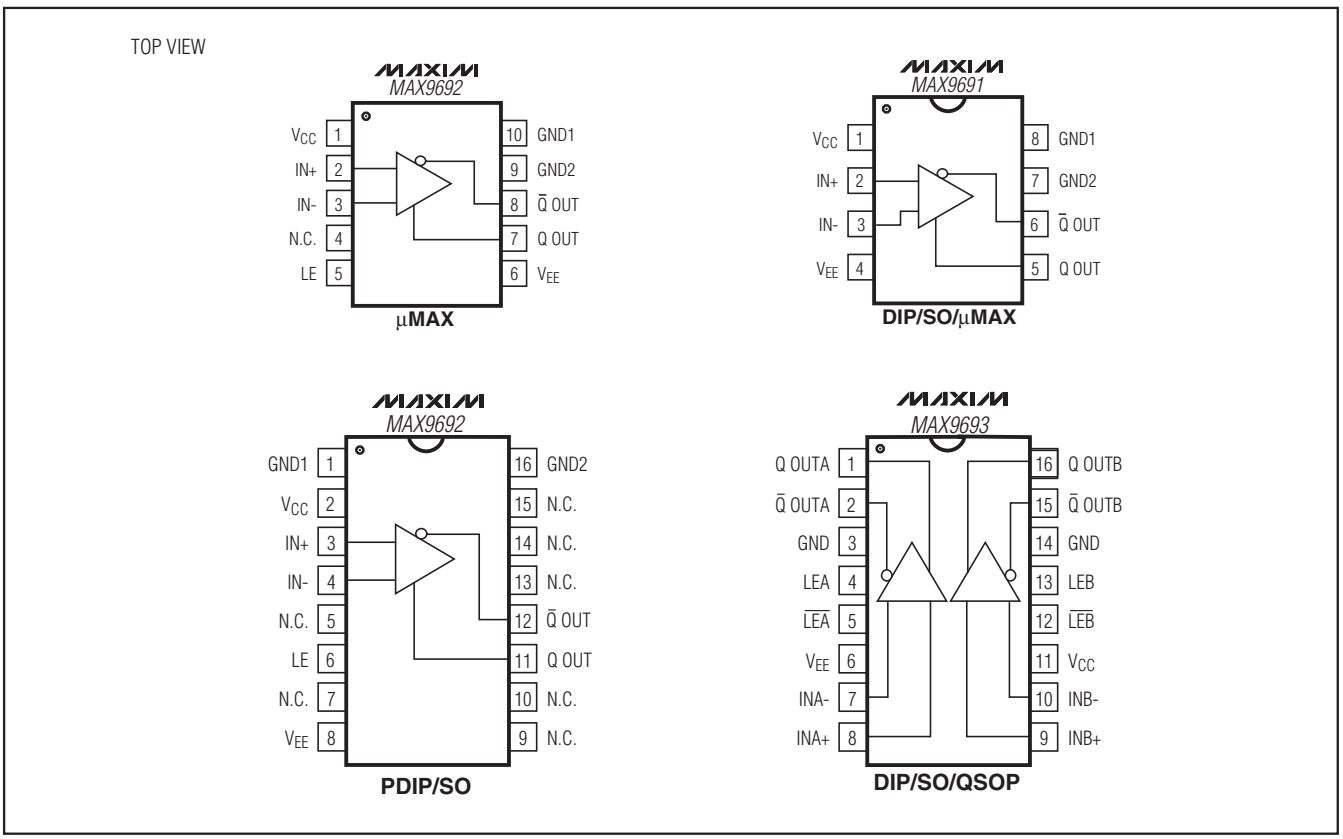
PART	TEMP RANGE	PIN-PACKAGE
MAX9692EUB	-40°C to +85°C	10 µMAX
MAX9692ESE	-40°C to +85°C	16 Narrow SO
MAX9692EPE	-40°C to +85°C	16 PDIP
MAX9693ESE	-40°C to +85°C	16 Narrow SO
MAX9693EEE	-40°C to +85°C	16 QSOP
MAX9693EPE	-40°C to +85°C	16 PDIP

Note: *Devices are also available in lead(Pb)-free/RoHS-compliant packages. Specify lead-free by adding a "+" after the part number.*

Single/Dual, Ultra-Fast, ECL-Output Comparators with Latch Enable

Pin Configurations

TOP VIEW



Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 µMAX	U8+1	21-0036	90-0092
8 SO	S8+2	21-0041	90-0096
8 PDIP	P8+5	21-0043	—
10 µMAX	U10+2	21-0061	90-0330
16 QSOP	E16+1	21-0055	90-0167
16 SO	S16+3	21-0041	90-0097
16 PDIP	P16+1	21-0043	—

Single/Dual, Ultra-Fast, ECL-Output Comparators with Latch Enable

Package Information (continued)

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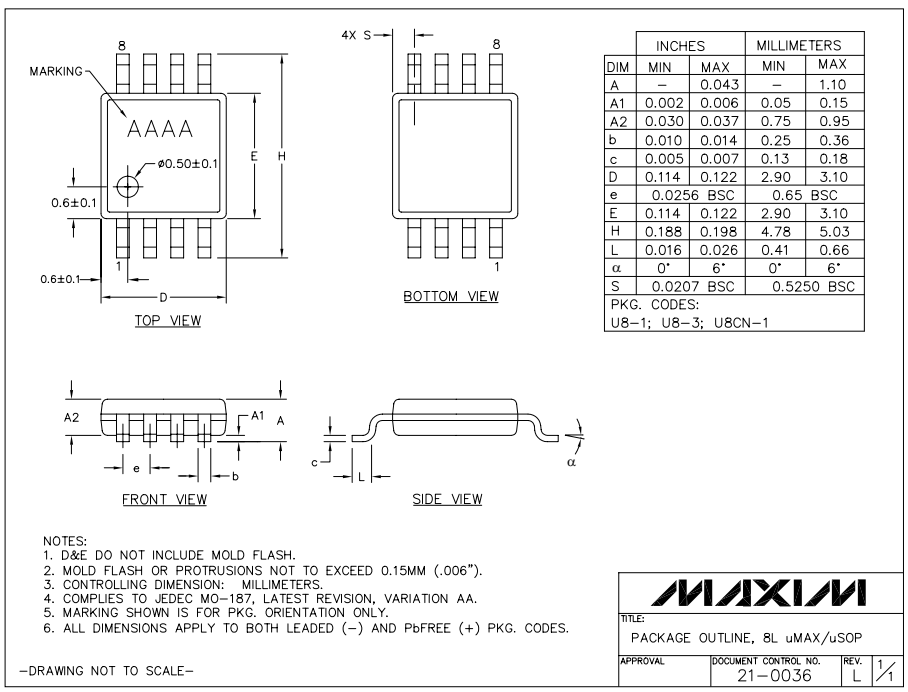


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	–	0.043	–	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.114	0.122	2.90	3.10
e	0.0256 BSC		0.65 BSC	
E	0.114	0.122	2.90	3.10
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC	
PKG. CODES: U8-1; U8-3; U8CN-1				

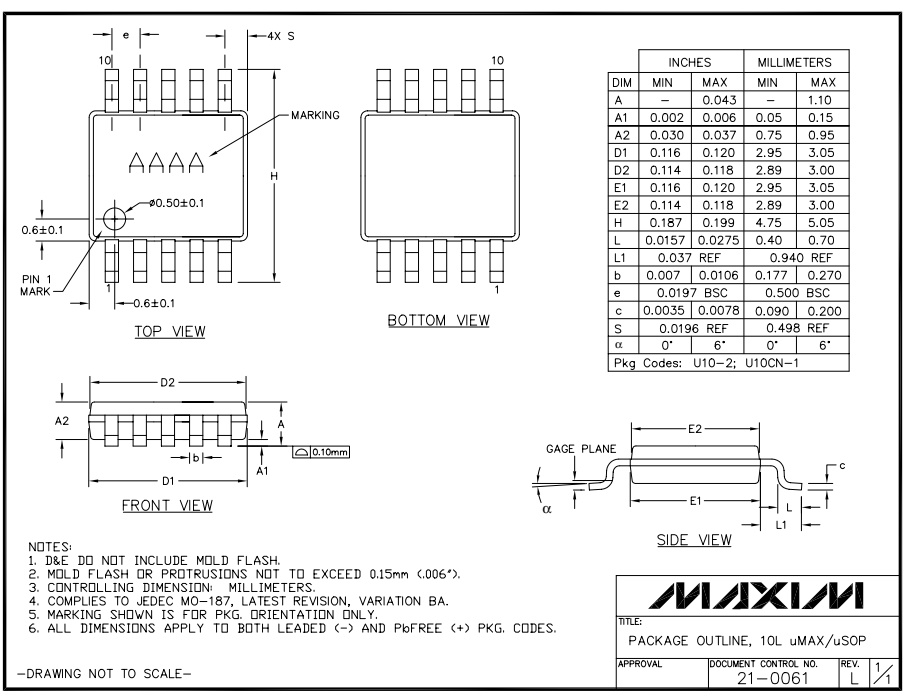
NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COMPLIES TO JEDEC MO-187, LATEST REVISION, VARIATION AA.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

MAXIM

TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0036	L	1/1



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	–	0.043	–	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°
Pkg Codes: U10-2; U10CN-1				

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COMPLIES TO JEDEC MO-187, LATEST REVISION, VARIATION BA.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

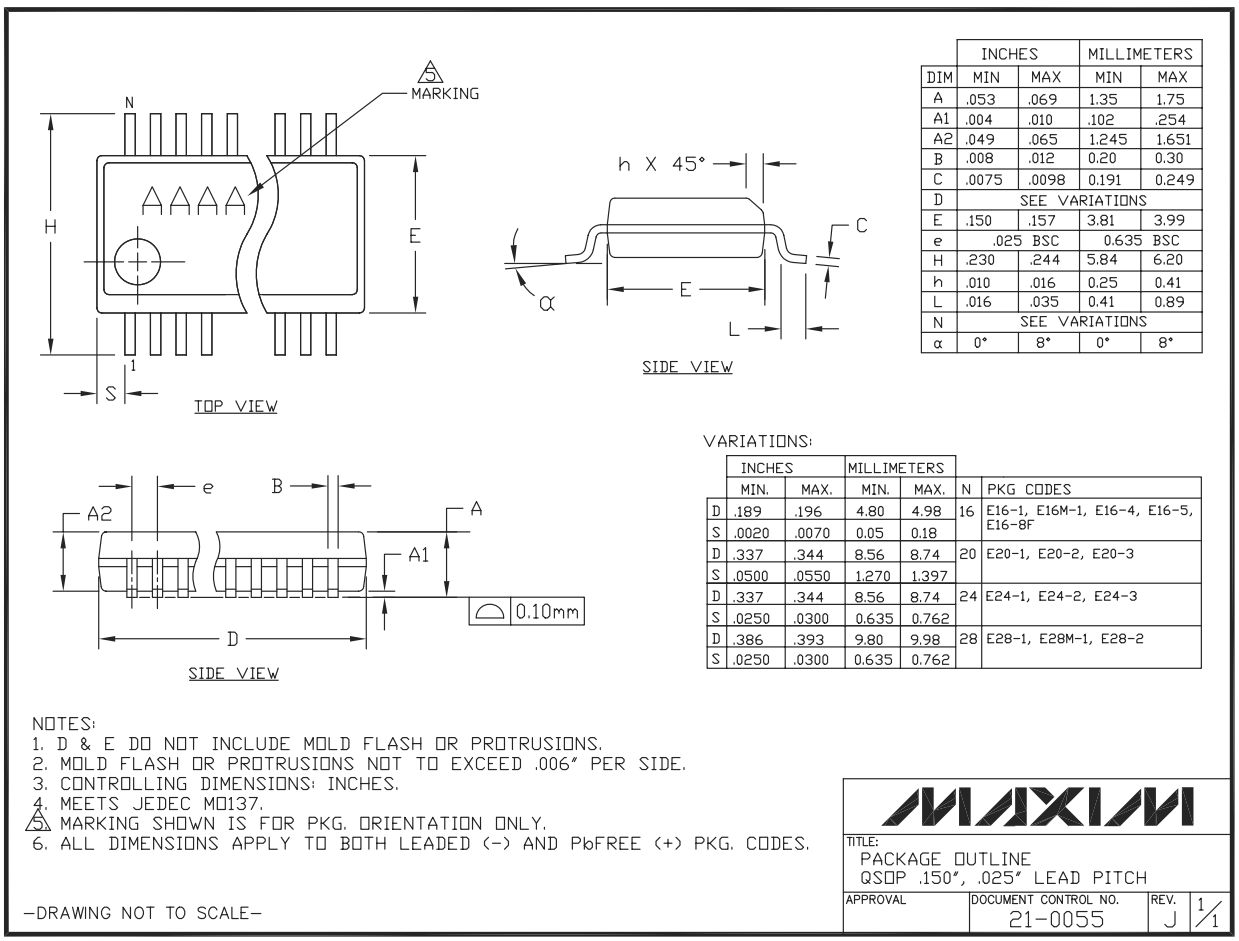
MAXIM

TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0061	L	1/1

Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.102	.254
A2	.049	.065	1.245	1.651
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	PKG CODES
D	.189	.196	4.80	4.98	16	E16-1, E16M-1, E16-4, E16-5, E16-8F
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	E20-1, E20-2, E20-3
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	E24-1, E24-2, E24-3
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	E28-1, E28M-1, E28-2
S	.0250	.0300	0.635	0.762		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. CONTROLLING DIMENSIONS: INCHES.
4. MEETS JEDEC MO137.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

—DRAWING NOT TO SCALE—

MAXIM

TITLE:
PACKAGE OUTLINE
QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	J	1/1

Single/Dual, Ultra-Fast, ECL-Output Comparators with Latch Enable

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/00	Initial release	—
1	10/02	Updated Ordering Information.	7
2	1/12	Revised *Ordering Information*, *Absolute Maximum Ratings*, and *Pin Description*.	1, 2, 5, 7

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