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MAX98050 Low-Power, High-Performance Audio Codec

General Description

The MAX98050 is a low-power, high-performance audio CODEC with integrated low-latency digital filters for wireless hearables, headsets, and headphones.

The device features a mono playback channel with a 5-band biquad equalizer and a high-efficiency, fully differential hybrid class-AB/class-D headphone amplifier. The playback headphone amplifier is optimized for extremely low output noise levels and minimized quiescent power consumption while maximizing output power efficiency.

The device includes three microphone input channels capable of supporting voice, ambient, and anti-noise record use cases. Each channel can individually record from either an external analog or digital microphone, and then can route audio data to both the record channels (to the digital audio interface) and the internal low-latency digital filter channels. A fourth record channel to the digital audio interface is provided to allow the host to monitor the playback channel output digital data.

Two low-latency, digital filter channels are provided that can support a variety of use cases. These include noise cancellation applications (feed-forward, feedback, and hybrid filter profiles), both voice and ambient enhancement and transparency applications, and sidetone applications. Each channel provides a 12-band digital biquad filter, a DRC or Limiter stage, a digital volume control block, and an ultrasound filter. In addition, a third internal digital filter channel is provided in the playback channel that is structured for playback compensation and/or general feedback compensation filters. This channel includes a 10-band biquad filter and a digital volume control block. To support dynamic or adaptive filter and use case transitions, the biquad filters and volume controls provide banked profiles that can be updated/swapped without disruption to audio playback.

The flexible digital audio interface supports common PCM audio data formats such as I^2S, left-justified, and TDM timing with 16-bit, 24-bit, or 32-bit data word and channel lengths. The PCM interface supports playback sample rates from 8kHz to 192kHz and record sample rates from 8kHz to 48kHz. The device requires external bit and frame clocks but eliminates the need for a high-speed external master clock.

The device is available in a small 6.7mm^2 36-bump WLP package (0.4mm pitch) with a low 0.5mm height ideal for tight form factors. The device operates over the extended -40°C to +85°C temperature range.

Applications

- True Wireless Hearables and Headsets
- Stereo Bluetooth Headsets and Headphones
- Mono Bluetooth Earpieces
- PSAP Devices and Hearing Assist Devices
- VR/AR Headsets and Head-Mounted Devices

Benefits and Features

- Low-Latency Digital Filter Channels
  - 96kHz/192kHz/384kHz Sample Rate Options
  - Channel Support Applications Including Feed-Forward (FF) and Feedback (FB) ANC, Ambient/Voice Enhancement and Transparency, and Playback Compensation
  - Filters Allowing Smooth, Dynamic Transitions / Updates without Playback Disruption
- Mono Headphone Playback Channel
  - High-Efficiency Hybrid Class-AB/D Amplifier
  - 114dB Playback Dynamic Range
  - 2.55mW P_Q (f_S = 48kHz, No Noise Gate)
  - 1.9mW P_Q (f_S = 48kHz, With Noise Gate)
- Three Microphone Record Channels
  - Analog or Digital Microphone Inputs
  - 107dB Dynamic Range (AMIC Single-Ended)
  - 113dB Dynamic Range (AMIC Differential))
  - 5.3mW P_Q (f_S = 16kHz, 2 AMIC Record)
  - 2.1mW P_Q (f_S = 16kHz, 2 DMIC Record)
- Playback with ANC Filter Profile (f_S = 192kHz)
  - 9.85mW P_Q (AMIC FF+FB Profile)
  - 6.7mW P_Q (AMIC FF Only Profile)
  - 7mW P_Q (DMIC FF+FB Profile)
- Full-Scale Playback Power at 1% THD+N:
  - 31mW into 32Ω ($1V_{RMS}$ Full-Scale Mode)
  - 15mW into 32Ω (Reduced Swing Mode)
  - 61mW into 16Ω ($1V_{RMS}$ Full-Scale Mode)
- Flexible I^2S/TDM Digital Audio Interface
  - Support for 16/24/32-Bit Audio Data
  - Playback Sample Rates of 8kHz to 192kHz
  - No High-Speed Master Clock Required
- Audio CODEC Evaluation Platform Available
  - Includes Maxim Reference Headset Design
- 6.7mm^2 36-Bump WLP Package
  - 0.4mm Pitch with a 0.5mm Height

***Ordering Information* appears at end of data sheet.**

19-100956; Rev 0; 11/20

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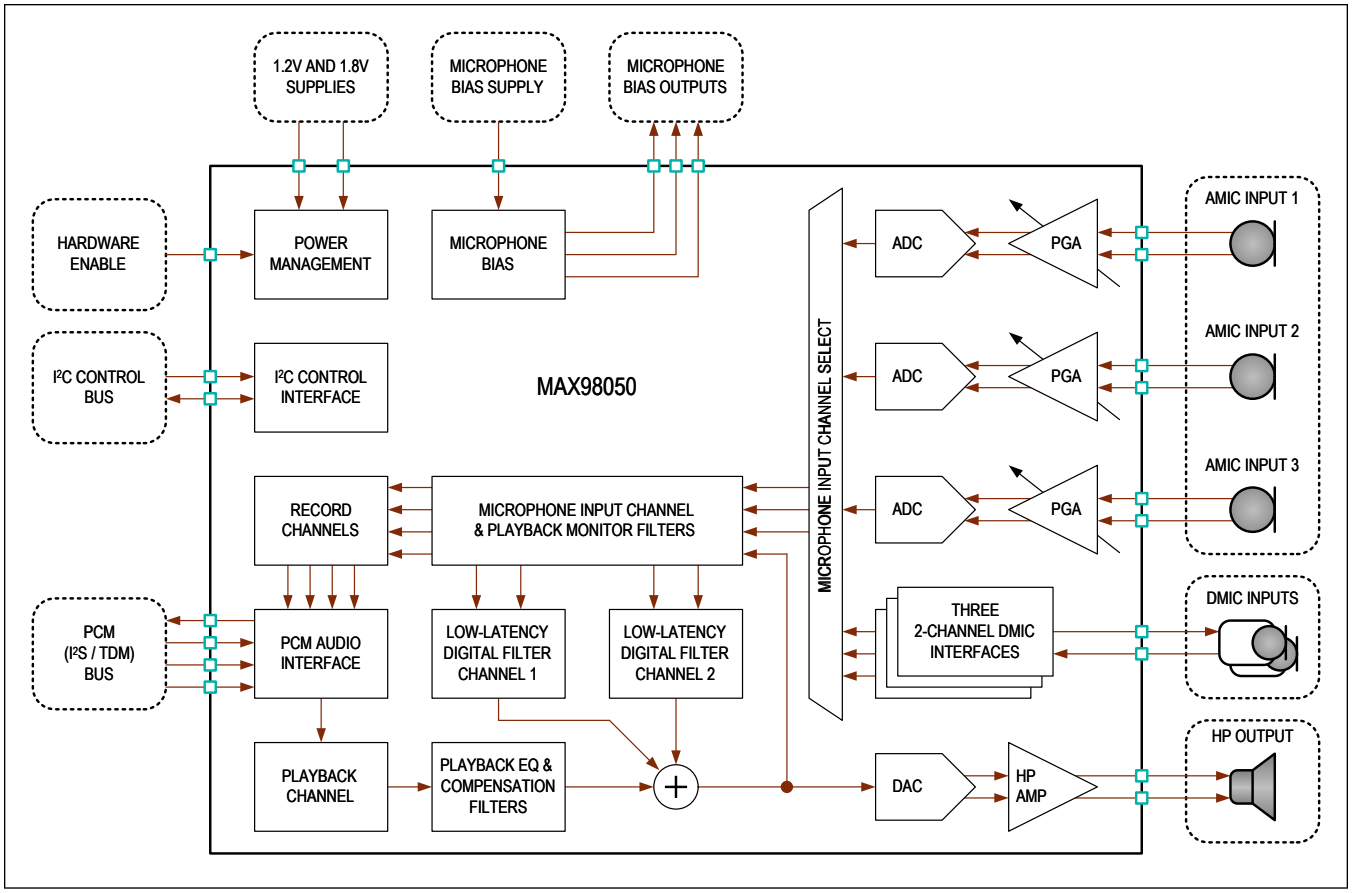
Simplified Block Diagram



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Absolute Maximum Ratings

DGND to GND ..... -0.1V to +0.1V
MBVDD to GND ..... -0.3V to +5.5V
MICBIAS to GND ..... -0.3V to V_{MBVDD} + 0.3V
AVDD1 to GND ..... -0.3V to +2.2V
AVDD2 to GND ..... -0.3V to +1.85V
AVDD3 to DGND ..... -0.3V to +1.85V
AVDD1_REG to GND ..... -0.3V to +1.85V
DVDDIO to DGND ..... -0.3V to +2.2V
DVDD to DGND ..... -0.3V to +1.85V
INPn, INNn to GND ..... -0.3V to V_{AVDD1} + 0.3V
OUTP, OUTN to GND ..... -0.3V to V_{AVDD1} + 0.3V
MICBIASn to GND ..... -0.3V to V_{MBVDD} + 0.3V
SCL, SDA, ADDR to DGND ..... -0.3V to +2.2V
All Other Pins ..... -0.3V to V_{DVDDIO} + 0.3V
Short-Circuit of OUTP/OUTN and AVDDn ..... Continuous
Short-Circuit of OUTP/OUTN and AVDD1_REG ..... Continuous
Short-Circuit of OUTP/OUTN and GND/DGND ..... Continuous
Short-Circuit of OUTP and OUTN ..... Continuous
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 21.87mW/°C above +70°C) 1.75W
Junction Temperature ..... +150°C
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

36-WLP

Package Code	N362F2+1
Outline Number	21-100518
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	45.72°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM / POWER SUPPLIES						
Power Supply Voltage Range	V_{MBVDD}		1.3	3.6	4.8	V
	V_{AVDD1}		1.71	1.8	1.95	
	V_{AVDD2}		1.1	1.2	1.3	
	V_{AVDD3}		1.1	1.2	1.3	
	V_{DVDDIO}	1.8V digital interface mode	1.65	1.8	1.95	
		1.2V digital interface mode	1.1	1.2	1.3	
	V_{DVDD}		1.1	1.2	1.3	
AVDD1 Undervoltage Lockout Threshold		V_{AVDD1} falling	1.24		1.46	V

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AVDD2 Undervoltage Lockout Threshold		V_{AVDD2} falling	0.85		1.01	V
AVDD3 Undervoltage Lockout Threshold		V_{AVDD3} falling	0.85		1.01	V
DVDD Undervoltage Lockout Threshold		V_{DVDD} falling	0.85		1.01	V
DVDDIO Undervoltage Lockout Threshold		V_{DVDDIO} falling	0.85		1.01	V
AVDD1 UVLO Hysteresis		(Note 2)	90			mV
AVDD2 UVLO Hysteresis		(Note 2)	24			mV
AVDD3 UVLO Hysteresis		(Note 2)	24			mV
DVDD UVLO Hysteresis		(Note 2)	24			mV
DVDDIO UVLO Hysteresis		(Note 2)	24			mV
SYSTEM / QUIESCENT POWER CONSUMPTION / AUDIO PLAYBACK						
Quiescent Supply Current	I_{Q_DVDD}	High-performance mode, playback at 48kHz, audio playback silent (dither disabled), P_{OUT} = 0mW, Z_{LOAD} = 32Ω + 33µH		1.6	2.2	mA
		High-performance mode, playback at 48kHz, audio playback silent, clock and data monitor enable, P_{OUT} = 0mW, Z_{LOAD} = 32Ω + 33µH		1.7		
	I_{Q_DVDDIO}	High-performance mode, playback at 48kHz, audio playback silent, P_{OUT} = 0mW, Z_{LOAD} = 32Ω + 33µH		0.01		
	I_{Q_AVDD1}			0.03	0.06	
	I_{Q_AVDD2}			0.45	0.75	
	I_{Q_AVDD3}			0.012	0.04	
	I_{Q_AVDD2}	Low-power mode, playback at 48kHz, audio playback silent, P_{OUT} = 0mW, Z_{LOAD} = 32Ω + 33µH		0.37		

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM / QUIESCENT POWER CONSUMPTION / AUDIO PLAYBACK WITH LOW-LATENCY DIGITAL FILTER CHANNELS						
Quiescent Supply Current	I_{Q_DVDD}	High-performance playback and record, playback at 48kHz, stereo AMIC to low-latency digital filter channels at 192kHz, hybrid ANC tuning profile with typical number of biquad filter bands active (8 bands in DF1/DF2 and 6 bands in PBC), audio playback silent (dither disabled), AMIC record silent, P_{OUT} = 0mW, Z_{LOAD} = 32Ω + 33µH		5.16	7.6	mA
	I_{Q_DVDDIO}			0.013		
	I_{Q_AVDD1}			2.18	3.6	
	I_{Q_AVDD2}			0.45	0.75	
	I_{Q_AVDD3}			0.012	0.04	
	I_{Q_AVDD1}	Low-power playback and record, playback at 48kHz, stereo AMIC to low-latency digital filter channels at 192kHz, hybrid ANC tuning profile with typical number of biquad filter bands active (8 bands in DF1/DF2 and 6 bands in PBC), audio playback silent (dither disabled), AMIC record silent, P_{OUT} = 0mW, Z_{LOAD} = 32Ω + 33µH		1.7		
	I_{Q_AVDD2}			0.37		
SYSTEM / QUIESCENT POWER CONSUMPTION / AUDIO PLAYBACK WITH STEREO RECORD						
Quiescent Supply Current	I_{Q_DVDD}	High-performance record and playback modes, playback and stereo AMIC record at 48kHz, audio playback silent (dither disabled), record silent, P_{OUT} = 0mW, Z_{LOAD} = 32Ω + 33µH		2.85	4	mA
	I_{Q_DVDDIO}			0.013		
	I_{Q_AVDD1}			2.18	3.6	
	I_{Q_AVDD2}			0.45	0.75	
	I_{Q_AVDD3}			0.012	0.04	
	I_{Q_AVDD1}	Low-power record and playback modes, playback and stereo AMIC record at 48kHz, audio playback silent (dither disabled), record silent, P_{OUT} = 0mW, Z_{LOAD} = 32Ω + 33µH		1.7		
	I_{Q_AVDD2}			0.37		

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM / SOFTWARE SHUTDOWN POWER CONSUMPTION						
Software Shutdown Supply Current	I_{MBVDD_SW}	V_{MBVDD} = 3.6V, software shutdown state, digital interfaces not driven, T_A = +25°C		0.08	3	µA
	I_{DVDDIO_SW}	V_{DVDDIO} = 1.8V, software shutdown state, digital interfaces not driven, T_A = +25°C		0.18	3	
	I_{DVDD_SW}	V_{DVDD} = 1.2V, software shutdown state, digital interfaces not driven, T_A = +25°C		0.55	2	
	I_{AVDD1_SW}	V_{AVDD1} = 1.8V, software shutdown state, digital interfaces not driven, T_A = +25°C		1	3	
	I_{AVDD2_SW}	V_{AVDD2} = 1.2V, software shutdown state, digital interfaces not driven, T_A = +25°C		0.05	2	
	I_{AVDD3_SW}	V_{AVDD3} = 1.2V, software shutdown state, digital interfaces not driven, T_A = +25°C		0.09	2	
SYSTEM / HARDWARE SHUTDOWN POWER CONSUMPTION						
Hardware Shutdown Supply Current	I_{MBVDD_HW}	V_{MBVDD} = 3.6V, hardware shutdown state, digital audio interfaces not driven, T_A = +25°C		0.01	3	µA
	I_{DVDDIO_HW}	V_{DVDDIO} = 1.8V, hardware shutdown state, digital audio interfaces not driven, T_A = +25°C		0.01	3	
	I_{DVDD_HW}	V_{DVDD} = 1.2V, hardware shutdown state, digital audio interfaces not driven, T_A = +25°C		0.55	2	
	I_{AVDD1_HW}	V_{AVDD1} = 1.8V, hardware shutdown state, digital audio interfaces not driven, T_A = +25°C		0.1	3	
	I_{AVDD2_HW}	V_{AVDD2} = 1.2V, hardware shutdown state, digital audio interfaces not driven, T_A = +25°C		0.05	2	
	I_{AVDD3_HW}	V_{AVDD3} = 1.2V, hardware shutdown state, digital audio interfaces not driven, T_A = +25°C		0.09	2	
ENABLE / DISABLE TIMING						
Hardware Enable Time	t_{HW_EN}	Transition time from hardware shutdown to software shutdown (Initialization Done interrupt) (Note 3)			2.5	ms
Hardware Disable Assert Time	t_{HW_DIS}	Minimum time HW_EN must be asserted low to ensure the device transitions to hardware shutdown (Note 3)	1			µs

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Audio Turn-On Time	t_{ON}	Transition time from software shutdown to audio record and playback with digital filter channels active (Record and Playback Power-Up Done interrupts), volume ramping disabled	AMIC_CT_SEL = 0x0		3.7	4	ms
			AMIC_CT_SEL = 0x1		5.2	6	
			AMIC_CT_SEL = 0x2		9.2	10	
			AMIC_CT_SEL = 0x3		17.2	18	
Audio Turn-On Time with Ramping	t_{ON}	Transition time from software shutdown to audio playback with digital filter channels disabled or muted (Playback Power-Up Done interrupt), playback volume ramping enabled at 4ms, AMIC_CT_SEL = 0x1			9.2	10	ms
Audio Turn-On Time for Dynamic Record Channel Enable	t_{ON_REC}	Device already in audio state, time from dynamically setting RECn_PCM_EN high until record channel active with valid data (Note 4)			1.3	2	ms
Audio Turn-Off Time	t_{OFF}	Transition time from audio record and/or playback with digital filter channels active into software shutdown (Power Down Done interrupt), volume ramping disabled			0.01	0.1	ms
Audio Turn-Off Time with Ramping	t_{OFF}	Transition time from audio record and/or playback with digital filter channels muted or disabled into software shutdown (Power Down Done interrupt), playback volume ramping enabled at 4ms			4.4	4.5	ms

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG MICROPHONE INPUT TO ADC RECORD						
Dynamic Range	DR	PGA gain = +6dB, single-ended or differential input, AMICn_PGA_RIN = 1, DRE enabled (Note 5)		104		dB
		PGA gain = +3dB, single-ended or differential input, AMICn_PGA_RIN = 0, DRE enabled (Note 5)		104		
		PGA gain = +3dB, single-ended or differential input, AMICn_PGA_RIN = 1, DRE enabled (Note 5)		107		
		PGA gain = 0dB, differential input, AMICn_PGA_RIN = 1, DRE enabled (Note 5)		110		
		PGA gain = -3dB, differential input, AMICn_PGA_RIN = 1, DRE enabled (Note 5)		113		
Total Harmonic Distortion + Noise	THD+N	PGA gain = +6dB, single-ended or differential input, f_{IN} = 1kHz, -6dBFS digital output, high-performance mode		-82	-75	dB
		PGA gain = +6dB, single-ended or differential input, f_{IN} = 1kHz, -6dBFS digital output, low-power mode		-80		
		PGA gain = +0dB, differential input, f_{IN} = 1kHz, -6dBFS digital output, high performance mode (Note 2)		-82	-75	
		PGA gain = +21dB, single-ended or differential input, f_{IN} = 1kHz, -6dBFS digital output, high performance mode		-78		
Crosstalk		Between any pair of record channels, f_{IN} = 1kHz		-120		dB
Common Mode Rejection Ratio	CMRR	PGA Gain = 0dB, V_{IN_CM} = 100mV_{PP}, f_{IN_CM} = 217Hz		75		dB
ANALOG MICROPHONE INPUT TO ADC RECORD / PROGRAMMABLE GAIN AMPLIFIER (PGA)						
Full-Scale Input Voltage	V_{FS}	PGA gain = +6dB, single-ended or differential input, THD+N ≤ -40dB		0.5		V_{RMS}
		PGA gain = +3dB, single-ended or differential input, THD+N ≤ -40dB		0.707		
		PGA gain = 0dB, differential input, THD+N ≤ -40dB		1		
		PGA gain = -3dB, differential input, THD+N ≤ -40dB		1.414		

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Disabled AMIC Preamp Input Resistance	$R_{IN\_PA\_OFF}$	Measured single-ended to ground, device in software shutdown or AMIC preamp disabled, AMICn_PGA_HIZ_EN = 1 (Note 5)	100	200		kΩ
Active AMIC Preamp Input Resistance	$R_{IN\_PA\_ON}$	Measured single-ended to ground, device in active state and AMIC preamp enabled, AMICn_PGA_RIN = 0 (Note 5)	28	35		kΩ
		Measured single-ended to ground, device in active state and AMIC preamp enabled, AMICn_PGA_RIN = 1 (Note 5)	8	10		
Minimum PGA Gain		AMICn_PGA_GAIN = 0x0 (Note 5)	-6.5	-6	-5.5	dB
Maximum PGA Gain		AMICn_PGA_GAIN = 0x9 (Note 5)	20.5	21	21.5	dB
ANALOG MICROPHONE INPUT TO ADC RECORD / POWER SUPPLY REJECTION						
Power Supply Rejection Ratio	PSRR	V_{AVDD1} = 1.71V to 1.95V		90		dB
		V_{RIPPLE} = 100mV_{P-P} on AVDD1, f_{RIPPLE} = 217Hz		110		
		V_{RIPPLE} = 100mV_{P-P} on AVDD1, f_{RIPPLE} = 1kHz		110		
		V_{RIPPLE} = 100mV_{P-P} on AVDD1, f_{RIPPLE} = 20kHz		95		
		V_{AVDD2} = 1.71V to 1.95V		95		
		V_{RIPPLE} = 100mV_{P-P} on AVDD2, f_{RIPPLE} = 217Hz		95		
		V_{RIPPLE} = 100mV_{P-P} on AVDD2, f_{RIPPLE} = 1kHz		95		
		V_{RIPPLE} = 100mV_{P-P} on AVDD2, f_{RIPPLE} = 20kHz		90		
MICROPHONE BIAS GENERATOR						
Output Voltage	$V_{MICBIAS}$	AMIC_BIAS_SEL = 0x0	1.1	1.2	1.3	V
		AMIC_BIAS_SEL = 0x1 (Note 2)	1.4	1.5	1.6	
		AMIC_BIAS_SEL = 0x2	1.7	1.8	1.9	
		AMIC_BIAS_SEL = 0x3 (Note 2)	1.9	2	2.1	
		AMIC_BIAS_SEL = 0x4 (Note 2)	2.15	2.25	2.35	
		AMIC_BIAS_SEL = 0x5	2.4	2.5	2.6	
		AMIC_BIAS_SEL = 0x6 (Note 2)	2.65	2.75	2.85	
		AMIC_BIAS_SEL = 0x7 (Note 2)	2.9	3	3.1	
Dropout Voltage		V_{MBVDD} - $V_{MICBIASn}$ (Note 2)	200			mV
Enable Charge Time		$V_{MICBIASn}$ = 1.8V (90% charged), $C_{MICBIAS1}$ = 2.2µF, three microphones connected (0.1µF each)		15		µs
Disable Discharge Time		$V_{MICBIASn}$ = 3V, microphone bias disabled (90% discharged), $C_{MICBIAS1}$ = 2.2µF, three microphones connected (0.1µF each)		7		ms

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Transition Time		$V_{MICBIASn}$ changed from 1.2V to 3V (90% transition), $C_{MICBIAS1}$ = 2.2µF, three microphones connected (0.1µF each)			15		µs
		$V_{MICBIASn}$ changed from 3V to 1.2V (90% transition), $C_{MICBIAS1}$ = 2.2µF, three microphones connected (0.1µF each) (Note 6)	Low-noise mode		24		ms
			Low-power mode		51		
MICROPHONE BIAS GENERATOR / QUIESCENT CURRENT							
MBVDD Quiescent Current	I_{MBVDD}	No microphones connected	$V_{MICBIASn}$ = 1.2V, low-power mode		22		µA
			$V_{MICBIASn}$ = 1.8V, low-noise mode		74		
			$V_{MICBIASn}$ = 1.8V, low-power mode		33		
			$V_{MICBIASn}$ = 2.5V, low-power mode		47		
AVDD1 Additive Quiescent Current	I_{AVDD1}	No microphones connected, additional current when enabled in software shutdown	Low-power mode		70		µA
		No microphones connected, additional current when enabled in the audio state	Low-noise mode		65		
			Low-power mode		50		
AVDD2 Additive Quiescent Current	I_{AVDD2}	No microphones connected, additional current when enabled in software shutdown			40		µA

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MICROPHONE BIAS GENERATOR / OUTPUT NOISE							
Integrated Output Noise		A-weighted, f = 20Hz to 20kHz, $V_{MICBIASn}$ = 1.2V	Low-noise mode		3.4		μV_{RMS}
			Low-power mode		4.1		
		A-weighted, f = 20Hz to 20kHz, $V_{MICBIASn}$ = 1.8V	Low-noise mode		5.2		
			Low-power mode		6.7		
		A-weighted, f = 20Hz to 20kHz, $V_{MICBIASn}$ = 2.5V	Low-noise mode		7.6		
			Low-power mode		9.6		
MICROPHONE BIAS GENERATOR / OUTPUTS CHARACTERISTICS							
Output Current Drive	$I_{MICBIAS}$	Any combination of MICBIAS1, MICBIAS2, and MICBIAS3 enabled, up to three analog microphones connected total (Note 2)		3			mA
Load Regulation		MICBIAS1 output	$V_{MICBIAS1}$ = 1.8V, 0mA ≤ $I_{MICBIAS}$ ≤ 1mA (Note 2)		±0.5	±3.5	mV
			$V_{MICBIAS1}$ = 1.8V, 1mA < $I_{MICBIAS}$ ≤ 3mA (Note 2)		±1.1	±6.5	
		MICBIAS2 or MICBIAS3 output	$V_{MICBIASn}$ = 1.8V, 0mA ≤ $I_{MICBIAS}$ ≤ 1mA (Note 2)		±1.5	±4.5	
			$V_{MICBIASn}$ = 1.8V, 1mA ≤ $I_{MICBIAS}$ ≤ 3mA (Note 2)		±3.1	±9	
Line Regulation		$V_{MICBIASn}$ = 1.8V, V_{MBVDD} = 2V to 4.8V (Note 2)			±0.1		mV

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MICROPHONE BIAS GENERATOR / POWER SUPPLY REJECTION							
Power Supply Rejection Ratio	PSRR	MBVDD DC PSRR	$V_{MICBIASn}$ = 1.2V, V_{MBVDD} = 1.4V to 4.8V		90		dB
			$V_{MICBIASn}$ = 1.8V, V_{MBVDD} = 2V to 4.8V		90		
		V_{RIPPLE} = 100mV_{P-P} on MBVDD, $V_{MICBIASn}$ = 1.8V, I_{LOAD} < 3mA	f_{RIPPLE} = 217Hz		90		
			f_{RIPPLE} = 1kHz		90		
			f_{RIPPLE} = 20kHz		80		
		AVDD1 DC PSRR	$V_{MICBIASn}$ = 1.8V, V_{AVDD1} = 1.71V to 1.95V		80		
		V_{RIPPLE} = 100mV_{P-P} on AVDD1, $V_{MICBIASn}$ = 1.8V, I_{LOAD} < 3mA	f_{RIPPLE} = 217Hz		90		
			f_{RIPPLE} = 1kHz		90		
			f_{RIPPLE} = 20kHz		80		
		AVDD2 DC PSRR	$V_{MICBIASn}$ = 1.8V, V_{AVDD2} = 1.1V to 1.3V		60		
		V_{RIPPLE} = 100mV_{P-P} on AVDD2, $V_{MICBIASn}$ = 1.8V, I_{LOAD} < 3mA	f_{RIPPLE} = 217Hz		75		
			f_{RIPPLE} = 1kHz		75		
			f_{RIPPLE} = 20kHz		75		
RECORD CHANNEL DIGITAL CHARACTERISTICS / DIGITAL VOLUME CONTROL (Channels 1, 2, and 3)							
Maximum Digital Volume		REC_VOL = 0x00			0		dB
Minimum Digital Volume		REC_VOL = 0x7F			-63.5		dB
Digital Volume Control Step Size					0.5		dB
RECORD CHANNEL DIGITAL CHARACTERISTICS / DIGITAL GAIN CONTROL (Channels 1, 3, and 3)							
Minimum Digital Gain		REC_GAIN = 0x00			0		dB
Maximum Digital Gain		REC_GAIN = 0x1F			+31		dB
Digital Gain Control Step Size					1		dB
RECORD CHANNEL DIGITAL CHARACTERISTICS / DIGITAL HIGH PASS FILTER CHARACTERISTICS (Channels 1, 2, 3, Note 7)							
DC Attenuation					80		dB

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC Blocking Cutoff Frequency		Scales with sample rate	f_{S_REC} = 48kHz, RECn_DCBLK = 0x0		1.872		Hz
			f_{S_REC} = 8kHz, RECn_DCBLK = 0x0		0.312		
			f_{S_REC} = 48kHz, RECn_DCBLK = 0x1		14.976		
			f_{S_REC} = 8kHz, RECn_DCBLK = 0x1		2.496		
RECORD CHANNEL DIGITAL CHARACTERISTICS / DIGITAL FILTER CHARACTERISTICS (Note 7)							
Nominal Sample Rates	f_{S_REC}			8		48	kHz
Passband Cutoff	f_{PLP}	Ripple < δ_P		0.460 x f_S			Hz
		Droop < -3dB		0.471 x f_S			Hz
Passband Ripple	δ_P	f_{IN} < f_{PLP}, referenced to signal level at 1kHz		-0.1		+0.1	dB
Passband Matching		f_{IN} < f_{PLP}, record channel 4 output to playback amplifier output		-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}	Attenuation > δ_S				0.519 x f_S	Hz
Stopband Attenuation	δ_S	f_{IN} > f_{SLP}		-70			dB
RECORD CHANNEL DIGITAL CHARACTERISTICS / RECORD CHANNEL GROUP DELAY							
Group Delay		f_{IN} = 1kHz, f_S = 8kHz, AMIC input to PCM interface data output			875		µs
		f_{IN} = 1kHz, f_S = 48kHz, AMIC input to PCM interface data output			192		

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Record Channel Group Delay Matching		f_{IN} = 1kHz, matched input type (AMIC or DMIC), microphone to PCM interface data output channels enabled synchronously	Maximum difference in channel-to-channel matching for record channels 1/2/3		1.3		µs
			Maximum difference in device-to-device matching for record channels 1/2/3		1.3		
		f_{IN} = 1kHz, f_{S_REC} = 48kHz, matched input type (AMIC or DMIC), microphone to PCM interface data output channels enabled synchronously	Typical offset in matching from playback monitor channel (record 4) to record channels 1/2/3		20		
		f_{IN} = 1kHz, matched input type (AMIC or DMIC), microphone to PCM interface data output channels enabled synchronously	Maximum difference (plus offset) in matching from playback monitor channel (record 4) to record channels 1/2/3		1.3		
LOW-LATENCY DIGITAL FILTER CHANNEL 1 AND 2 CHARACTERISTICS (DF1 and DF2) / LOW-LATENCY DIGITAL FILTER CHANNEL SAMPLE RATE							
Channel Sample Rate	f_{S_DSP}	Playback sample rate is a 48kHz timebase	DSP_SR = 0x0		96		kHz
			DSP_SR = 0x1		192		
			DSP_SR = 0x2		384		
LOW-LATENCY DIGITAL FILTER CHANNEL 1 AND 2 CHARACTERISTICS (DF1 and DF2) / LOW-LATENCY DIGITAL FILTER CHANNEL VOLUME CONTROL							
Maximum Digital Volume		DF1_VOL_BKn or DF2_VOL_BKn = 0x00			0		dB
Minimum Digital Volume		DF1_VOL_BKn or DF2_VOL_BKn = 0x3F			-31.5		dB
Digital Volume Step Size					0.5		dB
Digital Mute Attenuation		Digital filter channel active			100		dB

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOW-LATENCY DIGITAL FILTER CHANNEL 1 AND 2 CHARACTERISTICS (DF1 and DF2) / LOW-LATENCY DIGITAL FILTER CHANNEL GAIN CONTROL							
Minimum Digital Gain		DF1_GAIN_BKn or DF2_GAIN_BKn = 0x7			+42		dB
Maximum Digital Gain		DF1_GAIN_BKn or DF2_GAIN_BKn = 0x0			0		dB
Digital Gain Step Size					6		dB
LOW-LATENCY DIGITAL FILTER CHANNEL 1 AND 2 CHARACTERISTICS (DF1 and DF2) / LOW-LATENCY DIGITAL FILTER CHANNEL HIGH-PASS FILTER CHARACTERISTICS (Note 7)							
DC Attenuation					80		dB
DC Blocking Cutoff Frequency		Sample rate is 192kHz or 384kHz (DSP_SR)	DFn_DCBLK = 0x0		1.872		Hz
			DFn_DCBLK = 0x1		7.488		
			DFn_DCBLK = 0x2		14.976		
			DFn_DCBLK = 0x3		29.952		
		Sample rate is 96kHz (DSP_SR)	DFn_DCBLK = 0x0		3.744		
			DFn_DCBLK = 0x1		14.976		
			DFn_DCBLK = 0x2		29.952		
			DFn_DCBLK = 0x3		59.904		
LOW-LATENCY DIGITAL FILTER CHANNEL 1 AND 2 CHARACTERISTICS (DF1 and DF2) / LOW-LATENCY DIGITAL FILTER CHANNEL ELLIPTICAL ULTRA-SOUND FILTER CHARACTERISTICS (Note 7)							
Coefficient Width		Coefficient data format is 2.22 (2 integer bits and 22 decimal bits)			24		Bits
Passband Cutoff Frequency	f_{PLP}	Ripple < δ_P	DSP_SR = 0x0, sample rate = 96kHz	5		50	kHz
			DSP_SR = 0x1, sample rate = 192kHz	5		50	
			DSP_SR = 0x2, sample rate = 384kHz	5		42	
Stopband Cutoff Frequency	f_{SLP}	Attenuation > δ_S	DSP_SR = 0x0, sample rate = 96kHz	10		60	kHz
			DSP_SR = 0x1, sample rate = 192kHz	10		60	
			DSP_SR = 0x2, sample rate = 384kHz	10		45	

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Transition Bandwidth		DSP_SR = 0x0, sample rate = 96kHz		5			kHz
		DSP_SR = 0x1, sample rate = 192kHz		3			
		DSP_SR = 0x2, sample rate = 384kHz		2			
Passband Ripple	δ_P	$f_{IN} < f_{PLP}$, referenced to signal level at 1kHz		±0.1			dB
Stopband Attenuation	δ_S	$f_{IN} > f_{SLP}$				60	dB
LOW-LATENCY DIGITAL FILTER CHANNEL 1 AND 2 CHARACTERISTICS (DF1 and DF2) / LOW-LATENCY DIGITAL FILTER CHANNEL GROUP DELAY							
MIC Input to Amplifier Output Loop Group Delay		f_{IN} = 1kHz, measured from microphone input to headphone amplifier output, biquad bands enabled in pass-through, volume ramping enabled	AMIC input, sample rate = 96kHz		89		µs
			AMIC input, sample rate = 192kHz		45		
			AMIC input, sample rate = 384kHz		35		
			DMIC input, sample rate = 192kHz, DMIC sample rate = 3.072MHz		44		
PLAYBACK CHANNEL DIGITAL CHARACTERISTICS / DIGITAL VOLUME CONTROLS							
Maximum Digital Volume		Playback channel	PB_VOL = 0x0		0		dB
Minimum Digital Volume		Playback channel	PB_VOL = 0x7F		-63.5		dB
Maximum Digital Volume		Playback compensation channel	PBC_VOL_BKA or PBC_VOL_BKB = 0x00		0		dB
Minimum Digital Volume		Playback compensation channel	PBC_VOL_BKA or PBC_VOL_BKB = 0x3F		-31.5		dB
Digital Volume Control Step Size					0.5		dB
Digital Mute Attenuation		Digital audio interface active			100		dB
PLAYBACK CHANNEL DIGITAL CHARACTERISTICS / DIGITAL GAIN CORRECTION							
Minimum Digital Gain		PB_GAIN = 0x00			-6		dB
Maximum Digital Gain		PB_GAIN = 0x30			+6		dB
Digital Gain Control Step Size					0.25		dB
PLAYBACK CHANNEL DIGITAL CHARACTERISTICS / DIGITAL GAIN CONTROL							
Minimum Digital Gain		PBC_GAIN_BKA or PBC_GAIN_BKB = 0x7			+42		dB

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Digital Gain		PBC_GAIN_BKA or PBC_GAIN_BKB = 0x0			0		dB
Digital Gain Step Size					6		dB
PLAYBACK CHANNEL DIGITAL CHARACTERISTICS / DIGITAL HIGH PASS FILTER CHARACTERISTICS (Note 7)							
DC Attenuation				80			dB
DC Blocking Cutoff Frequency		Scales with sample rate up to 48kHz	f_S = 48kHz, PB_DCBLK = 0x0		1.872		Hz
			f_S = 8kHz, PB_DCBLK = 0x0		0.312		
			f_S = 48kHz, PB_DCBLK = 0x1		14.976		
			f_S = 8kHz, PB_DCBLK = 0x1		2.496		
PLAYBACK CHANNEL DIGITAL CHARACTERISTICS / DIGITAL FILTER CHARACTERISTICS (Sample Rate < 50kHz, Note 7)							
Valid Sample Rate Settings				8		48	kHz
Passband Cutoff	f_{PLP}	Ripple < δ_P		0.454 x f_S			Hz
		Droop < -3dB		0.459 x f_S			Hz
Passband Ripple	δ_P	f_{IN} < f_{PLP}, referenced to signal level at 1kHz		-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}	Attenuation > δ_S				0.49 x f_S	Hz
Stopband Attenuation	δ_S	f_{IN} > f_{SLP}		75			dB
PLAYBACK CHANNEL DIGITAL CHARACTERISTICS / DIGITAL FILTER CHARACTERISTICS (Sample Rate ≥ 50kHz, Note 7)							
Valid Sample Rate Settings				88.2		192	kHz
Passband Cutoff	f_{PLP}	Ripple < δ_P, 50kHz ≤ f_S < 100kHz		0.227 x f_S			Hz
		Droop < -3dB, 50kHz ≤ f_S < 100kHz		0.314 x f_S			Hz
Passband Ripple	δ_P	f < f_{PLP}, referenced to signal level at 1kHz		-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}	Attenuation < δ_S				0.49 x f_S	Hz
Stopband Attenuation	δ_S	f > f_{SLP}		80			dB

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PLAYBACK CHANNEL DIGITAL CHARACTERISTICS / GROUP DELAY						
Group Delay		f_{IN} = 1kHz, f_S = 8kHz, PCM interface data input to amplifier output		670		µs
		f_{IN} = 1kHz, f_S = 48kHz, PCM interface data input to amplifier output		130		
		f_{IN} = 1kHz, f_S = 192kHz, PCM interface data input to amplifier output		34		
Playback Channel Group Delay Matching		f_{IN} = 1kHz, f_{S_DSP} = 192kHz, PCM interface data input to amplifier output, maximum difference in device-to-device matching for playback channel		5.2		µs
BIQUAD FILTER CHARACTERISTICS						
Coefficient Width		Coefficient data format is 2.22 (2 integer bits and 22 decimal bits)		24		Bits
Number of Bands		Playback equalizer		5		Bands
		Playback compensation filter channel		10		
		Low-latency digital filter channel 1 and 2		12		
Frequency Range	f_0	Low-pass filter corner frequency	0.5			kHz
		High-pass filter corner frequency	0.02			
		Peaking filter center frequency	0.02			
		Low-shelf filter midpoint frequency	0.02			
		High-shelf filter midpoint frequency	0.02			
Quality Factor	Q	Low-pass filter	0.2		5	
		High-pass filter	0.2		5	
		Peaking filter	0.2		5	
		Low-shelf filter	0.2		5	
		High-shelf filter	0.2		5	
Gain Range	A	Peaking filter	-20		+20	dB
		Low-shelf filter	-20		+20	
		High-shelf filter	-20		0	
PLAYBACK OUTPUT AMPLIFIER						
Full Scale Output Voltage	V_{FS}	Playback volume = 0dB	0.962	1	1.03	V_{RMS}
		Playback volume = -3dB, PB_AMP_MODE = 0x1 (Note 2)	0.683	0.707	0.727	
Dynamic Range	DR	High-performance playback mode (Note 5)	109	114		dB
		Low-power playback mode (Notes 2 and 5)	106	111		

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Noise		A-weighted, audio playback silent, high-performance mode (Note 2)		2	3.5	μV_{RMS}
		A-weighted, audio playback silent, low-power mode (Note 2)		2.8	5	
Output Power	P_{OUT}	f_{IN} = 1kHz, playback volume = 0dB, R_{LOAD} = 32Ω, THD+N ≤ -40dB		31		mW
		f_{IN} = 1kHz, playback volume = 0dB, R_{LOAD} = 16Ω, THD+N ≤ -40dB		61		
		f_{IN} = 1kHz, playback volume = -3dB, PB_AMP_MODE = 0x1, R_{LOAD} = 32Ω, THD+N ≤ -40dB		15		
		f_{IN} = 1kHz, playback volume = -3dB, PB_AMP_MODE = 0x1, R_{LOAD} = 16Ω, THD+N ≤ -40dB		30		
Total Harmonic Distortion + Noise	THD+N	f_{IN} = 1kHz, P_{OUT} = 20mW, R_{LOAD} = 32Ω, playback volume = 0dB		-75		dB
		f_{IN} = 1kHz, P_{OUT} = 31mW, R_{LOAD} = 32Ω, playback volume = 0dB (Note 2)		-65	-60	
		f_{IN} = 1kHz, P_{OUT} = 10mW, R_{LOAD} = 32Ω, playback volume = -3dB, PB_AMP_MODE = 0x1		-76		
Output Offset Voltage	V_{OS}			±0.1	±0.65	mV
Click-and-Pop Level	K_{CP}	Audio playback silent, amplifier enabled by software (Note 8)		-75		dBV
		Audio playback silent, amplifier disabled by software (Note 8)		-75		
Minimum Output Load Resistance		Differential between OUTP and OUTN		12.8		Ω
Minimum Output Load Capacitance		Differential between OUTP and OUTN		0		pF

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Output Load Capacitance		Differential between OUTP and OUTN, playback high performance mode or playback low power mode with PB_AMP_LOAD_OP_BIAS = 0x1 (default)			50		pF
			R_{LOAD} ≤ 100Ω		75		
		Differential between OUTP and OUTN, playback low power mode, PB_AMP_LOAD_OP_BIAS = 0x3			100		
Maximum Output Load Inductance		Differential between OUTP and OUTN			75		µH
Amplifier OVC Auto Restart Time	t_{OVC_RETRY}	Time the amplifier output is disabled before being re-enabled when an overcurrent fault occurs, auto OVC recovery mode, AMIC_CT_SEL = 0x1, ramping disabled (ramp time added if enabled)			5.2		µs
EMI Margin to EN55022B		6" cable, Z_{LOAD} = 16Ω + 32µH, P_{OUT} = 10mW			-12		dB
PLAYBACK OUTPUT AMPLIFIER / INCREMENTAL EFFICIENCY							
Playback Amplifier Incremental Efficiency		Z_{LOAD} = 32Ω + 32µH (Note 9)	P_{OUT} = 0.1mW	11.5	18		%
			P_{OUT} = 1mW	47.5	59		
			P_{OUT} = 10mW		80		
			PB_AMP_MODE = 0x1, P_{OUT} = 10mW		84		
PLAYBACK OUTPUT AMPLIFIER / POWER SUPPLY REJECTION							
AVDD1 Power Supply Rejection Ratio	PSRR	DC, V_{AVDD1} = 1.71V to 1.95V			100		dB
		V_{RIPPLE} = 100mV_{P-P} on AVDD1, f_{RIPPLE} = 217Hz			100		
		V_{RIPPLE} = 50mV_{P-P} on AVDD1, f_{RIPPLE} = 1kHz			100		
		V_{RIPPLE} = 50mV_{P-P} on AVDD1, f_{RIPPLE} = 20kHz			90		

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AVDD2 Power Supply Rejection Ratio	PSRR	DC, V_{AVDD2} = 1.1V to 1.3V		90		dB
		V_{RIPPLE} = 50mV_{P-P} on AVDD2, f_{RIPPLE} = 217Hz		95		
		V_{RIPPLE} = 50mV_{P-P} on AVDD2, f_{RIPPLE} = 1kHz		95		
		V_{RIPPLE} = 50mV_{P-P} on AVDD2, f_{RIPPLE} = 20kHz		85		
AVDD3 Power Supply Rejection Ratio	PSRR	DC, V_{AVDD3} = 1.1V to 1.3V		100		dB
		V_{RIPPLE} = 50mV_{P-P} on AVDD3, f_{RIPPLE} = 217Hz		100		
		V_{RIPPLE} = 50mV_{P-P} on AVDD3, f_{RIPPLE} = 1kHz		100		
		V_{RIPPLE} = 50mV_{P-P} on AVDD3, f_{RIPPLE} = 20kHz		95		
DIGITAL I/O / INPUT—BCLK, LRCLK, DIN, DMD1, DMD2, DMD3, HW_EN						
Input Voltage High	V_{IH}		0.7 x V_{DVDDIO}			V
Input Voltage Low	V_{IL}				0.3 x V_{DVDDIO}	V
Input Leakage Current			-1		+1	µA
Input Hysteresis	V_{HYS}	(Note 2)	75			mV
Maximum Input Capacitance	C_{IN}			10		pF
Internal Pulldown Resistance	R_{PD}	BCLK, LRCLK		3		MΩ
DIGITAL I/O / INPUT—SDA, SCL, ADDR						
Input Voltage High	V_{IH}		0.7 x V_{DVDDIO}			V
Input Voltage Low	V_{IL}				0.3 x V_{DVDDIO}	V
Input Leakage Current		T_A = +25°C, input high	-1		+1	µA
Input Hysteresis	V_{HYS}	(Note 2)	75			mV
Input Capacitance	C_{IN}			10		pF
DIGITAL I/O / OPEN-DRAIN OUTPUT—SDA, IRQ						
Output Voltage Low	V_{OL}	I_{SINK} = 3mA			0.4	V

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Leakage Current	I_{OH}	T_A = +25°C	-1		+1	µA
DIGITAL I/O / PUSH-PULL OUTPUT—DOUT, DMC1, DMC2, DMC3, IRQ						
Output Voltage High	V_{OH}	I_{OH} = 3mA	V_{DVDDIO} - 0.3			V
Output Voltage Low	V_{OL}	I_{OL} = 3mA			0.3	V
Output Current	I_{OH}	DOUT, DMC1, DMC2, DMC3, maximum drive mode		8		mA
		DOUT, DMC1, DMC2, DMC3, high drive mode		6		
		DOUT, DMC1, DMC2, DMC3, standard drive mode		4		
		DOUT, DMC1, DMC2, DMC3, reduced drive mode		2		
PCM AUDIO INTERFACE TIMING						
Nominal LRCLK Frequency Range Settings	f_{LRCLK}	All PCM interface operating modes	8		192	kHz
Nominal BCLK Frequency Range Settings	f_{BCLK}	I^2S mode or left-justified mode	0.256		12.288	MHz
		TDM mode	0.256		24.576	
BCLK Duty Cycle	DC_{BCLK}		45		55	%
BCLK Period	t_{BCLK}	I^2S mode or left-justified mode	80			ns
		TDM mode	40			
Maximum BCLK Input Low-Frequency Jitter		Maximum allowable jitter before a -20dBFS, 20kHz input has a 1dB reduction in THD+N, RMS jitter ≤ 40kHz		0.25		ns
Maximum BCLK Input High-Frequency Jitter		Maximum allowable jitter before a -60dBFS, 20kHz input has a 1dB reduction in THD+N, RMS jitter > 40kHz		1		ns
PCM AUDIO INTERFACE TIMING / PCM INTERFACE TIMING						
LRCLK to BCLK Active Edge Setup Time	$t_{SYNCSET}$		4			ns
LRCLK to BCLK Active Edge Hold Time	$t_{SYNCHOLD}$		4			ns
DIN to BCLK Active Edge Setup Time	t_{SETUP}		4			ns
DIN to BCLK Active Edge Hold Time	t_{HOLD}		4			ns

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIN Frame Delay After LRCLK Edge		Measured in number of BCLK cycles, set by selected TDM mode	0		2	cycles
PCM AUDIO INTERFACE TIMING / PCM INTERFACE TIMING / DOUT						
BCLK Inactive Edge to DOUT Delay	t_{CLKTX}				14	ns
BCLK Active Edge to DOUT Hi-Z Delay	t_{HIZ}		4		16	ns
BCLK Inactive Edge to DOUT Active Delay	t_{ACTV}		0		14	ns
I²C SLAVE CONTROL INTERFACE TIMING						
Serial Clock Frequency	f_{SCL}				1000	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		0.5			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.26			µs
SCL Pulse-Width Low	t_{LOW}		0.5			µs
SCL Pulse-Width High	t_{HIGH}		0.26			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.26			µs
Data Hold Time	$t_{HD,DAT}$		0		450	ns
Data Setup Time	$t_{SU,DAT}$		50			ns
SDA and SCL Receiving Rise Time	t_R		20 x V_{DVDDIO} / 5.5V		120	ns
SDA and SCL Receiving Fall Time	t_F		20 x V_{DVDDIO} / 5.5V		120	ns
SDA Transmit Fall Time	t_F		20 x V_{DVDDIO} / 5.5V		120	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.26			µs
Bus Capacitance	C_B				550	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

Electrical Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIASn}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Low-Noise Microphone Bias Mode, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = -40°C to +85°C unless otherwise noted, Typical values at T_A = +25°C, Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL MICROPHONE INTERFACE TIMING CHARACTERISTICS						
DMIC Clock Output Frequency	f_{DMIC_CLK}	f_{BCLK} from the 48kHz family clock base, DMIC_RATE = 0x0		0.768		MHz
		f_{BCLK} from the 48kHz family clock base, DMIC_RATE = 0x1		1.536		
		f_{BCLK} from the 48kHz family clock base, DMIC_RATE = 0x2		3.072		
DMIC Clock Output Duty Cycle			45		55	%
DMIC Data to DMIC Clock Setup Time	t_{DMIC_SETUP}	Either DMIC clock edge	40			ns
DMIC Clock to DMIC Data Hold Time	t_{DMIC_HOLD}	Either DMIC clock edge	0			ns

Note 1: 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design or characterization, unless otherwise noted.

Note 2: Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

Note 3: Maximum hardware enable time is specified assuming no initialization errors occur during the hardware shutdown to software shutdown state transition. If an error occurs, then the device retries up to 5 times (before either succeeding or failing to initialize) resulting in a maximum hardware enable time that is up to six times longer (for a failed initialization).

Note 4: Assumes AMIC PGA input common mode bias voltage was pre-charged and retained for inactive input channel n (AMICn_PGA_HIZ = 1).

Note 5: Dynamic range measurements are performed with the EIAJ method (-60dBFS output signal at 1kHz, A-weighted, and normalized to full scale).

Note 6: For faster transitions from higher AMIC bias voltages to lower ones, disable the AMIC bias output with fast discharge enabled, and then re-enable it after setting it to the new voltage output level.

Note 7: Digital filter performance is invariant over temperature and is production tested at T_A = +25°C.

Note 8: Click and pop measurement performed by taking the peak voltage at 32 samples per second with an A-weighted filter.

Note 9: Incremental efficiency is calculated as P_{OUT} / (P_{IN} - P_Q) x 100% where P_{OUT} is the amplifier output power, P_{IN} is the active power needed to drive the load, and P_Q is the quiescent power for the given use case. Incremental efficiency allows for the calculation of total use case power for any given configuration at the selected output load.

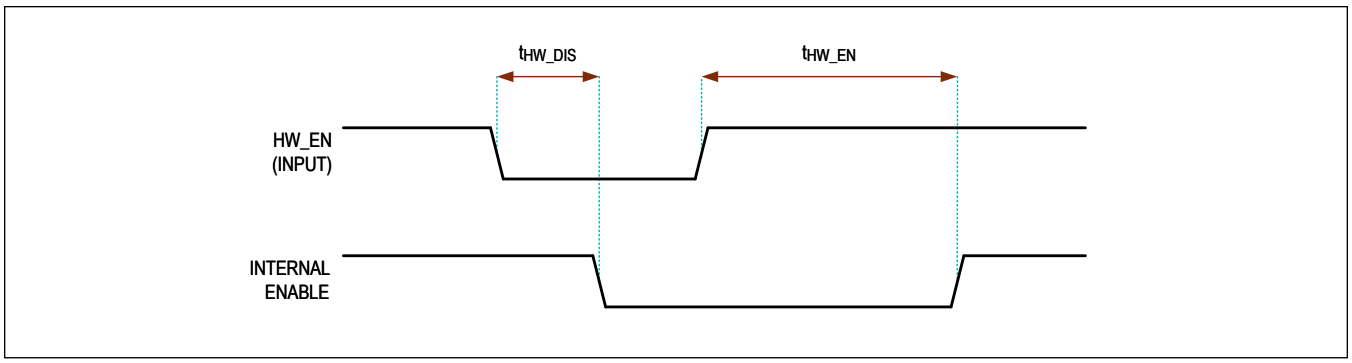


Figure 1. Hardware Enable and Disable Timing Diagram

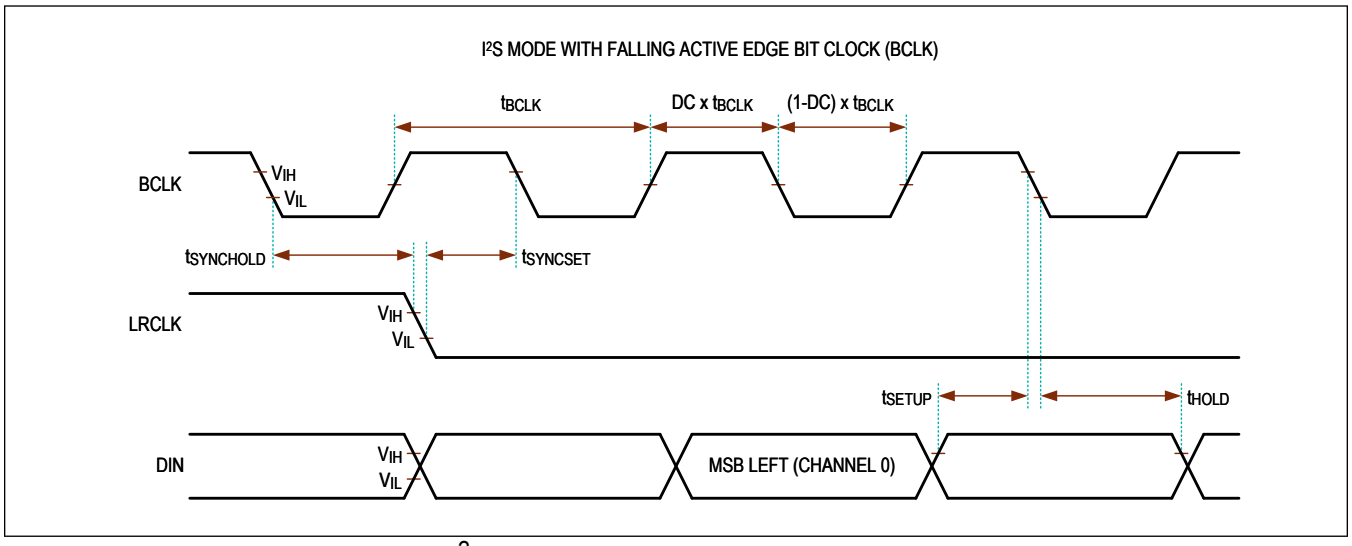


Figure 2. PCM Interface Timing Diagram for I^2S Mode

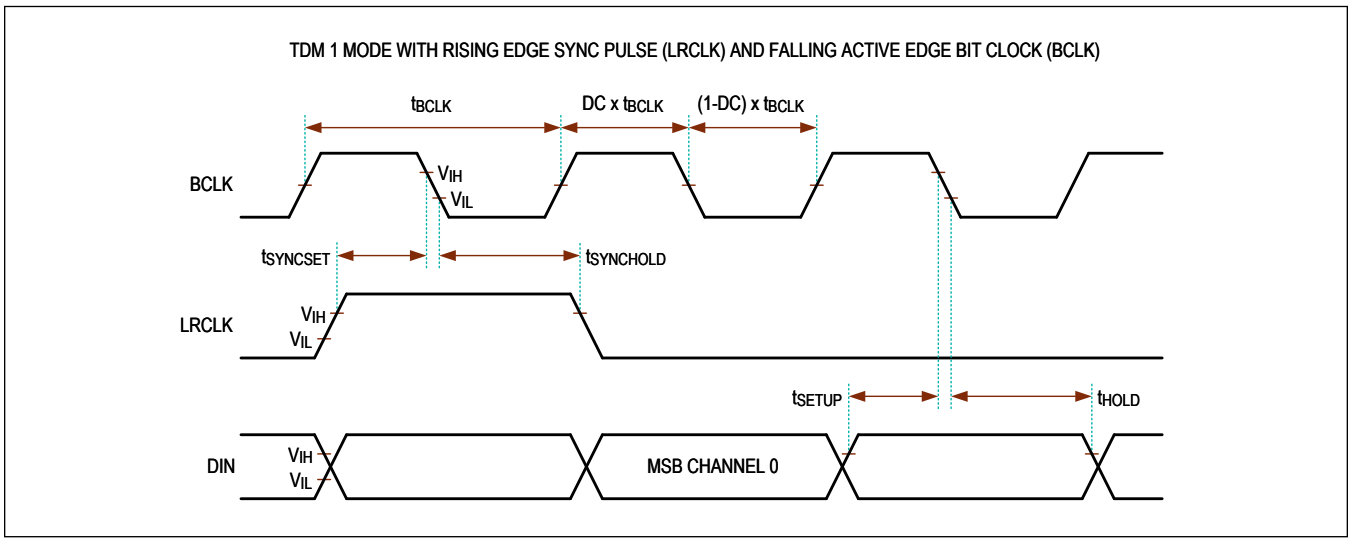


Figure 3. PCM Interface Timing Diagram for TDM 1 Mode

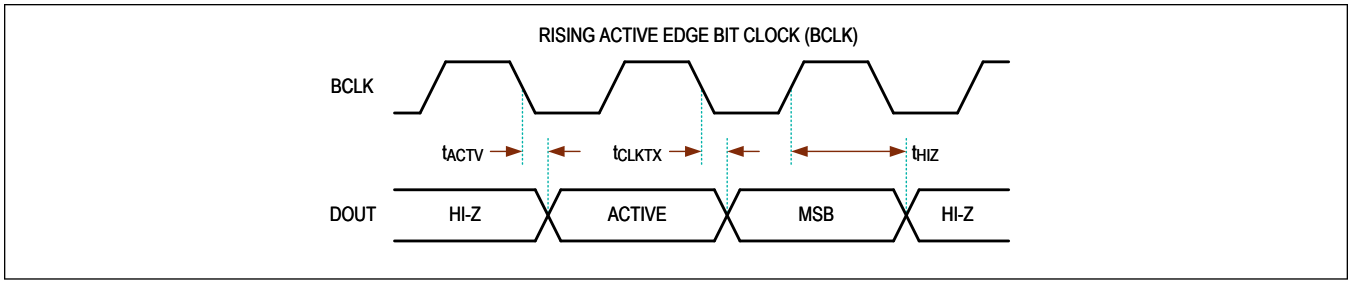


Figure 4. PCM Interface Data Output Timing Diagram

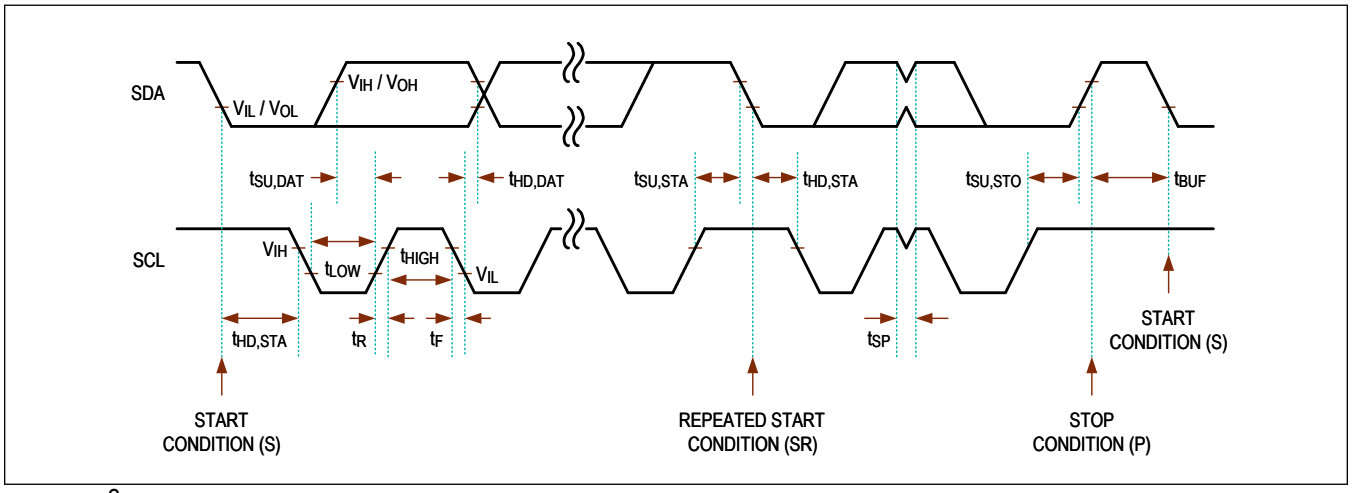


Figure 5. I^2C Slave Control Interface Timing Diagram

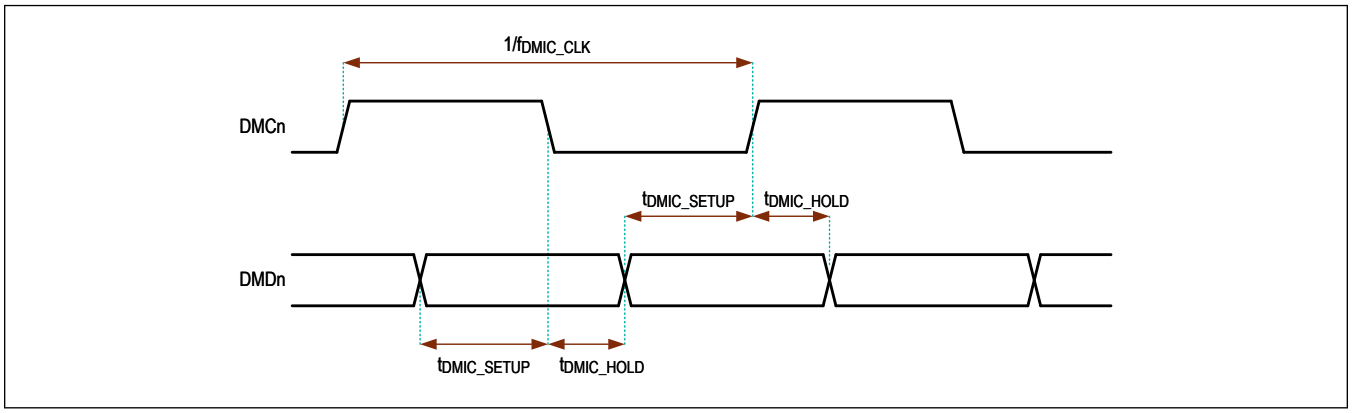
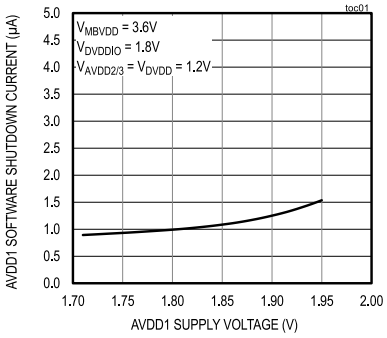


Figure 6. Digital Microphone Interface Timing Diagram

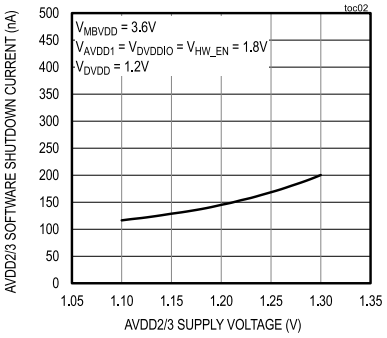
Typical Operating Characteristics

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIAS1}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, Typical values at T_A = +25°C)

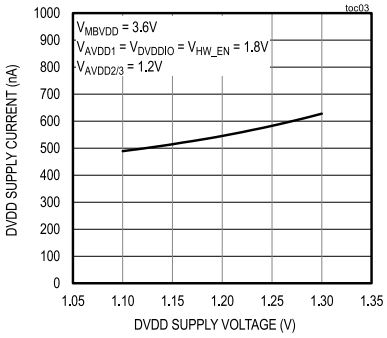
AVDD1 SOFTWARE SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



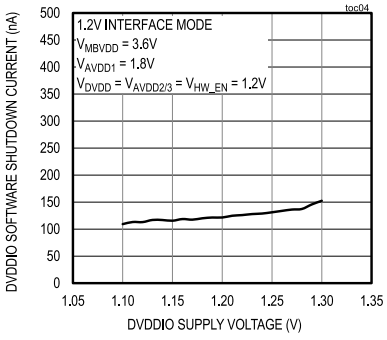
AVDD2/3 SOFTWARE SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



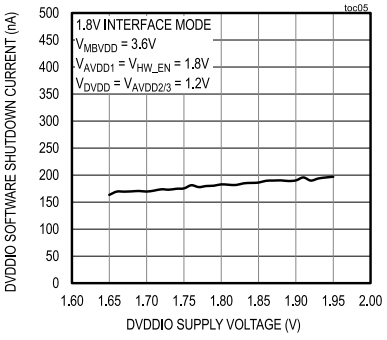
DVDD SOFTWARE SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



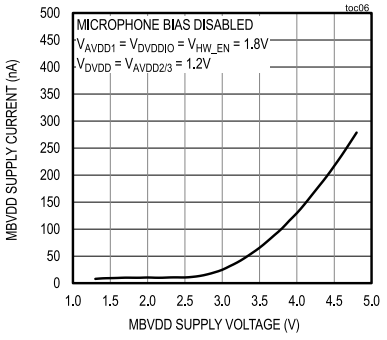
DVDDIO SOFTWARE SHUTDOWN CURRENT vs. SUPPLY CURRENT



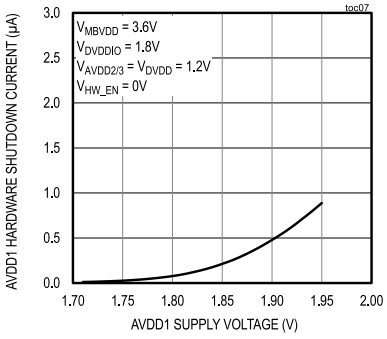
DVDDIO SOFTWARE SHUTDOWN CURRENT vs. SUPPLY CURRENT



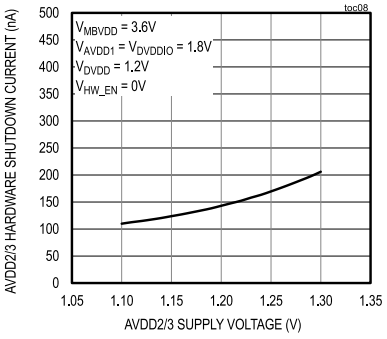
MBVDD SOFTWARE SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



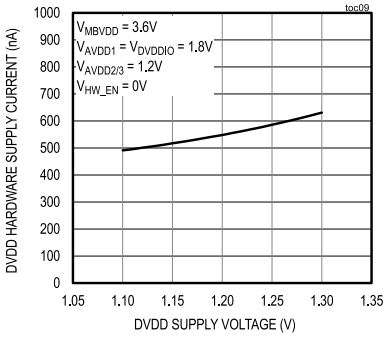
AVDD1 HARDWARE SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



AVDD2/3 HARDWARE SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



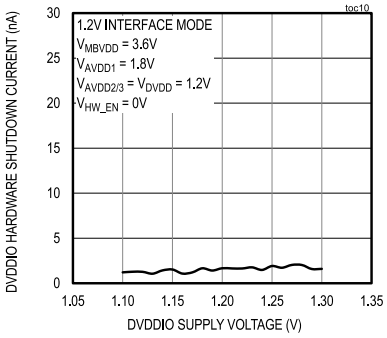
DVDD HARDWARE SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



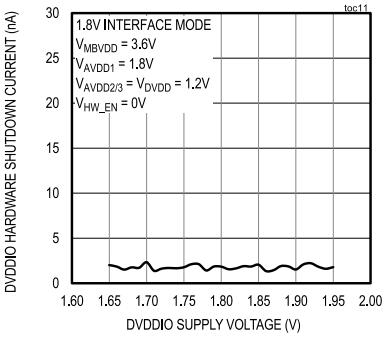
Typical Operating Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIAS1}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, Typical values at T_A = +25°C)

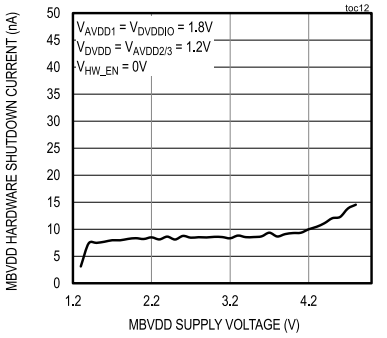
DVDDIO HARDWARE SHUTDOWN CURRENT vs. SUPPLY CURRENT



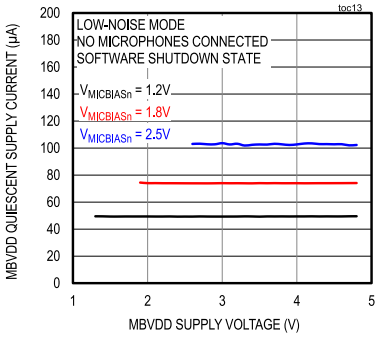
DVDDIO HARDWARE SHUTDOWN CURRENT vs. SUPPLY CURRENT



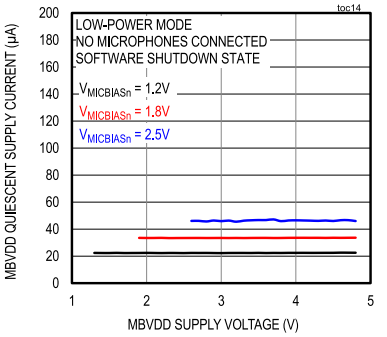
MBVDD HARDWARE SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



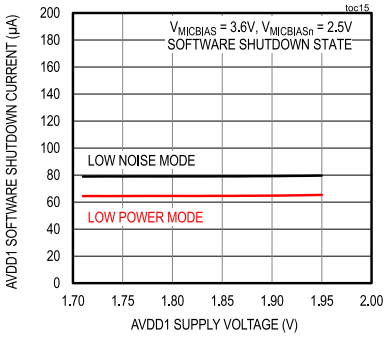
MICROPHONE BIAS ENABLED: MBVDD QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



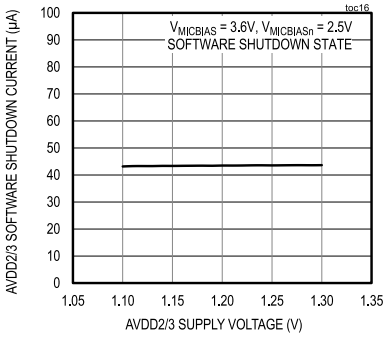
MICROPHONE BIAS ENABLED: MBVDD QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



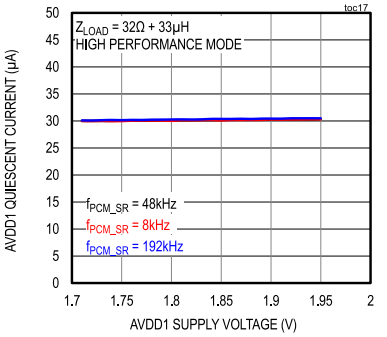
MICROPHONE BIAS ENABLED: AVDD1 QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



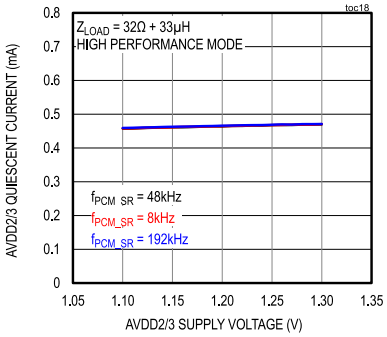
MICROPHONE BIAS ENABLED: AVDD2/3 QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



PLAYBACK ONLY: AVDD1 QUIESCENT CURRENT vs. AVDD1 SUPPLY VOLTAGE



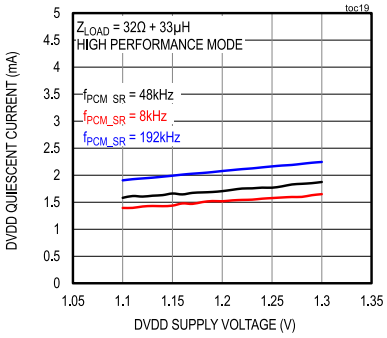
PLAYBACK ONLY: AVDD2/3 QUIESCENT CURRENT vs. AVDD2/3 SUPPLY VOLTAGE



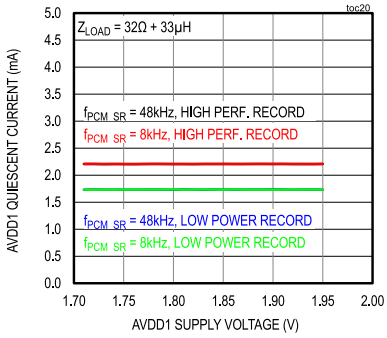
Typical Operating Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIAS1}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, Typical values at T_A = +25°C)

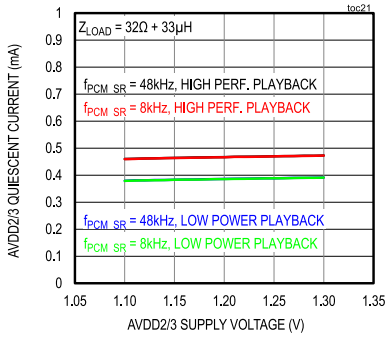
PLAYBACK ONLY: DVDD QUIESCENT CURRENT vs. DVDD SUPPLY VOLTAGE



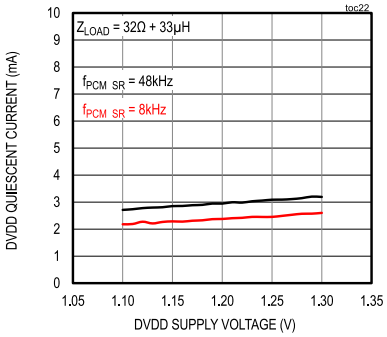
PLAYBACK + TWO CHANNEL RECORD: AVDD1 QUIESCENT CURRENT vs. AVDD1 SUPPLY VOLTAGE



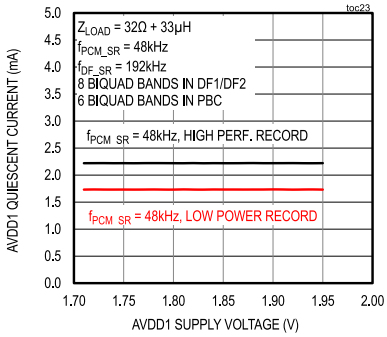
PLAYBACK + TWO CHANNEL RECORD: AVDD2/3 QUIESCENT CURRENT vs. AVDD2/3 SUPPLY VOLTAGE



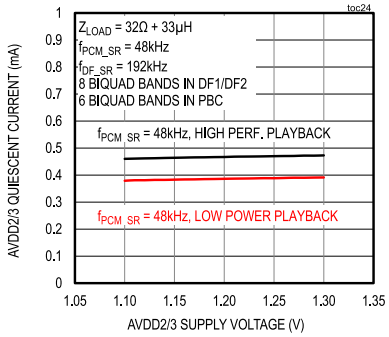
PLAYBACK + TWO CHANNEL RECORD: DVDD QUIESCENT CURRENT vs. DVDD SUPPLY VOLTAGE



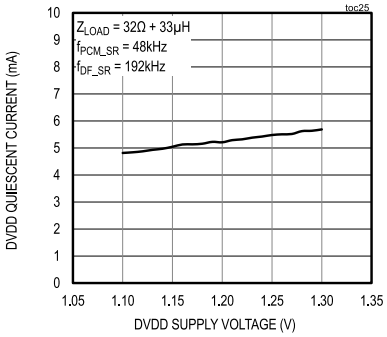
TYPICAL HYBRID TUNING PROFILE: AVDD1 QUIESCENT CURRENT vs. AVDD1 SUPPLY VOLTAGE



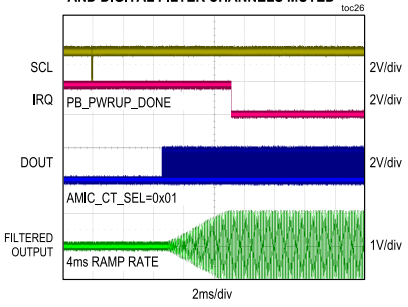
TYPICAL HYBRID TUNING PROFILE: AVDD2/3 QUIESCENT CURRENT vs. AVDD2/3 SUPPLY VOLTAGE



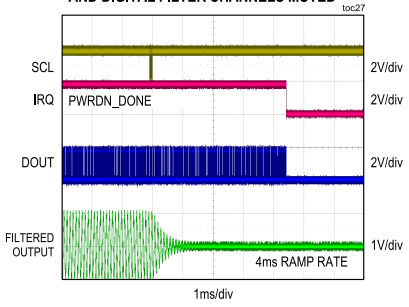
TYPICAL HYBRID TUNING PROFILE: DVDD QUIESCENT CURRENT vs. DVDD SUPPLY VOLTAGE



SYSTEM TURN-ON RESPONSE: PLAYBACK VOLUME RAMPING ENABLED AND DIGITAL FILTER CHANNELS MUTED



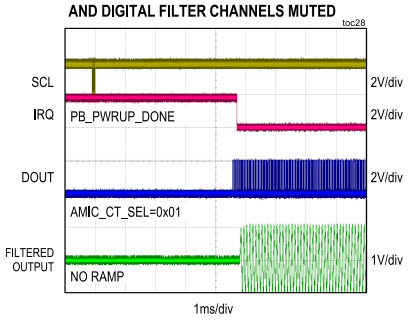
SYSTEM TURN-OFF RESPONSE: PLAYBACK VOLUME RAMPING ENABLED AND DIGITAL FILTER CHANNELS MUTED



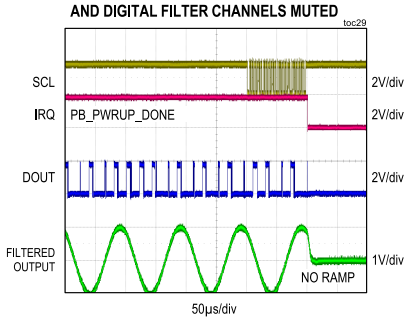
Typical Operating Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIAS1}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, Typical values at T_A = +25°C)

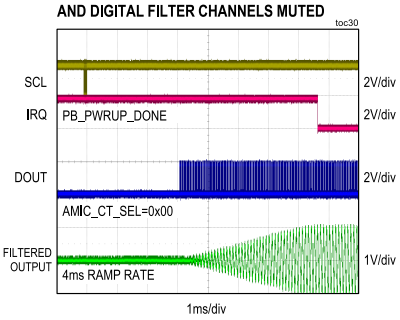
SYSTEM TURN-ON RESPONSE:
PLAYBACK VOLUME RAMPING DISABLED
AND DIGITAL FILTER CHANNELS MUTED



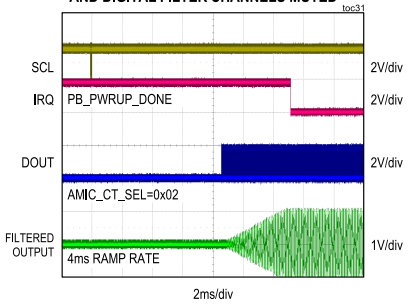
SYSTEM TURN-OFF RESPONSE
PLAYBACK VOLUME RAMPING DISABLED
AND DIGITAL FILTER CHANNELS MUTED



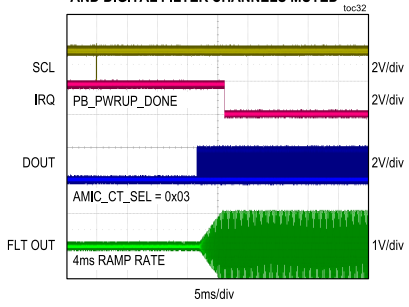
SYSTEM TURN-ON RESPONSE:
PLAYBACK VOLUME RAMPING ENABLED
AND DIGITAL FILTER CHANNELS MUTED



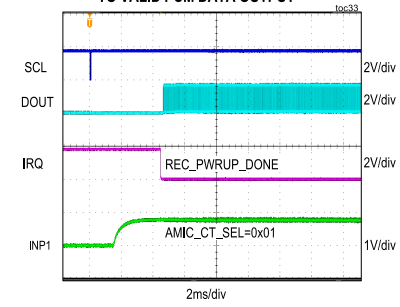
SYSTEM TURN-ON RESPONSE:
PLAYBACK VOLUME RAMPING ENABLED
AND DIGITAL FILTER CHANNELS MUTED



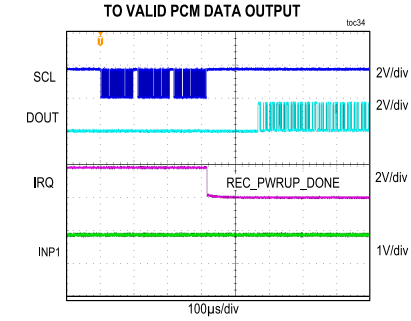
SYSTEM TURN-ON RESPONSE:
PLAYBACK VOLUME RAMPING ENABLED
AND DIGITAL FILTER CHANNELS MUTED



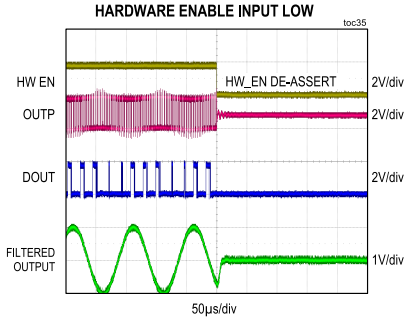
RECORD CHANNEL TURN-ON RESPONSE:
STATIC ENABLE FROM SHUTDOWN
TO VALID PCM DATA OUTPUT



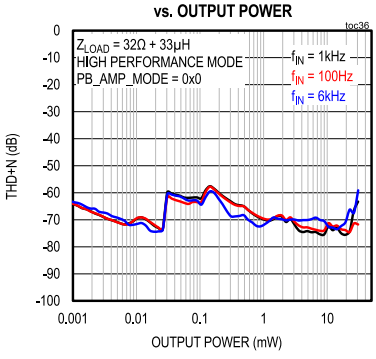
RECORD CHANNEL TURN ON RESPONSE
DYNAMIC ENABLE DURING PLAYBACK
TO VALID PCM DATA OUTPUT



SYSTEM TURN-OFF RESPONSE:
HARDWARE ENABLE INPUT LOW



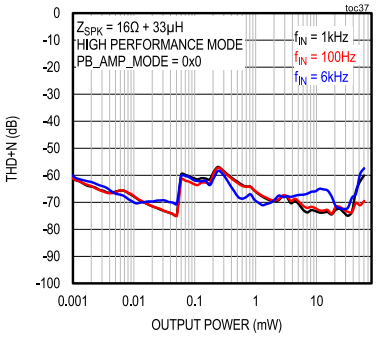
PLAYBACK CHANNEL:
TOTAL HARMONIC DISTORTION + NOISE
vs. OUTPUT POWER



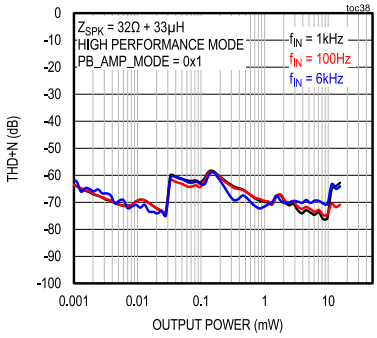
Typical Operating Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIAS1}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, Typical values at T_A = +25°C)

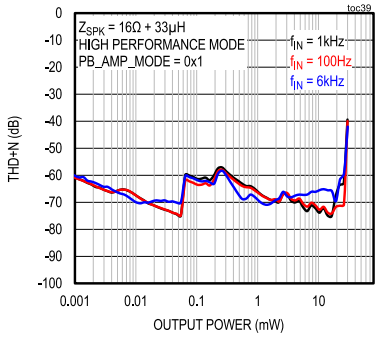
PLAYBACK CHANNEL: TOTAL HARMONIC DISTORTION + NOISE vs. OUTPUT POWER



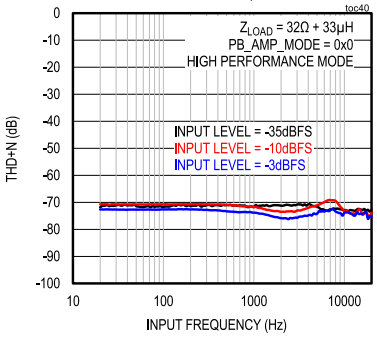
PLAYBACK CHANNEL: TOTAL HARMONIC DISTORTION + NOISE vs. OUTPUT POWER



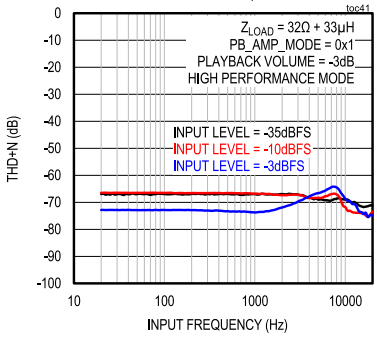
PLAYBACK CHANNEL: TOTAL HARMONIC DISTORTION + NOISE vs. OUTPUT POWER



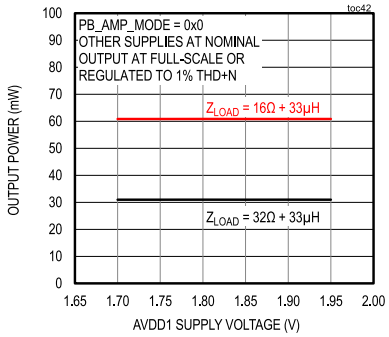
PLAYBACK CHANNEL: TOTAL HARMONIC DISTORTION + NOISE vs. INPUT FREQUENCY



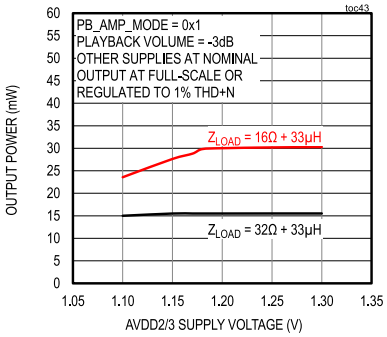
PLAYBACK CHANNEL: TOTAL HARMONIC DISTORTION + NOISE vs. INPUT FREQUENCY



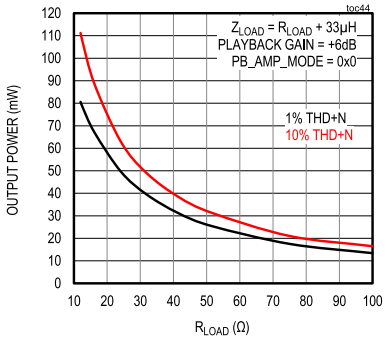
PLAYBACK CHANNEL: OUTPUT POWER vs. AVDD1 SUPPLY VOLTAGE



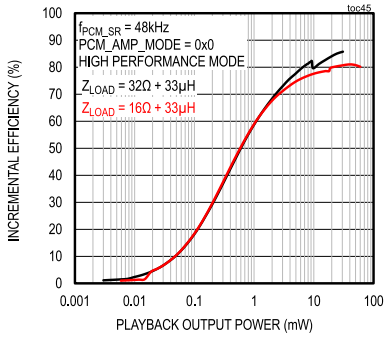
PLAYBACK CHANNEL: OUTPUT POWER vs. AVDD2/3 SUPPLY VOLTAGE



PLAYBACK CHANNEL: OUTPUT POWER vs. LOAD RESISTANCE



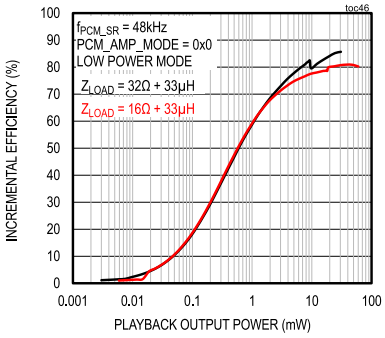
PLAYBACK CHANNEL: INCREMENTAL EFFICIENCY vs. PLAYBACK OUTPUT POWER



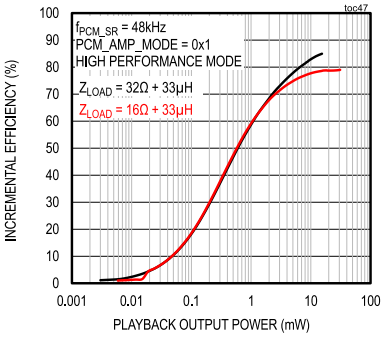
Typical Operating Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIAS1}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, Typical values at T_A = +25°C)

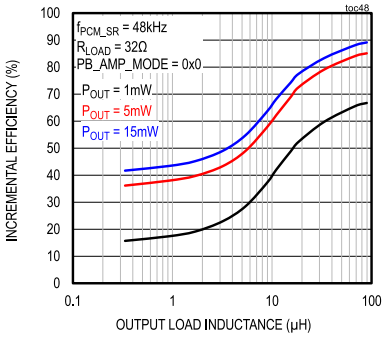
PLAYBACK CHANNEL: INCREMENTAL EFFICIENCY vs. PLAYBACK OUTPUT POWER



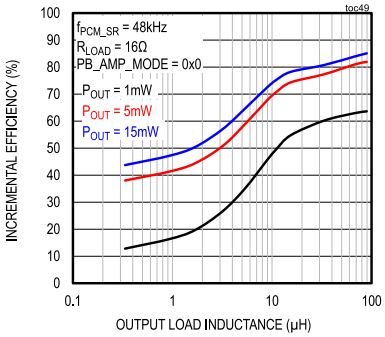
PLAYBACK CHANNEL: INCREMENTAL EFFICIENCY vs. PLAYBACK OUTPUT POWER



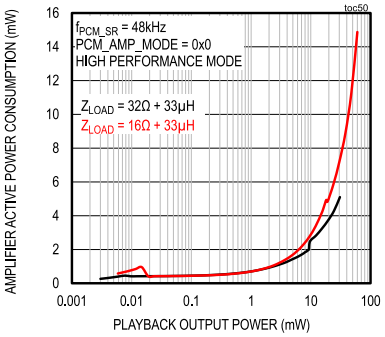
PLAYBACK CHANNEL: INCREMENTAL EFFICIENCY vs. OUTPUT LOAD INDUCTANCE



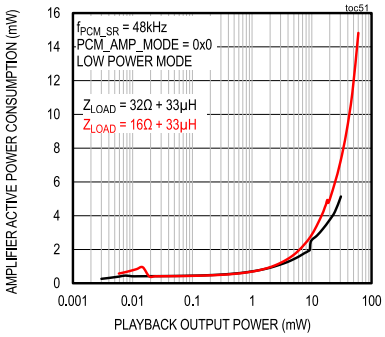
PLAYBACK CHANNEL: INCREMENTAL EFFICIENCY vs. OUTPUT LOAD INDUCTANCE



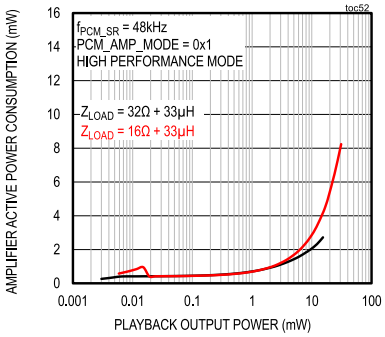
PLAYBACK CHANNEL: AMPLIFIER ACTIVE POWER CONSUMPTION vs. OUTPUT POWER



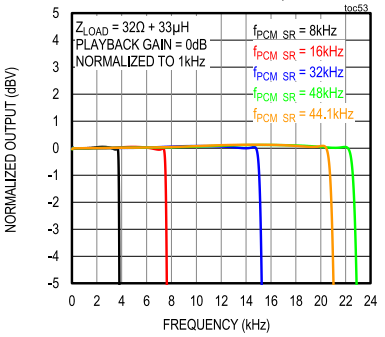
PLAYBACK CHANNEL: AMPLIFIER ACTIVE POWER CONSUMPTION vs. OUTPUT POWER



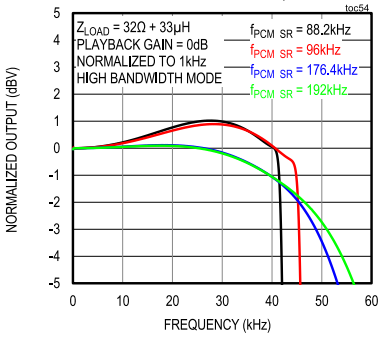
PLAYBACK CHANNEL: AMPLIFIER ACTIVE POWER CONSUMPTION vs. OUTPUT POWER



PLAYBACK CHANNEL: NORMALIZED OUTPUT LEVEL vs. FREQUENCY



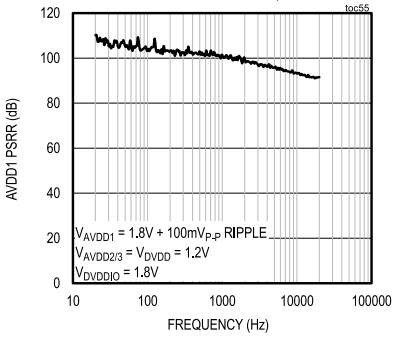
PLAYBACK CHANNEL: NORMALIZED OUTPUT LEVEL vs. FREQUENCY



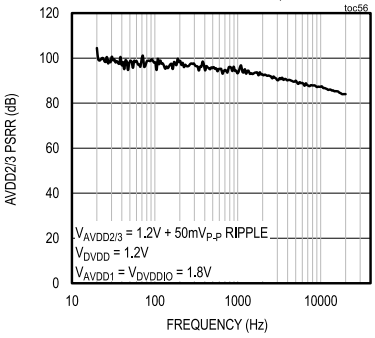
Typical Operating Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIAS1}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, Typical values at T_A = +25°C)

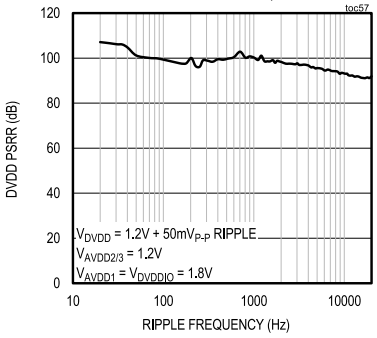
PLAYBACK CHANNEL: AVDD1 PSRR vs. FREQUENCY



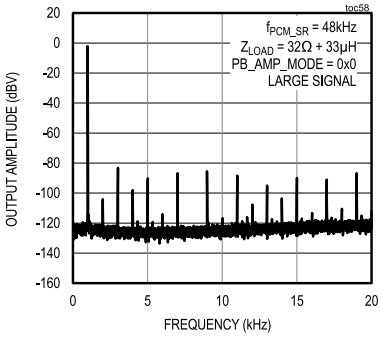
PLAYBACK CHANNEL: AVDD2/3 PSRR vs. FREQUENCY



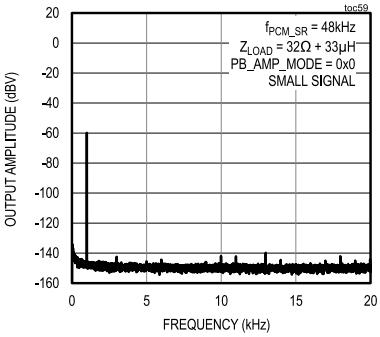
PLAYBACK CHANNEL: DVDD PSRR vs. FREQUENCY



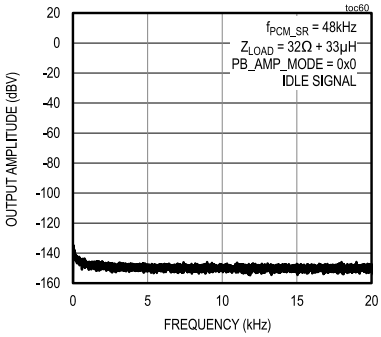
PLAYBACK CHANNEL: INBAND OUTPUT SPECTRUM



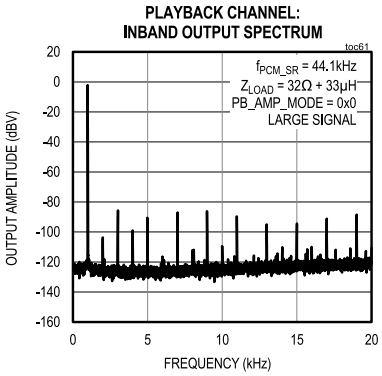
PLAYBACK CHANNEL: INBAND OUTPUT SPECTRUM



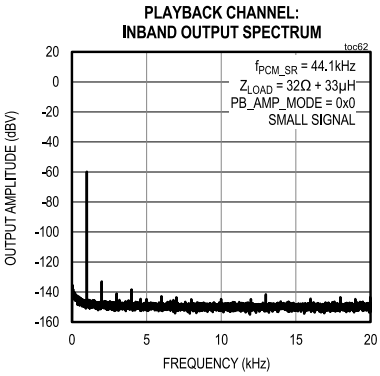
PLAYBACK CHANNEL: INBAND OUTPUT SPECTRUM



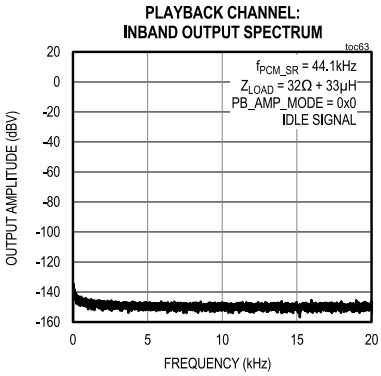
PLAYBACK CHANNEL: INBAND OUTPUT SPECTRUM



PLAYBACK CHANNEL: INBAND OUTPUT SPECTRUM



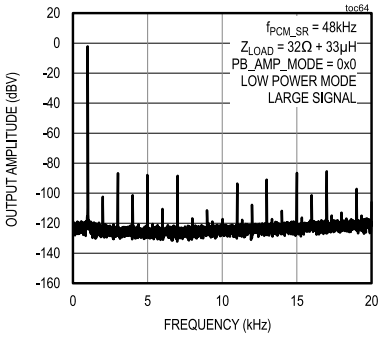
PLAYBACK CHANNEL: INBAND OUTPUT SPECTRUM



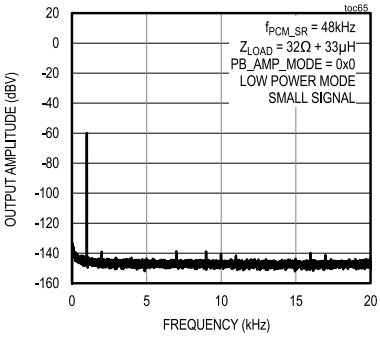
Typical Operating Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIAS1}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, Typical values at T_A = +25°C)

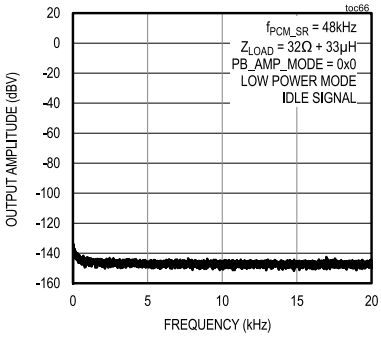
PLAYBACK CHANNEL: INBAND OUTPUT SPECTRUM



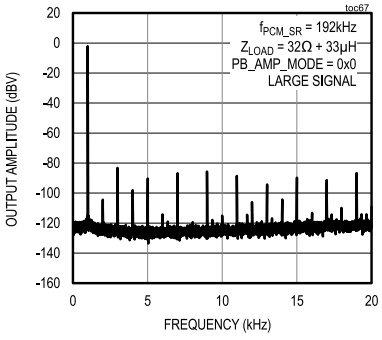
PLAYBACK CHANNEL: INBAND OUTPUT SPECTRUM



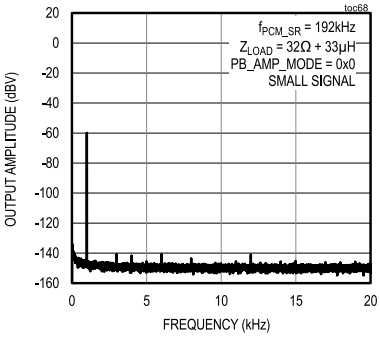
PLAYBACK CHANNEL: INBAND OUTPUT SPECTRUM



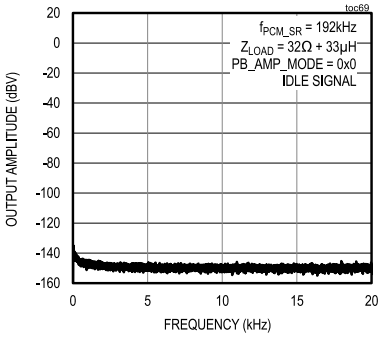
PLAYBACK CHANNEL: INBAND OUTPUT SPECTRUM



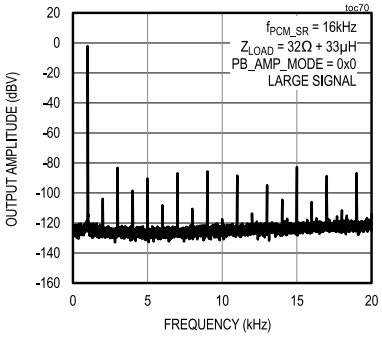
PLAYBACK CHANNEL: INBAND OUTPUT SPECTRUM



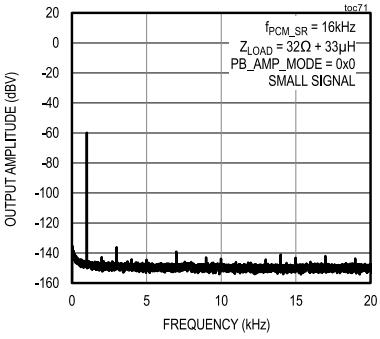
PLAYBACK CHANNEL: INBAND OUTPUT SPECTRUM



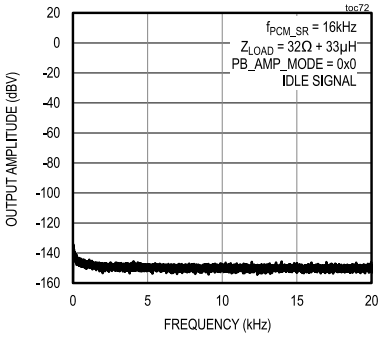
PLAYBACK CHANNEL: INBAND OUTPUT SPECTRUM



PLAYBACK CHANNEL: INBAND OUTPUT SPECTRUM



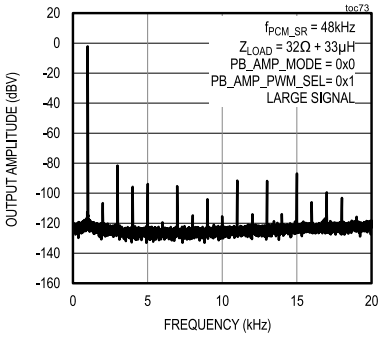
PLAYBACK CHANNEL: INBAND OUTPUT SPECTRUM



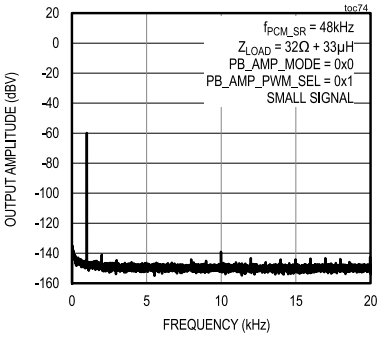
Typical Operating Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIAS1}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, Typical values at T_A = +25°C)

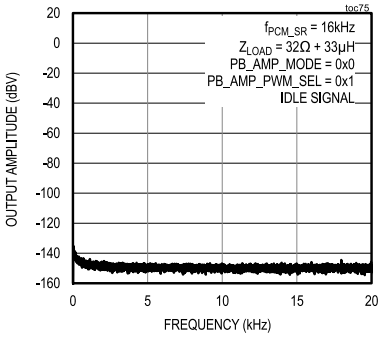
PLAYBACK CHANNEL:
INBAND OUTPUT SPECTRUM



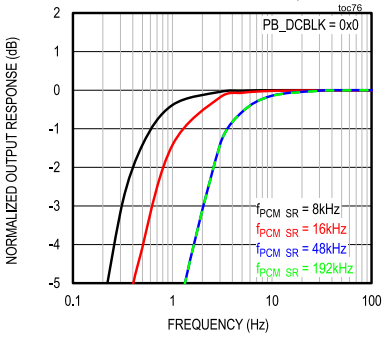
PLAYBACK CHANNEL:
INBAND OUTPUT SPECTRUM



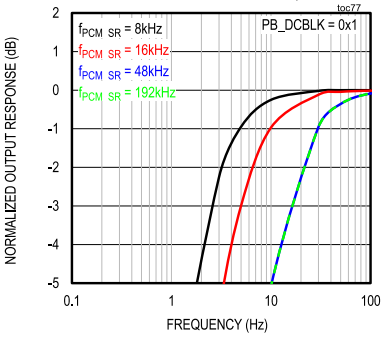
PLAYBACK CHANNEL:
INBAND OUTPUT SPECTRUM



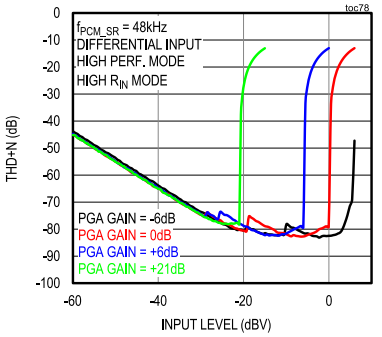
PLAYBACK CHANNEL:
DC BLOCKER CORNER FREQUENCY



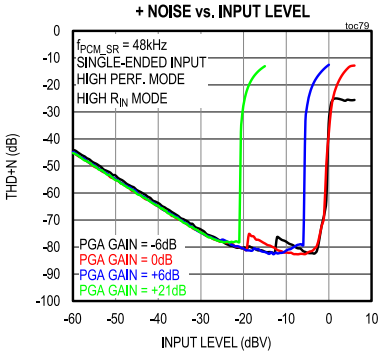
PLAYBACK CHANNEL:
DC BLOCKER CORNER FREQUENCY



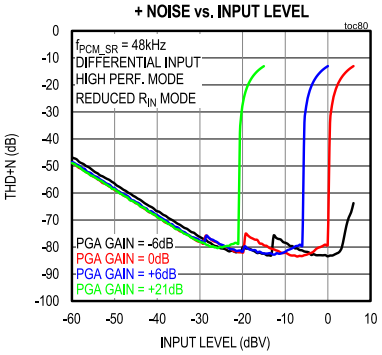
ANALOG MICROPHONE RECORD:
TOTAL HARMONIC DISTORTION
+ NOISE vs. INPUT LEVEL



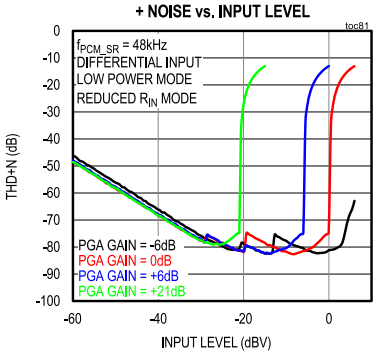
ANALOG MICROPHONE RECORD:
TOTAL HARMONIC DISTORTION
+ NOISE vs. INPUT LEVEL



ANALOG MICROPHONE RECORD:
TOTAL HARMONIC DISTORTION
+ NOISE vs. INPUT LEVEL



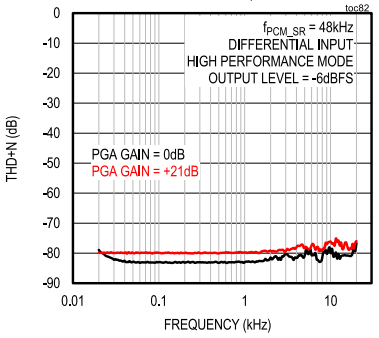
ANALOG MICROPHONE RECORD:
TOTAL HARMONIC DISTORTION
+ NOISE vs. INPUT LEVEL



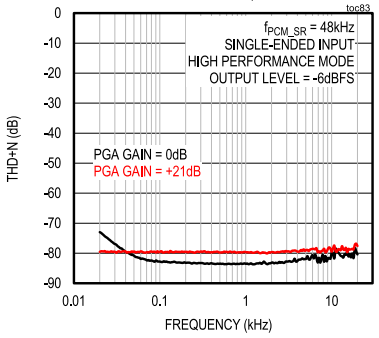
Typical Operating Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIAS1}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, Typical values at T_A = +25°C)

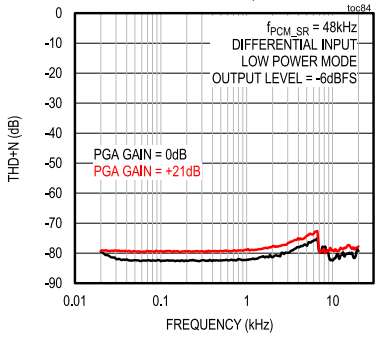
ANALOG MICROPHONE RECORD:
TOTAL HARMONIC DISTORTION + NOISE
vs. INPUT FREQUENCY



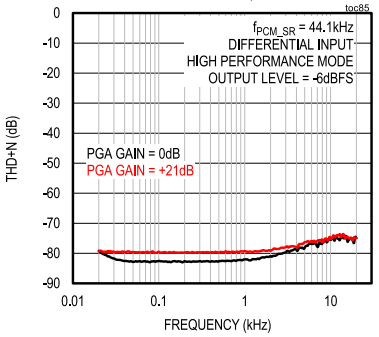
ANALOG MICROPHONE RECORD:
TOTAL HARMONIC DISTORTION + NOISE
vs. INPUT FREQUENCY



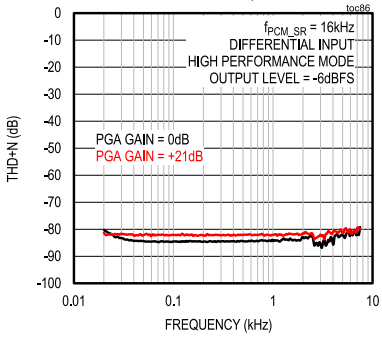
ANALOG MICROPHONE RECORD:
TOTAL HARMONIC DISTORTION + NOISE
vs. INPUT FREQUENCY



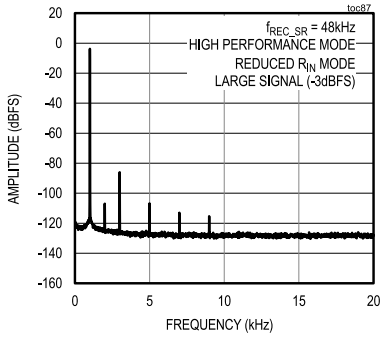
ANALOG MICROPHONE RECORD:
TOTAL HARMONIC DISTORTION + NOISE
vs. INPUT FREQUENCY



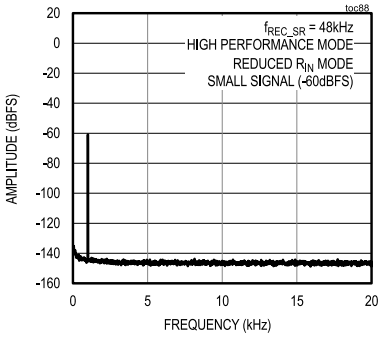
ANALOG MICROPHONE RECORD:
TOTAL HARMONIC DISTORTION + NOISE
vs. INPUT FREQUENCY



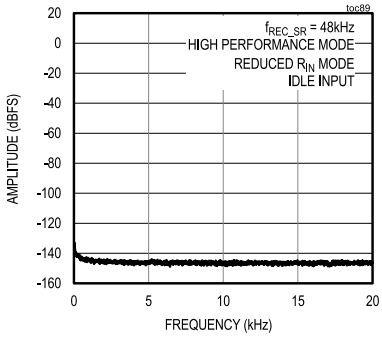
ANALOG MICROPHONE RECORD:
INBAND SPECTRUM



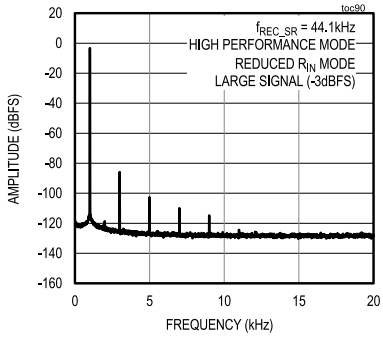
ANALOG MICROPHONE RECORD:
INBAND SPECTRUM



ANALOG MICROPHONE RECORD:
INBAND SPECTRUM



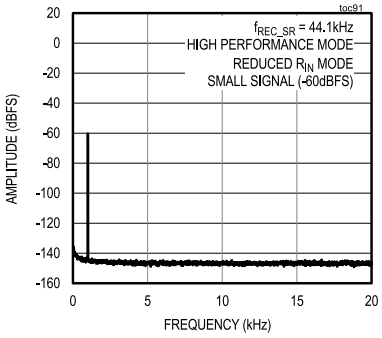
ANALOG MICROPHONE RECORD:
INBAND SPECTRUM



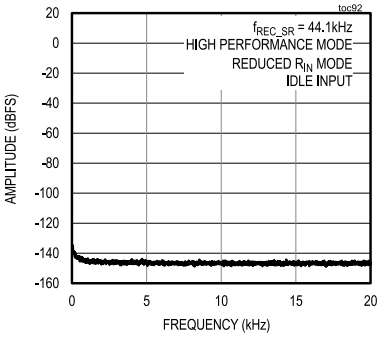
Typical Operating Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIAS1}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, Typical values at T_A = +25°C)

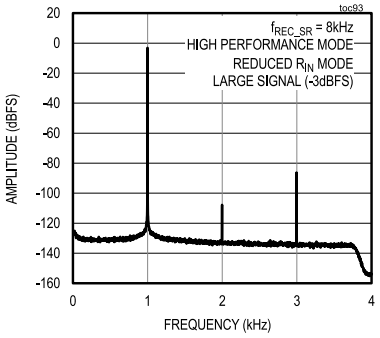
ANALOG MICROPHONE RECORD: INBAND SPECTRUM



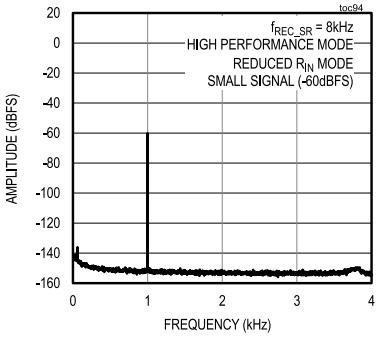
ANALOG MICROPHONE RECORD: INBAND SPECTRUM



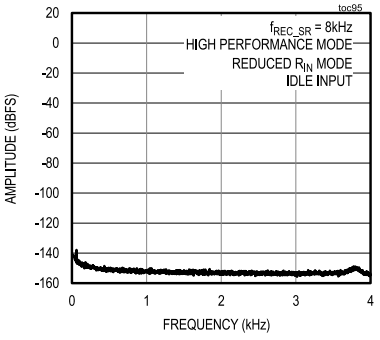
ANALOG MICROPHONE RECORD: INBAND SPECTRUM



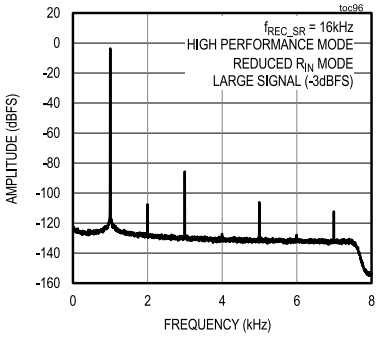
ANALOG MICROPHONE RECORD: INBAND SPECTRUM



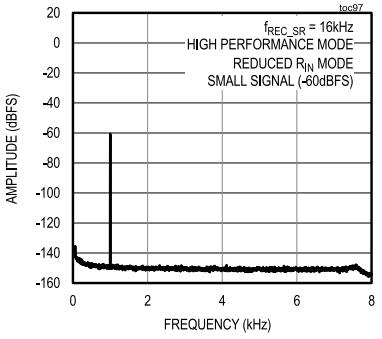
ANALOG MICROPHONE RECORD: INBAND SPECTRUM



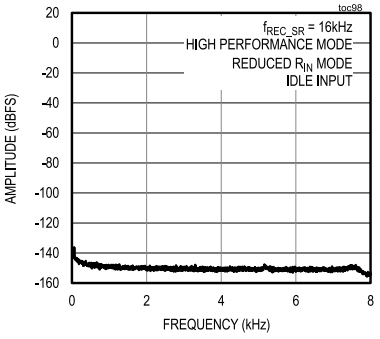
ANALOG MICROPHONE RECORD: INBAND SPECTRUM



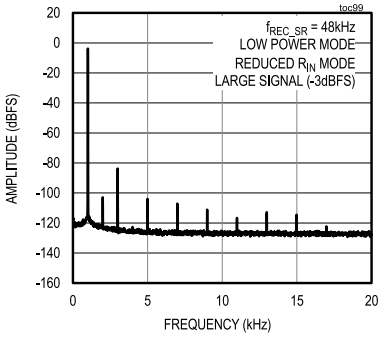
ANALOG MICROPHONE RECORD: INBAND SPECTRUM



ANALOG MICROPHONE RECORD: INBAND SPECTRUM



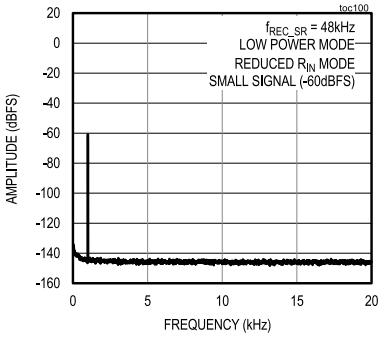
ANALOG MICROPHONE RECORD: INBAND SPECTRUM



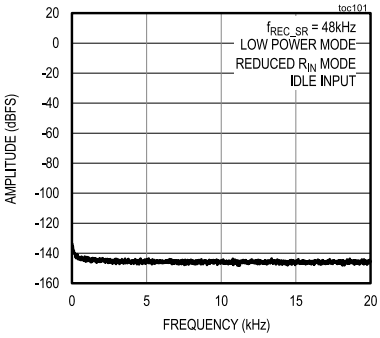
Typical Operating Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIAS1}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, Typical values at T_A = +25°C)

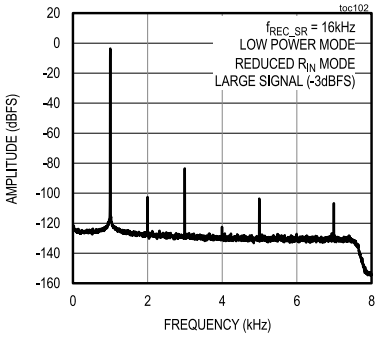
ANALOG MICROPHONE RECORD: INBAND SPECTRUM



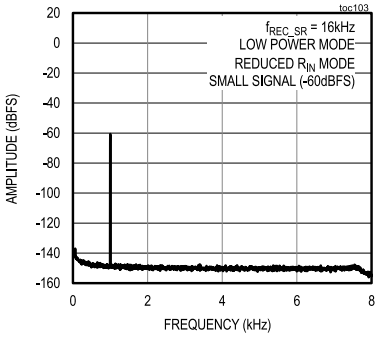
ANALOG MICROPHONE RECORD: INBAND SPECTRUM



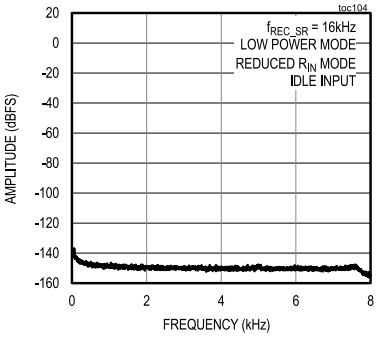
ANALOG MICROPHONE RECORD: INBAND SPECTRUM



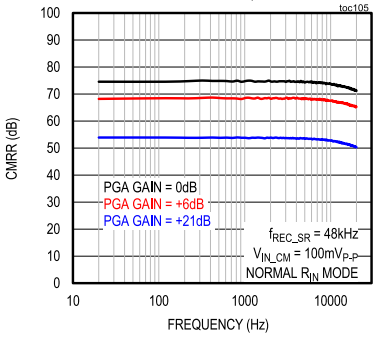
ANALOG MICROPHONE RECORD: INBAND SPECTRUM



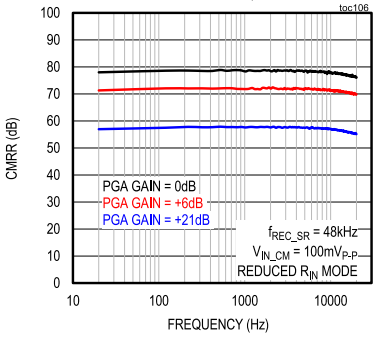
ANALOG MICROPHONE RECORD: INBAND SPECTRUM



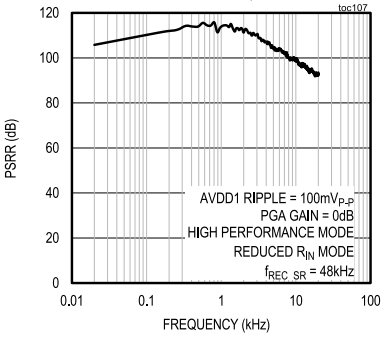
ANALOG MICROPHONE INPUT: COMMON MODE REJECTION RATIO vs. FREQUENCY



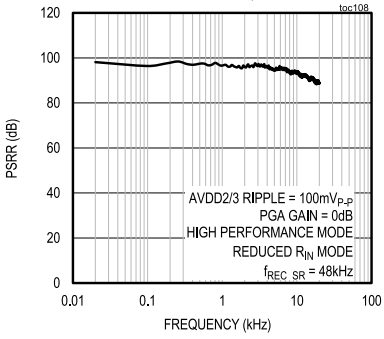
ANALOG MICROPHONE INPUT: COMMON MODE REJECTION RATIO vs. FREQUENCY



ANALOG MICROPHONE RECORD: AVDD1 POWER SUPPLY REJECTION RATIO vs. FREQUENCY



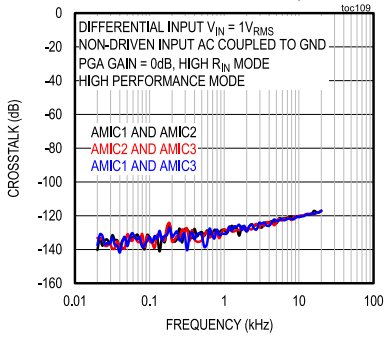
ANALOG MICROPHONE RECORD: AVDD2/3 POWER SUPPLY REJECTION RATIO vs. FREQUENCY



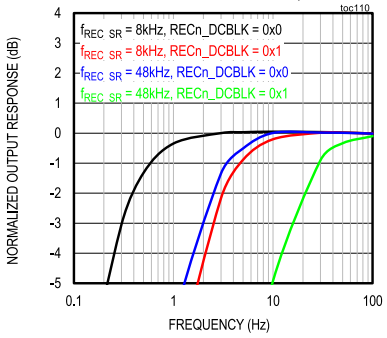
Typical Operating Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIAS1}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, Typical values at T_A = +25°C)

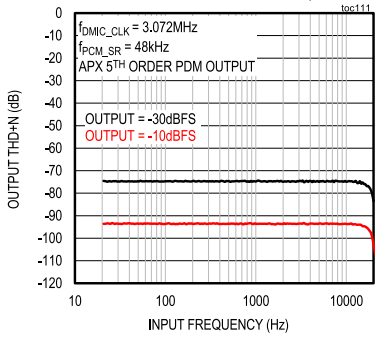
ANALOG MICROPHONE RECORD: INPUT CROSSTALK vs. FREQUENCY



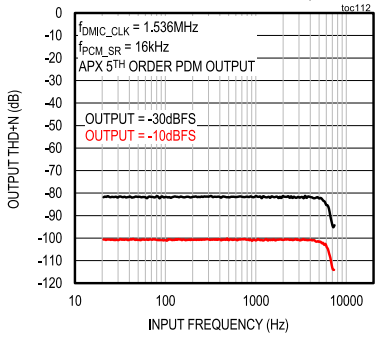
MICROPHONE RECORD CHANNEL: DC BLOCKER CORNER FREQUENCY



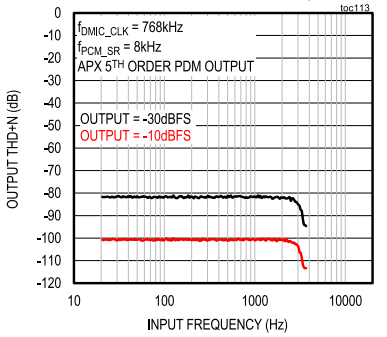
DIGITAL MICROPHONE RECORD: OUTPUT THD+N vs. INPUT FREQUENCY



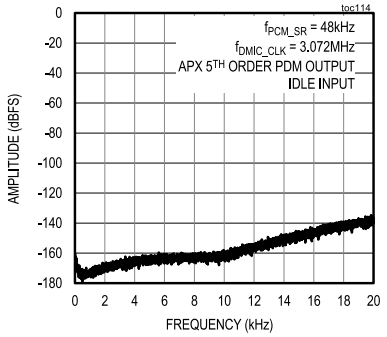
DIGITAL MICROPHONE RECORD: OUTPUT THD+N vs. INPUT FREQUENCY



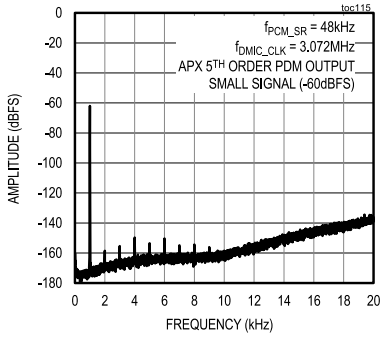
DIGITAL MICROPHONE RECORD: OUTPUT THD+N vs. INPUT FREQUENCY



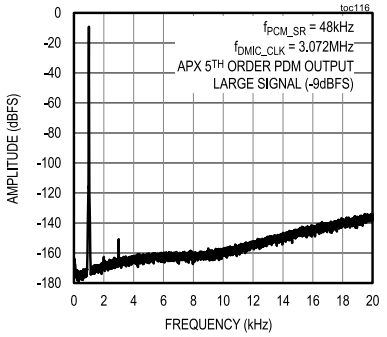
DIGITAL MICROPHONE RECORD: INBAND SPECTRUM



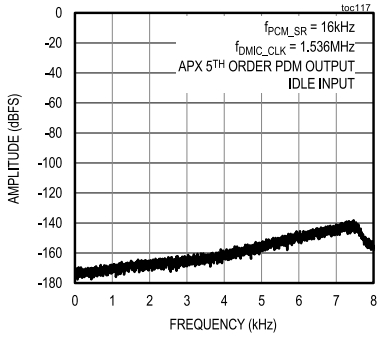
DIGITAL MICROPHONE RECORD: INBAND SPECTRUM



DIGITAL MICROPHONE RECORD: INBAND SPECTRUM



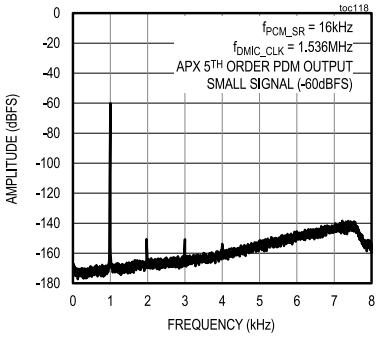
DIGITAL MICROPHONE RECORD: INBAND SPECTRUM



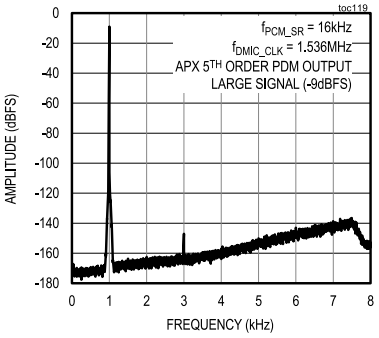
Typical Operating Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIAS1}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, Typical values at T_A = +25°C)

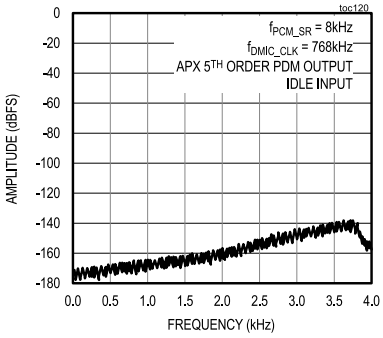
DIGITAL MICROPHONE RECORD: INBAND SPECTRUM



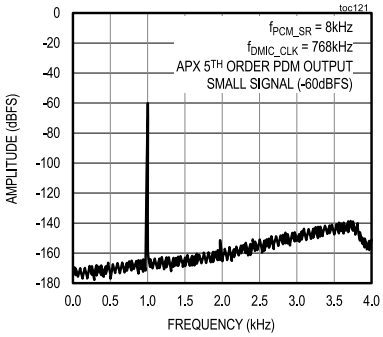
DIGITAL MICROPHONE RECORD: INBAND SPECTRUM



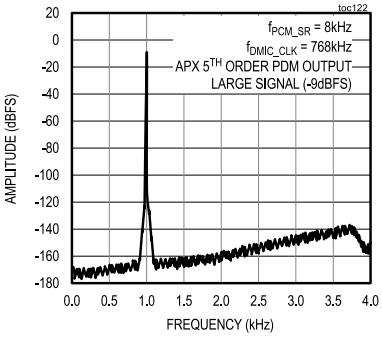
DIGITAL MICROPHONE RECORD: INBAND SPECTRUM



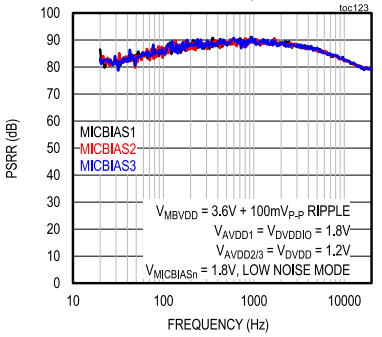
DIGITAL MICROPHONE RECORD: INBAND SPECTRUM



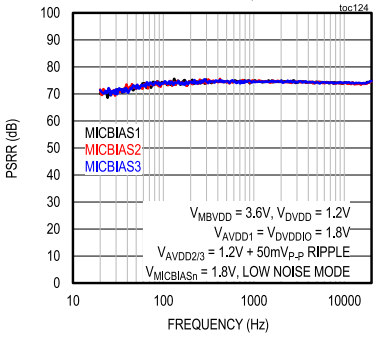
DIGITAL MICROPHONE RECORD: INBAND SPECTRUM



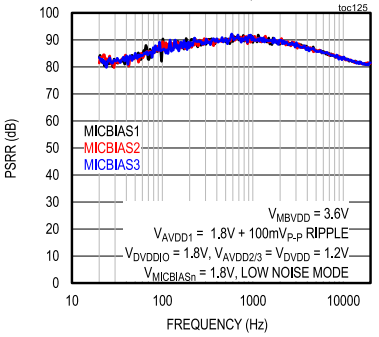
MICROPHONE BIAS OUTPUTS: MBVDD POWER SUPPLY REJECTION RATIO vs. FREQUENCY



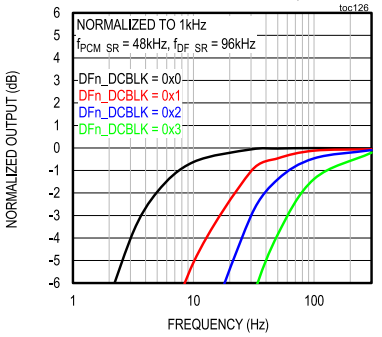
MICROPHONE BIAS OUTPUTS: AVDD2/3 POWER SUPPLY REJECTION RATIO vs. FREQUENCY



MICROPHONE BIAS OUTPUTS: AVDD1 POWER SUPPLY REJECTION RATIO vs. FREQUENCY



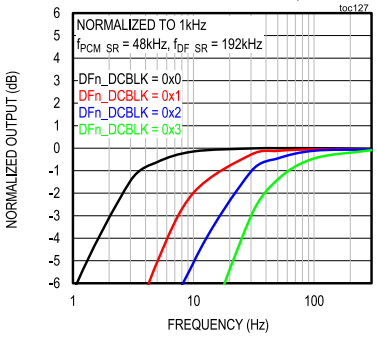
DIGITAL FILTER CHANNEL: DC BLOCKER CORNER FREQUENCY



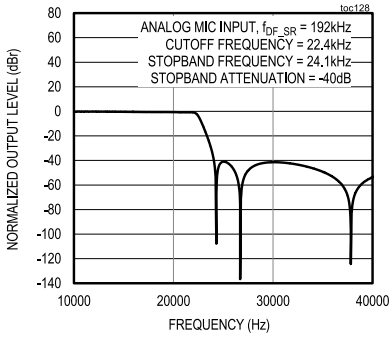
Typical Operating Characteristics (continued)

(V_{AVDD1} = V_{DVDDIO} = 1.8V, V_{AVDD2} = V_{AVDD3} = V_{DVDD} = 1.2V, V_{MBVDD} = 3.6V, GND = DGND = 0V, C_{MBVDD} = $C_{MICBIAS1}$ = 2.2µF, C_{AVDD1} = C_{AVDD1_REG} = C_{AVDD2} = C_{AVDD3} = C_{DVDD} = 1µF, C_{DVDDIO} = $C_{MICBIAS2}$ = $C_{MICBIAS3}$ = 0.1µF, High-Performance Record and Playback Modes, Z_{LOAD} = OPEN, f_{LRCLK} = 48kHz, f_{S_DF} = 192kHz, f_{BCLK} = 3.072MHz, f_{DMIC_CLK} = 3.072MHz, AC Measurement Bandwidth = 20Hz to 20kHz, Typical values at T_A = +25°C)

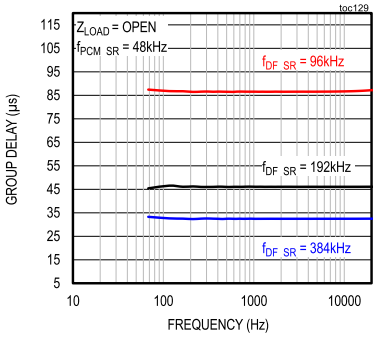
DIGITAL FILTER CHANNEL: DC BLOCKER CORNER FREQUENCY



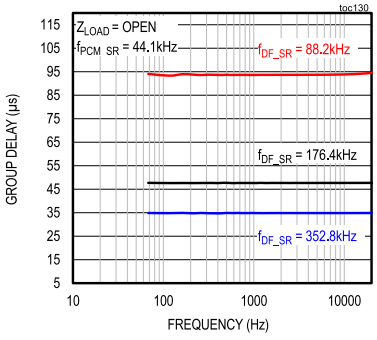
DIGITAL FILTER CHANNEL: EXAMPLE ULTRASOUND FILTER MAGNITUDE RESPONSE



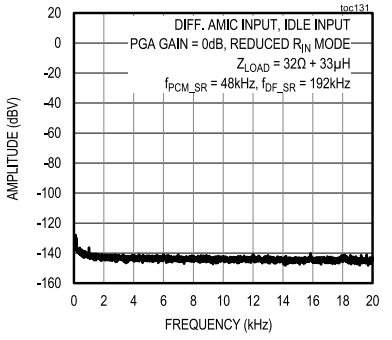
DIGITAL FILTER CHANNEL: MICROPHONE INPUT TO PLAYBACK OUTPUT GROUP DELAY



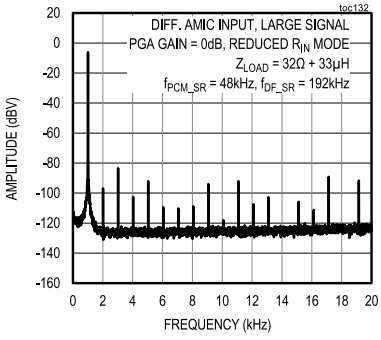
DIGITAL FILTER CHANNEL: MICROPHONE INPUT TO PLAYBACK OUTPUT GROUP DELAY



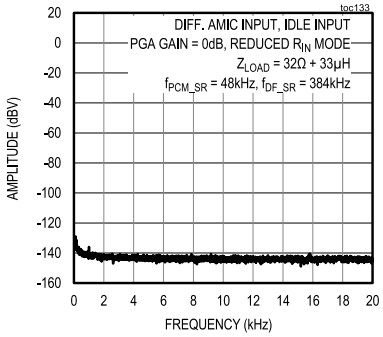
AMIC INPUT TO DIGITAL FILTER CHANNEL TO PLAYBACK OUTPUT: INBAND SPECTRUM



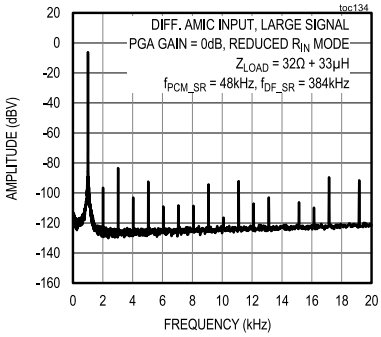
AMIC INPUT TO DIGITAL FILTER CHANNEL TO PLAYBACK OUTPUT: INBAND SPECTRUM



AMIC INPUT TO DIGITAL FILTER CHANNEL TO PLAYBACK OUTPUT: INBAND SPECTRUM

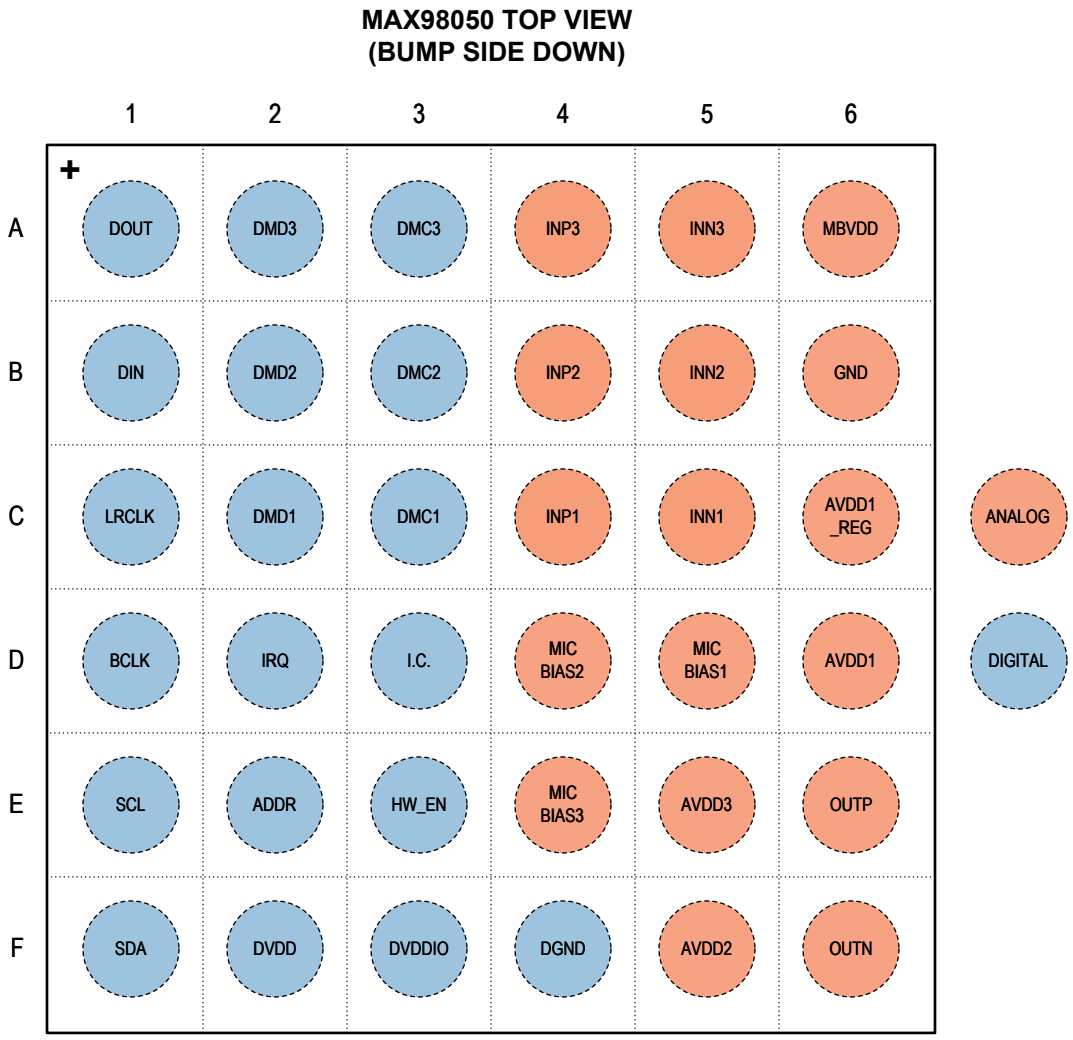


AMIC INPUT TO DIGITAL FILTER CHANNEL TO PLAYBACK OUTPUT: INBAND SPECTRUM



Pin Configuration

MAX98050 WLP Package



Pin Description

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
D6	AVDD1	Analog High Supply. This is the input supply for the high voltage analog, the amplifier high-swing class-D mode, and the analog 1.6V linear regulator. The device transitions to hardware shutdown, and all registers are reset to their PoR values when this drops below its UVLO threshold. Bypass to GND with at least a 1µF capacitor.	—	Power
F5	AVDD2	Analog Low Supply. This is the input supply for low voltage analog and the amplifier in class-AB mode. The device transitions to hardware shutdown, and all registers are reset to their PoR values when this drops below its UVLO threshold. This can be connected directly to AVDD3, and both supplies share a single bypass capacitor to DGND of at least 1µF. If not connected to AVDD3, then bypass it separately to GND.	—	Power
E5	AVDD3	Amplifier Low Supply. This is the amplifier low power class-D mode supply. The device transitions to hardware shutdown, and all registers are reset to their PoR values when this drops below its UVLO threshold. This can be connected directly to AVDD2, and both supplies share a single bypass capacitor to DGND of at least 1µF. If not connected to AVDD2, then bypass it separately to DGND.	—	Power
F2	DVDD	Digital Core Input Power Supply. The device transitions to hardware shutdown, and all registers are reset to their PoR values when this drops below its UVLO threshold. Bypass to DGND with at least a 1µF capacitor.	—	Power
F3	DVDDIO	Digital Interface Logic Level Power Supply. Selects the reference logic voltage level for the PCM and I^2C digital interfaces. Bypass to DGND with at least a 0.1µF capacitor.	—	Power
A6	MBVDD	Microphone Bias Input Supply. Provides the input to the microphone bias linear regulator. Connect to a supply exceeding the minimum dropout voltage for the selected output microphone bias level. Can be directly connected to a single cell battery. Connect to GND or leave unconnected if the microphone bias is not used (always disabled). If microphone bias is used, bypass to GND with a 1µF capacitor.	—	Power
C6	AVDD1_REG	Analog High Supply Linear Regulator Output. This is the output of the analog 1.6V linear regulator. Bypass to GND with a 1µF capacitor. This should never be connected to an external load.	AVDD1	Power
D5	MICBIAS1	Direct Microphone Bias Output 1 and Bypass Connection. Whenever microphone bias is enabled, this output always provides the selected microphone bias output voltage (cannot be gated). Leave unconnected if microphone bias is never enabled, otherwise always bypass to GND with a 2.2µF capacitor.	MBVDD	
D4	MICBIAS2	Gated Microphone Bias Output 2. This output provides the selected microphone bias output voltage when both microphone bias is enabled and this output is enabled. Leave unconnected if this microphone bias output is never enabled, otherwise bypass to GND with at least a 0.1µF capacitor (may be shared if the analog microphone requires bypass as well).	MBVDD	

Pin Description (continued)

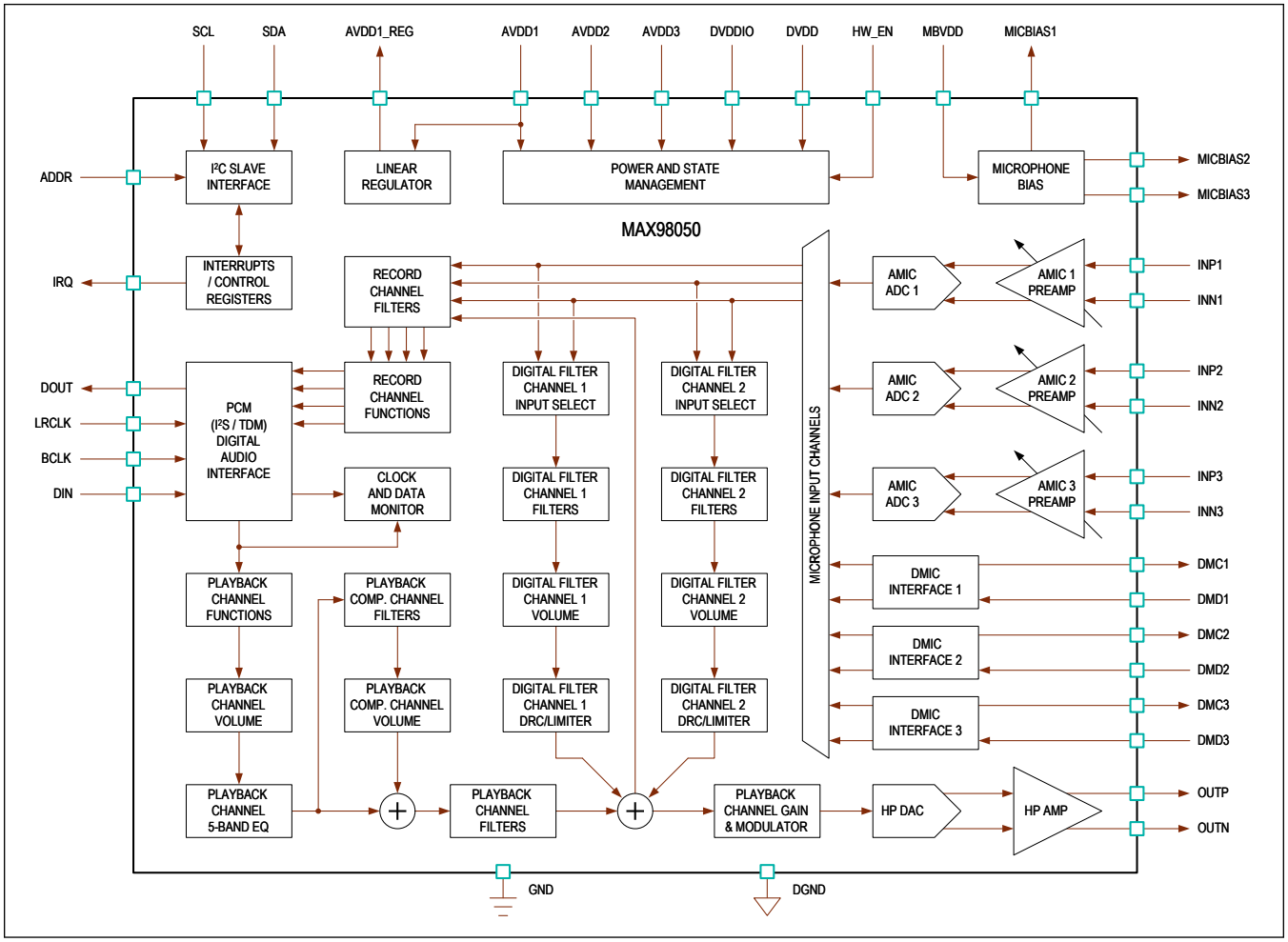
PIN	NAME	FUNCTION	REF SUPPLY	TYPE
E4	MICBIAS3	Gated Microphone Bias Output 3. This output provides the selected microphone bias output voltage when both microphone bias is enabled and this output is enabled. Leave unconnected if this microphone bias output is never enabled, otherwise bypass to GND with at least a 0.1µF capacitor (may be shared if the analog microphone requires bypass as well).	MBVDD	
B6	GND	Device Quiet Ground. Ground reference for all sensitive and core analog blocks.	—	Power
F4	DGND	Device Digital Ground. Ground reference for the amplifier class-D switching stage, the digital interfaces, and the digital core.	—	Power
E1	SCL	I^2C-Compatible Serial-Clock Input. For the full signal swing, connect an external pullup resistor (typically 1.5kΩ for FM+ clock rate support) to DVDDIO.	DVDDIO	
F1	SDA	I^2C-Compatible Serial-Data Input/Output. For the full signal swing, connect an external pullup resistor (typically 1.5kΩ for FM+ clock rate support) to DVDDIO.	DVDDIO	
D2	IRQ	Hardware Interrupt Output. For the full signal swing in open-drain mode, connect an external pullup resistor (typically at least 1.5kΩ) to DVDDIO. A software enabled internal 100kΩ pullup resistor is also available. A pullup resistor is not needed in push-pull mode.	DVDDIO	
E2	ADDR	Serial Interface Address Select. This connection selects from four possible I^2C slave addresses.	DVDDIO	
E3	HW_EN	Device Hardware Enable Input. When pulled low, the device is placed into and held in hardware shutdown. When pulled high to DVDDIO, the device can exit hardware shutdown if all supplies are above their UVLO thresholds.	DVDDIO	
D1	BCLK	PCM Bit Clock Input. Internally pulled down to DGND (R_{PD}).	DVDDIO	
C1	LRCLK	PCM Frame Clock Input. Internally pulled down to DGND (R_{PD}).	DVDDIO	
B1	DIN	PCM Data Input. Internally pulled down to DGND (R_{PD}).	DVDDIO	
A1	DOUT	PCM Data Output Bus. Internally pulled down to DGND (R_{PD}) when disabled.	DVDDIO	
E6	OUTP	Headphone Amplifier Positive Output	AVDD1	
F6	OUTN	Headphone Amplifier Negative Output	AVDD1	
C4	INP1	Analog Microphone 1 Positive Input	AVDD1_REG	
C5	INN1	Analog Microphone 1 Negative Input	AVDD1_REG	
B4	INP2	Analog Microphone 2 Positive Input	AVDD1_REG	
B5	INN2	Analog Microphone 2 Negative Input	AVDD1_REG	
A4	INP3	Analog Microphone 3 Positive Input	AVDD1_REG	
A5	INN3	Analog Microphone 3 Negative Input	AVDD1_REG	
C3	DMC1	Digital Microphone Interface 1 Clock Output	DVDDIO	
C2	DMD1	Digital Microphone Interface 1 Data Input	DVDDIO	
B3	DMC2	Digital Microphone Interface 2 Clock Output	DVDDIO	
B2	DMD2	Digital Microphone Interface 2 Data Input	DVDDIO	

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
A3	DMC3	Digital Microphone Interface 3 Clock Output	DVDDIO	
A2	DMD3	Digital Microphone Interface 3 Data Input	DVDDIO	
D3	I.C.	Internally Connected. Not used for normal device operation. Connect to GND externally.	—	Power

Functional Diagrams

Detailed Block Diagram



Detailed Description

Device State Control

The device supports three distinct operating states. Hardware shutdown and software shutdown are low-power states that support very limited device functionality. Audio playback and/or record are only possible in the audio state.

A combination of hardware and software controls are provided to configure the current device operating state. If properly sequenced, the state transitions do not result in audible glitches. The device protection and monitor features can also force operating state changes (and are detailed separately from the state descriptions). Forced state transitions that are the result of fault conditions may result in audible glitches.

Hardware Shutdown State

When the device is first powered up or after a hardware reset event, the device always initializes into the hardware shutdown (or reset) state. In hardware shutdown, the device is configured to its lowest power state. Upon entering hardware shutdown, the device is globally placed into a reset condition. As a result, the I^2C control interface is disabled and all device registers are returned to their PoR states.

When exiting hardware shutdown, the device initializes and then transitions into the software shutdown state. During this transition (as part of initialization), the OTP register trim settings are loaded. If the transition to software shutdown completes successfully, an INIT_DONE_* interrupt is generated. If this interrupt is seen unexpectedly during normal operation, this may be interpreted by software as an unexpected device reset or re-initialization.

If the OTP load routine fails to complete successfully during the transition, the device automatically retries several times. If the retries continue to fail, the transition is completed and an OTP_FAIL_* interrupt is generated once the device reaches the software shutdown state. To manually retry initialization, the software can reset the device with the software reset bit (RST). However, if the transition to software shutdown continues to fail (even with stable supplies in place prior to the transition), this may be indicative of a damaged or incorrectly trimmed device and it should not be operated.

When the hardware reset input (HW_EN) is asserted low, the device enters (or remains in) hardware shutdown. The device is also placed into hardware shutdown anytime the AVDDn, DVDD, or DVDDIO supplies drop below their respective UVLO thresholds. The device only exits hardware shutdown when all of these supplies are all above their respective UVLO thresholds, and the hardware reset input (HW_EN) is asserted high. Once all these conditions are met, the device automatically exits hardware shutdown, and transitions into software shutdown.

Software Shutdown State

The device enters the software shutdown state after it transitions out of hardware shutdown state and when exiting the audio state. When the device is in the software shutdown state (AUDIO_EN = 0), all blocks are automatically disabled and in their lowest power states except for interfaces (including I^2C for programming), fault recovery monitors (such as clock stop auto recovery), and the AMIC bias generator. In the software shutdown state, all device registers can be programmed without restriction and all programmed register states are retained. If the software reset bit (RST) is written with a 1, the device is reset (all register states return to PoR values), and the device automatically transitions back into the software shutdown state.

The audio enable bit (AUDIO_EN) must be set high to allow the device to transition out of software shutdown state and into the audio state. Once it is set high the device may transition to the audio state (if at least one audio channel is enabled) and the transition is complete when the appropriate interrupts have been generated (PB_PWRUP_DONE_* and/or REC_PWRUP_DONE_* if enabled). When the audio enable bit (AUDIO_EN) is set low (or all audio channels are disabled) the device transitions back from the audio state to the software shutdown state, and when the transition is completed, a power down done (PWRDN_DONE_*) interrupt is generated (if enabled).

Audio State

The device transitions from the software shutdown state to the audio state when the audio enable bit (AUDIO_EN) is set high, and at least one PCM record channel enable bit (RECn_PCM_EN) or the PCM playback channel enable bit (PB_EN) is also set high.

The transition from the software shutdown state to the audio state is complete and the enabled audio channels are ready when the appropriate interrupts have been generated (PB_PWRUP_DONE_* and/or REC_PWRUP_DONE_* if enabled). In addition, if the device is already in the audio state (with only record active) and the playback channel is dynamically enabled, the playback power-up done interrupt (PB_PWRUP_DONE_*) is generated when the device is ready to receive playback data. Likewise, if the device is already in the audio state (with only playback active) and one or more audio record channels are dynamically enabled (when previously all three were disabled), the record power-up done interrupt (REC_PWRUP_DONE_*) is generated when the device is ready to transmit record data. The record power-up done interrupt does not flag again if additional record channels are dynamically enabled while one or more record channels are already active.

In the audio state, dynamically enabling or disabling the record channels does not disrupt active audio on the playback channel (with or without active digital filter channels). When either the audio enable control bit (AUDIO_EN) is set low or when all three record channels and the playback channel are all disabled, the audio channels are powered down normally and the device transitions back into software shutdown state.

Audio State Quiescent Power Consumption

The typical device quiescent power consumption in the audio state for a variety of common use case configurations are detailed below. All supplies and operation conditions are configured to the global default settings (as shown in the *Electrical Characteristics Table* unless otherwise indicated). A typical hybrid filter profile (feedback and feed-forward microphone record) has two low-latency digital filter channels and the playback compensation channel active. A typical feed-forward (microphone record) filter profile has just a single low-latency digital filter channel active. These profiles can be used to implement common filter use cases including ambient / voice filters and ANC filters. Typical profiles assume each active low-latency digital filter channel has eight biquad bands enabled and tuned, and that when active the playback compensation channel has six biquad bands enabled and tuned.

Table 1. PCM Interface Playback Only Quiescent Power

DEVICE MODE AND CONFIGURATION	I_{AVDD1} (mA)	I_{AVDD2} (mA)	I_{DVDD} (mA)	I_{DVDDIO} (mA)	POWER (mW)
Playback at f_S = 48kHz, High-Performance Mode	0.03	0.46	1.7	0.002	2.65
Playback at f_S = 48kHz, Low-Power Mode	0.03	0.38	1.7	0.002	2.55
Playback at f_S = 48kHz, Noise Gate Enabled, High-Performance Mode	0.03	0.46	1.09	0.002	1.92
Playback at f_S = 48kHz, 5-Band Equalizer Enabled in Pass-Through, High-performance Mode	0.03	0.46	1.78	0.002	2.75
Playback at f_S = 8kHz, High-Performance Mode	0.03	0.46	1.49	0.002	2.40
Playback at f_S = 192kHz, High-Performance Mode	0.03	0.46	2.07	0.002	3.09

Table 2. PCM Interface Record Only Quiescent Power

DEVICE MODE AND CONFIGURATION	I_{AVDD1} (mA)	I_{AVDD2} (mA)	I_{DVDD} (mA)	I_{DVDDIO} (mA)	POWER (mW)
Two AMIC Record Channels at f_S = 48kHz, High-Performance Mode	2.18	0.05	2.11	0.013	6.54
Three AMIC Record Channels at f_S = 48kHz, High-Performance Mode	3.26	0.05	2.41	0.013	8.84
Two AMIC Record Channels at f_S = 48kHz, Low-Power Mode	1.71	0.05	2.11	0.013	5.69
Three AMIC Record Channels at f_S = 48kHz, Low-Power Mode	2.55	0.05	2.41	0.013	7.56
Two AMIC Record Channels at f_S = 16kHz, Low-Power Mode	1.71	0.05	1.76	0.003	5.26
Two DMIC Record Channels at f_S = 48kHz, DMIC Clock at 3.072MHz	0.016	0.05	1.92	0.14	2.64
Two DMIC Record Channels at f_S = 8kHz, DMIC Clock at 768kHz	0.016	0.05	1.50	0.04	1.96

Table 3. PCM Interface Record and Playback Quiescent Power

DEVICE MODE AND CONFIGURATION	I_{AVDD1} (mA)	I_{AVDD2} (mA)	I_{DVDD} (mA)	I_{DVDDIO} (mA)	POWER (mW)
Playback and Two AMIC Record Channels at f_S = 48kHz, High-Performance Modes	2.18	0.46	2.95	0.013	8.04
Playback and Three AMIC Record Channels at f_S = 48kHz, High-Performance Modes	3.26	0.46	3.27	0.013	10.36
Playback and Two AMIC Record Channels at f_S = 48kHz, Low-Power Modes	1.71	0.38	2.95	0.013	7.09
Playback and Three AMIC Record Channels at f_S = 48kHz, Low-Power Modes	2.55	0.38	3.27	0.013	8.99
Playback and Two AMIC Record Channels at f_S = 16kHz, High-Performance Modes	2.18	0.46	2.50	0.005	7.49
Playback and Two DMIC Record Channels at f_S = 48kHz, DMIC Clock at 3.072MHz	0.03	0.46	2.79	0.14	4.20
Playback and Two DMIC Record Channels at f_S = 8kHz, DMIC Clock at 768kHz	0.03	0.46	2.21	0.04	3.33

Table 4. PCM Interface Playback with Digital Filter Channels Quiescent Power

DEVICE MODE AND CONFIGURATION	I_{AVDD1} (mA)	I_{AVDD2} (mA)	I_{DVDD} (mA)	I_{DVDDIO} (mA)	POWER (mW)
Playback with Compensation Enabled at f_S = 48kHz, Two AMIC Input Digital Filter Channels at f_S = 192kHz, Typical Hybrid Profile, High-Performance Modes	2.18	0.46	5.26	0.002	10.79
Playback with Compensation Enabled at f_S = 48kHz, Two AMIC Input Digital Filter Channels at f_S = 192kHz, Typical Hybrid Profile, Low-Power Modes	1.71	0.38	5.26	0.002	9.85
Playback with Compensation Enabled at f_S = 48kHz, Two AMIC Input Digital Filter Channels at f_S = 384kHz, Typical Hybrid Profile, High-Performance Modes	2.18	0.46	7.28	0.002	13.21
Playback at f_S = 48kHz, One AMIC Input Digital Filter Channel at f_S = 192kHz, Typical Feed-Forward Profile, High-Performance Modes	1.10	0.46	3.88	0.002	7.19
Playback at f_S = 48kHz, One AMIC Input Digital Filter Channel at f_S = 192kHz, Typical Feed-Forward Profile, Low-Power Modes	0.87	0.38	3.88	0.002	6.68
Playback with Compensation Enabled at f_S = 48kHz, Two DMIC Inputs at 3.072MHz to Digital Filter Channels at f_S = 192kHz, Typical Hybrid Profile, High-Performance Modes	0.03	0.46	5.17	0.13	7.04
Playback at f_S = 48kHz, One DMIC Input at 3.072MHz to Digital Filter Channel at f_S = 192kHz, Typical Feed-Forward Profile, High-Performance Modes	0.03	0.46	3.77	0.07	5.26

State Transition Diagram

Figure 7 shows the three device states and the state transition conditions. Normal state transitions between the audio state and the software shutdown state do not produce audible glitches on the output of the playback channel in excess of specifications (with the appropriate rate of volume ramping enabled on the playback channel and on any active digital filter channels).

If playback ramping is disabled, to avoid audible glitches the audio playback data needs to be silent (zero codes) and the low-latency digital filter channels should be disabled prior to enabling or disabling the playback channel (playback data ramping is then the responsibility of the host after enabling and prior to disabling the playback channel). Furthermore, the host should stop accepting record channel data prior to disabling a channel and/or initiating a transition from the audio state to the software shutdown state.

Forced state transitions occur immediately and may impact record data and/or produce audible playback glitches (see Figure 7). Fault events (such as clock failure, data error, amplifier overcurrent, FLL unlock, etc.) that occur unexpectedly during active audio record and/or playback (audio state) result in a forced state transition to the software shutdown state. Before initiating a software reset event (RST bit), de-asserting the hardware enable input (HW_EN pin), or disabling supplies (AVDDn, DVDD, or DVDDIO to below UVLO thresholds), the device should always be placed into the software shutdown state. If these actions are taken while the device is in the audio state, they trigger a forced state transition either to the hardware shutdown state (hardware enable and supply UVLO) or to the software shutdown state (reset event transitions briefly to hardware shutdown state to reset PoRs and then transition back into the software shutdown state).

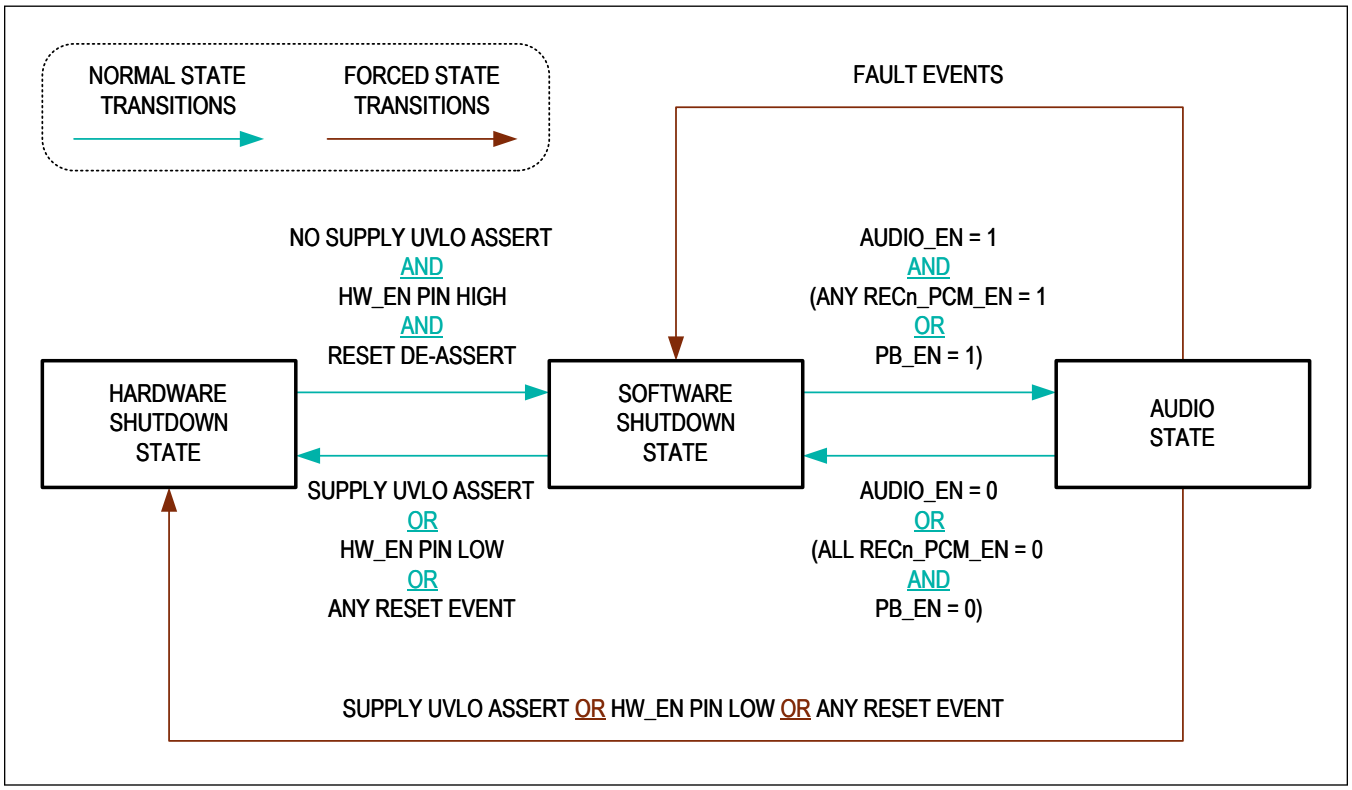


Figure 7. Device State Transition Diagram

Device Sequencing

The recommended device power-up and power-down sequences are provided for two use cases: simple record and/or playback and for playback with the low-latency digital filter channels enabled. Steps with the same number followed by a letter can be performed in any order (i.e., steps nA, nB, and nC are non-sequential sub-steps of step n). Note that these example sequences are for static use cases, and that for details regarding dynamic use case switching (enabling and disabling of audio channels while in the audio state) see the corresponding section for a given audio channel.

Example Sequencing for Audio Playback and/or Record

The following recommended device sequencing examples apply to audio playback, audio record, or use cases with both (all with the internal low-latency digital filter channels disabled). Note that while not described here, once the device is in the audio state, it is also possible to dynamically enable and disable audio playback and audio record channels without interrupting any already active channels as long as the register control bit restrictions are observed.

Table 5. Recommended Power-Up Sequence: Audio Record and/or Playback

STEP	ACTION (STATE)	DETAILED DESCRIPTION
0	None (Hardware Shutdown State)	This is the lowest power state. The device and all registers are fully reset in this state, and no control or audio interface interactions are possible.
1A	Power Up Device Supplies (Hardware Shutdown State)	Power the AVDD1, AVDD2, AVDD3, DVDD, and DVDDIO supplies to above the respective UVLO thresholds. No supply sequencing is required. Optionally, if an analog microphone bias output is needed, also power MBVDD.
1B	Set the Hardware Enable (Hardware Shutdown State)	Drive the hardware enable input (HW_EN) high or always connect to DVDDIO.
2	Transition to the Software Shutdown State (State Transition)	Once all conditions are met (steps 1A and 1B), the device automatically transitions to the software shutdown state. The transition is complete after the hardware enable time (t_{HW_EN}) has elapsed (if no errors/retries are needed). Do not attempt to program the device during this transition. When the transition successfully completes, an INIT_DONE interrupt is generated.
3	None (Software Shutdown State)	This is the lowest power state where register settings are retained and the I^2C interface is active. Can be used for a system idle/standby case or when system is active, but no audio use case is active. It is recommended that the system software verifies and then clears any interrupts upon entering this state.
4A	Program Device Registers (Software Shutdown State)	The system software should fully configure the device registers (except AUDIO_EN) for the desired audio use case.
4B	Configure the Analog Microphone Bias if Needed (Software Shutdown State)	If the analog microphone bias is needed while the device is in the software shutdown state, it can be configured and enabled at any time. If not, then it can be configured here but not enabled. It is then best to sequence the microphone bias enable (AMIC_BIAS_EN) just before the audio enable in step 5.
4C	Enable the External Clocks (Software Shutdown State)	Start the PCM interface clocks before exiting the software shutdown state.
5	Set Global Audio Enable Bit (Software Shutdown State)	Set the global audio enable bit high (AUDIO_EN) to allow the device to transition to the audio state (if all other conditions are met). If playback is enabled and playback volume ramping is disabled, then the input PCM playback data should be silent prior to and during the state transition.
6	Transition to the Audio State (State Transition)	The state transition is complete after the audio turn-on time (t_{ON}) has elapsed. Note that the duration of the audio turn-on time (t_{ON}) varies based on the configured record input charge time and playback volume ramp time. The transition has successfully completed when the power-up done interrupts are generated (REC_PWRUP_DONE_* and/or PB_PWRUP_DONE_*).

Table 5. Recommended Power-Up Sequence: Audio Record and/or Playback (continued)

STEP	ACTION (STATE)	DETAILED DESCRIPTION
7	Audio Record/Playback (Audio State)	The device is in the audio state with record and/or playback active (as configured). To avoid errors and audible glitches during any device programming in the audio state, all register restrictions must be observed.

Table 6. Recommended Power-Down Sequence: Audio Record and/or Playback

STEP	ACTION (STATE)	DETAILED DESCRIPTION
0	Audio Record/Playback (Audio State)	The device is in the audio state with record and/or playback active.
1	Clear Global Audio Enable Bit (Audio State)	Set the global audio enable bit (AUDIO_EN) low to direct the device to transition to the software shutdown state. If playback was enabled and playback volume ramping was disabled, then the input PCM playback data should be silent prior to and during the state transition.
2	Transition to the Software Shutdown State (State Transition)	The transition is complete after the audio turn-off time (t_{OFF}) has elapsed. Note that the duration of the audio turn-off time (t_{OFF}) varies based on the configured playback volume ramp time. The transition has successfully completed when the power down interrupt is generated (PWRDN_DONE_*).
3	Idle/Reprogram Device (Software Shutdown State)	The device can idle in the software shutdown state, and the clocks can be disabled to save power. The device can be freely reconfigured in this state. It is recommended that the system software verify and then clear any interrupts upon entering this state. To return from this idle state to the audio state, start from step 3 in Table 5 and follow the power-up sequence from there.
4	Transition to the Hardware Shutdown State (State Transition)	Before transitioning to the hardware shutdown state, first ensure that the external clocks are disabled. Then, either assert the hardware enable input (HW_EN) to a valid logic low level for longer than the hardware disable time (t_{HW_DIS}) or power down any supply with a UVLO to below the threshold.
5	None (Hardware Shutdown State)	This is the lowest power state. All supplies may be disabled if desired. The device (including all interfaces and registers) is fully reset in this state.

Example Sequencing for Audio Playback with Low-Latency Digital Filters Active

The following recommended device sequencing applies to a use case of audio playback with one or both low-latency digital filter channels enabled. It is very similar to the sequencing for audio playback and/or record. However, a few extra steps are included for low-latency digital filter channel enable and disable.

Table 7. Recommended Typical Power-Up Sequence: Audio Playback with Low-Latency Digital Filter Channels

STEP	ACTION (STATE)	DETAILED DESCRIPTION
0	None (Hardware Shutdown State)	This is the lowest power state. The device and all registers are fully reset in this state, and no control or audio interface interactions are possible.
1A	Power Up Device Supplies (Hardware Shutdown State)	Power the AVDD1, AVDD2, AVDD3, DVDD, and DVDDIO supplies to above the respective UVLO thresholds. No supply sequencing is required. Optionally, if an analog microphone bias output is needed, also power MBVDD.
1B	Set the Hardware Enable (Hardware Shutdown State)	Drive the hardware enable input (HW_EN) high or always connect to DVDDIO.
2	Transition to the Software Shutdown State (State Transition)	Once all conditions are met (steps 1A and 1B), the device automatically transitions to the software shutdown state. The transition is complete after the hardware enable time (t_{HW_EN}) has elapsed (with no errors/retries). Do not program the device during this transition. When the transition successfully completes, an INIT_DONE interrupt is generated.
3	None (Software Shutdown State)	This is the lowest power state where register settings are retained and the I^2C interface is active. Can be used for a system idle/standby case or when system is active, but no audio use case is active. It is recommended that the system software verify and then clear any interrupts upon entering this state.
4A	Program the Device Registers (Software Shutdown State)	The system software should fully configure the device registers (except AUDIO_EN) for the playback with low-latency digital filters (DF) use case. Ensure that the desired microphone inputs channel(s), digital filter channel(s), playback compensation channel, and the playback channel are all configured and ready to be enabled. For a smooth startup, enable volume ramping and enable digital mute on all channels.
4B	Configure the Analog Microphone Bias if Needed (Software Shutdown State)	If the analog microphone bias is needed while the device is in the software shutdown state, it can be configured and enabled at any time. Otherwise, to save power it should not be enabled until just before the state transition.
4C	Enable the External Clocks (Software Shutdown State)	Start the PCM interface clocks before exiting the software shutdown state. To save power, this should not be done until just before the state transition.
5	Set Global Audio Enable Bit (Software Shutdown State)	Set the global audio enable bit (AUDIO_EN) high to allow the device to transition to the audio state (if all other conditions are met). If playback volume ramping is disabled, then the input PCM playback data should be silent prior to and during the state transition.
6	Transition to the Audio State (State Transition)	The state transition is complete after the audio turn-on time (t_{ON}) has elapsed. Note that the duration of the audio turn-on time (t_{ON}) can vary based on the configured record input charge time and playback volume ramp time (if not muted). The transition has successfully completed when the playback power-up done interrupt (PB_PWRUP_DONE_*) is generated.
7A	Begin Audio Playback (Audio State)	The device is in the audio state and is receiving PCM playback data from the host. For smooth startup, first unmute the playback channel before unmuting the digital filter and playback compensation channels. If audio playback data starts after the playback volume/unmute ramp (or if playback volume ramping is disabled), the host is responsible for playback audio data ramping.
7B	Unmute the Low-Latency Digital Filter and Playback Compensation Channels (Audio State)	In the audio state, microphone input data samples begin filling and settling the low-latency digital filters. For best results, allow time for a few samples to propagate before un-muting the low-latency digital filter and playback compensation channels. The optimal timing depends on the tuned filter response and sample rate settings. Once unmuted, the channels ramp up and are mixed into the playback channel.

Table 7. Recommended Typical Power-Up Sequence: Audio Playback with Low-Latency Digital Filter Channels (continued)

STEP	ACTION (STATE)	DETAILED DESCRIPTION
8	Audio Playback with Digital Filter Channels Active (Audio State)	To avoid errors and audible glitches, during any device programming in the audio state all register restrictions must be observed.

Table 8. Recommended Typical Power-Down Sequence: Audio Playback with Low-Latency Digital Filter Channels

STEP	ACTION	DETAILED DESCRIPTION
0	Audio Playback with Digital Filter Channels Active (Audio State)	The device is in the audio state with playback and digital filters active.
1	Clear Global Audio Enable Bit (Audio State)	For a smooth power-down, enable volume ramping and first mute the digital filter channels, the playback compensation channel, and the playback channel prior to power-down. Next, set the global audio enable bit (AUDIO_EN) low to transition to the software shutdown state. If playback volume ramping is disabled, the input PCM playback data should be silent and digital filter data should be muted prior to and during the transition.
2	Transition to the Software Shutdown State (State Transition)	The transition is complete after the audio turn-off time (t_{OFF}) has elapsed. Note that the duration of the audio turn-off time (t_{OFF}) varies based on the configured playback volume ramp time. The transition has successfully completed when the power-down interrupt (PWRDN_DONE_*) is generated.
3	Idle/Reprogram Device (Software Shutdown State)	The device can idle in the software shutdown state and clocks can be disabled to save power. The device can be freely reconfigured in this state. It is recommended that the system software verify and then clear any interrupts upon entering this state. To return from this idle state to the audio state, start from step 3 in Table 7 and follow the power-up sequence from there.
4	Transition to the Hardware Shutdown State (State Transition)	Before transitioning to the hardware shutdown state, first ensure that the external clocks are disabled. Then, either assert the hardware enable input (HW_EN) to a valid logic low level for longer than the hardware disable time (t_{HW_DIS}) or power down any supply with a UVLO to below the threshold.
5	None (Hardware Shutdown State)	This is the lowest power state. All supplies may be disabled if desired. The device (including all interfaces and registers) is fully reset in this state.

PCM Digital Audio Interface

The flexible PCM slave digital audio interface supports a set of common audio playback channel sample rates from 8kHz to 192kHz and record channel sample rates from 8kHz to 48kHz. The PCM interface supports timing for standard I²S, left justified, and TDM data formats. The PCM interface is disabled and powered down when both the PCM data input (DIN) and PCM data output (DOUT) are disabled.

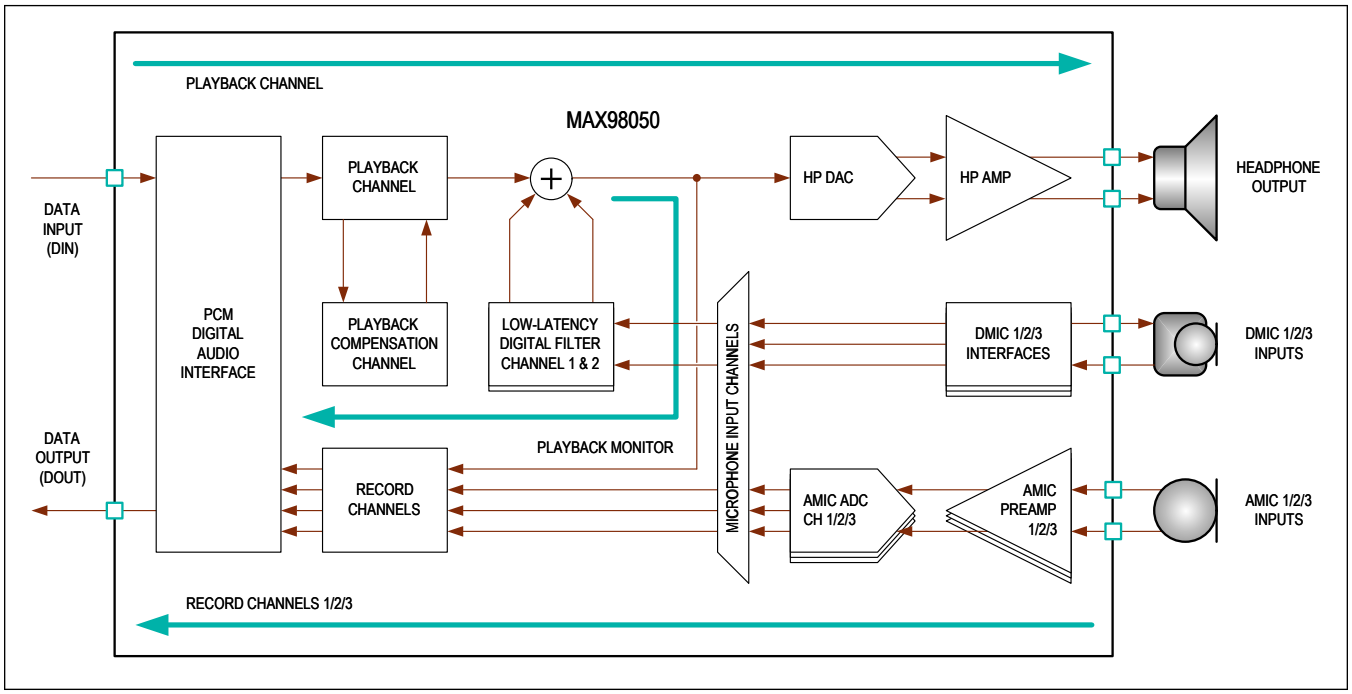


Figure 8. PCM Input and Output Audio Data Channels

PCM Clock Configuration

The PCM slave interface requires the host to supply both the bit clock (BCLK) and frame clock (LRCLK). To configure the PCM interface clock inputs, the host must program the PCM interface (and playback channel) sample rate (PCM_PB_SR) and the BCLK to LRCLK ratio (PCM_BSEL). The configured PCM interface (and playback) sample rate must match the frequency of the frame clock (LRCLK).

The PCM record channel sample rate (PCM_REC_SR) may be set to the same rate or a lower rate than the playback channel sample rate (PCM_PB_SR) according to the restrictions in Table 9. Only integer playback to record clock ratios are supported.

When the PCM record channel sample rate is set to a lower rate than the playback channel (DIN receive), the PCM output data (DOUT transmit) contains extra frames (based on the playback to record sample rate ratio). By default, the extra record channel output data frames contain repeated record data samples. However, by setting the PCM_TX_NO_RPT_SAMP bit high, each record data sample is sent only once, instead of repeated samples, followed by zero code data in the extra frames.

Table 9. Supported Playback to Record Sample Rate Ratios

N/A = NOT AVAILABLE N/S = NOT SUPPORTED		PCM RECORD CHANNEL SAMPLE RATE IN KILOHERTZ (REC_SR)								
		48	**44.1**	**32**	**24**	**22.05**	**16**	**12**	**11.025**	**8**
PCM PLAYBACK CHANNEL SAMPLE RATE IN KILOHERTZ (PCM_PB_SR)	**192**	4	N/S	6	8	N/S	12	16	N/S	24
	176.4	N/S	4	N/S	N/S	8	N/S	N/S	16	N/S
	96	2	N/S	3	4	N/S	6	8	N/S	12
	88.2	N/S	2	N/S	N/S	4	N/S	N/S	8	N/S
	48	1	N/S	N/S	2	N/S	3	4	N/S	6
	44.1	N/A	1	N/S	N/S	2	N/S	N/S	4	N/S
	32	N/A	N/A	1	N/S	N/S	2	N/S	N/S	4
	24	N/A	N/A	N/A	1	N/S	N/S	2	N/S	3
	22.05	N/A	N/A	N/A	N/A	1	N/S	N/S	2	N/S
	16	N/A	N/A	N/A	N/A	N/A	1	N/S	N/S	2
	12	N/A	N/A	N/A	N/A	N/A	N/A	1	N/S	N/S
	11.025	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1	N/S
	8	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1

The device supports a range of BCLK to LRCLK clock ratios (PCM_BSEL) ranging from 32 to 512. However, based on the selected PCM interface sample rate (LRCLK frequency) the configured clock ratio cannot result in a required BLCK frequency that exceeds 24.576MHz.

PCM Data Format Configuration

The device supports the I²S, left-justified, and TDM data formats, and the PCM operating mode is selected using the PCM_FORMAT bit field.

I²S and Left-Justified Mode

The I²S and left-justified PCM data formats support two channels that can be 16, 24, or 32 bits in length. The BCLK to LRCLK ratio (PCM_BSEL) must be configured to be twice the desired channel length. The audio data word size is then configurable to 16, 24, or 32 bits in length using the PCM_CHANSZ bit, and must be programmed to be less than or equal to the configured channel length. If the configured channel length exceeds the configured data word size, the data input LSBs are truncated and the data output LSBs are padded with either zero or Hi-Z data (based on the PCM_TX_EXTRA_HIZ bit setting). If only one data output channel is needed and the bus is shared with another device, the unused channel should not have data assigned to it and Hi-Z padding is recommended to avoid potential data collisions.

Table 10. Supported I²S and Left-Justified Mode Configurations

CHANNELS	CHANNEL LENGTH	BCLK TO LRCLK RATIO (PCM_BSEL)	SUPPORTED DATA WORD SIZES (PCM_CHANSZ)
2	16	32	16
	24	48	16, 24
	32	64	16, 24, 32

With the default settings, a falling LRCLK edge indicates the start of a new frame and the left channel data (Channel 0), while a rising LRCLK edge indicates the right channel data (Channel 1). In I²S mode, the MSB of the audio word is latched on the second active BCLK edge after an LRCLK transition. In left-justified mode, the MSB of the audio word is latched on the first active BCLK edge after an LRCLK transition.

The BCLK active edge (rising or falling) used for data capture (DIN receive) and data output (DOUT transmit) is selected using the PCM_BCLKEDGE bit. The PCM_CHANSEL bit configures which LRCLK edge indicates the start of a new frame (and channel 0), and LRCLK transitions always align with the inactive BCLK edge. The data output is valid on the same active BCLK edge as the data input. The data output also transitions on the same edge as the data input.

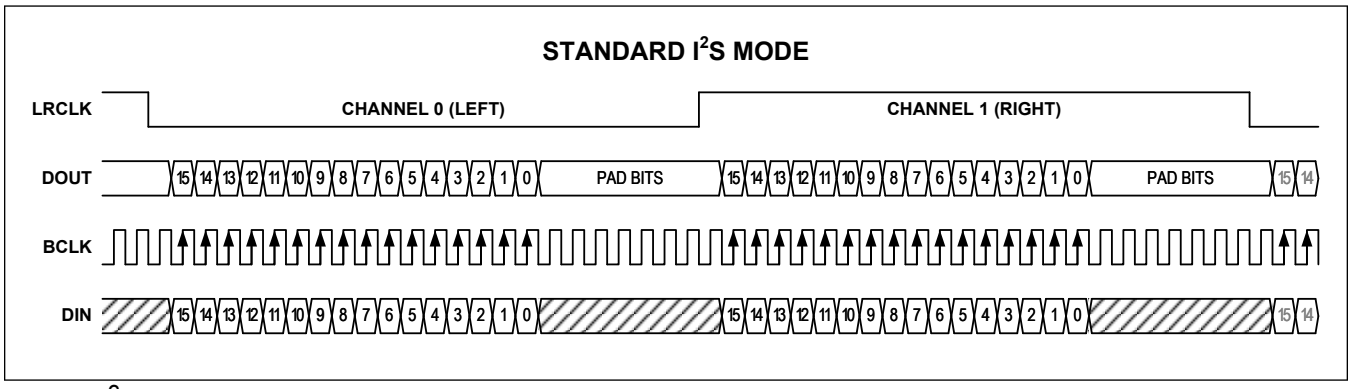


Figure 9. I²S Timing Mode Example

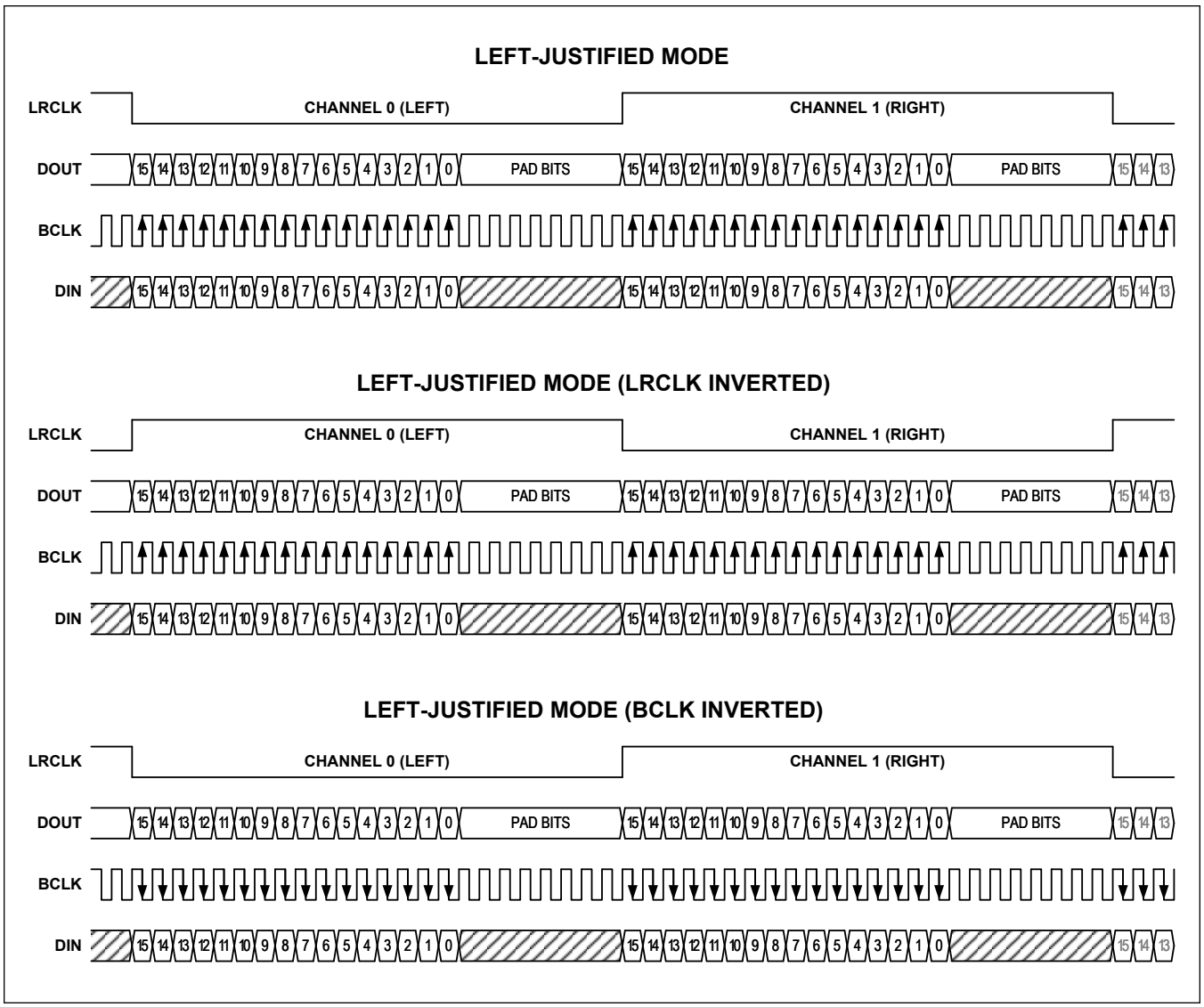


Figure 10. Left-Justified Mode Timing Examples

TDM Modes

The provided TDM modes support timing for up to eight digital audio input channels (DIN receive) each containing 16, 24, or 32 bits of data. The record channel data output (DOUT transmit) is structured into 8-bit slots, and the timing can support up to a maximum of 64 data output slots. The data output word size is always 24 bits (for record channels 1 through 4) and output data can be assigned to any set of sequential data output slots. 16-bit output data and transmit timing can also be supported by assigning data to partially overlapping data output slots. The number of TDM input channels and output slots is determined by both the selected BCLK to LRCLK ratio (PCM_BSEL) and the selected data word and channel length (PCM_CHANSZ).

For a given valid configuration, the number of available data input (DIN) channels per frame is calculated as follows:

Number of Available Data Input Channels = BCLK to LRCLK Ratio / Channel Length

For a given valid configuration, the number of available 8-bit data output (DOUT) slots per frame is calculated as follows:

Number of Available Data Output Slots = BCLK to LRCLK Ratio / 8

Table 11 shows the supported TDM mode configurations. In some configurations, the maximum PCM interface and playback sample rate is limited to less than 192kHz to avoid violating the BCLK frequency limit of 24.576MHz.

Table 11. Supported TDM Mode Configurations

INPUT DATA CHANNELS	OUTPUT DATA SLOTS	INPUT DATA WORD SIZE (PCM_DATA_WIDTH)	BCLK TO LRCLK RATIO (PCM_BSEL)	MAXIMUM PLAYBACK SAMPLE RATE (PCM_PB_SR)
2	4	16	32	192kHz
	6	24	48	
	8	32	64	
4	8	16	64	
	12	24	96	
	16	32	128	
8	16	16	128	
	24	24	192	96kHz
	32	32	256	
16	32	16	256	
	48	24	384	48kHz
	64	32	512	

With the default PCM interface settings, in TDM mode a rising frame clock (LRCLK) edge acts as the frame sync pulse and indicates the start of a new frame. The frame sync pulse width must be at least one bit wide, however the falling edge can occur at any time as long as it does not violate the setup time of the next frame sync pulse rising edge. The PCM_CHANSEL bit can be used to invert the active LRCLK edge (sync pulse) used to start a TDM frame.

In TDM mode, the MSB of the first audio word can be latched on the first (TDM Mode 0), second (TDM Mode 1), or third (TDM Mode 2) active BCLK edge after the sync pulse, and this is programmed with the PCM_FORMAT bit field. Additionally, the PCM_BCLKEDGE bit selects the active BCLK edge that is used for data capture and data output. The data output is valid on the same active BCLK edge as the data input, and the data output also transitions on the same edge as data input.

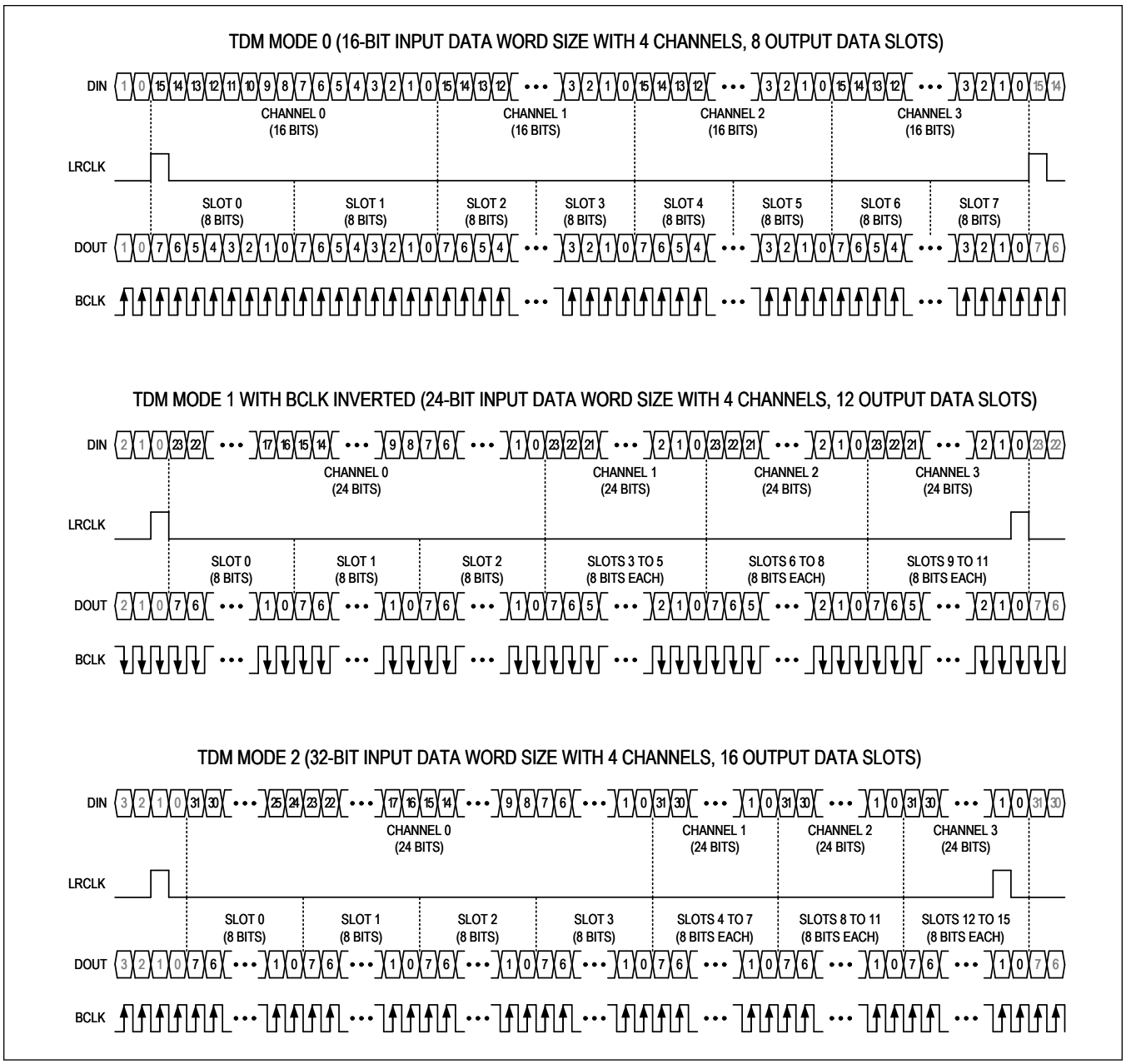


Figure 11. TDM Mode Timing Examples

PCM Data Channel Configuration

The PCM interface data input (DIN) receives the source data for the playback channel (and playback compensation channel), while the data output (DOUT) can transmit the data from both the three microphone record channels and the playback DSP output monitor channel. In addition, the PCM interface also provides a data loopback mode (PCM data input looped back to the PCM data output) and an internal data loop-through mode (any microphone record channel output data looped through to become the input of the playback channel).

PCM Data Input

The PCM interface data input (DIN) is enabled with the PCM_RX_EN bit, and the playback channel can accept data from any valid PCM input data channel. The PCM data input (DIN) channel to the playback channel is selected with the PCM_PB_SOURCE bit field. In I²S and left-justified modes, only 2 input data channels are available while in TDM mode up to 16 channels of input data may be available. If the PCM data input is disabled (PCM_RX_EN = 0), a zero code value is driven into the playback channel.

PCM Data Output

The PCM interface data output (DOUT) is enabled by the PCM_TX_EN bit field, and can transmit any output data source onto any valid output channel or slot. The PCM data output accepts source data from both the microphone record channels and the playback DSP monitor channel.

In I²S and left-justified mode, only 2 data output channels are available in each output transmit frame (channel 0 and 1). Only a single output data source can be assigned to each data output channel (unless channel interleaving is enabled). The PCM data output word length (PCM_CHANSZ) and channel length (PCM_BSEL) are configured independently.

In TDM mode, each output transmit frame can contain up to 64 sequential 8-bit data output slots, each of which is numbered from 0 up to a maximum of 63. The record channel data outputs are assigned individually to data output slots (8 bits). Unlike the PCM playback data input (where in TDM mode the data word and channel length are always identical at 16, 24, or 32 bits), in TDM mode the PCM record data output channels are always 24 bits in length (3 slots). The data output sources and control bit fields are shown in Table 12.

Table 12. PCM Record Output Data Sources

OUTPUT DATA SOURCE	OUTPUT SOURCE ENABLE	SLOT ASSIGNMENT
Microphone Record Channel 1	REC1_PCM_EN	PCM_REC1_SLOT
Microphone Record Channel 2	REC2_PCM_EN	PCM_REC2_SLOT
Microphone Record Channel 3	REC3_PCM_EN	PCM_REC3_SLOT
Playback DSP Monitor Channel	REC4_PCM_EN	PCM_REC4_SLOT

An individual enable and slot assignment bit field is provided for each output data source. In I²S and left-justified modes, use output slot 0 to assign data to channel 0 and output slot 1 to assign data to channel 1. In TDM mode, the slot assignment selects the slot where the 24-bit record output data transmit begins (i.e., if the 24-bit output data is assigned to slot 5, slots 5, 6 and 7 are occupied).

In TDM mode, each record data output source can be assigned to any valid data output slot. It is invalid to assign record output channels to the same starting slot. However, it is valid to truncate the 24-bit data by partially overlapping channel assignments (for example, to create 16-bit record data outputs). It is, however, invalid to assign a data source to any starting slot that does not exist in the frame structure of the current PCM interface configuration (for example, if the configuration has 16 slots, assigning data to slot 20 is invalid). Table 13 shows a few TDM mode configuration examples.

Any data output (DOUT) slots that exist in the current frame structure but have no output data type assigned to them (unused slots) are either Hi-Z or driven with a 0 code (set by slot with the PCM_TX_SLOT_HIZ bit field). Likewise, if a data output source is disabled, then the assigned data output slots are considered unused and are also either Hi-Z or driven with a 0 code (as set by the PCM_TX_SLOT_HIZ bit field).

Table 13. Example Record Output Data Slot Assignments

USE CASE DESCRIPTION	RECORD 1	RECORD 2	RECORD 3	RECORD 4
32-Bit Input Data with 2 Channels 16-Bit Output Data (No Padding) with 8 Slots	Slot 0	Slot 2	Slot 4	Slot 6
24-Bit Input Data with 4 Channels 24-Bit Output Data (No Padding) with 12 Slots	Slot 0	Slot 3	Slot 6	Slot 9
32-Bit Input Data with 4 Channels 24-Bit Output Data (8-Bit Pad) with 16 Slots	Slot 0	Slot 4	Slot 8	Slot 12

PCM Data Output Channel Interleaving

In I²S and left-justified use cases, the PCM interface limits the number of available data output channels to 2 making it impossible to fit more than 2 record channel data output channels (from either a single or multiple devices) onto a single shared data output (DOUT) line. For these cases, the PCM data output (DOUT) can be configured to allow output data sources from a single device to share a single data output channel. To enable channel-interleaved mode, perform the following:

1. Set the PCM_TX_INTERLEAVE bit high.
2. Set the PCM_TX_INTERLEAVE_SEL bit field to select which two microphone record channels (microphone record channel 1, 2, or 3) can be interleaved. The playback monitor data on record channel 4 cannot be interleaved.
3. Assign the two selected record channel data output sources to the same valid data output channel (using the PCM_RECn_SLOT bit fields).

In this configuration, the record data sources are frame interleaved on the assigned data output channel. The data words are both equal in length, but if the channel length is longer than data word size the trailing padding bits are set to either Hi-Z or 0 code depending on the state of the PCM_TX_EXTRA_HIZ bit field.

To identify the record channel data source in channel-interleaved mode, the LSB of the data word is dropped (truncated). The data word is then right shifted by a single bit, and the now vacant MSB is replaced with either a 0 to indicate the first record channel number or a 1 to indicate the second record channel number (in order as set by the PCM_TX_INTERLEAVE_SEL bit field). For phase alignment, the first record channel data for a single sampling instant is always transmitted in the assigned channel on the first frame, followed by the second record channel data on the second frame. The MSB value and the transmission order allow the host to identify and phase-align the record channel output data across frames.

Since the record channel data is frame interleaved, the sample rate for the PCM interface and playback channel (PCM_PB_SR) must be greater than that of the record channel (PCM_REC_SR) by an integer ratio of 2 or greater. The example in Figure 12 shows a basic case where the sample rate of the PCM interface is twice that of the record channel.

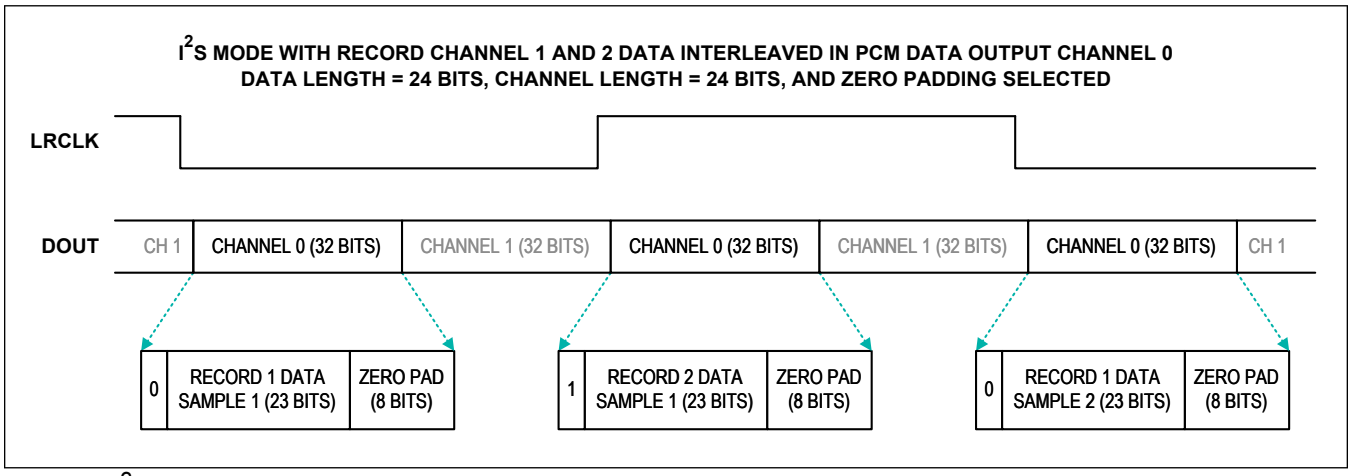


Figure 12. I²S Mode PCM Data Output Channel Interleaving Example

PCM Data Output Drive Strength

The PCM data output logic level drive strength is configured with the PCM_DOUT_DRV bit field, and four different CMOS drive strength selections are available.

PCM Data Loopback and Loop-Through Modes

The PCM interface also supports data loopback and loop-through operating modes. The PCM data input (DIN) to data output (DOUT) loopback mode is enabled by setting the PCM_LB_DOUT_EN bit high. When enabled, the PCM input data source channel (as set by PCM_PB_SOURCE bit) replaces the the PCM record channel output data for any enabled microphone record channels (based on the RECn_PCM_EN settings). PCM data loopback mode requires that both the data input and data output interfaces be enabled (PCM_TX_EN and PCM_RX_EN), and configured to operate at the same sample rate (PCM_PB_SR and PCM_REC_SR set equal).

The PCM microphone record data to playback channel internal loop-through mode is configured with the PCM_PB_LT_EN bit field. When enabled, the selected microphone record channel data (microphone record channel 1, 2, or 3) replaces the PCM data input (DIN) as the input source for the playback channel. PCM internal data loop-through mode requires both the selected microphone record channel and playback channel be enabled (RECn_PCM_EN and PB_EN), and configured to operate at the same sample rate (PCM_PB_SR and PCM_REC_SR set equal).

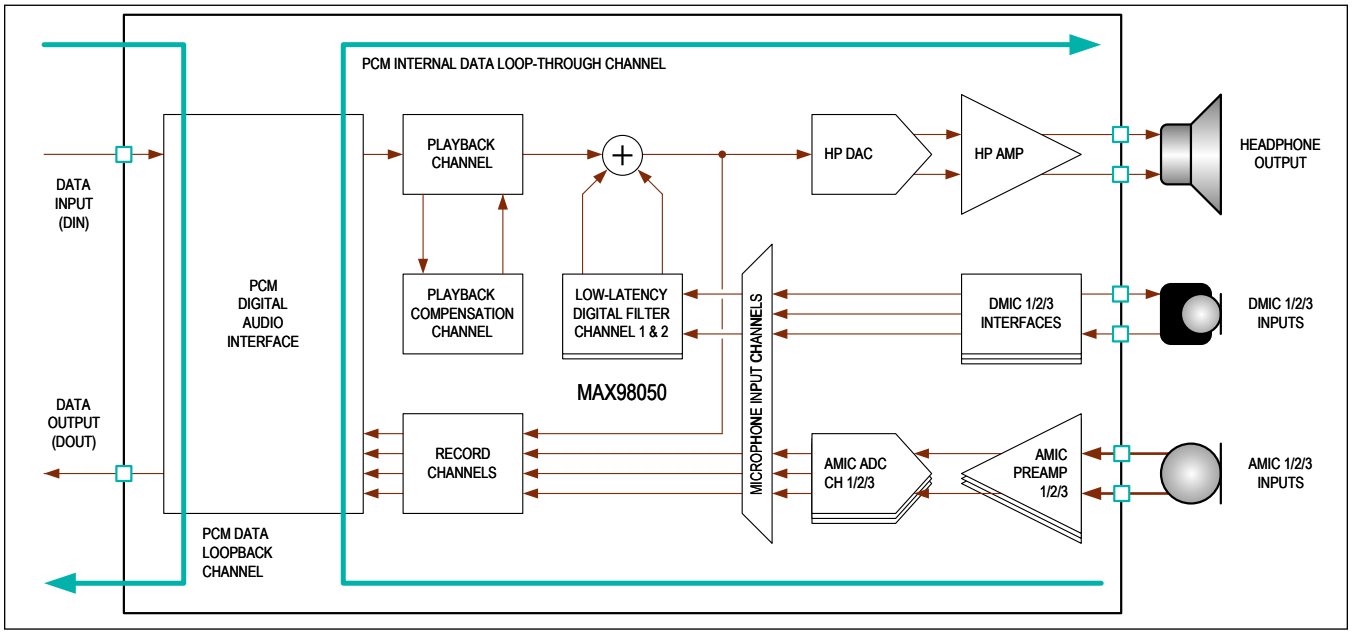


Figure 13. PCM Data Loopback and Loop-Through Channels

I²C Slave Control Interface

The device provides an I²C slave control interface that is used to program the control registers. The device control registers in user space that are programmable with the I²C interface reside in the address space from 0x2000 to 0x27FF.

I²C Interface Address

When the I²C slave interface is active, the device slave address is defined as the seven most significant bits (MSBs) followed by the read/write bit. The address is programmable with the ADDR pin and is configured as shown in Table 14. The ADDR pin state is checked and locked in at the beginning of each I²C transaction on the connected bus. The ADDR input cannot be left unconnected.

In addition to the address set by the ADDR input, a group write address of 0x6A is available for cases where synchronized write transactions are needed across multiple devices. The group write address is enabled by default, but can be disabled by setting the I2C_GROUP_ADDR_EN = 0. When enabled, the device (or a group of devices) accept write transactions through the group address regardless of the ADDR connection. Group read transactions are not supported (and should not be attempted to avoid data collisions). The I2C_GW_DONE interrupt triggers when a transaction is successfully completed through the group write address. If a device in a given group does not generate the I2C_GW_DONE interrupt, the device state and register configuration should be checked. When the group write address is disabled, the device does not respond to any transactions through the group write address. Regardless of the state of the I2C_GROUP_ADDR_EN bit, transactions through the primary device address set by the ADDR input always function normally.

Table 14. Available I²C Slave Addresses

CONDITIONS	I²C SLAVE WRITE ADDRESS	I²C SLAVE READ ADDRESS
ADDR Connected to DVDDIO	0x62	0x63
ADDR Connected to DGND	0x64	0x65
ADDR Connected to SDA	0x66	0x67
ADDR Connected to SCL	0x68	0x69
I2C_GROUP_ADDR_EN = 1	0x6A	NA

I²C Interface Bit Transfer Protocol

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (START and STOP conditions).

I²C Interface START and STOP Conditions

SDA and SCL idle high when the bus is not in use. An I²C master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high. A START condition from the master signals the beginning of a transmission to the slave. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

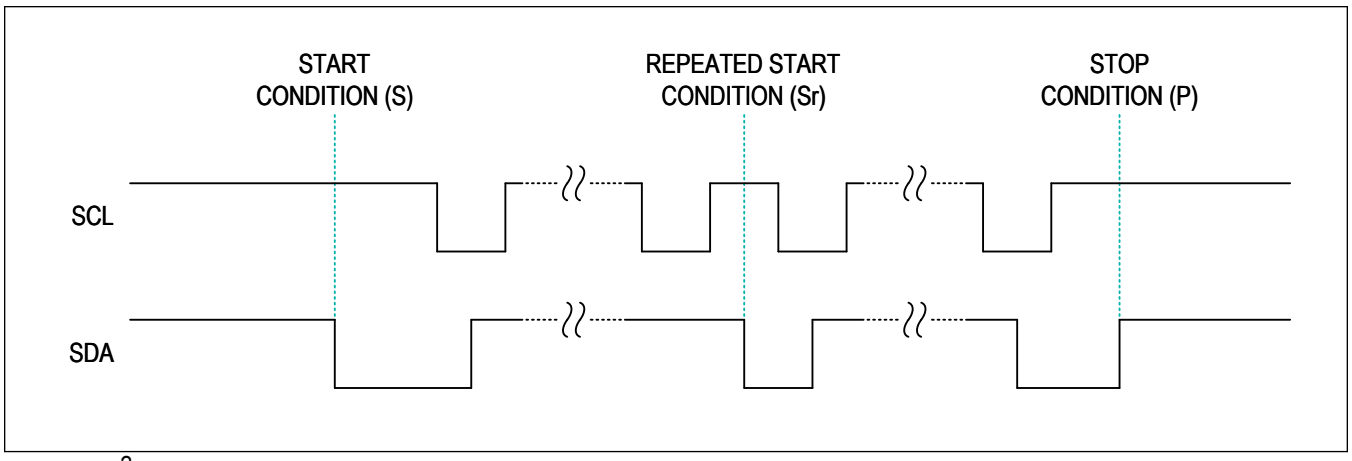


Figure 14. I²C Slave Interface START and STOP Condition Example

I²C Interface Early STOP Condition

The device recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

I²C Interface Acknowledge Bit

The acknowledge bit (ACK) is a clocked ninth bit that the slave uses to handshake receipt each byte of data when in write mode (Figure 15). The slave pulls down SDA during the entire master-generated ninth clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may retry communication.

The master pulls down SDA during the ninth clock cycle to acknowledge receipt of data when the slave is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge (NACK) is sent when the master reads the final byte of data from the slave followed by a STOP condition.

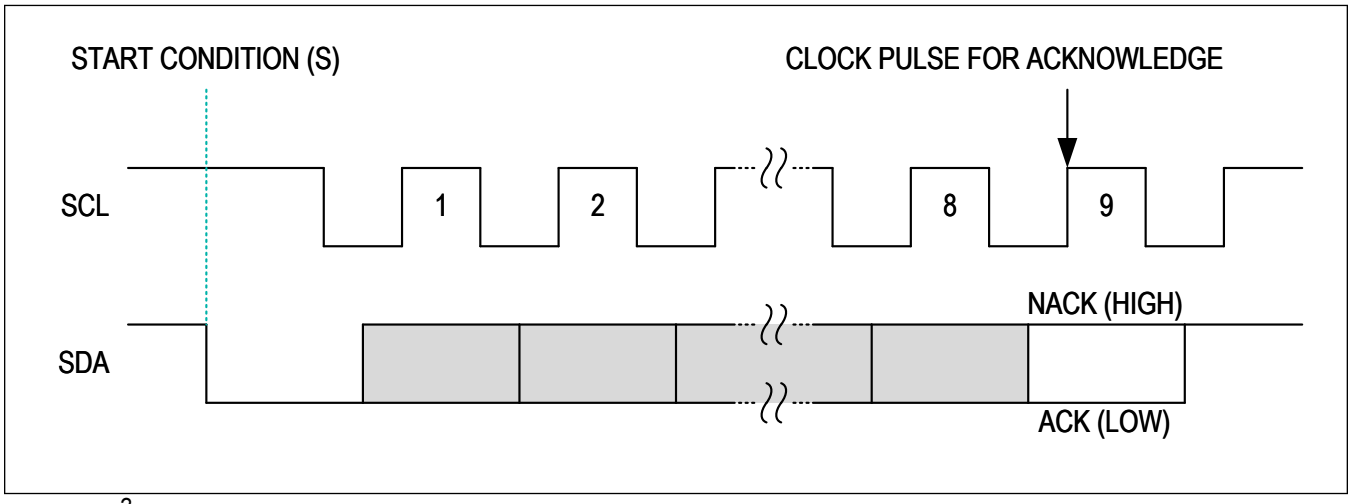


Figure 15. I²C Slave Interface Acknowledge Bit Example

I²C Interface Write Data Format

A write to the device through the I²C slave interface includes transmission of a START condition, the slave address with the READ-$\overline{\text{WRITE}}$ bit set to 0, two bytes of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition.

Transmission of the slave address with the READ-$\overline{\text{WRITE}}$ bit set to 0 indicates that the I²C master intends to write data to the device. The device acknowledges receipt of the address byte during the ninth SCL pulse.

The second and third bytes transmitted from the master configure the device's internal register address pointer. The pointer tells the device where to write the next byte of data. An acknowledge pulse is sent by the device upon receipt of each byte of the register address data.

The fourth byte sent to the device contains the data to be written to the chosen register address. An acknowledge pulse from the device signals receipt of the data byte. The address pointer auto increments to the next register address after each received data byte. This auto-increment feature allows the master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition.

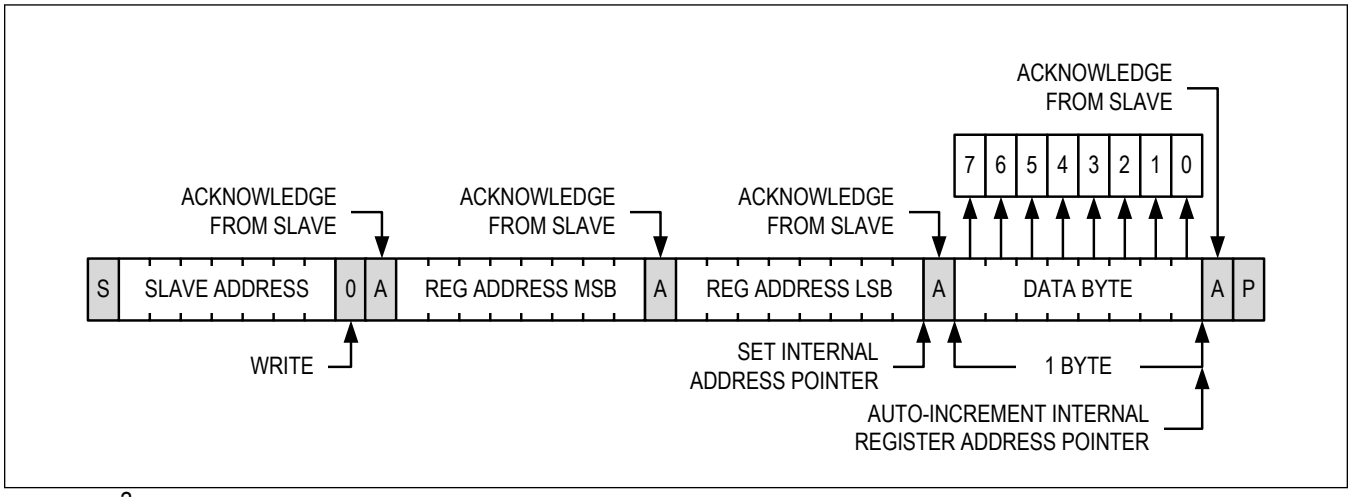


Figure 16. I²C Master Writing One Byte of Data to the Slave Device

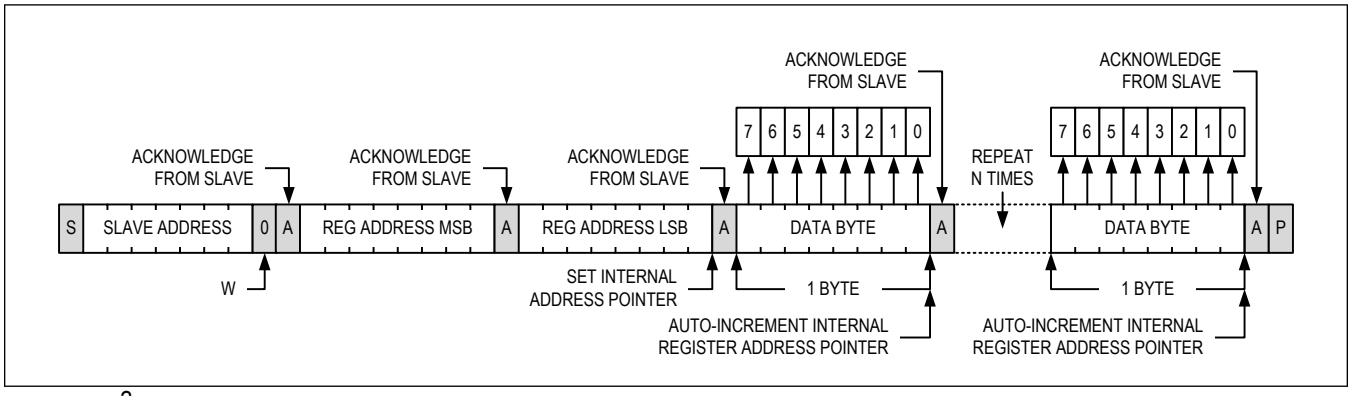


Figure 17. I²C Master Writing n-Bytes of Data to the Slave Device

I²C Interface Read Data Format

There are two ways to read data back from the slave device. First, a START condition followed by a read command resets the address pointer to the default starting register at address 0x2000. Therefore, simply sending the devices slave address with the READ-$\overline{\text{WRITE}}$ bit set to 1 initiates a read operation with the internal register address pointer starting from 0x2000. In this case, the device acknowledges receipt of its slave address by pulling SDA low during the ninth SCL clock pulse.

Instead, the address pointer can be preset to a specific target register address before a read command is issued. The master can preset the slave register address pointer by first sending the device's slave address with the READ-$\overline{\text{WRITE}}$ bit set to 0 (write command) followed by two commands containing the target register address for the address pointer. A REPEATED START condition is then sent followed by the read command (slave address with the READ-$\overline{\text{WRITE}}$ bit set to 1). This begins a read command with the internal register address pointer set to the target register address.

In either scenario, the first byte transmitted from the device contains the contents of the register that the address pointer is set to. Transmitted data is valid on the rising edge of SCL. The master acknowledges (ACK) receipt of each read byte during the acknowledge clock pulse. The address pointer then auto-increments after each acknowledged read data byte. This auto-increment feature allows multiple registers to be read sequentially within one continuous frame.

The master must issue an acknowledge (ACK) for all correctly received bytes except the last byte. To terminate the read operation, the final byte must be followed by a not acknowledge (NACK) from the master and then a STOP condition. A not-acknowledge (NACK) followed by a STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the address pointer is reset and the first data byte to be read is from register 0x2000.

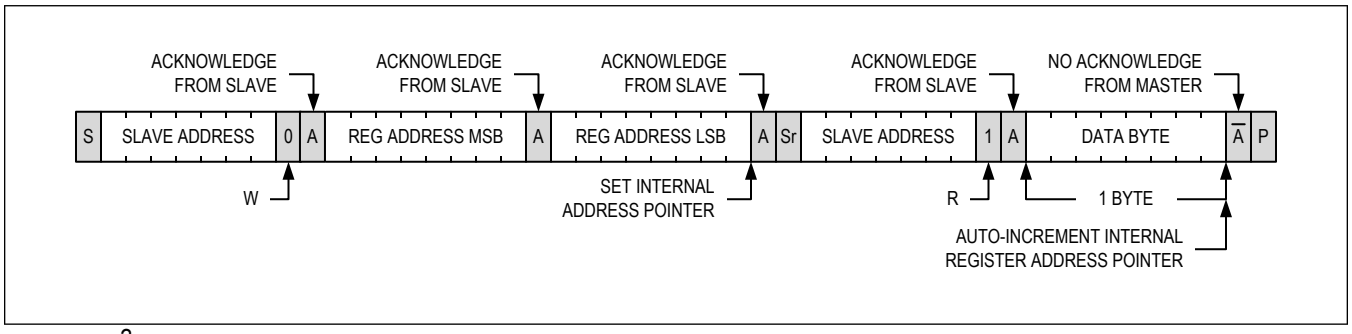


Figure 18. I²C Master Reading One Byte of Data from the Slave Device

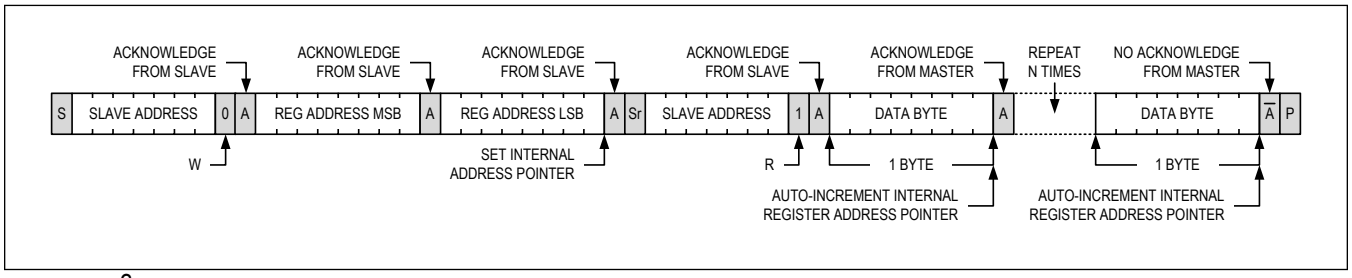


Figure 19. I²C Master Reading n-Bytes of Data from the Slave Device

Interrupts

The device supports individually enabled status interrupts for sending feedback to the host about events that have occurred on-chip. When enabled, device interrupts are sent on the IRQ output.

Interrupt Bit Field Composition

Each device interrupt source has five individual bit field components. The function of each component is detailed below and the corresponding bit fields for each source can be identified by the appended suffix (shown in parentheses).

Raw Status (RAW)

Each interrupt source has a read-only bit to indicate the real-time raw status of the interrupt source.

State (STATE)

Each interrupt source has a read-only state bit that is set whenever a rising edge occurs on the associated raw status bit. The state bit is set regardless of the setting of the source enable bit.

Flag (FLAG)

Each interrupt source has a read-only flag bit. If the source enable bit is set, then the flag bit is set and an interrupt can be generated whenever the source state bit is set.

Enable (EN)

Each interrupt source has a dynamic read/write enable bit. When the enable bit is set, the associated flag bit is set and an interrupt can be generated whenever the source state bit is set.

Clear (CLR)

Each interrupt source has a dynamic write-only clear bit that resets the associated state and flag bits low when a 1 is written. Writing a 0 to the clear bit has no effect. The IRQ bus is de-asserted if all flag bits are low.

Interrupt IRQ Output Configuration

The IRQ output is used to signal the host when an interrupt event occurs, and is enabled when the IRQ_EN bit is 1. Once enabled, the IRQ output asserts anytime an interrupt event occurs (any FLAG bit is set high), and de-asserts when all events are cleared (all FLAG bits set low). The IRQ_POL bit selects the assert polarity of the IRQ bus. Interrupt events assert the IRQ bus low if IRQ_POL is 0 and high if IRQ_POL is 1.

The device allows the user to configure the drive mode, drive strength, and polarity of the IRQ output. The IRQ_MODE bit controls the output drive mode. If IRQ_MODE is 0, the IRQ output is configured as an open-drain output, and requires an external pullup resistor (typically 1.5kΩ). Alternatively, setting the IRQ_INT_PU bit to 1 enables an internal 100kΩ weak pullup resistor.

If IRQ_MODE is 1, then the IRQ output is configured as a push-pull CMOS output. In this mode, the IRQ_DRV bit field sets the drive strength of the IRQ output. Four different drive strength options are available.

Interrupt Event Sources

The events listed in Table 15 and Table 16 can cause IRQ bus interrupts when enabled (if the interrupt source enable bit is high).

Table 15. Device Interrupt Event Sources 1

REGISTER ADDRESS	BIT NUMBER	INTERRUPT SOURCE	BIT NAME	DESCRIPTION
0x2001 0x2003 0x2005 0x2007 0x2009	7	Device Initialization Done Event	INIT_DONE_*	Indicates when the device has completed the transition from a reset event or the hardware shutdown state into the software shutdown state. Once this occurs, the device is ready to accept programming through the I²C control interface.
	6	OTP Load Failed Event	OTP_FAIL_*	Indicates that the OTP load routine that runs when initializing the device has failed to complete successfully.
	5	Power Down to Software Shutdown State Done Event	PWRDN_DONE_*	Indicates the device has successfully completed power down into the software shutdown state from the audio state.
	4	Playback Channel Enabled in the Audio State	PB_PWRUP_DONE_*	Indicates the device has both transitioned out of the software shutdown state, and that the playback channel is enabled and ready to receive audio data.
	3	Record Channel Enabled in the Audio State	REC_PWRUP_DONE_*	Indicates the device has both transitioned out of the software shutdown state, and that at least one record channel is enabled and ready to transmit audio data. This interrupt is not generated when at least one record channel is already active, and additional record channels are dynamically enabled.
	2	Clock Monitor Error Event	CLOCK_ERR_*	Indicates that the clock monitor has detected a clock error event. Clock error events can only be generated when the audio enable bit (AUDIO_EN) is first set high.
	1	Clock Monitor Auto Recovery Event	CLOCK_REC_*	Indicates that the clock monitor has detected a clock recovery event. Clock recovery events can only generated in auto mode after a clock error event has first occurred.
	0	Data Monitor Error Event	DATA_ERR_*	Indicates that the playback data monitor has detected a data error event. Data error events can only be generated when the audio enable bit (AUDIO_EN) is first set high.

Table 16. Device Interrupt Event Sources 2

REGISTER ADDRESS	BIT NUMBER	INTERRUPT SOURCE	BIT NAME	DESCRIPTION
0x2002 0x2004 0x2006 0x2008 0x200A	7	FLL Unlock Error Event	FLL_ERR_*	Indicates that the FLL either failed to lock while transitioning from software shutdown to the audio state, or that FLL lock was lost while the device was operating in the audio state.
	6	I2C Group Write Done Event	I2C_GW_DONE_*	Indicates that the I2C slave interface received and completed a write transaction through the I2C Group Address of 0x6A.
	5	-	-	-
	4	Playback Amplifier Overcurrent Protection Event	AMP_OCP_*	Indicates that the playback amplifier output overcurrent protection limit was exceeded.
	3	Playback Compensation Channel Ramp Done Event	PBC_RMP_DONE_*	Indicates that the playback compensation channel has finished ramp-up or down during an enable, mute, unmute, or volume change.
	2	Digital Filter Channel 2 Ramp Done Event	DF2_RMP_DONE_*	Indicates that digital filter channel 2 has finished ramp-up or down during an enable, disable, mute, unmute, or volume change.
	1	Digital Filter Channel 1 Ramp Done Event	DF1_RMP_DONE_*	Indicates that digital filter channel 1 has finished ramp-up or down during an enable, disable, mute, unmute, or volume change.
	0	Playback Channel Ramp Done Event	PB_RMP_DONE_*	Indicates that the playback channel has finished ramp-up or down during an enable, disable, mute, unmute, or volume change.

Microphone Input Channels

The device features three microphone input channels. The three channels can operate concurrently, and each is capable of independently selecting either an analog microphone (AMIC) or digital microphone (DMIC) as the input source with the respective RECn_SEL bit field. This allows for any combination of three analog and/or digital microphones to be active concurrently. The digital filters in each channel are automatically configured based on both the selected input source (AMIC or DMIC inputs) and the internal digital filter sample rate setting (DSP_SR).

The device provides three audio input pairs each with a pre-amplifier and an ADC capable of supporting either a single-ended or differential analog microphone (or a line level) input. The device also provides three separate digital microphone interfaces each capable of supporting either a mono or stereo digital microphone connection. More than three microphones may be connected to the device (for multiple use cases), however only three can be accepted as concurrent inputs for any given single use case.

Each microphone input channel can route output data concurrently to both a designated record channel and a low-latency digital filter channel (microphone input channel 3 can route data to both the DF1 and DF2 channels). Table 17 shows all of the input source and output data options for each of the three microphone input channels.

Table 17. Microphone Input Channel Connections

CHANNEL	INPUT SOURCE SELECTION	OUTPUT DATA ROUTING
Microphone Input 1	AMIC ADC 1 or Any DMIC Interface	Record Channel 1 and/or Digital Filter Channel 1
Microphone Input 2	AMIC ADC 2 or Any DMIC Interface	Record Channel 2 and/or Digital Filter Channel 2
Microphone Input 3	AMIC ADC 3 or Any DMIC Interface	Record Channel 3 and/or Digital Filter Channel 1 and/or 2

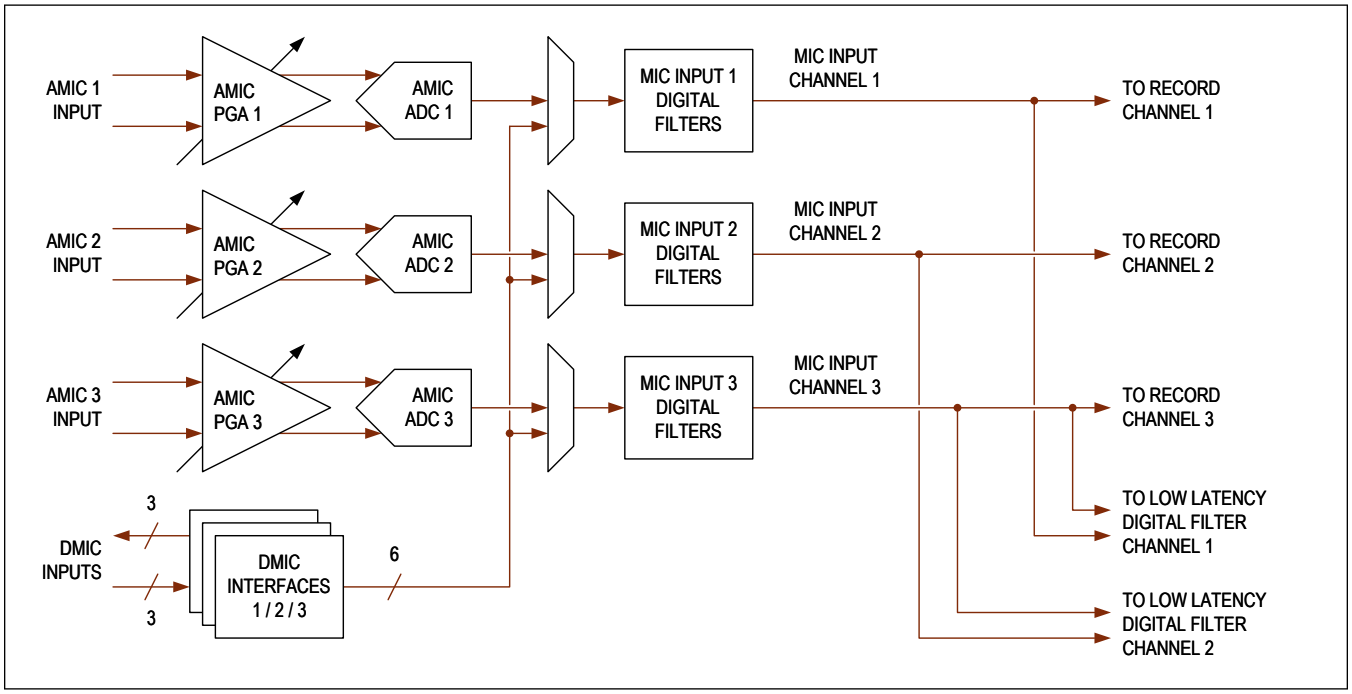


Figure 20. Microphone Input Channel Detailed Block Diagram

Analog Microphone Inputs

The device provides three analog inputs each capable of supporting one differential or single-ended analog microphone (AMIC) or line level connection. Each input includes a dedicated AMIC pre-amplifier and ADC stage, and is individually enabled and disabled with the respective AMICn_EN bit. The device also provides a programmable, low-noise AMIC bias generator with three separate output connections.

The device includes settings that adjust both the power consumption and performance of the analog microphone inputs. Prior to enabling a given analog microphone input, the AMIC pre-amplifier and ADC can be configured with the AMICn_LP_MODE bit to operate in either high performance mode or low power mode. All three AMIC input channels are clocked at the same rate with the same oversampling ratio (OSR). To reduce power consumption, the ADC clock rate and OSR can be reduced by setting the AMIC_ADC_RATE bit to 1 prior to enabling any of the AMIC inputs.

Differential analog microphones must be AC-coupled to both the positive and negative analog microphone inputs directly. For single-ended analog microphones, AC-couple the microphone output to the positive input directly, and AC-couple the negative input to ground (either directly near the device or if possible to a point close to the ground connection of the analog microphone). Each analog microphone pre-amplifier provides a separate programmable analog gain level and input impedance setting. The pre-amplifier programmable gain range is from -6dB to +21dB with a 3dB step size, and is selected by channel with the respective AMICn_PGA_GAIN bit field setting. Each pre-amplifier can be individually configured with the AMICn_PGA_RIN bit to present (when active) either the normal (35kΩ) or reduced (10kΩ) input impedance. Reduced input impedance mode provides a significant reduction in noise, but may not be compatible with all analog microphones and input coupling capacitors. The gain and input impedance settings should be configured based on the connected microphone prior to enabling a given AMIC input, and should not be changed while that input is enabled.

By default, the analog microphone input channels have dynamic range extension (DRE) and ADC output data dither enabled. When DRE is enabled, the gain structure of the input channel adjusts automatically based on the detected input signal level to maximize ADC dynamic range, while preserving the input headroom determined by the selected pre-amplifier gain setting. DRE can be independently disabled for a given AMIC input channel by setting the respective AMICn_DRE_EN bit to 0. In addition, dither can also be disabled for any input channel by setting the respective AMICn_DITH_EN bit to 0.

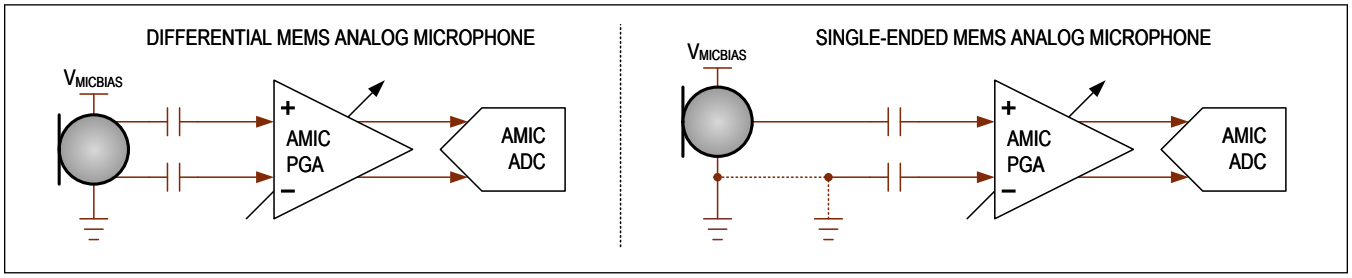


Figure 21. Differential and Single-Ended Analog Microphone Connections

Analog Microphone Control Sequencing

Analog microphone input channels can only be active when the device is in the audio state. The enable bits (AMICn_EN) are all located in the same register, and can be programmed in either the software shutdown state or dynamically in the audio state. When dynamically enabling record or digital filter channels with an analog microphone input, the analog microphone input enable bit should be set first before setting the enable for either the destination record channel (RECn_PCM_EN) and/or the digital filter channel (DF1_EN or DF2_EN). Likewise, when dynamically disabling record and/or digital filter channels with analog microphone inputs, the record and/or digital filter channels should be disabled first before disabling the analog microphone input.

If one or more AMICn_EN bits is set high while the device is in the software shutdown state, the configured analog microphone input channels are not enabled until the device transitions to the audio state. During this transition, the input common mode bias level of the analog microphone input amplifiers is automatically fast charged. However, the minimum required fast charge duration varies depending upon the size of the attached input coupling capacitor, and this can be

configured for four common values with the AMIC_CT_SEL bit field. To prevent the automatic fast charging of a given input channel, set the respective AMICn_FAST_CHRG_BYPASS bit high prior to exiting the software shutdown state.

When an analog microphone input channel is dynamically enabled while the device is already in the audio state, the input common mode bias is not automatically fast charged. If fast charging is needed, to manually force it first set the respective fast charge force bit (AMICn_FAST_CHRG_FORCE) high prior to dynamically enabling that channel. Next, set the respective input channel enable bit (AMICn_EN) high. Finally, after an appropriate fast charge duration has elapsed (based on the attached input coupling capacitor), set the fast charge force bit low to transition to normal operation for that input channel.

If individual analog microphone inputs (pre-amplifier and ADC) need to be dynamically disabled to save power (independent of the remaining active inputs, and without disrupting the digital timing and phase alignment of the destination record or digital filter channels), leave the appropriate AMICn_EN bits set high and instead set the AMICn_PD bit high. This has the same effect as setting the AMICn_EN bit low except that the AMIC input source still provides zero code data to the microphone input channel and any active destination channels (record or digital filter).

To retain the common mode bias level (for currently unused analog microphone inputs when exiting software shutdown or after a given input is dynamically disabled), set the respective AMICn_PGA_HIZ_EN bit high prior to disabling the input channel or transitioning to/from the software shutdown state. This results in a slight increase in quiescent power, but it allows disabled analog microphone input channels (dynamically disabled or in software shutdown) to present a high impedance value over the entire full-scale input swing range. This allows an analog microphone input to share a single analog microphone with another device in the system (by presenting high impedance when the other device is using the microphone).

Analog Microphone Bias Generator

The device provides a regulated, low noise analog microphone bias generator that includes three separate voltage outputs. The analog microphone bias generator and the primary output (MICBIAS1) are enabled by setting the AMIC_BIAS_EN bit to 1. Once MICBIAS1 is enabled, the other two voltage outputs (MICBIAS2 and MICBIAS3) can also be enabled by setting the AMIC_BIAS_OUT2 and AMIC_BIAS_OUT3 bits to 1. Setting AMIC_BIAS_EN to 0 disables all three voltage outputs.

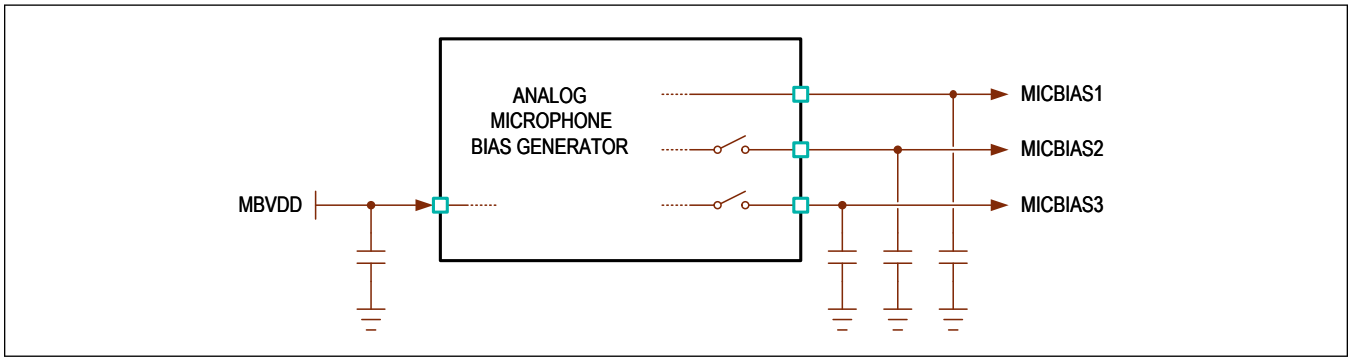


Figure 22. Analog Microphone Bias Generator Diagram

The analog microphone bias generator only operates when the MBVDD supply is powered. The voltage output level can then be configured to any of eight possible voltage levels (ranging from 1.2V up to 3V) with the AMIC_BIAS_SEL bit field. For the output voltage regulation to meet specifications, the MBVDD voltage level must exceed the minimum drop out voltage for the configured microphone bias output voltage level. The microphone bias generator can quickly charge up to a selected output level (either on enable, or if the AMIC_BIAS_SEL bit is dynamically changed from a lower setting to a higher setting while the AMIC bias is active). However, by default AMIC bias discharge is slower (on disable or dynamically from a higher level to a lower level). While this is not an issue when dynamically changing from a higher AMIC bias level to a lower one, this could be a problem if a fast turn off is required. For this scenario, the discharge speed on AMIC bias disable can be increased by setting the AMIC_BIAS_PD_EN bit to 1 (prior to disable).

By default, the analog microphone bias generator operates in low-noise mode. This operating mode minimizes output noise and is best used with microphones with very high SNR or with low-power supply rejection. An example of this is a typical electret condenser microphone (ECM) where the bias input and microphone output share the same connection. The microphone bias generator can instead be placed into lower power mode by setting the AMIC_BIAS_LP_MODE bit to 1. In this operating mode, bias voltage output noise is increased but quiescent power is significantly decreased. Microphone bias low-power mode is best used with microphones with sufficient power supply rejection to tolerate the increased output noise (such as typical analog and digital MEMs microphones).

Digital Microphone Interface

The device provides three separate digital microphone interfaces, each with a clock output and data input connection capable of supporting either a mono or stereo digital microphone connection. This allows for a maximum of six digital microphones to be connected to the device for different use case configurations. However, as the device only provides three microphone input channels, it supports concurrent record (in any given use case) from a maximum of three digital microphone channels (or a combined total of three channels split between analog and digital microphones).

Each of the three digital microphone interfaces can be independently enabled and disabled with the appropriate DMICn_EN bit, and each of the 6 DMIC input data channels can be routed to any of the three microphone input channels (as selected by the respective RECn_SEL bit field). Most digital microphones do not provide an enable/disable control input connection, and if the supply is connected it actively consumes power anytime it is clocked. To minimize inactive digital microphone power, whenever a given interface is disabled the clock output is gated and both the clock output and data input connections are placed in a high impedance state. Four different drive strength options are provided for the clock output of each interface, and the drive strength is configured with the respective DMICn_DRV bit field.

All three digital microphone interfaces share a single source clock, and the clock frequency (and therefore sample rate) is selected from three supported rates with the DMIC_RATE bit field. The three supported digital microphone interface clock frequencies vary depending on whether or not the device is operating from a bit clock that is an integer multiple of either a 48kHz (default) time base or a 44.1kHz time base.

Table 18. Supported Digital Microphone Interface Sample Rates

DMIC CLOCK RATE SETTING	BIT CLOCK ON A 48kHz TIME BASE	BIT CLOCK ON A 44.1kHz TIME BASE
DMIC_RATE = 0x0	f_{DMIC} = 768kHz	f_{DMIC} = 705.6kHz
DMIC_RATE = 0x1	f_{DMIC} = 1.536MHz	f_{DMIC} = 1.4112MHz
DMIC_RATE = 0x2	f_{DMIC} = 3.072MHz	f_{DMIC} = 2.8224MHz

The fastest digital microphone clock rate setting (DMIC_RATE = 0x2) provides the best performance when DMIC inputs are routed to the internal low-latency digital filter channels. While all three digital microphone clock rates are compatible with the PCM record channels, performance degrades as the DMIC to record channel sample rate ratio (over sampling ratio) decreases. Table 19 shows which DMIC clock rate settings are compatible with each channel and sample rate combination.

Table 19. Digital Microphone to Channel Sample Rate Combinations

DIGITAL MICROPHONE CLOCK RATE	DIGITAL FILTER CHANNEL SAMPLE RATE	PCM RECORD CHANNEL SAMPLE RATE
768kHz/705.6kHz	Not Recommended	$f_S \le$ 16kHz
1.536MHz/1.4112MHz	Not Recommended	$f_S \le$ 32kHz
3.072MHz/2.8224MHz	f_S = 96kHz/192kHz/384kHz	$f_S \le$ 48kHz

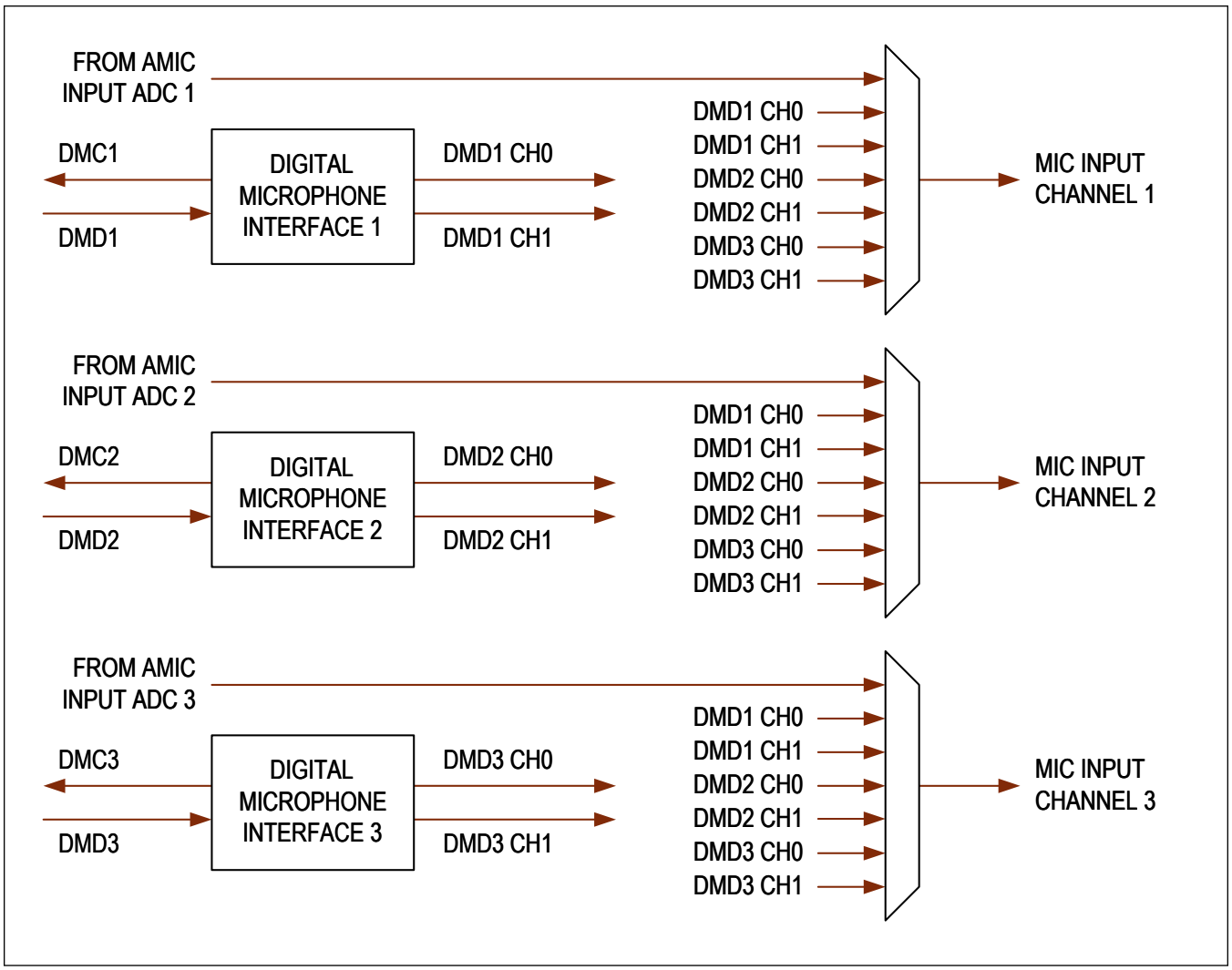


Figure 23. Digital Microphone Input Channel Detailed Block Diagram

Digital Microphone Control Sequencing

Digital microphone interfaces can only be active when the device is in the audio state. The enable bits (DMICn_EN) are all located in the same register, and can be programmed in either the software shutdown state or dynamically in the audio state. When dynamically enabling record or digital filter channels with a digital microphone input, the digital microphone interface enable bits should be set first before setting the enable for (and later unmuting) either the destination record channel (RECn_PCM_EN) and/or the digital filter channel (DF1_EN or DF2_EN). Likewise, when dynamically disabling record and/or digital filter channels with digital microphone inputs, the record and/or digital filter channels should be first muted and then disabled before disabling the digital microphone input interface.

Digital Microphone Interface Frame Configuration

By default, a new digital microphone interface frame starts on a falling clock edge with data for interface channel 0 captured on the next rising edge and data for interface channel 1 captured on the next falling edge. If the DMIC_FRAME_SEL bit is set to 1, this is reversed with each new frame starting on a rising edge instead. When a digital microphone interface is connected to a stereo pair of digital microphones, it is critical that the two connected digital microphones be configured to use opposite edges for data output transmission to avoid contention.

All three digital microphone interfaces use the same frame start polarity (as selected by DMIC_FRAME_SEL). This ensures that data captured in the same frame from any of the three interfaces (and from either channel 0 or channel 1) is phase aligned internally when routed separately to different record or digital filter channels.

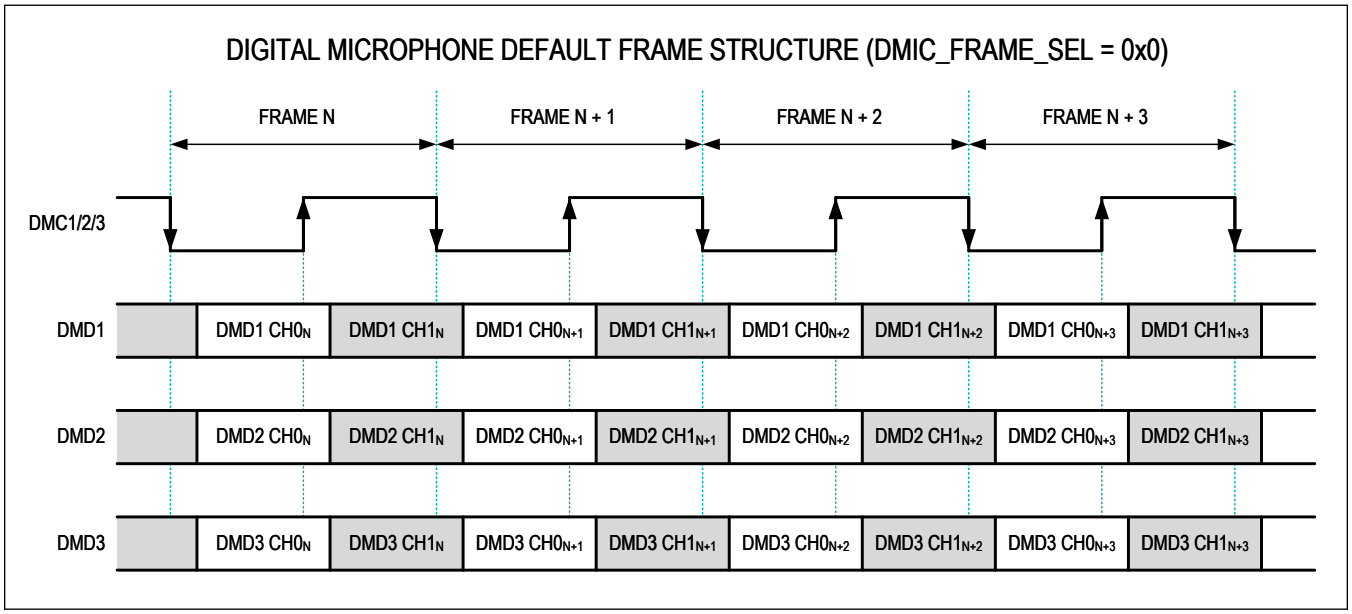


Figure 24. Digital Microphone Interface Default Frame Structure Example

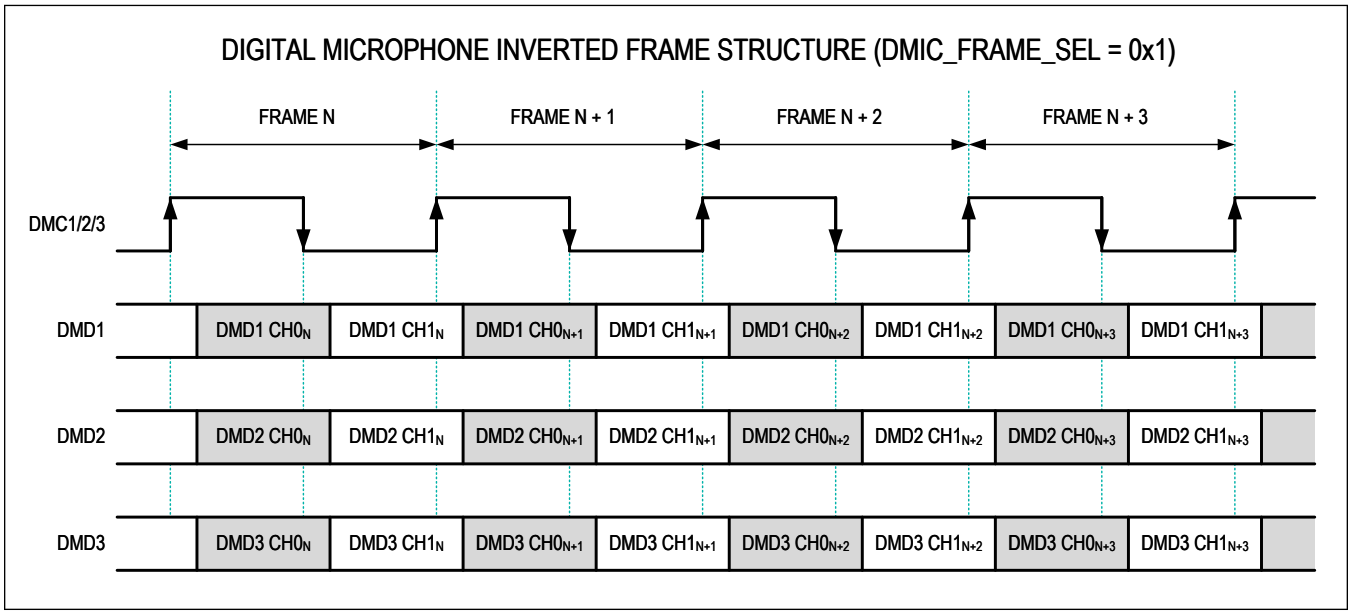


Figure 25. Digital Microphone Interface Inverted Frame Structure Example

Record Channel Configuration

The device provides 4 record channels, each of which outputs audio data through the PCM interface. Three of the record channels (record channels 1, 2, and 3) directly accept microphone data (AMIC or DMIC) from the respective microphone input channel (microphone input channels 1, 2, and 3). The fourth record channel (record channel 4) provides a subset of digital stages and can only accept data from the playback channel monitor. The audio data in each channel is routed through the record channel filters and signal processing before reaching the PCM interface transmitter (DOUT).

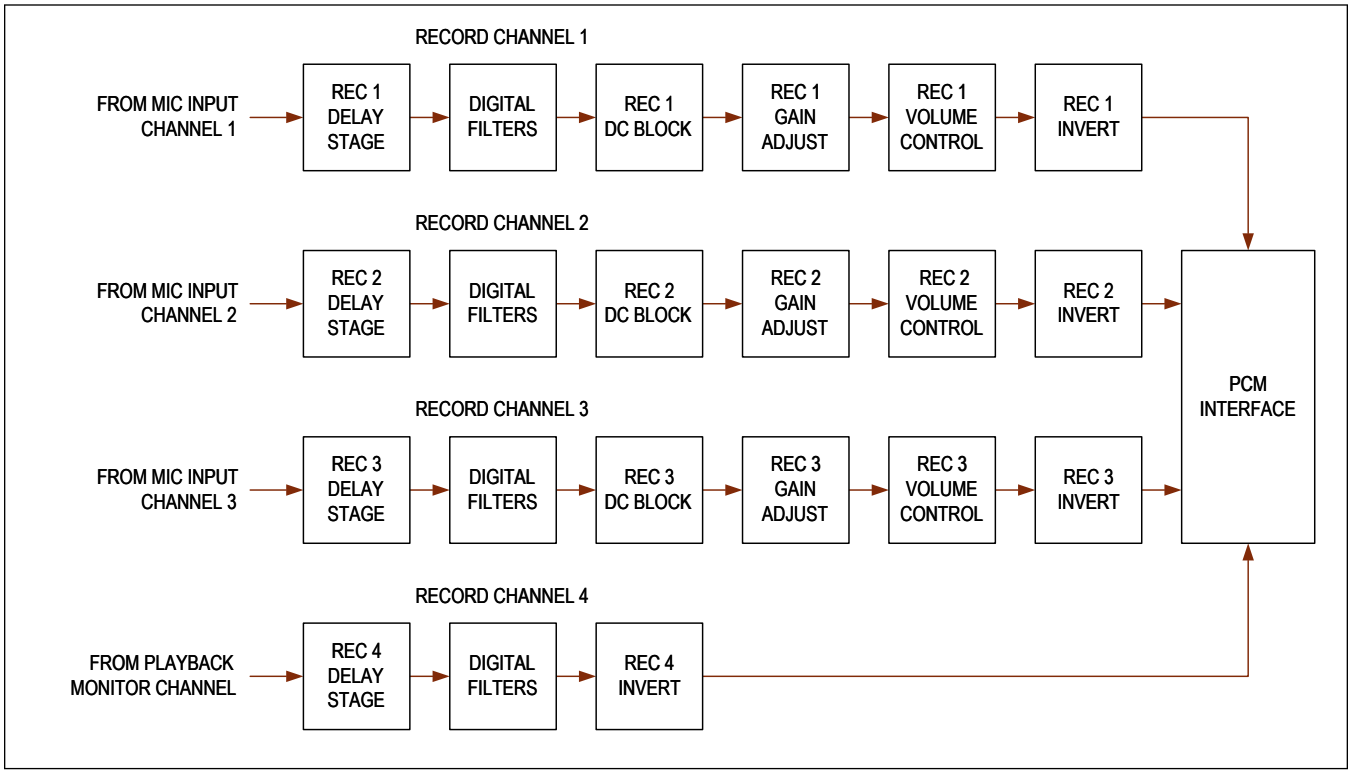


Figure 26. Record Channel Detailed Block Diagram

Record Channel Control Sequencing

Record channels can only be active when the device is in the audio state. Each individual record channel is enabled and disabled with the respective record channel enable bit (RECn_PCM_EN). If one or more RECn_PCM_EN bit is set high while the device is in the software shutdown state, the selected record channels are not enabled until the device transitions to the audio state. Alternatively, the record channel enable bits may be set dynamically while the device is already in the audio state. To guarantee that input data is available, the respective input source channel (microphone and/or playback) should be enabled prior to enabling the destination record channel(s). Likewise, for dynamic disable sequencing, the record channel(s) should be disabled first before disabling the respective input source channel.

For static record channel enable (record channel configuration while in the software shutdown state), record channels are always phase aligned as long as all of the required record channels for a given use case have their respective enable bits (RECn_PCM_EN) set high prior to the device transitioning from the software shutdown state to the audio state. While in the software shutdown state, the record channels can be configured (or reconfigured) without any sequencing restrictions (as long as the audio enable bit is set last in the sequence).

To ensure record channel phase alignment for dynamic record channel enables (record channel configuration while in the active state), all of the channels needed for a given use case should be enabled at the same time. To facilitate this, the record channel enable bits (RECn_PCM_EN) are all located in the same register and can be programmed with a single command. If record channels are enabled dynamically at different times with separate write commands then channel phase alignment may not be preserved. Record channel enables should never be dynamically changed while any given record channel activation or deactivation is already in progress.

When the first enabled record channel (or channels) is active and ready for use (either through a dynamic or static enable), the device generates a REC_PWRUP_DONE_* interrupt event. A dynamic enable of additional record channels (when at least one channel is already active) does not generate additional interrupts. In this case, the host system does not receive an interrupt and should wait for the maximum turn-on time (for dynamic record channel enable) to expire before using the newly enabled record channel.

Record Channel Data Inversion

The output data from each record channel (1 through 4) can optionally be inverted by setting the respective RECn_INVERT bit to 1.

Record Channel DC Blocking Filters

A DC blocking filter can be individually enabled for each of the three primary record channels (record 1, 2, and 3) by setting the respective RECn_DCBLK_EN bit to 1. Record channel 4 (playback monitor channel) does not include the DC blocking filter function.

The DC blocking filter corner frequency is selected for each record channel with the respective RECn_DCBLK bit field, and the corner frequency scales with the record sample rate. The higher corner frequency setting reduces audio band flatness but results in faster settling times for record channel enables.

Record Channel Digital Volume Control

The three primary record channels (record 1, 2, and 3) include a programmable digital volume control. Record channel 4 (playback monitor channel) does not include a digital volume control. The record channel digital volume controls provide an attenuation range of 0dB to -63.5dB in 0.5dB steps, and is configured with the respective RECn_VOL bit field. Record channel volume should not be changed while the channel is active.

Record Channel Digital Gain Adjust

The three primary record channels (record 1, 2, and 3) include a programmable digital gain adjustment. Record channel 4 (playback monitor channel) does not include the digital gain adjustment. The record channel digital gain adjustment provides a gain range of 0dB to +31dB in 1dB steps, and is programmed by channel with the respective RECn_GAIN bit field. The record gain adjust is provided for use cases where a positive record channel gain offset is required, and is commonly required with digital microphone inputs (to match the full-scale input signal level to the full scale of the record channel). The record channel gain adjust setting should not be changed while the respective record channel is active.

Record Channel Delay Stage

The record channel delay stage can individually add from 0 to 7.5 samples of delay to each record channel, and is configured with the respective RECn_DELAY bit field. The record channel delay stage is positioned between the first and second stage of record channel decimation filters. At this point in the record filter chain, the data sample rate is determine by the selected internal DSP sample rate (as set by DSP_SR bit, regardless of the selected PCM record channel sample rate). As a result, record channel delay is configured in terms of the number of samples at this selected internal DSP sample rate (DSP_SR) rather than in terms of the record channel output sample rate (PCM_REC_SR).

The only exception occurs when the record channel sample rate (PCM_REC_SR) is set to 32kHz, and the DSP sample rate (DSP_SR) is set to 96kHz. In this case, the maximum record channel delay is limited to 3.5 samples (and all settings of RECn_DELAY above this are limited to this value).

Internal Digital Filter Channel Configuration

The device provides two internal low-latency digital filter channels denoted respectively as the digital filter channel 1 (DF1) and digital filter channel 2 (DF2). The two channels are functionally identical and are used to support a variety of applications. These include noise cancellation applications (feed-forward, feedback, and hybrid filter profiles), both voice and ambient enhancement applications, transparency applications, and traditional sidetone applications. In addition, a third internal digital filter channel called the playback compensation channel (PBC) is provided in the playback channel. This channel is optimized for (but not limited to) implementing music/voice compensation and/or general feedback compensation filters.

The enable/disable controls, mute toggles, and bank switch controls for all three internal digital channels are placed in the same register (by function). Any programming changes initiated by a single register write command results in a synchronized response across all active internal digital filter channels (affected by the command). The banked DF1, DF2, and PBC channel and filter structure is designed to support dynamic or adaptive filter changes and use case transitions without disruption to active audio playback.

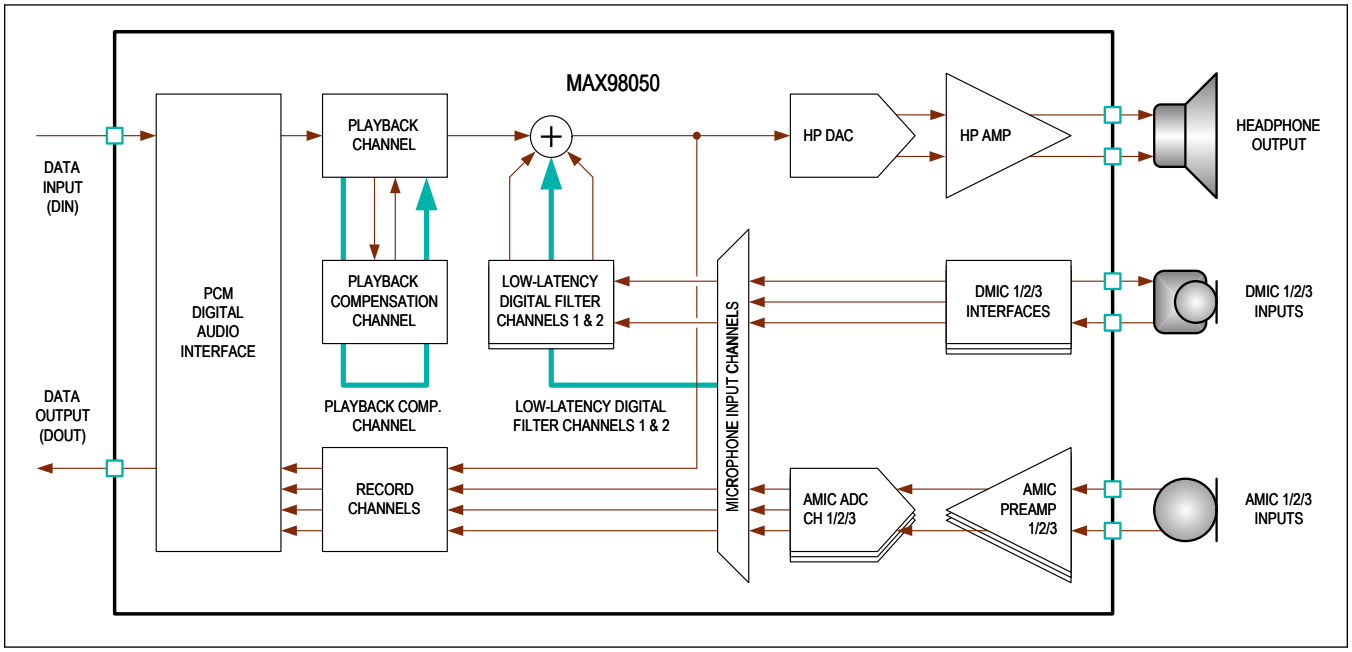


Figure 27. Internal Playback Compensation and Low-Latency Digital Filter Channels

Low-Latency Digital Filter Channel 1 (DF1) and Channel 2 (DF2) Configuration

The 2 low-latency digital filter channels contain the same functional blocks, and can be independently and dynamically enabled with the DF1_EN and DF2_EN bits. The digital filter channel enables are in the same register as the playback compensation channel enable (PBC_EN), and if any of the three enable bits are changed simultaneously with a single write command, the start of the enable (unmute) or disable (mute) action is synchronized across all channels (that are affected by the command).

Digital filter channel 1 can accept data from either microphone input channel 1 or channel 3, and the input data source is selected with the DF1_SEL bit. Likewise, digital filter channel 2 can accept data from microphone input channel 2 or channel 3, and the input data source is instead selected with the DF2_SEL bit. The low-latency digital filter channels both operate at the same sample rate, which is configured with the system level DSP_SR bit field.

The low-latency digital filter channels each provide two banks that can be dynamically swapped, and a subset of the DF1/DF2 register settings (12-band biquad filter coefficients, gain adjust level, and digital volume setting) are duplicated in each bank. The digital filter channel bank selection bits (DF1_BQ_BK_SEL and DF2_BQ_BK_SEL) are used to either select the active bank (prior to enabling the digital filter channel) or to dynamically switch the active bank (while the digital filter channel is active).

A dynamic bank switch temporarily requires additional processing, and as a result this feature is not supported when the digital filter channels are operating at the highest sample rate of 384kHz (as set by the DSP_SR bit). Attempting a dynamic bank swap when operating at a 384khz sample rate could result in an audible glitch. Instead (when operating at 384kHz), a dynamic bank swap can still be accomplished by first muting and disabling the digital filter channel (and active bank), then selecting the inactive bank, and finally by re-enabling and unmuting the channel.

Table 20. Low-Latency Digital FIlter Channel Dynamic Bank Select Restrictions

DIGITAL FILTER CHANNEL PARAMETER	CONFIGURATION SUPPORT		
Channel Sample Rate (DSP_SR)	f_S = 96kHz	f_S = 192kHz	f_S = 384kHz
Dynamic Active Bank Switch Supported	Yes	Yes	No

As with the enable bits, the digital filter channel bank select controls are also in the same register as the playback compensation channel bank select control (PBC_BQ_BK_SEL). If any of the three bank select bits are dynamically changed simultaneously with a single write command, the bank switch action is synchronized across all active channels (that are affected by the command). While some bank specific register controls are restricted and cannot be changed for the currently active bank, the inactive bank controls can be programmed fully at any time.

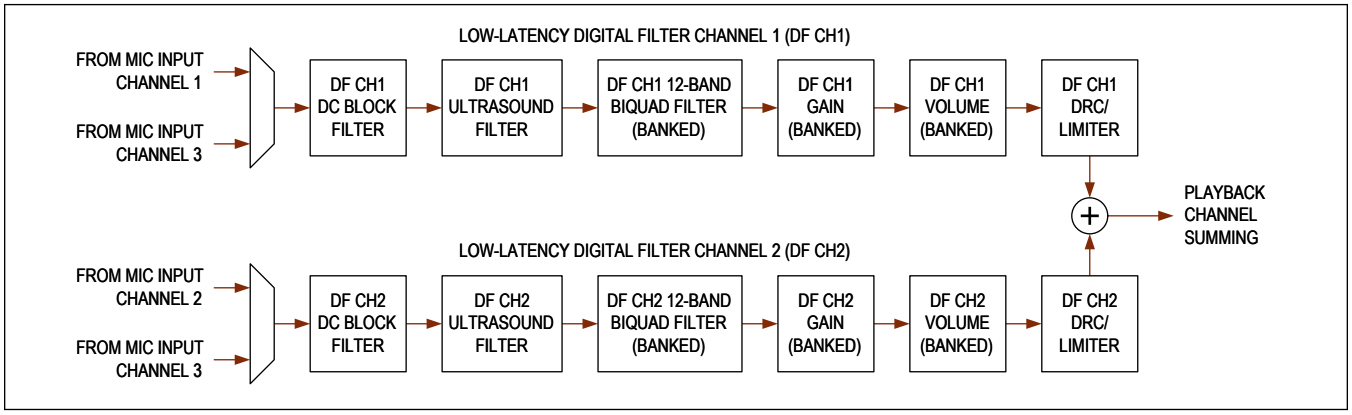


Figure 28. Low-Latency Digital Filter Channel 1 and 2 Detailed Block Diagram

DF1/DF2 Channel Ultrasound Polyphase Elliptical Filter

Low-latency digital filter channels 1 and 2 each feature a fully programmable, 9th order polyphase elliptical all-pass filter. This filter is provided primarily for use cases requiring a high-order ultrasound filter, and can be enabled for the digital filter channels with the DF1_ULTRA_EN and DF2_ULTRA_EN bits respectively. Enabling the ultrasound filter results in increased channel latency (both baseline and based on the filter configuration). Furthermore, due to the increased processing required when the ultrasound filters in both channels are active, the record channel cannot have more than two channels active concurrently with them.

The nine ultrasound filter coefficients can be independently programmed for digital filter channels 1 and 2, and each individual coefficient is 3 bytes (24 bits) long. Each set of three registers (per coefficient) must be programmed consecutively for the settings to take effect. The coefficients are stored using a signed two's complement format where the first 4 bits are the integer portion and the last 20 bits are the decimal portion (which results in an approximate +8 to -8 range for each coefficient). The ultrasound filter structure and coefficient placement is illustrated in Figure 29.

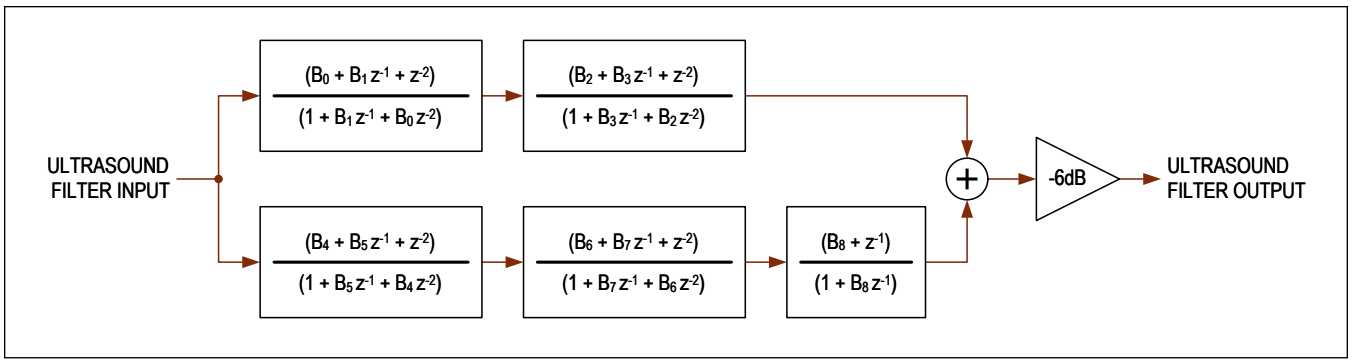


Figure 29. Low-Latency Digital Filter Channel Ultrasound Filter Structure

DF1/DF2 Channel Ultrasound Filter Coefficient Registers

The low-latency digital filter channels each contain a 9th order polyphase elliptical all-pass filter. The register structure for each coefficient is identical and repeated.

Each coefficient is sequentially placed in the register map covering a total of 36 addresses per digital filter channel. Within this structure, each individual coefficient spans four addresses, the first of which is blank followed by the three addresses that make up the 24-bit coefficient (lowest bits, middle bits, and highest bits in that order). Coefficient segments must be consecutively written for the new settings to take effect, but blank addresses may be skipped or written with any value as needed (when creating a programming sequence). All coefficients can be programmed when the device is in software shutdown, but should not be programmed while the ultrasound filter in a given digital filter channel is active.

Table 21 shows the address space where the coefficients for each digital filter channel are placed in the device register space.

Table 21. Ultrasound Filter Register Address Ranges

CHANNEL	START ADDRESS	END ADDRESS
Digital Filter Channel 1	0x2100	0x2123
Digital Filter Channel 2	0x2140	0x2163

Table 22 and Table 23 show the register address locations for each ultrasound filter coefficient for each of the respective digital filter channels.

Table 22. Digital Filter Channel 1 Ultrasound Filter Coefficient Register Addresses

COEFFICIENT	BLANK REGISTER	BITS [7:0] REGISTER	BITS [15:8] REGISTER	BITS [23:16] REGISTER
1	0x2100	0x2101	0x2102	0x2103
2	0x2104	0x2105	0x2106	0x2107
3	0x2108	0x2109	0x210A	0x210B
4	0x210C	0x210D	0x210E	0x210F
5	0x2110	0x2111	0x2112	0x2113
6	0x2114	0x2115	0x2116	0x2117
7	0x2118	0x2119	0x211A	0x211B
8	0x211C	0x211D	0x211E	0x211F
9	0x2120	0x2121	0x2122	0x2123
Blank	0x2124 to 0x213F			

Table 23. Digital Filter Channel 2 Ultrasound Filter Coefficient Register Addresses

COEFFICIENT	BLANK REGISTER	BITS [7:0] REGISTER	BITS [15:8] REGISTER	BITS [23:16] REGISTER
1	0x2140	0x2141	0x2142	0x2143
2	0x2144	0x2145	0x2146	0x2147
3	0x2148	0x2149	0x214A	0x214B
4	0x214C	0x214D	0x214E	0x214F
5	0x2150	0x2151	0x2152	0x2153
6	0x2154	0x2155	0x2156	0x2157
7	0x2158	0x2159	0x215A	0x215B
8	0x215C	0x215D	0x215E	0x215F
9	0x2160	0x2161	0x2162	0x2163
Blank	0x2164 to 0x21FF			

DF1/DF2 Channel Ultrasound Filter Example Coefficients

Six example ultrasound filter implementations are provided for each of the three supported digital filter channel sample rate options. For each supported sample rate, the examples provided have three different levels of stopband attenuation (-20dB, -40dB, and -60dB) and are provided for both a low cutoff frequency (approximate $f_C \approx$ 24kHz to 26kHz) and a higher cutoff frequency (approximate $f_C \approx$ 30kHz to 32kHz). Generally, as ultrasound filter stopband attenuation is increased, the latency of the implemented filter is also increased.

Table 24. Example Ultrasound Filters for f_S = 384kHz with Low Cutoff Frequencies

FILTER PARAMETER	FILTER CONFIGURATION		
Cutoff Frequency	22.9kHz	22.5kHz	22.3kHz
Stopband Frequency	24.1kHz	24.2kHz	24.3kHz
Stopband Attenuation	-20dB	-40dB	-60dB
Coeficient B0 Value	0x0CAD01	0x0FAD3B	0x0F3665
Coeficient B1 Value	0xE531C9	0xE26DDC	0xE2AD5F
Coeficient B2 Value	0x100000	0x0C3F03	0x0C8470
Coeficient B3 Value	0x100000	0xE4E90D	0xE43CD8
Coeficient B4 Value	0x0F7454	0x0E9573	0x0FCAE8
Coeficient B5 Value	0xE2B8E3	0xE33EA6	0xE24A01
Coeficient B6 Value	0x100000	0x100000	0x0E1FD4
Coeficient B7 Value	0x100000	0x100000	0xE35139
Coeficient B8 Value	0xF4A53D	0xF31F18	0xF2623D

Table 25. Example Ultrasound Filters for f_S = 384kHz with High Cutoff Frequencies

FILTER PARAMETER	FILTER CONFIGURATION		
Cutoff Frequency	29.1kHz	28.7kHz	28.4kHz
Stopband Frequency	30.7kHz	30.8kHz	30.9kHz
Stopband Attenuation	-20dB	-40dB	-60dB
Coeficient B0 Value	0x0BEF71	0x0F986B	0x0F042C
Coeficient B1 Value	0xE6FEC5	0xE3C81B	0xE4022E
Coeficient B2 Value	0x100000	0x0B6525	0x0BB38D
Coeficient B3 Value	0x100000	0xE66C42	0xE57E28
Coeficient B4 Value	0x0F51A9	0x0E3D4B	0x0FBD79
Coeficient B5 Value	0xE4299A	0xE4AC67	0xE39A30
Coeficient B6 Value	0x100000	0x100000	0x0DAB2A
Coeficient B7 Value	0x100000	0x100000	0xE4A0A8
Coeficient B8 Value	0xF5B820	0xF3E4A2	0xF2FDEE

Table 26. Example Ultrasound Filters for f_S = 192kHz with Low Cutoff Frequencies

FILTER PARAMETER	FILTER CONFIGURATION		
Cutoff Frequency	22.9kHz	22.5kHz	22.8kHz
Stopband Frequency	24.0kHz	24.1kHz	28.0kHz
Stopband Attenuation	-20dB	-40dB	-60dB
Coeficient B0 Value	0x0A4D62	0x0F66F5	0x0EFD02
Coeficient B1 Value	0xEC541F	0xE8A6EC	0xE91AB5
Coeficient B2 Value	0x100000	0x0971F5	0x096DD2
Coeficient B3 Value	0x100000	0xEABB66	0xE9C6E4
Coeficient B4 Value	0x0F0044	0x0D6EB8	0x0C8C21
Coeficient B5 Value	0xE93E15	0xE96CA7	0xE9A46B
Coeficient B6 Value	0x100000	0x100000	0x100000
Coeficient B7 Value	0x100000	0x100000	0x100000
Coeficient B8 Value	0xF85198	0xF5D8E5	0xF4E487

Table 27. Example Ultrasound Filters for f_S = 192kHz with High Cutoff Frequencies

FILTER PARAMETER	FILTER CONFIGURATION		
Cutoff Frequency	29.0kHz	28.6kHz	28.4kHz
Stopband Frequency	30.4kHz	30.5kHz	30.5kHz
Stopband Attenuation	-20dB	-40dB	-60dB
Coeficient B0 Value	0x0963F7	0x0F490A	0x0E4393
Coeficient B1 Value	0xF0B021	0xED54AF	0xED06B9
Coeficient B2 Value	0x100000	0x0843D2	0x0883C3
Coeficient B3 Value	0x100000	0xEE3198	0xEBE21F
Coeficient B4 Value	0x0ECFF0	0x0CF249	0x0F89CE
Coeficient B5 Value	0xEE07AD	0xEDBD21	0xED0565
Coeficient B6 Value	0x100000	0x100000	0x0BE92F
Coeficient B7 Value	0x100000	0x100000	0xEC9B63
Coeficient B8 Value	0xFA160F	0xF74017	0xF5BAFF

Table 28. Example Ultrasound Filters for f_S = 96kHz with Low Cutoff Frequencies

FILTER PARAMETER	FILTER CONFIGURATION		
Cutoff Frequency	22.6kHz	23.3kHz	22.6kHz
Stopband Frequency	23.4kHz	27.3kHz	26.1kHz
Stopband Attenuation	-20dB	-40dB	-60dB
Coeficient B0 Value	0x082BBC	0x061BB0	0x0E8754
Coeficient B1 Value	0xFD0F31	0xFAB98D	0xFCE546
Coeficient B2 Value	0x100000	0x100000	0x05C22F
Coeficient B3 Value	0x100000	0x100000	0xF5E252
Coeficient B4 Value	0x0E8E5A	0x0D1A19	0x0AE1CA
Coeficient B5 Value	0xFD352D	0xFE1FAE	0xFA7F38
Coeficient B6 Value	0x100000	0x100000	0x100000
Coeficient B7 Value	0x100000	0x100000	0x100000
Coeficient B8 Value	0xFE6733	0xFBD99C	0xF97944

Table 29. Example Ultrasound Filters for f_S = 96kHz with High Cutoff Frequencies

FILTER PARAMETER	FILTER CONFIGURATION		
Cutoff Frequency	28.6kHz	29.2kHz	28.6kHz
Stopband Frequency	29.4kHz	32.8kHz	31.8kHz
Stopband Attenuation	-20dB	-40dB	-60dB
Coeficient B0 Value	0x08582E	0x05FCA8	0x0E948E
Coeficient B1 Value	0x068144	0x035588	0x08BE0C
Coeficient B2 Value	0x100000	0x100000	0x04EF35
Coeficient B3 Value	0x100000	0x100000	0xFDC25B
Coeficient B4 Value	0x0E9CB7	0x0D3C61	0x0ADDA8
Coeficient B5 Value	0x090B05	0x095A64	0x05011D
Coeficient B6 Value	0x100000	0x100000	0x100000
Coeficient B7 Value	0x100000	0x100000	0x100000
Coeficient B8 Value	0x018FCE	0xFEEC70	0xFC4EAF

DF1/DF2 Channel 12-Band Biquad Filter

The low-latency digital filter channels each feature a banked 12-band filter where each band is a full, individually programmable digital biquad filter. The biquad filter can be enabled (and the number of active bands selected) by the digital filter channel and bank with the DF1_BQ_EN_BKn and DF2_BQ_EN_BKn bit fields (where n is A for bank A and B for bank B). Each channel and bank can be configured to have from 0 to 12 bands active, and inactive bands do not consume additional quiescent power. The gain (A), quality factor (Q), and frequency (f_0) limitations by biquad band vary by implemented filter type, and are described in the *Electrical Characteristics Table*.

The transfer function for biquad band is defined as:

$$H(z) = \frac{\left(B_0 + B_1 z^{-1} + B_2 z^{-2}\right)}{\left(A_0 + A_1 z^{-1} + A_2 z^{-2}\right)}$$

The biquad filter in each band has five user-programmable coefficients (B0, B1, B2, A1, and A2 with A0 fixed at 1), and each individual coefficient is 3 bytes (24 bits) long. Each set of three registers (per coefficient) must be programmed consecutively (in order) for the settings to take effect. The coefficients are stored using a signed two's complement format where the first 2 bits are the integer portion and the last 22 bits are the decimal portion (which results in an approximate +2 to -2 range for each coefficient). This coefficient range and resolution allows for the implementation of several common filter types including peaking filters, high and low pass filters, and high and low shelving filters. The 2.22 format is a fixed point coefficient implementation that results in some range and resolution boundary limits for filter parameters (see the Biquad Filter Characteristics in the *Electrical Characteristics Table*).

The biquad filter coefficient register bits are uninitialized when the device first powers up, and the coefficients for any given channel, bank, and biquad band should be fully programmed before being enabled. The biquad filter coefficients can be freely written and read back when the device is in software shutdown (AUDIO_EN = 0) or when the respective digital filter channel (DF1 or DF2) is disabled (DF1_EN or DF2_EN set to 0). However, once enabled only inactive biquad banks and bands can be safely written (for example DF1 bank B can be written freely while DF1 bank A is enabled). Readback is restricted by channel enable, and attempting to read back the coefficients for either digital filter channel 1 or 2 while the respective channel is enabled and active may return all zero values.

DF1/DF2 Channel Biquad Filter Coefficient Registers

The low-latency digital filter channels each contain a 12-band biquad filter. Each of the filter bands and coefficients are duplicated over two banks to allow for the inactive bank to be dynamically updated (prior to initiating a bank swap for smooth filter profile transitions). The register structure for each band (and the five coefficients within each) is identical and repeated.

The coefficients of each band are sequentially placed in the same order in the register map (B0, B1, B2, A1, A2) for a total of 20 addresses per filter band. Within this structure, each coefficient spans four addresses, the first of which is blank followed by the three addresses that make up the 24-bit coefficient (lowest bits, middle bits, and highest bits in order). Coefficient segments must be consecutively written for the new settings to take effect, but blank addresses may be skipped or written with any value as needed (when creating a programming sequence). All coefficients can be programmed when the device is in software shutdown, but only inactive banks can be safely programmed while a given digital filter channel is active.

Table 30 shows the address space where the coefficients for each digital filter channel and bank are placed in the device register space.

Table 30. Digital Filter Channel Biquad Filter Register Address Ranges

CHANNEL	BANK	START ADDRESS	END ADDRESS
Digital Filter Channel 1	A	0x2400	0x24FF
	B	0x2500	0x25FF
Digital Filter Channel 2	A	0x2600	0x26FF
	B	0x2700	0x27FF

Table 31 shows how each filter band and coefficient are structured in the register space for each of the respective channels and banks. The underscore denotes where to insert the appropriate value (4, 5, 6, or 7) depending on which digital filter channel (1 or 2) and bank (A or B) are being programmed or read back.

Table 31. Digital Filter Channel and Bank Biquad Filter Coefficient Register Addresses

FILTER BAND	FILTER COEFFICIENT	BLANK REGISTER	BITS [7:0] REGISTER	BITS [15:8] REGISTER	BITS [23:16] REGISTER
1	B0	0x2_00	0x2_01	0x2_02	0x2_03
	B1	0x2_04	0x2_05	0x2_06	0x2_07
	B2	0x2_08	0x2_09	0x2_0A	0x2_0B
	A1	0x2_0C	0x2_0D	0x2_0E	0x2_0F
	A2	0x2_10	0x2_11	0x2_12	0x2_13
2	B0	0x2_14	0x2_15	0x2_16	0x2_17
	B1	0x2_18	0x2_19	0x2_1A	0x2_1B
	B2	0x2_1C	0x2_1D	0x2_1E	0x2_1F
	A1	0x2_20	0x2_21	0x2_22	0x2_23
	A2	0x2_24	0x2_25	0x2_26	0x2_27
3	B0	0x2_28	0x2_29	0x2_2A	0x2_2B
	B1	0x2_2C	0x2_2D	0x2_2E	0x2_2F
	B2	0x2_30	0x2_31	0x2_32	0x2_33
	A1	0x2_34	0x2_35	0x2_36	0x2_37
	A2	0x2_38	0x2_39	0x2_3A	0x2_3B
4	B0	0x2_3C	0x2_3D	0x2_3E	0x2_3F
	B1	0x2_40	0x2_41	0x2_42	0x2_43
	B2	0x2_44	0x2_45	0x2_46	0x2_47
	A1	0x2_48	0x2_49	0x2_4A	0x2_4B
	A2	0x2_4C	0x2_4D	0x2_4E	0x2_4F
5	B0	0x2_50	0x2_51	0x2_52	0x2_53
	B1	0x2_54	0x2_55	0x2_56	0x2_57
	B2	0x2_58	0x2_59	0x2_5A	0x2_5B
	A1	0x2_5C	0x2_5D	0x2_5E	0x2_5F
	A2	0x2_60	0x2_61	0x2_62	0x2_63
6	B0	0x2_64	0x2_65	0x2_66	0x2_67
	B1	0x2_68	0x2_69	0x2_6A	0x2_6B
	B2	0x2_6C	0x2_6D	0x2_6E	0x2_6F
	A1	0x2_70	0x2_71	0x2_72	0x2_73
	A2	0x2_74	0x2_75	0x2_76	0x2_77
7	B0	0x2_78	0x2_79	0x2_7A	0x2_7B
	B1	0x2_7C	0x2_7D	0x2_7E	0x2_7F
	B2	0x2_80	0x2_81	0x2_82	0x2_83
	A1	0x2_84	0x2_85	0x2_86	0x2_87
	A2	0x2_88	0x2_89	0x2_8A	0x2_8B

Table 31. Digital Filter Channel and Bank Biquad Filter Coefficient Register Addresses (continued)

FILTER BAND	FILTER COEFFICIENT	BLANK REGISTER	BITS [7:0] REGISTER	BITS [15:8] REGISTER	BITS [23:16] REGISTER
8	B0	0x2_8C	0x2_8D	0x2_8E	0x2_8F
	B1	0x2_90	0x2_91	0x2_92	0x2_93
	B2	0x2_94	0x2_95	0x2_96	0x2_97
	A1	0x2_98	0x2_99	0x2_9A	0x2_9B
	A2	0x2_9C	0x2_9D	0x2_9E	0x2_9F
9	B0	0x2_A0	0x2_A1	0x2_A2	0x2_A3
	B1	0x2_A4	0x2_A5	0x2_A6	0x2_A7
	B2	0x2_A8	0x2_A9	0x2_AA	0x2_AB
	A1	0x2_AC	0x2_AD	0x2_AE	0x2_AF
	A2	0x2_B0	0x2_B1	0x2_B2	0x2_B3
10	B0	0x2_B4	0x2_B5	0x2_B6	0x2_B7
	B1	0x2_B8	0x2_B9	0x2_BA	0x2_BB
	B2	0x2_BC	0x2_BD	0x2_BE	0x2_BF
	A1	0x2_C0	0x2_C1	0x2_C2	0x2_C3
	A2	0x2_C4	0x2_C5	0x2_C6	0x2_C7
11	B0	0x2_C8	0x2_C9	0x2_CA	0x2_CB
	B1	0x2_CC	0x2_CD	0x2_CE	0x2_CF
	B2	0x2_D0	0x2_D1	0x2_D2	0x2_D3
	A1	0x2_D4	0x2_D5	0x2_D6	0x2_D7
	A2	0x2_D8	0x2_D9	0x2_DA	0x2_DB
12	B0	0x2_DC	0x2_DD	0x2_DE	0x2_DF
	B1	0x2_E0	0x2_E1	0x2_E2	0x2_E3
	B2	0x2_E4	0x2_E5	0x2_E6	0x2_E7
	A1	0x2_E8	0x2_E9	0x2_EA	0x2_EB
	A2	0x2_EC	0x2_ED	0x2_EE	0x2_EF
Blank	-	0x2_F0 to 0x2_FF			

DF1/DF2 Channel DC Blocking Filter

Low-latency digital filter channels 1 and 2 provide a DC blocking filter that can be enabled by setting the DF1_DCBLK_EN and DF2_DCBLK_EN bits to 1. The respective DC blocking filter corner frequencies are selected with the DF1_DCBLK and DF2_DCBLK bit fields. The configured corner frequency for each setting depends on the digital filter channel sample rate (DSP_SR) selected. The higher corner frequency settings reduce low-frequency audio band flatness, but result in faster settling times after digital filter channel enable.

DF1/DF2 Channel Digital Gain Adjust

The low-latency digital filter channels include a banked, programmable coarse digital gain adjustment. The digital filter channel digital gain adjustment provides a gain range of 0dB to +42dB in 6dB steps, and is programmed individually by channel and bank with the DF1_GAIN_BKn and DF2_GAIN_BKn bit fields (where n is A for bank A and B for bank B). The digital filter channel gain adjust is provided for use cases where a large positive gain offset is required, and should not be changed while the respective digital filter channel and bank is active.

DF1/DF2 Channel Digital Volume Control

The low-latency digital filter channels include a banked, dynamically programmable digital volume control. The digital volume control provides an attenuation range of 0dB to -31.5dB in 0.5dB steps, and is configured individually by channel and bank with the DF1_VOL_BKn and DF2_VOL_BKn bit fields (where n is A for bank A and B for bank B).

A digital mute is also provided for each digital filter channel, and is enabled with the DF1_VOL_MUTE and DF2_VOL_MUTE bits respectively. The digital filter and playback compensation channel mutes are all in the same register, and if any of the channel mute bits are changed simultaneously with a single write command the start of the mute or unmute action (and volume ramp if enabled) is synchronized across all affected channels.

When enabled, digital volume ramping occurs during digital filter channel startup, dynamic bank changes, volume changes, and digital mute toggling. Digital filter channel volume ramping can be dynamically enabled and disabled with the DF1_VOL_RMP_EN and DF2_VOL_RMP_EN bits, however the setting should never be changed while a volume ramp is in progress. For matched behavior and channel latency between the two channels, volume ramping should always be either enabled for both channels or disabled for both channels. When a volume ramp is complete, the device generates the appropriate ramp done interrupt (DF1_RMP_DONE_* and DF2_RMP_DONE_*). The duration of a given volume ramp is selected with the DF1_VOL_RMP_RATE and DF2_VOL_RMP_RATE bit fields respectively. Depending on the type of audio content and the characteristics of the speaker load, selecting faster ramp rates (typically those less than 32ms) or disabling ramping entirely can potentially result in audible glitches during volume changes.

DF1/DF2 Channel Dynamic Range Compression (DRC) and Limiter Stage

The low-latency digital filter channels include a flexible dynamic range compressor (DRC) and limiter stage that is enabled by channel with the DF1_DRC_EN and DF2_DRC_EN bits. The DRC/limiter stage features a programmable compression ratio, activation threshold, and attack and release time weighting factors.

When the digital filter channel DRC/limiter stage is enabled, if the signal (which is monitored with a running RMS level calculation) exceeds the configured compression threshold, the channel gain is reduced by the selected compression ratio. The compression threshold is programmable from a range of -62dBFS RMS to 0dBFS RMS, and the threshold is configured with the DF1_DRC_THR and DF2_DRC_THR bit fields. The compression ratio is also programmable with a limited number of settings covering a finite range from 2:1 up to 60:1, and is selected with the DF1_DRC_CMP and DF2_DRC_CMP bit fields. In addition, an infinite compression ratio setting is provided that effectively transforms the DRC stage into a signal limiter stage.

To determine the attack and release response, the channel DRC/Limiter stage internally uses a running RMS level calculation. The calculated RMS level is then compared to the configured compression threshold. This running RMS level calculation includes a weighting factor α (sometimes called a forgetting factor) that determines the relative weighting (or ratio) of the absolute signal level and the current RMS level result that is used to calculate the next RMS level result.

Each digital filter channel provides a separate attack weighting factor and release weighting factor setting for the RMS level calculations. The attack weighting factor (α_{ATK}) for a given channel is configured with the DF1_DRC_ATK_WF and DF2_DRC_ATK_WF bit fields. Likewise, the release weighting factor (α_{RLS}) for a given channel is configured with the DF1_DRC_RLS_WF and DF2_DRC_RLS_WF bit fields.

This RMS level calculation effectively sets the DRC attack time constant (t_{DRC_ATK}) and release time constant (t_{DRC_RLS}). To configure the desired DRC attack and release time constants relative to the configured digital filter channel sample rate (f_{S_DF} as set by DSP_SR), use the following equations to calculate the appropriate attack weighting factor and release weighting factor.

Attack Time Constant Calculation: $\alpha_{ATK} = (64 \times 2^{16}) / (f_{S\_DF} \times t_{DRC\_ATK} + 1)$

Release Time Constant Calculation: $\alpha_{RLS} = (64 \times 2^{16}) / (f_{S\_DF} \times t_{DRC\_RLS} + 1)$

The digital filter channel DRC/limiter stage also supports instant attack and release responses. The DF1_DRC_INST_ATK and DF2_DRC_INST_ATK bits are used to enable instant attack mode (by channel), while the DF1_DRC_INST_RLS and DF2_DRC_INST_RLS bits are used to enable instant release mode (by channel).

DF1/DF2 Channel DRC and Limiter Stage RMS Level Calculations

Each time a new data sample enters the digital filter channel DRC/limiter stage, the block must determine whether to attack or release. To do this, it must calculate the next RMS level value ($V_{RMS}(N)$) and this is done in multiple steps as follows.

Step 1:

The attack calculation is made using the attack weighting factor:

$V_{RMS\_ATK}(N) = (V_{ABSOLUTE}(N) \times \alpha_{ATK}) + (V_{RMS\_ATK}(N-1) \times (1- \alpha_{ATK}))$

If instant attack mode is enabled, the absolute value is used directly instead of the above calculation:

$V_{RMS\_ATK}(N) = V_{ABSOLUTE}(N)$

Step 2:

If $V_{RMS\_ATK}(N)$ is greater than the previous RMS level value ($V_{RMS}(N-1)$), then attack is selected and $V_{RMS\_ATK}(N)$ is used as the next RMS level value ($V_{RMS}(N)$).

$V_{RMS}(N) = V_{RMS\_ATK}(N)$

If $V_{RMS\_ATK}(N)$ is not greater than $V_{RMS}(N-1)$, then release is selected and the calculation proceeds to step 3.

Step 3:

The release calculation is made using the release weighting factor:

$V_{RMS\_RLS}(N) = (V_{RMS\_ATK}(N) \times \alpha_{RLS}) + (V_{RMS}(N-1) \times (1- \alpha_{RLS}))$

Note that the release calculation uses the result of the attack calculation. If instant attack mode is enabled, then the attack weighting factor must be set to the maximum value (0xFFFF) to allow for accurate release calculations.

If instant release mode is enabled, the result of the attack calculation is used directly instead of the release calculation:

$V_{RMS\_RLS}(N) = V_{RMS\_ATK}(N)$

The next RMS level value is defined as equal to the result:

$V_{RMS}(N) = V_{RMS\_RLS}(N)$

Playback Compensation (PBC) Digital Filter Channel

The playback compensation (PBC) digital filter channel is part of the playback channel, and can be dynamically enabled with the PBC_EN bit. The playback compensation channel enable is in the same register as the low-latency digital filter channel 1 and 2 enables (DF1_EN and DF2_EN), and if any of these enable bits are changed simultaneously with a single write command the start of the enable or disable action is synchronized across all active channels (that are affected by the command).

The playback compensation channel only accepts data from the playback channel, and as a result it operates at the same sample rate as the playback channel (as configured with the PCM_PB_SR bit field).

The playback compensation channel provides two banks (bank A and bank B) that can be dynamically swapped, and all channel functional blocks and register settings are duplicated in each bank. The PBC_BK_SEL bit is used to either select the active bank (prior to enabling the channel) or to dynamically switch the active bank (while the channel is active). A dynamic bank switch temporarily requires additional processing, and as a result the maximum number of active playback compensation biquad channels is limited at the highest playback sample rate of 192kHz (as set by the PCM_PB_SR bit). Attempting a dynamic bank swap when the limits are exceeded (as shown in Table 32) could result in an audible glitch. Instead, in this case a bank swap can still be accomplished by first muting and disabling the channel (and active bank), then selecting the inactive bank, and finally by re-enabling and unmuting the channel.

Table 32. Playback Compensation Channel Dynamic Bank Select Restrictions

FILTER PARAMETER	FILTER CONFIGURATION		
Sample Rate (PCM_PB_SR)	$f_S \le 96kHz$	f_S = 176.4kHz or 192kHz	
5-Band Playback Equalizer Enabled	N/A	Yes	No
Number of Active PBC Biquad Bands	All 10 Bands	7 Bands Maximum	9 Bands Maximum

The playback compensation channel bank select control is in the same register as the low-latency digital filter channel 1 and 2 bank select controls (DF1_BQ_BK_SEL and DF2_BQ_BK_SEL). If any of these bank select bits are dynamically changed simultaneously with a single write command, the start of the bank switch action is synchronized across all active channels (that are affected by the command).

While some playback compensation channel bank specific register controls are restricted and cannot be changed for the currently active bank, the inactive bank controls can be programmed fully at any time.

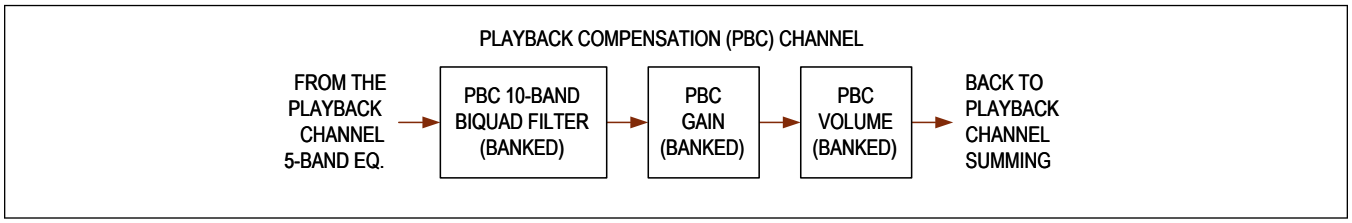


Figure 30. Playback Compensation Channel Detailed Block Diagram

PBC Channel 10-Band Biquad Filter

The playback compensation digital filter channel features a banked 10-band filter where each band is a full, individually programmable digital biquad filter. The biquad filter can be configured by bank with the PBC_BQ_EN_BKA and PBC_BQ_EN_BKB bit fields. Each bank can be configured to have from 0 to 10 bands active, and inactive bands do not consume additional quiescent power. The gain (A), quality factor (Q), and frequency (f_0) limitations by biquad band vary by implemented filter type, and are described in the *Electrical Characteristics Table*.

The transfer function for each biquad band is defined as:

$$H(z) = \frac{\left(B_0 + B_1 Z^{-1} + B_2 Z^{-2}\right)}{\left(A_0 + A_1 Z^{-1} + A_2 Z^{-2}\right)}$$

The biquad filter in each band has five user-programmable coefficients (B0, B1, B2, A1, and A2 with A0 fixed at 1), and each individual coefficient is 3 bytes (24 bits) long. Each set of three registers (per coefficient) must be programmed consecutively for the settings to take effect. The coefficients are stored using a signed two's complement format where the first 2 bits are the integer portion and the last 22 bits are the decimal portion (which results in an approximate +2 to -2 range for each coefficient). This coefficient range and resolution allows for the implementation of several common filter types including peaking filters, high and low pass filters, and high and low shelving filters. The 2.22 format is a fixed point coefficient implementation that results in some range and resolution boundary limits for filter parameters (see the Biquad Filter Characteristics in the *Electrical Characteristics Table*).

The biquad filter coefficient register bits are uninitialized when the device first powers up, and the coefficients for any given bank and biquad band should be fully programmed before that band is enabled. The biquad filter coefficients can be freely written and read back when the device is in software shutdown (AUDIO_EN = 0) or when the playback channel is disabled (PB_EN = 0). However, once the playback channel is enabled, only the inactive bank and bands can be safely written (for example PBC bank B can be written freely while PBC bank A is enabled). Readback is restricted by the overall playback channel enable, and attempting to read back the coefficients for the playback compensation channel while the playback channel is enabled and active may return all zero values.

PBC Channel Biquad Filter Coefficient Registers

The playback compensation (PBC) digital filter channel contains a 10-band biquad filter. Each of the filter bands and coefficients are duplicated over two banks to allow for the inactive bank to be dynamically updated (prior to initiating a bank swap for smooth filter profile transitions). The register structure for each band (and the 5 coefficients within each) is identical and repeated.

The coefficients in each band are sequentially placed in the same order in the register map (B0, B1, B2, A1, A2) for a total of 20 addresses per filter band. Within this structure, each coefficient spans four addresses, the first of which is blank followed by the three addresses that make up the 24-bit coefficient (lowest bits, middle bits, and highest bits in order). Coefficient segments must be consecutively written for the new settings to take effect, but blank addresses may be skipped or written with any value as needed (when creating a programming sequence). All coefficients can be programmed when the device is in software shutdown, but only the inactive bank can be safely programmed while the playback compensation channel is active.

Table 33 shows the address space where the coefficients for the channel are placed in the device register space.

Table 33. Playback Compensation Channel Biquad Filter Register Addresses

CHANNEL	BANK	START ADDRESS	END ADDRESS
Playback Compensation Channel	A	0x2264	0x232B
	B	0x232C	0x23F3

Table 34 shows how each filter band and coefficient is structured in the register space for the playback compensation channel bank A.

Table 34. Playback Compensation Channel Biquad Filter Bank A Coefficient Register Addresses

FILTER BAND	FILTER COEFFICIENT	BLANK REGISTER	BITS [7:0] REGISTER	BITS [15:8] REGISTER	BITS [23:16] REGISTER
1	B0	0x2264	0x2265	0x2266	0x2267
	B1	0x2268	0x2269	0x226A	0x226B
	B2	0x226C	0x226D	0x226E	0x226F
	A1	0x2270	0x2271	0x2272	0x2273
	A2	0x2274	0x2275	0x2276	0x2277
2	B0	0x2278	0x2279	0x227A	0x227B
	B1	0x227C	0x227D	0x227E	0x227F
	B2	0x2280	0x2281	0x2282	0x2283
	A1	0x2284	0x2285	0x2286	0x2287
	A2	0x2288	0x2289	0x228A	0x228B
3	B0	0x228C	0x228D	0x228E	0x228F
	B1	0x2290	0x2291	0x2292	0x2293
	B2	0x2294	0x2295	0x2296	0x2297
	A1	0x2298	0x2299	0x229A	0x229B
	A2	0x229C	0x229D	0x229E	0x229F
4	B0	0x22A0	0x22A1	0x22A2	0x22A3
	B1	0x22A4	0x22A5	0x22A6	0x22A7
	B2	0x22A8	0x22A9	0x22AA	0x22AB
	A1	0x22AC	0x22AD	0x22AE	0x22AF
	A2	0x22B0	0x22B1	0x22B2	0x22B3
5	B0	0x22B4	0x22B5	0x22B6	0x22B7
	B1	0x22B8	0x22B9	0x22BA	0x22BB
	B2	0x22BC	0x22BD	0x22BE	0x22BF
	A1	0x22C0	0x22C1	0x22C2	0x22C3
	A2	0x22C4	0x22C5	0x22C6	0x22C7
6	B0	0x22C8	0x22C9	0x22CA	0x22CB
	B1	0x22CC	0x22CD	0x22CE	0x22CF
	B2	0x22D0	0x22D1	0x22D2	0x22D3
	A1	0x22D4	0x22D5	0x22D6	0x22D7
	A2	0x22D8	0x22D9	0x22DA	0x22DB
7	B0	0x22DC	0x22DD	0x22DE	0x22DF
	B1	0x22E0	0x22E1	0x22E2	0x22E3
	B2	0x22E4	0x22E5	0x22E6	0x22E7
	A1	0x22E8	0x22E9	0x22EA	0x22EB
	A2	0x22EC	0x22ED	0x22EE	0x22EF

Table 34. Playback Compensation Channel Biquad Filter Bank A Coefficient Register Addresses (continued)

FILTER BAND	FILTER COEFFICIENT	BLANK REGISTER	BITS [7:0] REGISTER	BITS [15:8] REGISTER	BITS [23:16] REGISTER
8	B0	0x22F0	0x22F1	0x22F2	0x22F3
	B1	0x22F4	0x22F5	0x22F6	0x22F7
	B2	0x22F8	0x22F9	0x22FA	0x22FB
	A1	0x22FC	0x22FD	0x22FE	0x22FF
	A2	0x2300	0x2301	0x2302	0x2303
9	B0	0x2304	0x2305	0x2306	0x2307
	B1	0x2308	0x2309	0x230A	0x230B
	B2	0x230C	0x230D	0x230E	0x230F
	A1	0x2310	0x2311	0x2312	0x2313
	A2	0x2314	0x2315	0x2316	0x2317
10	B0	0x2318	0x2319	0x231A	0x231B
	B1	0x231C	0x231D	0x231E	0x231F
	B2	0x2320	0x2321	0x2322	0x2323
	A1	0x2324	0x2325	0x2326	0x2327
	A2	0x2328	0x2329	0x232A	0x232B

Table 35 shows how each filter band and coefficient is structured in the register space for the playback compensation channel bank B.

Table 35. Playback Compensation Channel Biquad Filter Bank B Coefficient Register Addresses

FILTER BAND	FILTER COEFFICIENT	BLANK REGISTER	BITS [7:0] REGISTER	BITS [15:8] REGISTER	BITS [23:16] REGISTER
1	B0	0x232C	0x232D	0x232E	0x232F
	B1	0x2330	0x2331	0x2332	0x2333
	B2	0x2334	0x2335	0x2336	0x2337
	A1	0x2338	0x2339	0x233A	0x233B
	A2	0x233C	0x233D	0x233E	0x233F
2	B0	0x2340	0x2341	0x2342	0x2343
	B1	0x2344	0x2345	0x2346	0x2347
	B2	0x2348	0x2349	0x234A	0x234B
	A1	0x234C	0x234D	0x234E	0x234F
	A2	0x2350	0x2351	0x2352	0x2353
3	B0	0x2354	0x2355	0x2356	0x2357
	B1	0x2358	0x2359	0x235A	0x235B
	B2	0x235C	0x235D	0x235E	0x235F
	A1	0x2360	0x2361	0x2362	0x2363
	A2	0x2364	0x2365	0x2366	0x2367
4	B0	0x2368	0x2369	0x236A	0x236B
	B1	0x236C	0x236D	0x236E	0x236F
	B2	0x2370	0x2371	0x2372	0x2373
	A1	0x2374	0x2375	0x2376	0x2377
	A2	0x2378	0x2379	0x237A	0x237B
5	B0	0x237C	0x237D	0x237E	0x237F
	B1	0x2380	0x2381	0x2382	0x2383
	B2	0x2384	0x2385	0x2386	0x2387
	A1	0x2388	0x2389	0x238A	0x238B
	A2	0x238C	0x238D	0x238E	0x238F
6	B0	0x2390	0x2391	0x2392	0x2393
	B1	0x2394	0x2395	0x2396	0x2397
	B2	0x2398	0x2399	0x239A	0x239B
	A1	0x239C	0x239D	0x239E	0x239F
	A2	0x23A0	0x23A1	0x23A2	0x23A3
7	B0	0x23A4	0x23A5	0x23A6	0x23A7
	B1	0x23A8	0x23A9	0x23AA	0x23AB
	B2	0x23AC	0x23AD	0x23AE	0x23AF
	A1	0x23B0	0x23B1	0x23B2	0x23B3
	A2	0x23B4	0x23B5	0x23B6	0x23B7

Table 35. Playback Compensation Channel Biquad Filter Bank B Coefficient Register Addresses (continued)

FILTER BAND	FILTER COEFFICIENT	BLANK REGISTER	BITS [7:0] REGISTER	BITS [15:8] REGISTER	BITS [23:16] REGISTER
8	B0	0x23B8	0x23B9	0x23BA	0x23BB
	B1	0x23BC	0x23BD	0x23BE	0x23BF
	B2	0x23C0	0x23C1	0x23C2	0x23C3
	A1	0x23C4	0x23C5	0x23C6	0x23C7
	A2	0x23C8	0x23C9	0x23CA	0x23CB
9	B0	0x23CC	0x23CD	0x23CE	0x23CF
	B1	0x23D0	0x23D1	0x23D2	0x23D3
	B2	0x23D4	0x23D5	0x23D6	0x23D7
	A1	0x23D8	0x23D9	0x23DA	0x23DB
	A2	0x23DC	0x23DD	0x23DE	0x23DF
10	B0	0x23E0	0x23E1	0x23E2	0x23E3
	B1	0x23E4	0x23E5	0x23E6	0x23E7
	B2	0x23E8	0x23E9	0x23EA	0x23EB
	A1	0x23EC	0x23ED	0x23EE	0x23EF
	A2	0x23F0	0x23F1	0x23F2	0x23F3

PBC Channel Digital Gain Adjust

The playback compensation channel includes a banked, programmable coarse digital gain adjustment. The channel digital gain adjustment provides a gain range of 0dB to +42dB in 6dB steps, and is programmed individually by bank with the PBC_GAIN_BKA and PBC_GAIN_BKB bit fields. The channel gain adjust is provided for use cases where a large positive gain offset is required, and should not be changed while the respective playback compensation channel bank is active.

PBC Channel Digital Volume Control

The playback compensation channel includes a banked, dynamically programmable digital volume control. The digital volume control provides an attenuation range of 0dB to -31.5dB in 0.5dB steps, and is configured individually by bank with the PBC_VOL_BKA and PBC_VOL_BKB bit fields.

A digital mute is also provided for the playback compensation channel, and is enabled with the PBC_VOL_MUTE bit. The playback compensation mute is in the same register as the low-latency digital filter channel 1 and 2 mute controls (DF1_VOL_MUTE and DF2_VOL_MUTE), and if any of these mute bits are changed simultaneously with a single write command the start of the mute or unmute action (and volume ramp if enabled) is synchronized across the active channels (that are affected by the write).

When enabled, digital volume ramping occurs during playback compensation channel startup, shutdown, volume changes, and digital mute toggling. Channel volume ramping can be dynamically enabled and disabled with the PBC_VOL_RMP_EN bit, however the setting should never be changed while a volume ramp is in progress. When a volume ramp is complete, the device generates the playback compensation ramp done interrupt (PBC_RMP_DONE_*). The duration of a given volume ramp is selected with the PBC_VOL_RMP_RATE bit field. Depending on the type of audio content and the characteristics of the speaker load, selecting faster ramp rates (typically those less than 32ms) or disabling ramping entirely can potentially result in audible glitches during volume changes.

Internal Digital Filter Channel Sequencing

The playback compensation and low-latency digital filter channels can all be either statically enabled (prior to the device exiting software shutdown) or dynamically enabled at any time without disrupting audio playback. To avoid audible glitches on channel enable, it is recommended that the channels should only be enabled (statically or dynamically) with the respective channel mute enabled (PBC_VOL_MUTE, DF1_VOL_MUTE, and DF2_VOL_MUTE respectively). This allows for the channel to power up, for data to propagate, and for the filter response to settle (duration required depends on filter implementation) prior to deactivating the channel mute. The channel mute(s) can be disabled with a single write command to ensure a synchronized response across active channels. The channel(s) then smoothly ramp up into the configured active state without creating an audible glitch.

To avoid audible glitches on channel disable, the appropriate channel mutes should be activated first (with a single write command and with volume ramping enabled). When the volume ramp down is complete, the appropriate channel volume ramp done interrupt(s) (PBC_RMP_DONE_*, DF1_RMP_DONE_*, and/or DF2_RMP_DONE_*) trigger. Once the interrupt (or interrupts) have asserted (or after the configured ramp time has expired), the channel (or channels) can be safely disabled without disrupting playback or causing an audible glitch. If the recommended sequencing is not followed and the digital filter channels are disabled (with volume ramping enabled) without first muting them, then no ramp down occurs, audible glitches are possible, and an erroneous ramp done interrupt can be produced.

Playback Channel Configuration

The playback amplifier channel accepts input data from the PCM interface receiver (DIN). The data is then routed through the playback channel filters and signal processing and is mixed with the playback compensation channel and low-latency digital filter channels before reaching the DAC and hybrid class-AB/D headphone amplifier. The output digital data from the end of the playback channel can also be routed back to the PCM interface transmitter through record channel 4.

The playback channel digital stages and amplifier can only be active when the device is in the audio state. The playback channel is enabled and disabled with the playback enable bit (PB_EN). The playback enable can be programmed in either the software shutdown state or dynamically in the audio state, but should not be changed while playback activation or deactivation is in progress. If the PB_EN bit is set high while the device is in the software shutdown state, the playback channel is not enabled until the device transitions to the audio state. Once the playback channel is enabled, the device generates a PB_PWRUP_DONE interrupt event when the channel is active and ready for use.

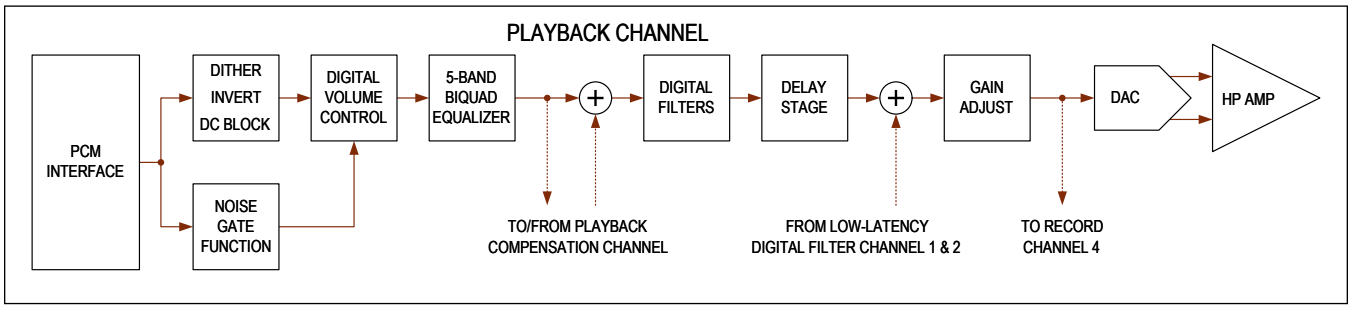


Figure 31. Playback Channel Detailed Block Diagram

Playback Channel Dither

The input data to the playback channel can optionally have dither (±1 LSB peak-to-peak) applied if PB_DITH_EN is set to 1. No dither is applied when PB_DITH_EN is set to 0.

Playback Channel Data Inversion

The input data to the playback channel can optionally be inverted by setting the PB_INVERT bit to 1.

Playback Channel DC Blocking Filter

A DC blocking filter can be enabled on the playback channel by setting the PB_DCBLK_EN bit to 1. The DC blocking filter corner frequency is selected with the PB_DCBLK bit field. The corner frequency scales with the playback sample rate from 8kHz to 48kHz, and is constant for sample rates above 48kHz. The higher corner frequency setting reduces audio band flatness but results in faster settling times for playback channel enable.

Playback Channel Digital Volume Control

The playback channel includes a dynamically programmable digital volume control. The digital volume control provides an attenuation range of 0dB to -63.5dB in 0.5dB steps, and is configured with the PB_VOL bit field. A digital mute is also provided and is enabled with the PB_VOL_MUTE bit.

When enabled, digital volume ramping occurs during playback channel startup, shutdown, volume changes, and digital mute toggling. Playback volume ramping can be dynamically enabled and disabled with the playback volume ramping enable bit (PB_VOL_RMP_EN), however the setting should never be changed while a volume ramp is in progress. When a volume ramp is complete, the device generates a playback ramp done interrupt (PB_RMP_DONE_*). When volume ramping is enabled, the playback turn-on and turn-off times are extended based on the configured playback volume ramp rates.

The duration of a given playback volume ramp is selected with the PB_VOL_RMP_RATE bit field. The only exception is for playback channel shutdown, where the shutdown volume ramp duration is instead selected with the PB_SHDN_RMP_RATE bit field. Depending on the type of audio content and the characteristics of the speaker load, selecting faster ramp rates (typically those less than 32ms) or disabling ramping entirely can potentially result in audible glitches during volume changes.

Playback Channel 5-Band Equalizer

The playback channel features a 5-band equalizer where each band is a full, individually programmable digital biquad filter. The biquad equalizer can be configured with the PB_BQ_EN bit field to have 0 to 5 bands active, and inactive bands do not consume additional quiescent power. The gain (A), quality factor (Q), and frequency (f_0) limitations by equalizer band vary by implemented filter type, and are described in the *Electrical Characteristics Table*.

The transfer function for each equalizer band is defined as:

$$H(z) = \frac{\left(B_0 + B_1 \times Z^{-1} + B_2 \times Z^{-2}\right)}{\left(A_0 + A_1 \times Z^{-1} + A_2 \times Z^{-2}\right)}$$

The biquad filter in each equalizer band has five user-programmable coefficients (B0, B1, B2, A1, and A2 with A0 fixed at 1), and each individual coefficient is 3 bytes (24 bits) long. Each set of three registers (per coefficient) must be programmed consecutively for the settings to take effect. The coefficients are stored using a signed two's complement format where the first 2 bits are the integer portion and the last 22 bits are the decimal portion (which results in an approximate +2 to -2 range for each coefficient). This coefficient range and resolution allows for the implementation of several common filter types including peaking filters, high and low pass filters, and high and low shelving filters. The 2.22 format is a fixed point coefficient implementation that results in some range and resolution boundary limits for filter parameters (see the Biquad Filter Characteristics in the *Electrical Characteristics Table*).

The playback biquad equalizer coefficient register bits are uninitialized when the device first powers up, and the coefficients for any given biquad band should be fully programmed before being enabled. The biquad filter coefficients can be freely written and read back when the device is in software shutdown (AUDIO_EN = 0) or when playback is disabled (PB_EN = 0). However, once the playback biquad equalizer is enabled only inactive bands can be safely written. Readback is restricted by playback enable, and attempting to read back the coefficients while the playback channel is enabled and active may return all zero values.

Playback Channel Equalizer Coefficient Registers

The playback channel contains a 5-band biquad filter for playback response equalization. The register structure for each band (and the 5 coefficients within each) is identical and repeated.

The coefficients in each band are sequentially placed in the same order in the register map (B0, B1, B2, A1, A2) for a total of 20 addresses per filter band. Within this structure, each coefficient spans four addresses, the first of which is blank followed by the three addresses that make up the 24-bit coefficient (lowest bits, middle bits, and highest bits in order). Coefficient segments must be consecutively written for the new settings to take effect, but blank addresses may be skipped or written with any value as needed (when creating a programming sequence). The coefficients should only be programmed when the device is in software shutdown or when the playback channel equalizer is completely disabled.

Table 36 shows how each playback equalizer band and the coefficients are structured in the register space.

Table 36. Playback Channel Equalizer Coefficient Register Addresses

FILTER BAND	FILTER COEFFICIENT	BLANK REGISTER	BITS [7:0] REGISTER	BITS [15:8] REGISTER	BITS [23:16] REGISTER
1	B0	0x2200	0x2201	0x2202	0x2203
	B1	0x2204	0x2205	0x2206	0x2207
	B2	0x2208	0x2209	0x220A	0x220B
	A1	0x220C	0x220D	0x220E	0x220F
	A2	0x2210	0x2211	0x2212	0x2213
2	B0	0x2214	0x2215	0x2216	0x2217
	B1	0x2218	0x2219	0x221A	0x221B
	B2	0x221C	0x221D	0x221E	0x221F
	A1	0x2220	0x2221	0x2222	0x2223
	A2	0x2224	0x2225	0x2226	0x2227
3	B0	0x2228	0x2229	0x222A	0x222B
	B1	0x222C	0x222D	0x222E	0x222F
	B2	0x2230	0x2231	0x2232	0x2233
	A1	0x2234	0x2235	0x2236	0x2237
	A2	0x2238	0x2239	0x223A	0x223B
4	B0	0x223C	0x223D	0x223E	0x223F
	B1	0x2240	0x2241	0x2242	0x2243
	B2	0x2244	0x2245	0x2246	0x2247
	A1	0x2248	0x2249	0x224A	0x224B
	A2	0x224C	0x224D	0x224E	0x224F
5	B0	0x2250	0x2251	0x2252	0x2253
	B1	0x2254	0x2255	0x2256	0x2257
	B2	0x2258	0x2259	0x225A	0x225B
	A1	0x225C	0x225D	0x225E	0x225F
	A2	0x2260	0x2261	0x2262	0x2263

Playback Channel Delay Stage

The playback channel programmable delay stage can add 0 to 7 samples of delay to the playback channel, and is configured with the PB_DELAY bit field. The playback delay stage is positioned after the first stage of playback channel interpolation filters, and as a result, delay in terms of number of samples is at a 384kHz sample rate (regardless of the selected PCM playback channel sample rate).

Playback Channel Digital Gain Adjust

The playback channel includes a programmable digital gain adjustment that is positioned at the end of the playback channel DSP. The playback channel digital gain adjustment is configured with the PB_GAIN bit field, and provides a range of -6dB to +6dB in 0.25dB steps. The digital gain is provided to allow for adjustment of the playback channel full-scale output (for example to compensate for the sensitivity of the attached headphone transducer). The selected digital gain level should not be changed while the playback channel is active.

Playback Channel Wide Band Mode

For sample rates above 48kHz, the playback channel bandwidth is normally limited by the digital filters to approximately 20kHz. However, if the PB_HBW_EN bit is set high, playback high bandwidth mode is enabled and the playback channel bandwidth is extended to approximately 40kHz. This mode can result in increased quiescent power consumption due to additional out of band energy at the playback amplifier output.

Playback Channel Digital Headroom Adjustment

The headroom of the digital sections of the playback channel and playback compensation channel can be increased with the PB_HR_SEL bit field. Selecting higher digital headroom reduces the overall data channel resolution (truncates lower bits), but can be used to prevent clipping in the intermediate digital processing and filter stages. If the total signal response is still above the full-scale output (at the point where the digital filter channels are summed into the playback channel), then playback channel digital clipping may still occur.

Playback Channel Noise Gate

The playback channel noise gate function is enabled when the device is in the audio state and the noise gate enable (PB_NG_EN) is set to 1. When the noise gate is enabled, the noise gate begins activation whenever the amplitude of the input audio data to the playback channel (from the PCM interface) is below the configured noise gate mute threshold (PB_NG_MUTE_THRESH) for more than 1024 consecutive data samples. Noise gate activation is not instant, as it must first ramp down the playback channel (and playback compensation channel) into a digital mute state and wait for signal propagation before idling in a reduced power state. The amplifier output remains active however, and data (such as ambient or anti-noise signals) from the low-latency digital filter channels is still played back.

The playback noise gate deactivates immediately if the amplitude of even a single playback channel input audio data sample exceeds the configured unmute threshold (PB_NG_UNMUTE_THRESH). When the noise gate deactivates, the playback channel (and playback compensation channel) is unmuted and returns to normal operation before the input audio data (that triggered deactivation) reaches the output.

The noise gate mute and unmute threshold settings are selected in terms of the number of bits (starting from the LSB) that must be toggling (or active) in order for the input signal amplitude to exceed the thresholds. It is invalid to set the noise gate unmute threshold such that it is less than the configured mute threshold. The location of the audio data LSB within the PCM input data channel is determined by the configured PCM data word size (PCM_CHANSZ). The supported combinations are shown in Table 37.

Table 37. Noise Gate Threshold LSB Location

INPUT DATA WORD SIZE	NOISE GATE FUNCTION LSB LOCATION
16	16
24	24
32	

Playback Amplifier

The playback channel features a fully differential hybrid Class-AB/Class-D mode amplifier output stage. To minimize quiescent power and maximize output efficiency, the device monitors the playback signal level and then (based on the selected amplifier configuration) selects the optimal amplifier operating mode, reference supply level, and gain structure. If no faults are present, the playback amplifier is enabled whenever the playback channel is enabled (PB_EN bit) and the device is in the audio state (AUDIO_EN bit).

By default, the playback amplifier operates in high-performance mode. For use cases where minimizing quiescent power consumption is critical, the amplifier can be configured to operate in low-power mode by setting the PB_POWER_MODE bit to 0 (prior to enabling playback). Low-power mode operation marginally increases playback amplifier THD+N and output noise.

Playback Amplifier Mode Configuration

Based on the playback signal level, the device automatically determines whether the amplifier output operates in class-AB mode or class-D mode. When the input signal level is small, the amplifier output operates in class-AB mode from the AVDD2 (1.2V) supply. Class-AB mode operation minimizes quiescent power consumption and the output noise level.

As the signal level increases, the amplifier output transitions to class-D mode operation to maximize efficiency. Once the amplifier output is in class-D mode, the device continues to monitor the playback signal level. To avoid clipping, by default the amplifier output automatically selects whether to operate from the lower power AVDD3 (1.2V) supply or the high swing AVDD1 (1.8V) supply. Alternatively, if the PB_AMP_MODE bit is set to 0x1 (prior to enabling playback) when the amplifier output is operating in class-D mode, it is restricted to using the lower power AVDD3 (1.2V) supply. This limits the amplifier full-scale output swing, but optimizes amplifier efficiency and limits peak output noise levels.

Table 38. Playback Amplifier Output Operating Mode and Supply Configuration

SIGNAL LEVEL	LESS THAN -30dBFS	-30dBFS TO -5dBFS	GREATER THAN -5dBFS
PB_AMP_MODE = 0x0	Class-AB Mode (AVDD2)	Class-D Mode (AVDD3)	Class-D Mode (AVDD1)
PB_AMP_MODE = 0x1	Class-AB Mode (AVDD2)	Class-D Mode (AVDD3)	Class-D Mode (AVDD3)

Playback Amplifier Class-D Mode Settings

For typical headphone loads placed near the playback amplifier, the amplifier output does not require the use of external LC filters or shielding to meet electromagnetic-interference (EMI) regulation standards. In addition, the playback amplifier supports two slightly different class-D mode output switching frequencies (PB_AMP_PWM_SEL). The secondary switching frequency setting can be used in cases where the default switching frequency could potentially result in system level interference.

The device also features emissions limiting circuitry that reduces the output switching harmonics that can directly contribute to EMI and radiated emissions. The programmable playback amplifier slew rate control bits are used to adjust the class-D mode output switching edge rate. Faster slew rates can slightly improve the amplifier performance and efficiency, while reducing the slew rate decreases active emissions. The playback amplifier rising edge slew rate is selected with the PB_AMP_SLEW_RISE bit field and the falling edge slew rate is selected with the PB_AMP_SLEW_FALL bit field.

The playback amplifier output also supports spread spectrum modulation (SSM). SSM is enabled with the PB_AMP_SSM_EN bit, and when active it optimizes the suppression and control of the output switching harmonics that can contribute to EMI and radiated emissions. The clock period variation in spread-spectrum mode is controlled by the PB_AMP_SSM_VAL bit field. Higher clock period variation settings spread out-of-band energy across a wider bandwidth. Above 10MHz, the wideband spectrum looks like noise for EMI purposes.

Playback Amplifier Overcurrent Limit Protection

The amplifier features overcurrent protection (OCP) monitoring that can protect the amplifier output from both high current and short circuit events (OUTP/OUTN shorted to AVDD1/2/3, AGND, or each other).

If the PB_AMP_OCP_AUTORESTART_EN bit is set to 1, the device is in automatic overcurrent protection (OCP) mode. In auto mode, if the amplifier output current exceeds the current limit threshold (120mA), the device generates an AMP_OCP_* interrupt and disables the amplifier output internally (without changing the control bit states). After the OCP restart time (t_{OCP_RETRY}), the amplifier output is automatically re-enabled. If the overcurrent condition still exists, the device continues to disable and re-enable the amplifier output automatically until the fault condition is removed. This could continue indefinitely if the fault condition persists and the software driver does not intervene. The values of PB_EN and AUDIO_EN (or any other control bit field) are not changed in auto OVC mode and remain in their previous states throughout the process.

If the PB_AMP_OCP_AUTORESTART_EN bit is set to 0, the device is in manual OCP mode. In manual mode, if an amplifier overcurrent event occurs, the device generates an AMP_OCP_* interrupt, disables the amplifier output, and disables the amplifier by setting the PB_EN bit to 0. As a result, the host must manually re-enable the amplifier output (PB_EN bit) after an overcurrent event.

Clock and Data Monitors

The device provides input data and external clock monitors that detect host and system level faults. The data monitor detects persistent stuck and high amplitude input signals, while the clock monitor detects external clock failures and invalid clock configurations.

Clock Monitor

The device provides an optional clock monitor that is enabled by setting CMON_EN to 1. Once enabled, it actively monitors the input BCLK and LRCLK anytime the device exits software shutdown (AUDIO_EN = 1). When active, the clock monitor detects clock activity, clock frequency, and frame timing (clock ratio). If faults are detected, the clock monitor automatically places the device into software shutdown and generates a clock error interrupt (CLOCK_ERR_*).

The clock monitor operates in automatic mode when CMON_AUTORESTART_EN = 1 and manual mode when CMON_AUTORESTART_EN = 0. Manual mode may be used with any device configuration (any combination of record, playback, and internal digital filter channels). However, automatic mode is only recommended for use with either playback only or playback with internal digital filter channel use cases (and not with any use cases that include active record channels to the host).

Table 39. Recommended Clock Monitor Modes

USE CASE ENABLED CHANNELS	RECOMMENDED CLOCK MONITOR MODE
Playback Channel	Manual or Automatic Mode
Digital Filter Channels 1/2	Manual or Automatic Mode
Record Channels 1/2/3	Manual Mode

In automatic mode, when a clock error places the device into software shutdown, the audio enable bit is not changed (AUDIO_EN remains 1), and the device automatically recovers from all clock errors. In automatic mode, both clock error (CLOCK_ERR_*) and clock recovery (CLOCK_REC_*) interrupts are generated in pairs (a clock recovery interrupt is not possible until after clock errors have occurred, and all clock errors have recovered).

In manual mode, when a clock error places the device into software shutdown, the audio enable bit (AUDIO_EN) is set to 0. Clock recovery (CLK_REC_*) interrupts are never generated in manual mode, and the device remains in software shutdown until the host sets AUDIO_EN back to 1. Once the device is re-enabled (AUDIO_EN set to 1 with one or more audio channel enabled), the clock monitor is reactivated and detects any new (or persisting) clock errors. If a clock error is detected, the device returns to software shutdown (AUDIO_EN = 0), and a new clock error interrupt (CLOCK_ERR_*) is generated.

Clock errors are fault conditions, and audible glitches may occur on clock monitor based transitions into and out of software shutdown. When the clock monitor is enabled, no false clock error or clock recovery interrupts are generated when the host software transitions the device normally into and out of software shutdown.

Clock Activity and Frequency Detection

When the clock monitor is enabled, the bit clock (BCLK) and frame clock (LRCLK) frequencies are monitored. The expected LRCLK frequency is equal to the PCM sample rate (PCM_SR). The expected BCLK frequency is based on the BCLK to LRCLK ratio (PCM_BSEL) relative to the PCM sample rate (PCM_SR).

The current frequency of each clock is measured relative to (and once per interval of) the programmed frame period (as set by PCM_SR). A clock frequency error is detected when the measured clock frequencies differ from programmed clock frequencies (faster or slower) by more than the frequency error threshold (45% typical). If either clock stops high or low, the frequency measurement result allows detection of the clock stop event.

The CMON_ERRTOL bit field sets the clock frequency error tolerance. The tolerance is the required number of consecutive frame clock periods (PCM_PB_SR) with an incorrect clock frequency before a clock error is generated. If the error persists for the selected number of frame periods, a clock error interrupt (CLOCK_ERR_*) is generated, and the device is placed into software shutdown.

In automatic mode, the CMON_ERRTOL bit field also sets the number of consecutive correct frame clock periods (with no clock frequency errors) that are required for error recovery before automatic restart occurs. Once the selected number of consecutive error free frames are detected, the clock error is cleared. Once all clock errors are cleared, a clock recovery interrupt (CLOCK_REC_*) is generated and the device automatically exits software shutdown.

In manual mode, no clock recovery interrupts are generated. The clock monitor remains disabled and the device remains in software shutdown until the host software sets AUDIO_EN back to 1.

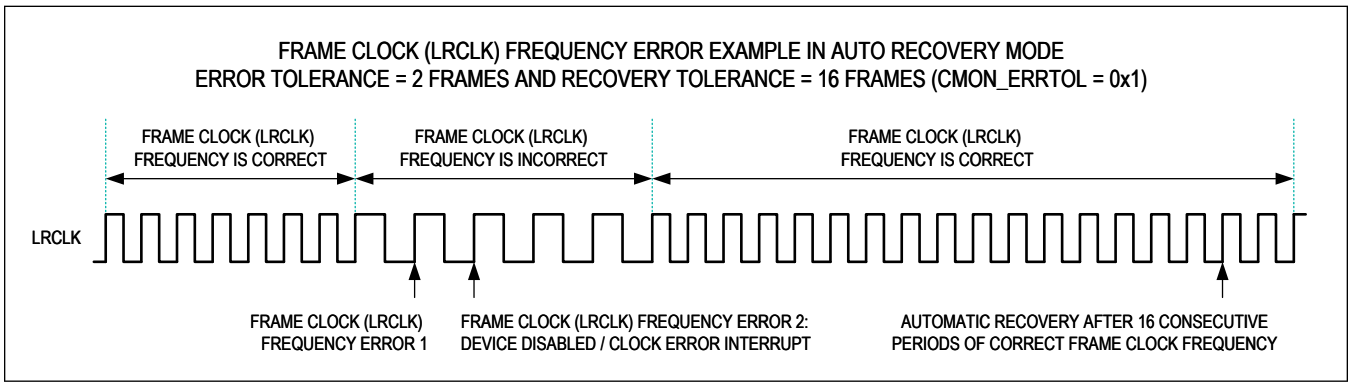


Figure 32. Clock Monitor Frame Clock (LRCLK) Frequency Error Example with CMON_ERRTOL = 0x1

Clock Frame Error Detection

When the clock monitor is enabled, the bit clock (BCLK) to frame clock (LRCLK) ratio is monitored. The clock monitor counts the number of BCLK periods per frame (LRCLK period), and then compares the count to the configured clock ratio (PCM_BSEL). In addition, in I^2S and left-justified (LJ) modes the clock monitor verifies the LRCLK duty cycle by checking that the number of BCLK periods per channel is equal. In TDM mode, data transport is synchronized to the active frame clock (LRCLK) edge, so no duty cycle restrictions are enforced (only the clock ratio is monitored).

A frame error is detected in each frame where the monitored bit clock (BCLK) to frame clock (LRCLK) ratio (and duty cycle in I^2S and LJ Modes) differs from the configured settings. The CMON_BSELTOL bit field sets the number of consecutive frames with frame errors that are required before a clock error interrupt (CLOCK_ERR_*) is generated and the device is placed into software shutdown.

In automatic mode, the CMON_BSELTOL bit field also sets the number of consecutive frames (with no frame errors) that are required for the frame error to recover (so automatic restart can occur). Once the selected number of consecutive error free frames are detected, the frame error recovers, a clock recover interrupt (CLOCK_REC_*) is generated (if all clock errors have been cleared), and the device automatically exits software shutdown.

In manual mode, no clock recovery interrupts are generated. The clock monitor remains disabled and the device remains in software shutdown until the host software sets AUDIO_EN back to 1.

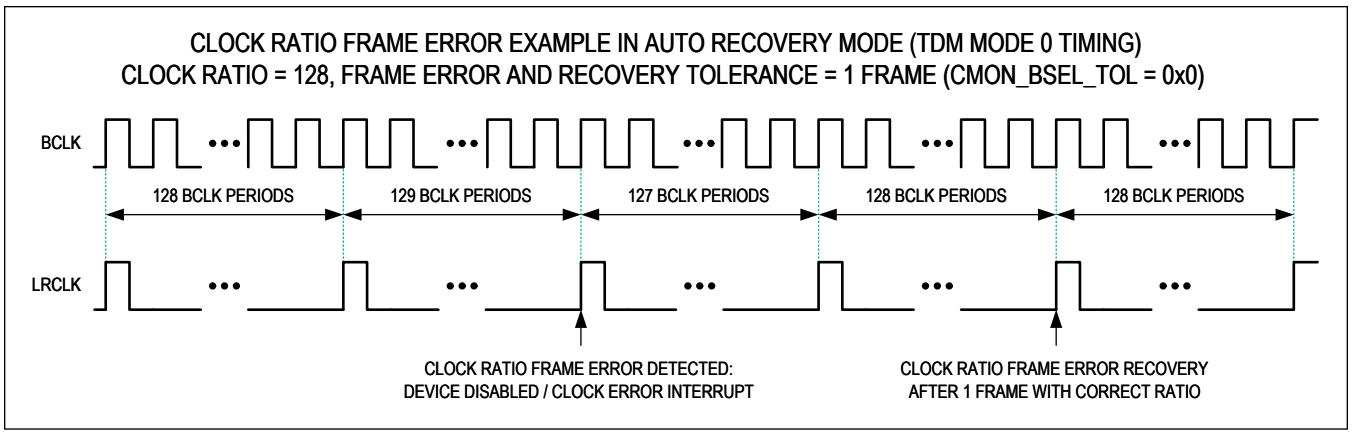


Figure 33. Clock Monitor Clock Ratio Frame Error Example with TDM Mode 0 Timing

Input Data Monitor

The device provides an optional input data monitor that is enabled by setting the DMON_MAG_EN bit to 1 (for the data magnitude monitor) and the DMON_STUCK_EN bit to 1 (for the data stuck monitor). When at least one data monitor function is enabled, it actively monitors the selected input data channel (from DIN) to the playback channel whenever the device exits software shutdown (AUDIO_EN = 1) and playback is enabled (PB_EN = 1).

When active, the data monitor checks the input playback data for the enabled data error types (data magnitude, data stuck, or both). The DMON_DURATION bit field selects the duration that a data stuck or magnitude error must persist for before a data error is detected. Once a data error is detected, the data monitor automatically places the device into software shutdown (sets AUDIO_EN to 0) and generates a data monitor error interrupt (DMON_ERR_*).

Data errors are fault conditions, and audible glitches may occur on data monitor based transitions into and out of software shutdown. When the data monitor is enabled, no false data error interrupts (DATA_ERR_*) are generated when the host software transitions the device normally into and out of software shutdown.

Data Stuck Error Detection

A data stuck error is detected if the input signal repeats a fixed value with a magnitude (positive or negative) that is beyond the data stuck threshold (DMON_STUCK_THRES) for longer than the data error duration (DMON_DURATION). If the input signal repeats a fixed value for any duration with a magnitude that is within the data stuck threshold limits (such as a zero or near zero code), no data stuck error is detected.

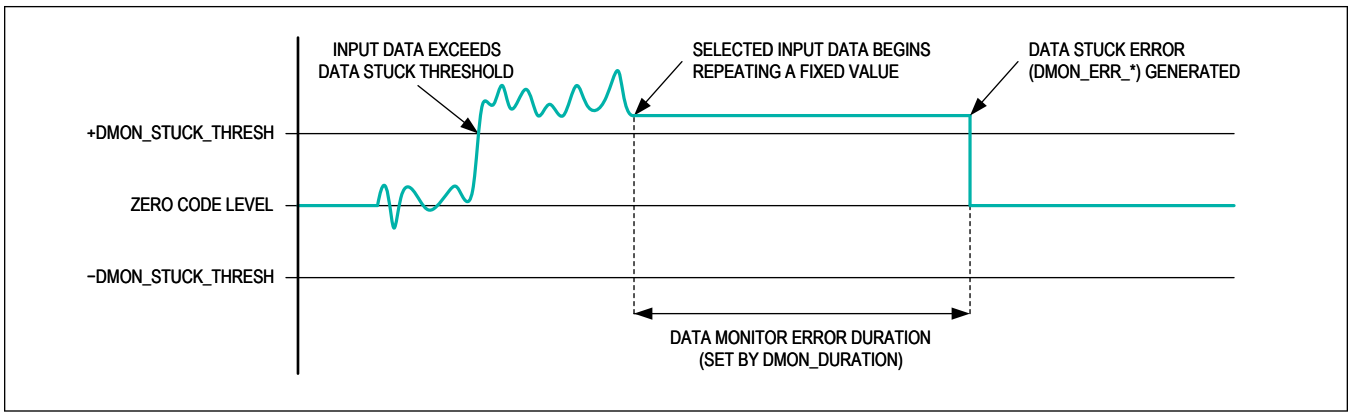


Figure 34. Data Monitor Error Generation Due to Input Data Stuck Error Detection

Data Magnitude Error Detection

A data magnitude error is detected if the input signal magnitude (positive or negative) is beyond the data magnitude threshold (set by DMON_MAG_THRES) for longer than the data error duration (set by DMON_DURATION).

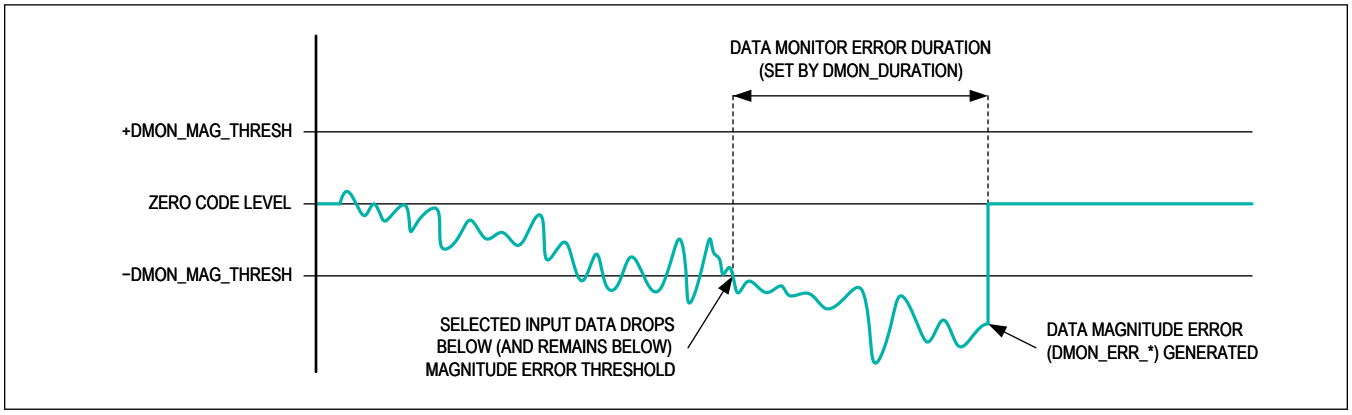


Figure 35. Data Monitor Error Generation Due to Input Data Magnitude Error Detection

Device and Revision Identification Number

The device provides two registers that contain the device identification number (DEV_ID). The device identification number is equivalent to the last 4 digits in the device part number (0x8050).

The device also provides a register containing the device revision identification number (REV_ID). The revision identification number reflects the current physical hardware version, and is updated with any hardware revision. The current revision identification number is 0x41.

Device Register Map Description

Register bit fields come in several varieties that are summarized in Table 40.

Table 40. Control Register Map Bit Field Types

Bit Field Type	Functional Description
Read-Only Bit Field	Writes to read-only bit fields have no effect.
Write-Only Bit Field	Write 1 to activate. Writing 0 has no effect. Readback always returns 0.
Read/Write Bit Field	Read and write these bit fields normally (May have write access restrictions)

Read-only bit fields (R) are used to indicate an internal device state, and cannot be changed directly by the host. Writing to these registers has no effect.

Write-only bit fields (W) are single-bit push-button controls. Writing a 1 to these bit fields performs an action (i.e., software reset, interrupt clear, etc.). Writing a 0 has no effect, and a read back always returns a 0.

Read/Write bit fields (RW) can be both read and written by the host, and the last written value is the value returned on readback.

Reserved bit fields are not used to program or control the device. When writing a register that contains reserved bit fields, always write a 0 to the reserved bit field segments.

Control Bit Write Access Restrictions

The device control bits fall into one of three basic types: read (R), write (W), or read and write (RW). There are no direct read restrictions (though some biquad filter coefficients may return zeroes if read when active), and any read enabled bit field can be read back anytime the I²C control interface is active. There are however write restrictions, and every write enabled bit field falls into one of two write access subtypes.

The first write access subtype is dynamic. Dynamic bit fields effectively have no write access restrictions, and can be safely changed (written) in any device state where the I²C control interface is active. The second bit field access subtype is restricted. Restricted bit fields should only be changed (written) when the related functional block (as shown in Table 41) is powered down. If the write access is restricted to the global enable (restriction EN), then the restricted bit field should only be changed (written) when the device is in software shutdown.

The bit field type and write access subtype is provided for every bit field in the detailed register description tables. For all bit fields with the restricted subtype, the dependency is also denoted in the "RES" column.

Table 41 provides a detailed description of all device register types, access subtypes, and restriction dependencies that are used by this device. The write access restrictions describe the specific device condition(s) that should be met (and the corresponding bit field settings) before the system attempts to change (write to) bit fields with that restriction type.

Table 41. Control Bit Types and Write Access Restrictions

REGISTER TYPE	WRITE ACCESS	WRITE ACCESS RESTRICTIONS		"RES" SYMBOL
		DESCRIPTION	CONDITION	
Read	Read-Only	None	—	—
Write or Write/Read	Dynamic	None	—	—
	Restricted	Device Held in Software Shutdown	AUDIO_EN = 0	EN
		IRQ Output Disabled	IRQ_EN = 0	IRQ
		PCM Interface Disabled	PCM_TX_EN = 0 and PCM_RX_EN = 0	PCM
		Playback Channel Disabled	PB_EN = 0	PB
		Record Channel **n** Disabled	Respective RECn_EN = 0	RECn
		Analog Microphone Input **n** Disabled	Respective AMICn_EN = 0	AMICn
		Analog Microphone Bias Disabled	AMIC_BIAS_EN = 0	MBIAS
		All Digital Microphone Interfaces Disabled	ALL 3 DMICn_EN = 0	DMIC
		Digital Filter Channel 1 Disabled	DF1_EN = 0	DF1
		Digital Filter Channel 2 Disabled	DF2_EN = 0	DF2
		Both Digital Filter Channels Disabled	DF1_EN = 0 and DF2_EN = 0	DF
		Playback Compensation Channel Disabled	PBC_EN = 0	PBC

Register Map

User Control Registers

ADDRESS	NAME	MSB							LSB
SOFTWARE RESET REGISTER									
0x2000	Software Reset[7:0]	–	–	–	–	–	–	–	RST
INTERRUPT GENERATION CONTROL REGISTERS									
0x2001	Interrupt Raw 1[7:0]	INIT_DONE_RAW	OTP_FAIL_RAW	PWRDN_DONE_RAW	PB_PWRUP_DONE_RAW	REC_PWRUP_DONE_RAW	CLOCK_ERR_RAW	CLOCK_REC_RAW	DATA_ERR_RAW
0x2002	Interrupt Raw 2[7:0]	FLL_ERR_RAW	I2C_GW_DONE_RAW	–	AMP_OCP_RAW	PBC_RMP_DONE_RAW	DF2_RMP_DONE_RAW	DF1_RMP_DONE_RAW	PB_RMP_DONE_RAW
0x2003	Interrupt State 1[7:0]	INIT_DONE_STATE	OTP_FAIL_STATE	PWRDN_DONE_STATE	PB_PWRUP_DONE_STATE	REC_PWRUP_DONE_STATE	CLOCK_ERR_STATE	CLOCK_REC_STATE	DATA_ERR_STATE
0x2004	Interrupt State 2[7:0]	FLL_ERR_STATE	I2C_GW_DONE_STATE	–	AMP_OCP_STATE	PBC_RMP_DONE_STATE	DF2_RMP_DONE_STATE	DF1_RMP_DONE_STATE	PB_RMP_DONE_STATE
0x2005	Interrupt Flag 1[7:0]	INIT_DONE_FLAG	OTP_FAIL_FLAG	PWRDN_DONE_FLAG	PB_PWRUP_DONE_FLAG	REC_PWRUP_DONE_FLAG	CLOCK_ERR_FLAG	CLOCK_REC_FLAG	DATA_ERR_FLAG
0x2006	Interrupt Flag 2[7:0]	FLL_ERR_FLAG	I2C_GW_DONE_FLAG	–	AMP_OCP_FLAG	PBC_RMP_DONE_FLAG	DF2_RMP_DONE_FLAG	DF1_RMP_DONE_FLAG	PB_RMP_DONE_FLAG
0x2007	Interrupt Enable 1[7:0]	INIT_DONE_EN	OTP_FAIL_EN	PWRDN_DONE_EN	PB_PWRUP_DONE_EN	REC_PWRUP_DONE_EN	CLOCK_ERR_EN	CLOCK_REC_EN	DATA_ERR_EN
0x2008	Interrupt Enable 2[7:0]	FLL_ERR_EN	I2C_GW_DONE_EN	–	AMP_OCP_EN	PBC_RMP_DONE_EN	DF2_RMP_DONE_EN	DF1_RMP_DONE_EN	PB_RMP_DONE_EN
0x2009	Interrupt Clear 1[7:0]	INIT_DONE_CLR	OTP_FAIL_CLR	PWRDN_DONE_CLR	PB_PWRUP_DONE_CLR	REC_PWRUP_DONE_CLR	CLOCK_ERR_CLR	CLOCK_REC_CLR	DATA_ERR_CLR
0x200A	Interrupt Clear 2[7:0]	FLL_ERR_CLR	I2C_GW_DONE_CLR	–	AMP_OCP_CLR	PBC_RMP_DONE_CLR	DF2_RMP_DONE_CLR	DF1_RMP_DONE_CLR	PB_RMP_DONE_CLR
INTERRUPT REQUEST OUTPUT REGISTERS									
0x2012	IRQ Control 1[7:0]	–	–	–	IRQ_DRV[1:0]		IRQ_INT_PU	IRQ_MODE	IRQ_POL
0x2013	IRQ Enable[7:0]	–	–	–	–	–	–	–	IRQ_EN

ADDRESS	NAME	MSB							LSB
I2C SLAVE INTERFACE REGISTERS									
0x2014	I2C Slave Configuration[7:0]	–	–	–	–	–	–	–	I2C_GROUP_ADDR_EN
PCM INTERFACE REGISTERS									
0x2020	PCM Interface Configuration 1[7:0]	–	–	–	PCM_CHANSZ[1:0]		PCM_FORMAT[2:0]		
0x2021	PCM Interface Configuration 2[7:0]	–	–	PCM_CHANSEL	PCM_BCLKEDGE	PCM_BSEL[3:0]			
0x2022	PCM Interface Configuration 3[7:0]	–	PCM_DOUT_DRV[1:0]		PCM_TX_NO_RPT_SAMP	PCM_TX_INTERLEAVE_SEL[1:0]		PCM_TX_INTERLEAVE	PCM_TX_EXTRA_HIZ
0x2024	PCM Sample Rate Configuration[7:0]	PCM_REC_SR[3:0]				PCM_PB_SR[3:0]			
0x2026	PCM Playback Channel Source[7:0]	–	–	–	–	PCM_PB_SOURCE[3:0]			
0x2028	PCM Record Channel 1 Slot Selection[7:0]	–	–	PCM_REC1_SLOT[5:0]					
0x2029	PCM Record Channel 2 Slot Selection[7:0]	–	–	PCM_REC2_SLOT[5:0]					
0x202A	PCM Record Channel 3 Slot Selection[7:0]	–	–	PCM_REC3_SLOT[5:0]					
0x202B	PCM Record Channel 4 Slot Selection[7:0]	–	–	PCM_REC4_SLOT[5:0]					
0x2031	PCM Data Output Tx Hi-Z Control 1[7:0]	PCM_TX_SLOT_HIZ[63:56]							
0x2032	PCM Data Output Tx Hi-Z Control 2[7:0]	PCM_TX_SLOT_HIZ[55:48]							
0x2033	PCM Data Output Tx Hi-Z Control 3[7:0]	PCM_TX_SLOT_HIZ[47:40]							
0x2034	PCM Data Output Tx Hi-Z Control 4[7:0]	PCM_TX_SLOT_HIZ[39:32]							
0x2035	PCM Data Output Tx Hi-Z Control 5[7:0]	PCM_TX_SLOT_HIZ[31:24]							
0x2036	PCM Data Output Tx Hi-Z Control 6[7:0]	PCM_TX_SLOT_HIZ[23:16]							
0x2037	PCM Data Output Tx Hi-Z Control 7[7:0]	PCM_TX_SLOT_HIZ[15:8]							
0x2038	PCM Data Output Tx Hi-Z Control 8[7:0]	PCM_TX_SLOT_HIZ[7:0]							
0x203E	PCM Interface Loop Enables[7:0]	–	–	–	–	–	PCM_LB_DOUT_EN	PCM_PB_LT_EN[1:0]	
0x203F	PCM Interface Enables[7:0]	–	–	–	–	–	–	PCM_TX_EN	PCM_RX_EN

ADDRESS	NAME	MSB							LSB
PLAYBACK CHANNEL CONTROL REGISTERS									
0x2060	Playback Block Configuration 1[7:0]	–	–	PB_POWER_MODE	PB_DITH_EN	PB_INVERT	PB_DCBLK[1:0]		PB_DCBLK_EN
0x2061	Playback Block Configuration 2[7:0]	–	–	PB_HBW_EN	PB_HR_SEL[1:0]		PB_DELAY[2:0]		
0x2062	Playback Biquad Enable[7:0]	–	–	–	–	PB_BQ_EN[3:0]			
0x2063	Playback Gain Correction[7:0]	–	–	PB_GAIN[5:0]					
0x2064	Playback Ramp Rate Configuration[7:0]	PB_SHDN_RMP_RATE[2:0]			PB_VOL_RMP_RATE[3:0]				PB_RMP_EN
0x2065	Playback Volume Control[7:0]	–	PB_VOL[6:0]						
0x2066	Playback Noise Gate Thresholds[7:0]	PB_NG_UNMUTE_THRESH[3:0]				PB_NG_MUTE_THRESH[3:0]			
0x2067	Playback Noise Gate Control[7:0]	–	–	–	–	–	–	–	PB_NG_EN
0x2069	Playback Amplifier Configuration[7:0]	–	PB_AMP_LOAD_OP_BIAS[1:0]		PB_AMP_PWM_SEL	PB_AMP_OCP_AUTORESTART_EN	PB_AMP_MODE[2:0]		
0x206A	Playback Amplifier Falling Slew Rate Controls[7:0]	–	–	–	–	–	–	PB_AMP_SLEW_FALL[1:0]	
0x206B	Playback Amplifier Rising Slew Rate Controls[7:0]	–	–	–	–	–	–	PB_AMP_SLEW_RISE[1:0]	
0x206C	Playback Amplifier SSM Controls[7:0]	–	–	–	–	–	PB_AMP_SSM_VAL[1:0]		PB_AMP_SSM_EN
0x206E	Playback Digital Mute Control[7:0]	–	–	–	–	–	–	–	PB_VOL_MUTE
0x206F	Playback Enable[7:0]	–	–	–	–	–	–	–	PB_EN
DMIC INPUT CONFIGURATION									
0x2075	DMIC Interface Clock Drive Strength Configuration[7:0]	–	–	DMIC3_DRV[1:0]		DMIC2_DRV[1:0]		DMIC1_DRV[1:0]	
0x2076	DMIC Interface Clock Configuration[7:0]	–	–	–	–	–	DMIC_FRAME_SEL	DMIC_RATE[1:0]	
0x2077	DMIC Interface Enables[7:0]	–	–	–	–	–	DMIC3_EN	DMIC2_EN	DMIC1_EN
AMIC INPUT CONFIGURATION									
0x2080	AMIC 1 Configuration 1[7:0]	AMIC1_FAST_CHRG_FORCE	AMIC1_FAST_CHRG_BYPASS	AMIC1_PGA_HIZ_EN	AMIC1_PGA_GAIN[3:0]				AMIC1_PGA_RIN

ADDRESS	NAME	MSB							LSB
0x2081	AMIC 1 Configuration 2[7:0]	–	–	–	–	–	–	AMIC1_DRE_EN	AMIC1_DITH_EN
0x2083	AMIC 2 Configuration 1[7:0]	AMIC2_FAST_CHRG_FORCE	AMIC2_FAST_CHRG_BYPASS	AMIC2_PGA_HIZ_EN	AMIC2_PGA_GAIN[3:0]				AMIC2_PGA_RIN
0x2084	AMIC 2 Configuration 2[7:0]	–	–	–	–	–	–	AMIC2_DRE_EN	AMIC2_DITH_EN
0x2086	AMIC 3 Configuration 1[7:0]	AMIC3_FAST_CHRG_FORCE	AMIC3_FAST_CHRG_BYPASS	AMIC3_PGA_HIZ_EN	AMIC3_PGA_GAIN[3:0]				AMIC3_PGA_RIN
0x2087	AMIC 3 Configuration 2[7:0]	–	–	–	–	–	–	AMIC3_DRE_EN	AMIC3_DITH_EN
0x208A	AMIC Power Down Controls[7:0]	–	–	–	–	–	AMIC3_PD	AMIC2_PD	AMIC1_PD
0x208B	AMIC Bias Configuration[7:0]	–	–	–	AMIC_BIAS_PD_EN	AMIC_BIAS_LP_MODE	AMIC_BIAS_SEL[2:0]		
0x208C	AMIC Bias Output Enables[7:0]	–	–	–	–	–	AMIC_BIAS_OUT3	AMIC_BIAS_OUT2	AMIC_BIAS_EN
0x208D	AMIC Input Configuration[7:0]	–	–	–	–	–	–	AMIC_CT_SEL[1:0]	
0x208E	AMIC Power Mode Select[7:0]	–	–	–	–	–	AMIC3_LP_MODE	AMIC2_LP_MODE	AMIC1_LP_MODE
0x208F	AMIC Enables[7:0]	–	–	–	–	–	AMIC3_EN	AMIC2_EN	AMIC1_EN
RECORD CHANNEL CONTROL REGISTERS									
0x20A0	Record Channel 1 Configuration 1[7:0]	REC1_DELAY[3:0]				REC1_INVERT	REC1_DCBLK[1:0]		REC1_DCBLK_EN
0x20A1	Record Channel 1 Configuration 2[7:0]	REC1_GAIN[4:0]					REC1_SEL[2:0]		
0x20A2	Record Channel 1 Digital Volume Control[7:0]	–	REC1_VOL[6:0]						
0x20A4	Record Channel 2 Configuration 1[7:0]	REC2_DELAY[3:0]				REC2_INVERT	REC2_DCBLK[1:0]		REC2_DCBLK_EN
0x20A5	Record Channel 2 Configuration 2[7:0]	REC2_GAIN[4:0]					REC2_SEL[2:0]		
0x20A6	Record Channel 2 Digital Volume[7:0]	–	REC2_VOL[6:0]						

ADDRESS	NAME	MSB							LSB
0x20A8	Record Channel 3 Configuration 1[7:0]	REC3_DELAY[3:0]				REC3_INVERT	REC3_DCBLK[1:0]		REC3_DCBLK_EN
0x20A9	Record Channel 3 Configuration 2[7:0]	REC3_GAIN[4:0]					REC3_SEL[2:0]		
0x20AA	Record Channel 3 Digital Volume[7:0]	–	REC3_VOL[6:0]						
0x20AC	Record Channel 4 Configuration 1[7:0]	REC4_DELAY[3:0]				REC4_INVERT	–	–	–
0x20AF	Record Channel Enables[7:0]	–	–	–	–	REC4_PCM_EN	REC3_PCM_EN	REC2_PCM_EN	REC1_PCM_EN
LOW LATENCY DIGITAL FILTER CHANNEL CONTROL REGISTERS									
0x20B0	Digital Filter Channel 1 Bank A Configuration[7:0]	–	DF1_GAIN_BKA[2:0]			DF1_BQ_BKA_EN[3:0]			
0x20B1	Digital Filter Channel 1 Bank A Volume[7:0]	–	–	DF1_VOL_BKA[5:0]					
0x20B2	Digital Filter Channel 1 Bank B Configuration[7:0]	–	DF1_GAIN_BKB[2:0]			DF1_BQ_BKB_EN[3:0]			
0x20B3	Digital Filter Channel 1 Bank B Volume[7:0]	–	–	DF1_VOL_BKB[5:0]					
0x20B4	Digital Filter Channel 1 Ramp Configuration[7:0]	–	–	–	DF1_VOL_RMP_RATE[3:0]				DF1_VOL_RMP_EN
0x20B5	Digital Filter Channel 1 Configuration[7:0]	–	–	–	–	DF1_DCBLK[1:0]		DF1_DCBLK_EN	DF1_ULTRA_EN
0x20B8	Digital Filter Channel 1 DRC Attack Configuration 1[7:0]	DF1_DRC_ATK_WF[15:8]							
0x20B9	Digital Filter Channel 1 DRC Attack Configuration 2[7:0]	DF1_DRC_ATK_WF[7:0]							
0x20BA	Digital Filter Channel 1 DRC Release Configuration 1[7:0]	DF1_DRC_RLS_WF[15:8]							
0x20BB	Digital Filter Channel 1 DRC Release Configuration 2[7:0]	DF1_DRC_RLS_WF[7:0]							
0x20BC	Digital Filter Channel 1 DRC Threshold[7:0]	–	–	DF1_DRC_THR[5:0]					
0x20BD	Digital Filter Channel 1 DRC Enable[7:0]	–	–	DF1_DRC_INST_RLS	DF1_DRC_INST_ATK	DF1_DRC_CMP[2:0]			DF1_DRC_EN
0x20C0	Digital Filter Channel 2 Bank A Enable[7:0]	–	DF2_GAIN_BKA[2:0]			DF2_BQ_BKA_EN[3:0]			
0x20C1	Digital Filter Channel 2 Bank A Volume[7:0]	–	–	DF2_VOL_BKA[5:0]					

ADDRESS	NAME	MSB							LSB
0x20C2	Digital Filter Channel 2 Biquad Bank B Enable[7:0]	–	DF2_GAIN_BKB[2:0]			DF2_BQ_BKB_EN[3:0]			
0x20C3	Digital Filter Channel 2 Bank B Volume[7:0]	–	–	DF2_VOL_BKB[5:0]					
0x20C4	Digital Filter Channel 2 Ramp Configuration[7:0]	–	–	–	DF2_VOL_RMP_RATE[3:0]				DF2_VOL_RMP_EN
0x20C5	Digital Filter Channel 2 Configuration[7:0]	–	–	–	–	DF2_DCBLK[1:0]		DF2_DCBLK_EN	DF2_ULTRA_EN
0x20C8	Digital Filter Channel 2 DRC Attack Configuration 1[7:0]	DF2_DRC_ATK_WF[15:8]							
0x20C9	Digital Filter Channel 2 DRC Attack Configuration 2[7:0]	DF2_DRC_ATK_WF[7:0]							
0x20CA	Digital Filter Channel 2 DRC Release Configuration 1[7:0]	DF2_DRC_RLS_WF[15:8]							
0x20CB	Digital Filter Channel 2 DRC Release Configuration 2[7:0]	DF2_DRC_RLS_WF[7:0]							
0x20CC	Digital Filter Channel 2 DRC Threshold[7:0]	–	–	DF2_DRC_THR[5:0]					
0x20CD	Digital Filter Channel 2 DRC Enable[7:0]	–	–	DF2_DRC_INST_RLS	DF2_DRC_INST_ATK	DF2_DRC_CMP[2:0]			DF2_DRC_EN
0x20D0	Playback Compensation Channel Bank A Biquad Enable[7:0]	–	PBC_GAIN_BKA[2:0]			PBC_BQ_BKA_EN[3:0]			
0x20D1	Playback Compensation Channel Bank A Volume[7:0]	–	–	PBC_VOL_BKA[5:0]					
0x20D2	Playback Compensation Channel Bank B Biquad Enable[7:0]	–	PBC_GAIN_BKB[2:0]			PBC_BQ_BKB_EN[3:0]			
0x20D3	Playback Compensation Channel Bank B Volume[7:0]	–	–	PBC_VOL_BKB[5:0]					
0x20D4	Playback Compensation Channel Ramp Configuration[7:0]	–	–	–	PBC_VOL_RMP_RATE[3:0]				PBC_VOL_RMP_EN
0x20DC	Digital Filter Channel Configuration[7:0]	–	–	–	–	–	–	DF2_SEL	DF1_SEL
0x20DD	Digital Filter Channel Biquad Bank Select[7:0]	–	–	–	–	–	PBC_BQ_BK_SEL	DF2_BQ_BK_SEL	DF1_BQ_BK_SEL
0x20DE	Digital Filter Channel Mute Controls[7:0]	–	–	–	–	–	PBC_VOL_MUTE	DF2_VOL_MUTE	DF1_VOL_MUTE

ADDRESS	NAME	MSB							LSB
0x20DF	Digital Filter Channel Enables[7:0]	–	–	–	–	–	PBC_EN	DF2_EN	DF1_EN
SYSTEM CONTROL REGISTERS									
0x20F1	Clock Monitor Configuration[7:0]	–	CMON_BSELTOL[2:0]			CMON_ERRTOL[2:0]			CMON_AUTORESTART_EN
0x20F2	Clock Monitor Enable[7:0]	–	–	–	–	–	–	–	CMON_EN
0x20F4	Data Monitor Configuration[7:0]	–	–	DMON_MAG_THRES[1:0]		DMON_STUCK_THRES[1:0]		DMON_DURATION[1:0]	
0x20F5	Data Monitor Enables[7:0]	–	–	–	–	–	–	DMON_MAG_EN	DMON_STUCK_EN
0x20FE	System Level Configuration[7:0]	–	–	–	–	–	FLL_ERR_AUTORESTART_EN	DSP_SR[1:0]	
0x20FF	Device System Level Enables[7:0]	–	–	–	–	–	–	–	AUDIO_EN
DEVICE REVISION AND IDENTIFICATION REGISTERS									
0x28FD	Device ID MSB[7:0]	DEV_ID[15:8]							
0x28FE	Device ID LSB[7:0]	DEV_ID[7:0]							
0x28FF	Revision ID[7:0]	REV_ID[7:0]							

Register Details

Software Reset (0x2000)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	RST
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write Only

BITFIELD	BITS	RES	DESCRIPTION	DECODE
RST	0	–	Used to trigger a software reset event. Writing a 1 resets the device and returns the general control registers to their PoR states. Writing a 0 has no effect, and a read back always returns 0.	0x0: No effect. 0x1: Triggers a software reset event.

Interrupt Raw 1 (0x2001)

BIT	7	6	5	4	3	2	1	0
Field	INIT_DONE_RAW	OTP_FAIL_RAW	PWRDN_DONE_RAW	PB_PWRUP_DONE_RAW	REC_PWRUP_DONE_RAW	CLOCK_ERR_RAW	CLOCK_REC_RAW	DATA_ERR_RAW
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	RES	DESCRIPTION	DECODE
INIT_DONE_RAW	7	–	Raw Status of the Device Initialization Done Interrupt	0x0: No active device initialization done interrupt. 0x1: Device initialization done interrupt active.
OTP_FAIL_RAW	6	–	Raw Status of the OTP Load Failed Interrupt	0x0: No OTP load failure. 0x1: The OTP load routine did not complete succesfully.
PWRDN_DONE_RAW	5	–	Raw Status of the Power-Down Done Interrupt	0x0: Device is not reporting a power down into software shutdown event. 0x1: Device is reporting a power down into software shutdown event.
PB_PWRUP_DONE_RAW	4	–	Raw Status of the Playback Power-Up Done Interrupt	0x0: Device is not reporting a playback power-up event. 0x1: Device is reporting a playback power-up event.
REC_PWRUP_DONE_RAW	3	–	Raw Status of the Record Power-Up Done Interrupt	0x0: Device is not reporting a record power-up event. 0x1: Device is reporting a record power-up event.
CLOCK_ERR_RAW	2	–	Raw Status of the Clock Monitor Error Interrupt	0x0: Clock monitor not reporting a clock error. 0x1: Clock monitor reporting a clock error.
CLOCK_REC_RAW	1	–	Raw Status of the Clock Monitor Recovery Interrupt	0x0: Clock monitor is not reporting a clock recovery event. 0x1: Clock monitor is reporting a clock recovery event.
DATA_ERR_RAW	0	–	Raw Status of the Data Error Monitor Interrupt	0x0: Data monitor is not reporting a data error. 0x1: Data monitor is reporting a data error.

Interrupt Raw 2 (0x2002)

BIT	7	6	5	4	3	2	1	0
Field	FLL_ERR_RAW	I2C_GW_DONE_RAW	–	AMP_OCP_RAW	PBC_RMP_DONE_RAW	DF2_RMP_DONE_RAW	DF1_RMP_DONE_RAW	PB_RMP_DONE_RAW
Reset	0x0	0x0	–	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	RES	DESCRIPTION	DECODE
FLL_ERR_RAW	7	–	Raw Status of the FLL Lock Error Interrupt	0x0: No FLL lock error reported. 0x1: I^2C slave interface group write done.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
I2C_GW_DONE_RAW	6	–	Raw Status of the I²C Slave Interface Group Write Done Interrupt	0x0: No I²C slave interface group write done. 0x1: I²C slave interface group write done.
AMP_OCP_RAW	4	–	Raw Status of the Amplifier Output Overcurrent Protection Limit Interrupt	0x0: Amplifier overcurrent protection limit not exceeded. 0x1: Amplifier overcurrent protection limit exceeded.
PBC_RMP_DONE_RAW	3	–	Raw Status of the Playback Compensation Channel Ramp Done Interrupt	0x0: Device is not reporting a playback compensation channel ramp done event. 0x1: Device is reporting an playback compensation channel ramp done event.
DF2_RMP_DONE_RAW	2	–	Raw Status of the Digital Filter Channel 2 Ramp Done Interrupt	0x0: Device is not reporting a DF2 ramp done event. 0x1: Device is reporting a DF2 ramp done event.
DF1_RMP_DONE_RAW	1	–	Raw Status of the Digital Filter Channel 1 Ramp Done Interrupt	0x0: Device is not reporting a DF1 ramp done event. 0x1: Device is reporting a DF1 ramp done event.
PB_RMP_DONE_RAW	0	–	Raw Status of the Playback Channel Ramp Done Interrupt	0x0: Device is not reporting a playback ramp done event. 0x1: Device is reporting a playback ramp done event.

Interrupt State 1 (0x2003)

BIT	7	6	5	4	3	2	1	0
Field	INIT_DONE_STATE	OTP_FAIL_STATE	PWRDN_DONE_STATE	PB_PWRUP_DONE_STATE	REC_PWRUP_DONE_STATE	CLOCK_ERR_STATE	CLOCK_REC_STATE	DATA_ERR_STATE
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	RES	DESCRIPTION	DECODE
INIT_DONE_STATE	7	–	Device Initialization Done Unmaskable Interrupt State Bit	0x0: No raw status rising edge since the last clear. 0x1: Raw status rising edge since the last clear.
OTP_FAIL_STATE	6	–	OTP Load Routine Failed Unmaskable Interrupt State Bit	0x0: No raw status rising edge since the last clear. 0x1: Raw status rising edge since the last clear.
PWRDN_DONE_STATE	5	–	Power-Down Done Unmaskable Interrupt State Bit	0x0: No raw status rising edge since the last clear. 0x1: Raw status rising edge since the last clear.
PB_PWRUP_DONE_STATE	4	–	Playback Power-Up Done Unmaskable Interrupt State Bit	0x0: No raw status rising edge since the last clear. 0x1: Raw status rising edge since the last clear.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
REC_PWR UP_DONE_ STATE	3	–	Record Power-Up Done Unmaskable Interrupt State Bit	0x0: No raw status rising edge since the last clear. 0x1: Raw status rising edge since the last clear.
CLOCK_ER R_STATE	2	–	Clock Monitor Error Unmaskable Interrupt State Bit	0x0: No raw status rising edge since the last clear. 0x1: Raw status rising edge since the last clear.
CLOCK_RE C_STATE	1	–	Clock Monitor Recovery Unmaskable Interrupt State Bit	0x0: No raw status rising edge since the last clear. 0x1: Raw status rising edge since the last clear.
DATA_ERR _STATE	0	–	Data Error Monitor Unmaskable Interrupt State Bit	0x0: No raw status rising edge since the last clear. 0x1: Raw status rising edge since the last clear.

Interrupt State 2 (0x2004)

BIT	7	6	5	4	3	2	1	0
Field	FLL_ERR_ STATE	I2C_GW_D ONE_STAT E	–	AMP_OCP_ STATE	PBC_RMP_ DONE_STA TE	DF2_RMP_ DONE_STA TE	DF1_RMP_ DONE_STA TE	PB_RMP_D ONE_STAT E
Reset	0x0	0x0	–	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	RES	DESCRIPTION	DECODE
FLL_ERR_ STATE	7	–	FLL Lock Error Unmaskable Interrupt State Bit.	0x0: No raw status rising edge since the last clear. 0x1: Raw status rising edge since the last clear.
I2C_GW_D ONE_STAT E	6	–	I^2C Slave Interface Group Write Done Unmaskable Interrupt State Bit	0x0: No raw status rising edge since the last clear. 0x1: Raw status rising edge since the last clear.
AMP_OCP_ STATE	4	–	Amplifier Output Overcurrent Protection Unmaskable Interrupt State Bit	0x0: No raw status rising edge since the last clear. 0x1: Raw status rising edge since the last clear.
PBC_RMP_ DONE_STA TE	3	–	Playback Compensation Channel Ramp Done Unmaskable Interrupt State Bit	0x0: No raw status rising edge since the last clear. 0x1: Raw status rising edge since the last clear.
DF2_RMP_ DONE_STA TE	2	–	Digital Filter Channel 2 Ramp Done Unmaskable Interrupt State Bit	0x0: No raw status rising edge since the last clear. 0x1: Raw status rising edge since the last clear.
DF1_RMP_ DONE_STA TE	1	–	Digital Filter Channel 1 Ramp Done Unmaskable Interrupt State Bit	0x0: No raw status rising edge since the last clear. 0x1: Raw status rising edge since the last clear.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PB_RMP_DONE_STATE	0	–	Playback Channel Ramp Done Unmaskable Interrupt State Bit	0x0: No raw status rising edge since the last clear. 0x1: Raw status rising edge since the last clear.

Interrupt Flag 1 (0x2005)

BIT	7	6	5	4	3	2	1	0
Field	INIT_DONE_FLAG	OTP_FAIL_FLAG	PWRDN_DONE_FLAG	PB_PWRUP_DONE_FLAG	REC_PWRUP_DONE_FLAG	CLOCK_ERR_FLAG	CLOCK_REC_FLAG	DATA_ERR_FLAG
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	RES	DESCRIPTION	DECODE
INIT_DONE_FLAG	7	–	Device Initialization Done Maskable Interrupt Flag Bit. If the IRQ output is enabled, an interrupt is generated on a flag bit rising edge.	0x0: The flag bit is either masked or the state bit has not gone high. 0x1: The flag bit is not masked and the state bit has gone high.
OTP_FAIL_FLAG	6	–	OTP Load Routine Failed Maskable Interrupt Flag Bit. If the IRQ output is enabled, an interrupt is generated on a flag bit rising edge.	0x0: The flag bit is either masked or the state bit has not gone high. 0x1: The flag bit is not masked and the state bit has gone high.
PWRDN_DONE_FLAG	5	–	Power-Down Done Maskable Interrupt Flag Bit. If the IRQ output is enabled, an interrupt is generated on a flag bit rising edge.	0x0: The flag bit is either masked or the state bit has not gone high. 0x1: The flag bit is not masked and the state bit has gone high.
PB_PWRUP_DONE_FLAG	4	–	Playback Power-Up Done Maskable Interrupt Flag Bit. If the IRQ output is enabled, an interrupt is generated on a flag bit rising edge.	0x0: The flag bit is either masked or the state bit has not gone high. 0x1: The flag bit is not masked and the state bit has gone high.
REC_PWRUP_DONE_FLAG	3	–	Record Power-Up Done Maskable Interrupt Flag Bit. If the IRQ output is enabled, an interrupt is generated on a flag bit rising edge.	0x0: The flag bit is either masked or the state bit has not gone high. 0x1: The flag bit is not masked and the state bit has gone high.
CLOCK_ERR_FLAG	2	–	Clock Monitor Error Maskable Interrupt Flag Bit. If the IRQ output is enabled, an interrupt is generated on a flag bit rising edge.	0x0: The flag bit is either masked or the state bit has not gone high. 0x1: The flag bit is not masked and the state bit has gone high.
CLOCK_REC_FLAG	1	–	Clock Monitor Recovery Maskable Interrupt Flag Bit. If the IRQ output is enabled, an interrupt is generated on a flag bit rising edge.	0x0: The flag bit is either masked or the state bit has not gone high. 0x1: The flag bit is not masked and the state bit has gone high.
DATA_ERR_FLAG	0	–	Data Error Monitor Maskable Interrupt Flag Bit. If the IRQ output is enabled, an interrupt is generated on a flag bit rising edge.	0x0: The flag bit is either masked or the state bit has not gone high. 0x1: The flag bit is not masked and the state bit has gone high.

Interrupt Flag 2 (0x2006)

BIT	7	6	5	4	3	2	1	0
Field	FLL_ERR_FLAG	I2C_GW_DONE_FLAG	–	AMP_OCP_FLAG	PBC_RMP_DONE_FLAG	DF2_RMP_DONE_FLAG	DF1_RMP_DONE_FLAG	PB_RMP_DONE_FLAG
Reset	0x0	0x0	–	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	RES	DESCRIPTION	DECODE
FLL_ERR_FLAG	7	–	FLL Lock Error Maskable Interrupt Flag Bit. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0x0: The flag bit is either masked or the state bit has not gone high. 0x1: The flag bit is not masked and the state bit has gone high.
I2C_GW_DONE_FLAG	6	–	I²C Slave Interface Group Write Done Maskable Interrupt Flag Bit. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0x0: The flag bit is either masked or the state bit has not gone high. 0x1: The flag bit is not masked and the state bit has gone high.
AMP_OCP_FLAG	4	–	Amplifier Output Overcurrent Protection Maskable Interrupt Flag Bit. If the IRQ output is enabled, an interrupt is generated on a flag bit rising edge.	0x0: The flag bit is either masked or the state bit has not gone high. 0x1: The flag bit is not masked and the state bit has gone high.
PBC_RMP_DONE_FLAG	3	–	Playback Compensation Channel Ramp Done Maskable Interrupt Flag Bit. If the IRQ output is enabled, an interrupt is generated on a flag bit rising edge.	0x0: The flag bit is either masked or the state bit has not gone high. 0x1: The flag bit is not masked and the state bit has gone high.
DF2_RMP_DONE_FLAG	2	–	Digital Filter Channel 2 Ramp Done Maskable Interrupt Flag Bit. If the IRQ output is enabled, an interrupt is generated on a flag bit rising edge.	0x0: The flag bit is either masked or the state bit has not gone high. 0x1: The flag bit is not masked and the state bit has gone high.
DF1_RMP_DONE_FLAG	1	–	Digital Filter Channel 1 Done Maskable Interrupt Flag Bit. If the IRQ output is enabled, an interrupt is generated on a flag bit rising edge.	0x0: The flag bit is either masked or the state bit has not gone high. 0x1: The flag bit is not masked and the state bit has gone high.
PB_RMP_DONE_FLAG	0	–	Playback Channel Ramp Done Maskable Interrupt Flag Bit. If the IRQ output is enabled, an interrupt is generated on a flag bit rising edge.	0x0: The flag bit is either masked or the state bit has not gone high. 0x1: The flag bit is not masked and the state bit has gone high.

Interrupt Enable 1 (0x2007)

BIT	7	6	5	4	3	2	1	0
Field	INIT_DONE_EN	OTP_FAIL_EN	PWRDN_DONE_EN	PB_PWRUP_DONE_EN	REC_PWRUP_DONE_EN	CLOCK_ERR_EN	CLOCK_REC_EN	DATA_ERR_EN
Reset	0x1	0x1	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
INIT_DONE_EN	7	–	Enables the Initialization Done Interrupt. This interrupt indicates when the device has completed the transition from a reset event or the hardware shutdown state into the software shutdown state. Once this occurs, the device is ready to accept programming through the I^2C control interface.	0x0: Flag bit is held low and cannot go high (masked). 0x1: Flag bit goes high whenever the state bit goes high (unmasked).
OTP_FAIL_EN	6	–	Enables the OTP Load Routine Fail Interrupt. Indicates that the OTP load routine that runs when initializing the device has failed to complete successfully.	0x0: Flag bit is held low and cannot go high (masked). 0x1: Flag bit goes high whenever the state bit goes high (unmasked).
PWRDN_DONE_EN	5	–	Enables the Power-Down Done Interrupt. Indicates the device has successfully completed power down into the software shutdown state from the audio state.	0x0: Flag bit is held low and cannot go high (masked). 0x1: Flag bit goes high whenever the state bit goes high (unmasked).
PB_PWRUP_DONE_EN	4	–	Enables the Playback Power-Up Done Interrupt. Indicates the device has both transitioned out of the software shutdown state, and that the playback channel is enabled and ready to receive audio data.	0x0: Flag bit is held low and cannot go high (masked). 0x1: Flag bit goes high whenever the state bit goes high (unmasked).
REC_PWRUP_DONE_EN	3	–	Enables the Record Power-Up Done Interrupt. Indicates the device has both transitioned out of the software shutdown state, and that at least one record channel is enabled and ready to transmit audio data. This interrupt is not generated when at least one record channel is already active, and additional record channels are dynamically enabled.	0x0: Flag bit is held low and cannot go high (masked). 0x1: Flag bit goes high whenever the state bit goes high (unmasked).
CLOCK_ERR_EN	2	–	Enables the Clock Monitor Error Interrupt. Indicates that the clock monitor has detected a clock error event. Clock error events can only be generated when the audio enable bit (AUDIO_EN) is first set high.	0x0: Flag bit is held low and cannot go high (masked). 0x1: Flag bit goes high whenever the state bit goes high (unmasked).
CLOCK_REC_EN	1	–	Enables the Clock Monitor Recovery Interrupt. Indicates that the clock monitor has detected a clock recovery event. Clock recovery events can only be generated in auto mode after a clock error event has first occurred.	0x0: Flag bit is held low and cannot go high (masked). 0x1: Flag bit goes high whenever the state bit goes high (unmasked).
DATA_ERR_EN	0	–	Enables the Data Error Monitor Interrupt. Indicates that the playback data monitor has detected a data error event. Data error events can only be generated when the audio enable bit (AUDIO_EN) is first set high.	0x0: Flag bit is held low and cannot go high (masked). 0x1: Flag bit goes high whenever the state bit goes high (unmasked).

Interrupt Enable 2 (0x2008)

BIT	7	6	5	4	3	2	1	0
Field	FLL_ERR_EN	I2C_GW_DONE_EN	–	AMP_OCP_EN	PBC_RMP_DONE_EN	DF2_RMP_DONE_EN	DF1_RMP_DONE_EN	PB_RMP_DONE_EN
Reset	0x0	0x0	–	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
FLL_ERR_EN	7	–	Enables the FLL Lock Error Interrupt. Indicates that the FLL either failed to lock (while transitioning from software shutdown to the audio state), or that FLL lock was lost while the device was operating in the audio state.	0x0: Flag bit is held low and cannot go high (masked). 0x1: Flag bit goes high whenever the state bit goes high (unmasked).
I2C_GW_DONE_EN	6	–	Enables the I²C Slave Interface Group Write Done Interrupt. This indicates that the device has completed an I²C write transaction through the group write address.	0x0: Flag bit is held low and cannot go high (masked). 0x1: Flag bit goes high whenever the state bit goes high (unmasked).
AMP_OCP_EN	4	–	Enables the Amplifier Output Overcurrent Protection Interrupt. Indicates that the overcurrent protection limit was exceeded.	0x0: Flag bit is held low and cannot go high (masked). 0x1: Flag bit goes high whenever the state bit goes high (unmasked).
PBC_RMP_DONE_EN	3	–	Enables the Playback Compensation Channel Ramping Done Interrupt. This interrupt indicates that the playback compensation channel has finished ramping.	0x0: Flag bit is held low and cannot go high (masked). 0x1: Flag bit goes high whenever the state bit goes high (unmasked).
DF2_RMP_DONE_EN	2	–	Enables the Digital Filter Channel 2 Ramping Done Interrupt. This interrupt indicates that digital filter channel 2 has finished ramping.	0x0: Flag bit is held low and cannot go high (masked). 0x1: Flag bit goes high whenever the state bit goes high (unmasked).
DF1_RMP_DONE_EN	1	–	Enables the Digital Filter Channel 1 Ramping Done Interrupt. This interrupt indicates that digital filter channel 1 has finished ramping.	0x0: Flag bit is held low and cannot go high (masked). 0x1: Flag bit goes high whenever the state bit goes high (unmasked).
PB_RMP_DONE_EN	0	–	Enables the Playback Channel Ramping Done Interrupt. This interrupt indicates that playback channel has finished ramping.	0x0: Flag bit is held low and cannot go high (masked). 0x1: Flag bit goes high whenever the state bit goes high (unmasked).

Interrupt Clear 1 (0x2009)

BIT	7	6	5	4	3	2	1	0
Field	INIT_DONE_CLR	OTP_FAIL_CLR	PWRDN_DONE_CLR	PB_PWRUP_DONE_CLR	REC_PWRUP_DONE_CLR	CLOCK_ERR_CLR	CLOCK_REC_CLR	DATA_ERR_CLR
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write Only	Write Only	Write Only	Write Only	Write Only	Write Only	Write Only	Write Only

BITFIELD	BITS	RES	DESCRIPTION	DECODE
INIT_DONE_CLR	7	–	Device Initialization Done Interrupt State and Flag Bit Clear	0x0: No effect. 0x1: Clears the state and flag bits to 0.
OTP_FAIL_CLR	6	–	OTP Load Routine Failed State and Flag Bit Clear	0x0: No effect. 0x1: Clears the state and flag bits to 0.
PWRDN_DONE_CLR	5	–	Power-Down Done State and Flag Bit Clear	0x0: No effect. 0x1: Clears the state and flag bits to 0.
PB_PWRUP_DONE_CLR	4	–	Playback Power-Up Done State and Flag Bit Clear	0x0: No effect. 0x1: Clears the state and flag bits to 0.
REC_PWRUP_DONE_CLR	3	–	Record Power-Up Done State and Flag Bit Clear	0x0: No effect. 0x1: Clears the state and flag bits to 0.
CLOCK_ERR_CLR	2	–	Clock Monitor Error State and Flag Bit Clear	0x0: No effect. 0x1: Clears the state and flag bits to 0.
CLOCK_REC_CLR	1	–	Clock Monitor Recovery State and Flag Bit Clear	0x0: No effect. 0x1: Clears the state and flag bits to 0.
DATA_ERR_CLR	0	–	Data Error Monitor State and Flag Bit Clear	0x0: No effect. 0x1: Clears the state and flag bits to 0.

Interrupt Clear 2 (0x200A)

BIT	7	6	5	4	3	2	1	0
Field	FLL_ERR_CLR	I2C_GW_DONE_CLR	–	AMP_OCP_CLR	PBC_RMP_DONE_CLR	DF2_RMP_DONE_CLR	DF1_RMP_DONE_CLR	PB_RMP_DONE_CLR
Reset	0x0	0x0	–	0x0	0x0	0x0	0x0	0x0
Access Type	Write Only	Write Only	–	Write Only	Write Only	Write Only	Write Only	Write Only

BITFIELD	BITS	RES	DESCRIPTION	DECODE
FLL_ERR_CLR	7	–	FLL Lock Error State and Flag Bit Clear	0x0: No effect. 0x1: Clears the state and flag bits to 0.
I2C_GW_DONE_CLR	6	–	I²C Slave Interface Group Write Done State and Flag Bit Clear	0x0: No effect. 0x1: Clears the state and flag bits to 0.
AMP_OCP_CLR	4	–	Amplifier Output Overcurrent Protection State and Flag Bit Clear	0x0: No effect. 0x1: Clears the state and flag bits to 0.
PBC_RMP_DONE_CLR	3	–	Playback Compensation Channel Ramp Done Interrupt Done State and Flag Bit Clear	0x0: No effect. 0x1: Clears the state and flag bits to 0.
DF2_RMP_DONE_CLR	2	–	Digital Filter Channel 2 Ramp Done Interrupt Done State and Flag Bit Clear	0x0: No effect. 0x1: Clears the state and flag bits to 0.
DF1_RMP_DONE_CLR	1	–	Digital Filter Channel 1 Ramp Done Interrupt Done State and Flag Bit Clear	0x0: No effect. 0x1: Clears the state and flag bits to 0.
PB_RMP_DONE_CLR	0	–	Playback Channel Ramp Done Interrupt Done State and Flag Bit Clear	0x0: No effect. 0x1: Clears the state and flag bits to 0.

IRQ Control 1 (0x2012)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	IRQ_DRV[1:0]		IRQ_INT_PU	IRQ_MODE	IRQ_POL
Reset	–	–	–	0x1		0x0	0x0	0x0
Access Type	–	–	–	Write, Read		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
IRQ_DRV	4:3	IRQ	Configures the Drive Strength of the IRQ Output. This setting is only applicable when the IRQ output is configured in CMOS push-pull mode.	0x0: Reduced drive mode (2mA) 0x1: Normal drive mode (4mA) 0x2: High drive mode (6mA) 0x3: Highest drive mode (8mA)
IRQ_INT_PU	2	IRQ	Enables the IRQ Output Internal Pullup Resistor (100kΩ typical)	0x0: IRQ internal pullup resistor disabled. 0x1: IRQ internal pullup resistor enabled.
IRQ_MODE	1	IRQ	Controls the Drive Mode of the IRQ Output	0x0: IRQ output is in open-drain mode, and an external pullup resistor is required. 0x1: IRQ output is in CMOS push-pull mode, and no external pullup resistor is required.
IRQ_POL	0	IRQ	Controls the IRQ Output Assert Polarity	0x0: IRQ output asserts low when any interrupt FLAG bits are high (active-low). 0x1: IRQ output asserts high when any interrupt FLAG bits are high (active-low).

IRQ Enable (0x2013)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	IRQ_EN
Reset	–	–	–	–	–	–	–	0x1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
IRQ_EN	0	–	Enables the IRQ Output. When enabled, interrupt assertions are generated on the IRQ output whenever an active (unmasked) interrupt source reports an event. The IRQ output deasserts when all asserted interrupt sources are cleared.	0x0: The IRQ output is disabled and is high-impedance. 0x1: The IRQ output is enabled and is controlled by the interrupt controller.

I2C Slave Configuration (0x2014)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	I2C_GROUP_ADDR_EN
Reset	–	–	–	–	–	–	–	0x1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
I2C_GROUP_ADDR_EN	0	–	Enables the I2C slave interface group write address of 0x6A. When enabled, the device responds to write transactions through the group address. Read transactions are not supported.	0x0: The group write address of 0x6A is disabled. 0x1: The group write address of 0x6A is enabled.

PCM Interface Configuration 1 (0x2020)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	PCM_CHANSZ[1:0]		PCM_FORMAT[2:0]		
Reset	–	–	–	0x3		0x0		
Access Type	–	–	–	Write, Read		Write, Read		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_CHANSZ	4:3	PCM	Configures the PCM Interface Data Word Length. In TDM modes, the channel length and word length are always equal, while in I2S and left-justified modes, the word length must be less than or equal to the channel length.	0x0: Reserved 0x1: 16-Bits 0x2: 24-Bits 0x3: 32-Bits
PCM_FORMAT	2:0	PCM	Selects the PCM Interface Data Format	0x0: I2S mode 0x1: Left-justified mode 0x2: Reserved 0x3: TDM mode 0 (no bit clock data delay) 0x4: TDM mode 1 (1 bit clock data delay) 0x5: TDM mode 2 (2 bit clock data delay) 0x6: Reserved 0x7: Reserved

PCM Interface Configuration 2 (0x2021)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_CHANSEL	PCM_BCLKEDGE	PCM_BSEL[3:0]			
Reset	–	–	0x0	0x0	0x4			
Access Type	–	–	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_CHANSEL	5	PCM	Selects whether the rising or falling edge of the frame clock indicates the start of a new frame (Channel 0).	0x0: In I2S and left-justified modes: Falling frame clock edge indicates the start of a new frame. In TDM modes: Rising frame clock edge indicates the start of a new frame. 0x1: In I2S and left-justified modes: Rising frame clock edge indicates the start of a new frame In TDM Modes: Falling frame clock edge indicates the start of a new frame.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_BCLKEDGE	4	PCM	Selects the PCM interface active bit clock edge (rising or falling).	0x0: PCM input data is captured and output data is valid on bit clock rising edges. 0x1: PCM input data is captured and output data is valid on bit clock falling edges.
PCM_BSEL	3:0	PCM	Selects the number of bit clock periods per frame clock period. In TDM Modes, the number of channels is equal to this selection divided by the data word size selected.	0x0: Reserved 0x1: Reserved 0x2: 32 0x3: 48 0x4: 64 0x5: 96 0x6: 128 0x7: 192 0x8: 256 0x9: 384 0xA: 512 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

PCM Interface Configuration 3 (0x2022)

BIT	7	6	5	4	3	2	1	0
Field	–	PCM_DOUT_DRV[1:0]		PCM_TX_NO_RPT_SAMP	PCM_TX_INTERLEAVE_SEL[1:0]		PCM_TX_INTERLEAVE	PCM_TX_EXTRA_HIZ
Reset	–	0x1		0x0	0x0		0x0	0x0
Access Type	–	Write, Read		Write, Read	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_DOUT_DRV	6:5	PCM	Configures the PCM interface transmitter data output (DOUT) drive strength.	0x0: Reduced drive mode (2mA) 0x1: Normal drive mode (4mA) 0x2: High drive mode (6mA) 0x3: Highest drive mode (8mA)
PCM_TX_NO_RPT_SAMP	4	PCM	By default, when the record channel sample rate (PCM_REC_SR) is set to a rate less than that of the PCM interface and playback channel sample rate (PCM_PB_SR), repeated record channel samples are transmitted on each of the extra frame slots (based on the record to playback channel sample rate ratio). If this is set, instead each record sample is sent only once followed by zero data in each of the repeated frame slots.	0x0: Repeated record channel samples are transmitted in extra record frame slots. 0x1: Record channel samples are transmitted once followed by zero data in extra record frame slots.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_INTERLEAVE_SEL	3:2	PCM	Selects which two record channel outputs are capable of PCM data output (DOUT) frame interleaving. Frame interleaving occurs (if enabled) when the selected record channels are assigned to the same PCM data output slot.	0x0: PCM data output from record channels 1 and 2 can be frame interleaved (in that order each frame). 0x1: PCM data output from record channels 1 and 3 can be frame interleaved (in that order each frame). 0x2: PCM data output from record channels 3 and 2 can be frame interleaved (in that order each frame). 0x3: Reserved
PCM_TX_INTERLEAVE	1	PCM	Controls whether or not record channel data assigned to the same channel is frame interleaved on the PCM data output (DOUT).	0x0: PCM data output interleave mode disabled. 0x1: PCM data output interleave mode enabled.
PCM_TX_EXTRA_HIZ	0	PCM	Selects whether the PCM transmitter data output (DOUT) is driven to zero or Hi-Z during extra bit clock (BCLK) cycles.	0x0: PCM data output is driven to zero for extra bit clock cycles (zero-padding). 0x1: PCM data output is set to Hi-Z for extra bit clock cycles.

PCM Sample Rate Configuration (0x2024)

BIT	7	6	5	4	3	2	1	0
Field	PCM_REC_SR[3:0]				PCM_PB_SR[3:0]			
Reset	0x8				0x8			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_REC_SR	7:4	PCM	Sets the PCM sample rate of the microphone record channel. The selected PCM record channel sample rate must always be less than or equal to (and be an integer ratio to) the PCM frame clock and playback channel sample rate.	0x0: 8kHz 0x1: 11.025kHz 0x2: 12kHz 0x3: 16kHz 0x4: 22.05kHz 0x5: 24kHz 0x6: 32kHz 0x7: 44.1kHz 0x8: 48kHz 0x9 to 0xF: Reserved
PCM_PB_SR	3:0	PCM	Sets the PCM interface frame clock (LRCLK) frequency and the sample rate of the amplifier playback channel.	0x0: 8kHz 0x1: 11.025kHz 0x2: 12kHz 0x3: 16kHz 0x4: 22.05kHz 0x5: 24kHz 0x6: 32kHz 0x7: 44.1kHz 0x8: 48kHz 0x9: 88.2kHz 0xA: 96kHz 0xB: 176.4kHz 0xC: 192kHz 0xD to 0xF: Reserved

PCM Playback Channel Source (0x2026)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PCM_PB_SOURCE[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_PB_SOURCE	3:0	PCM	Selects the PCM interface receiver input data channel to route to the playback channel. The PCM interface receiver data input must be enabled for the playback channel to receive the input data from the selected channel.	0x0: PCM interface receiver input data channel 0. 0x1: PCM interface receiver input data channel 1. ...: ... 0xE: PCM interface receiver input data channel 14. 0xF: PCM interface receiver input data channel 15.

PCM Record Channel 1 Slot Selection (0x2028)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_REC1_SLOT[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_REC1_SLOT	5:0	PCM	Selects the PCM transmitter data output slot (DOUT) for the PCM record channel 1 output data. If the PCM record channel 1 is disabled (with REC1_PCM_EN), the selected output channel/slots are considered unused. In non-TDM modes, only two output data channels are available and are selected with the Slot 0 and Slot 1 settings. In TDM modes, data transmit begins in the selected slot, and requires from 2 to 4 consecutive 8-bit slots to transmit (depending on the data word size).	0x0: PCM transmitter output data slot 0 (channel 0 in non-TDM modes). 0x1: PCM transmitter output data slot 1 (channel 1 in non-TDM modes). 0x2: PCM transmitter output data slot 2. 0x3: PCM transmitter output data slot 3. 0x4 to 0x3D: ... 0x3E: PCM transmitter output data slot 62. 0x3F: PCM transmitter output data slot 63.

PCM Record Channel 2 Slot Selection (0x2029)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_REC2_SLOT[5:0]					
Reset	–	–	0x01					
Access Type	–	–	Write, Read					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_REC2_SLOT	5:0	PCM	Selects the PCM transmitter data output slot (DOUT) for the PCM record channel 2 output data. If PCM record channel 2 is disabled (with REC2_PCM_EN), the selcted output channel/slots are considered unused. In non-TDM modes, only two output data channels are available and are selected with the Slot 0 and Slot 1 settings. In TDM modes, data transmit begins in the selected slot, and requires from 2 to 4 consecutive 8-bit slots to transmit (depending on the data word size).	0x0: PCM transmitter output data slot 0 (channel 0 in non-TDM modes). 0x1: PCM transmitter output data slot 1 (channel 1 in non-TDM modes). 0x2: PCM transmitter output data slot 2. 0x3: PCM transmitter output data slot 3. 0x4 to 0x3D: ... 0x3E: PCM transmitter output data slot 62. 0x3F: PCM transmitter output data slot 63.

PCM Record Channel 3 Slot Selection (0x202A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_REC3_SLOT[5:0]					
Reset	–	–	0x01					
Access Type	–	–	Write, Read					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_REC3_SLOT	5:0	PCM	Selects the PCM transmitter data output slot (DOUT) for the PCM record channel 3 output data. If PCM record channel 3 is disabled (with REC3_PCM_EN), the selcted output channel/slots are considered unused. In non-TDM modes, only two output data channels are available and are selected with the slot 0 and slot 1 settings. In TDM modes, data transmit begins in the selected slot, and requires from 2 to 4 consecutive 8-bit slots to transmit (depending on the data word size).	0x0: PCM transmitter output data slot 0 (channel 0 in non-TDM modes). 0x1: PCM transmitter output data slot 1 (channel 1 in non-TDM modes). 0x2: PCM transmitter output data slot 2. 0x3: PCM transmitter output data slot 3. 0x4 to 0x3D: ... 0x3E: PCM transmitter output data slot 62. 0x3F: PCM transmitter output data slot 63.

PCM Record Channel 4 Slot Selection (0x202B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_REC4_SLOT[5:0]					
Reset	–	–	0x01					
Access Type	–	–	Write, Read					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_REC4_SLOT	5:0	PCM	Selects the PCM transmitter data output slot (DOUT) for the PCM record channel 4 output data. If PCM record channel 4 is disabled (with REC4_PCM_EN), the selcted output channel/slots are considered unused. In non-TDM modes, only two output data channels are available and are selected with the Slot 0 and Slot 1 settings. In TDM modes, data transmit begins in the selected slot, and requires from 2 to 4 consecutive 8-bit slots to transmit (depending on the data word size).	0x0: PCM transmitter output data slot 0 (channel 0 in non-TDM modes). 0x1: PCM transmitter output data slot 1 (channel 1 in non-TDM modes). 0x2: PCM transmitter output data slot 2. 0x3: PCM transmitter output data slot 3. 0x4 to 0x3D: ... 0x3E: PCM transmitter output data slot 62. 0x3F: PCM transmitter output data slot 63.

PCM Data Output Tx Hi-Z Control 1 (0x2031)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[63:56]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	PCM	Configures the unused PCM transmitter data output slots to transmit either Hi-Z or 0. This setting only applies if the output data slot is unused, and is disregarded if an output data source is assigned to the slot, and the output data source is enabled.	0x0: Output zero (logic-low) on the output slot if unused. 0x1: Output high impedance (Hi-Z) on the output slot if unused.

PCM Data Output Tx Hi-Z Control 2 (0x2032)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[55:48]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	PCM	Configures the unused PCM transmitter data output slots to transmit either Hi-Z or 0. This setting only applies if the output data slot is unused, and is disregarded if an output data source is assigned to the slot, and the output data source is enabled.	0x0: Output zero (logic-low) on the output slot if unused. 0x1: Output high impedance (Hi-Z) on the output slot if unused.

PCM Data Output Tx Hi-Z Control 3 (0x2033)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[47:40]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	PCM	Configures the unused PCM transmitter data output slots to transmit either Hi-Z or 0. This setting only applies if the output data slot is unused, and is disregarded if an output data source is assigned to the slot, and the output data source is enabled.	0x0: Output zero (logic-low) on the output slot if unused. 0x1: Output high impedance (Hi-Z) on the output slot if unused.

PCM Data Output Tx Hi-Z Control 4 (0x2034)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[39:32]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	PCM	Configures the unused PCM transmitter data output slots to transmit either Hi-Z or 0. This setting only applies if the output data slot is unused, and is disregarded if an output data source is assigned to the slot, and the output data source is enabled.	0x0: Output zero (logic-low) on the output slot if unused. 0x1: Output high impedance (Hi-Z) on the output slot if unused.

PCM Data Output Tx Hi-Z Control 5 (0x2035)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[31:24]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	PCM	Configures the unused PCM transmitter data output slots to transmit either Hi-Z or 0. This setting only applies if the output data slot is unused, and is disregarded if an output data source is assigned to the slot, and the output data source is enabled.	0x0: Output zero (logic-low) on the output slot if unused. 0x1: Output high impedance (Hi-Z) on the output slot if unused.

PCM Data Output Tx Hi-Z Control 6 (0x2036)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[23:16]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	PCM	Configures the unused PCM transmitter data output slots to transmit either Hi-Z or 0. This setting only applies if the output data slot is unused, and is disregarded if an output data source is assigned to the slot, and the output data source is enabled.	0x0: Output zero (logic-low) on the output slot if unused. 0x1: Output high impedance (Hi-Z) on the output slot if unused.

PCM Data Output Tx Hi-Z Control 7 (0x2037)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[15:8]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	PCM	Configures the unused PCM transmitter data output slots to transmit either Hi-Z or 0. This setting only applies if the output data slot is unused, and is disregarded if an output data source is assigned to the slot, and the output data source is enabled.	0x0: Output zero (logic-low) on the output slot if unused. 0x1: Output high impedance (Hi-Z) on the output slot if unused.

PCM Data Output Tx Hi-Z Control 8 (0x2038)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	PCM	Configures the unused PCM transmitter data output slots to transmit either Hi-Z or 0. This setting only applies if the output data slot is unused, and is disregarded if an output data source is assigned to the slot, and the output data source is enabled.	0x0: Output zero (logic-low) on the output slot if unused. 0x1: Output high-impedance (Hi-Z) on the output slot if unused.

PCM Interface Loop Enables (0x203E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	PCM_LB_DOUT_EN	PCM_PB_LT_EN[1:0]	
Reset	–	–	–	–	–	0x0	0x0	
Access Type	–	–	–	–	–	Write, Read	Write, Read	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_LB_DOUT_EN	2	PCM	Enables the PCM data input (DIN) to PCM data output (DOUT) loop back function.	0x0: PCM data loop back function disabled. 0x1: PCM data loop back function enabled.
PCM_PB_LT_EN	1:0	PCM	Enables internal PCM data loop through from the selected PCM record channel output to the input of the PCM playback channel.	0x0: PCM internal data loop through disabled. 0x1: PCM internal data loop through from record channel 1 enabled. 0x2: PCM internal data loop through from record channel 2 enabled. 0x3: PCM internal data loop through from record channel 3 enabled.

PCM Interface Enables (0x203F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	PCM_TX_EN	PCM_RX_EN
Reset	–	–	–	–	–	–	0x0	0x1
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_EN	1	–	Enables the PCM Interface Transmitter Data Output (DOUT)	0x0: PCM interface transmitter disabled. 0x1: PCM interface transmitter enabled.
PCM_RX_EN	0	EN	Enables the PCM Interface Receiver Data Input (DIN)	0x0: PCM interface receiver disabled. 0x1: PCM interface receiver enabled.

Playback Block Configuration 1 (0x2060)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PB_POWER_MODE	PB_DITH_EN	PB_INVERT	PB_DCBLK[1:0]		PB_DCBLK_EN
Reset	–	–	0x0	0x1	0x0	0x0		0x1
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PB_POWER_MODE	5	PB	Selects the Playback Channel Power Mode.The playback channel can operate either in a high-performance mode or a reduced power mode.	0x0: Playback channel is in high-performance mode. 0x1: Playback channel is in low-power mode.
PB_DITH_EN	4	PB	Selects whether or not dither is applied to the input data to the playback channel.	0x0: Playback channel dither disabled. 0x1: Playback channel dither enabled.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PB_INVERT	3	PB	Inverts the Playback Channel Data	0x0: Non-inverted playback channel data. 0x1: Inverted playback channel data.
PB_DCBLK	2:1	PB	Sets the Playback Channel DC Blocking Filter Corner Frequency. The DC blocking corner frequency scales with playback sample rate from 8kHz to 48kHz, and is set based on the sample rate above 48kHz.	0x0: Playback channel DC blocking corner frequency f_C is: f_S = 8kHz to 48kHz: f_C scales from 0.312Hz to 1.872Hz f_S = 88.2kHz/96kHz: f_C = 0.144Hz f_S = 176.4kHz/192kHz: f_C = 1.872Hz 0x1: Playback channel DC blocking corner frequency f_C is: f_S = 8kHz to 48kHz: f_C scales from 2.496Hz to 14.976Hz f_S = 88.2kHz/96kHz: f_C = 14.976Hz f_S = 176.4kHz/192kHz: f_C = 14.976Hz 0x2: Reserved 0x3: Reserved
PB_DCBLK_EN	0	PB	Enables the Playback Channel DC Blocking Filter	0x0: DC blocking filter disabled. 0x1: DC blocking filter enabled.

Playback Block Configuration 2 (0x2061)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PB_HBW_EN	PB_HR_SEL[1:0]		PB_DELAY[2:0]		
Reset	–	–	0x0	0x0		0x0		
Access Type	–	–	Write, Read	Write, Read		Write, Read		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PB_HBW_EN	5	PB	Enables Playback Channel High-Bandwidth Mode. In this mode, the playback channel bandwidth is expanded to 40kHz. Playback channel high-bandwidth mode is only supported when the playback channel sample rate (PCM_PB_SR) is set to 88.2kHz, 96kHz, 176.4kHz, or 192kHz.	0x0: Playback channel high bandwidth mode. Disabled 0x1: Playback channel high bandwidth mode. Enabled
PB_HR_SEL	4:3	PB	Artificially increases the digital headroom of the playback and playback-compensation channels by 1, 2, or 3 bits. The overall system gain remains unchanged, and the additional headroom is instead created by shifting the channel gain structure (down before the playback equalizer and back up before summing the playback and DF1/DF2 channels). As a result of the gain structure shift, each additional bit of digital headroom results in the loss of the same number of overall channel resolution bits.	0x0: 0 Bit gain shift (30dB of channel headroom). 0x1: 1 Bit gain shift (36dB of channel Headroom). 0x2: 2 Bit gain shift (42dB of channel Headroom). 0x3: 3 Bit gain shift (48dB of channel Headroom).

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PB_DELAY	2:0	PB	Adds Delay to the Playback Channel Data. Delay is added in terms of number of samples at 384kHz.	0x0: No additional delay. 0x1: Adds a 1 sample delay. 0x2: Adds a 2 sample delay. 0x3: Adds a 3 sample delay. 0x4: Adds a 4 sample delay. 0x5: Adds a 5 sample delay. 0x6: Adds a 6 sample delay. 0x7: Adds a 7 sample delay.

Playback Biquad Enable (0x2062)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PB_BQ_EN[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PB_BQ_EN	3:0	PB	Enable Control for the Playback Channel Biquad Filter Bands. Bands are incrementally enabled in series.	0x0: Playback biquad filter fully disabled. 0x1: Playback biquad filter band 1 enabled. 0x2: Playback biquad filter bands 1 and 2 enabled. 0x3: Playback biquad filter bands 1 to 3 enabled. 0x4: Playback biquad filter bands 1 to 4 enabled. 0x5: Playback biquad filter bands 1 to 5 enabled. 0x6 to 0xF: Reserved

Playback Gain Correction (0x2063)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PB_GAIN[5:0]					
Reset	–	–	0x18					
Access Type	–	–	Write, Read					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PB_GAIN	5:0	PB	Sets the Fine Resolution Digital Gain Correction Level Applied to the End of the Playback Channel. This can be used to compensate for the overall channel response and external component variations.	0x0: -6.0dB 0x1: -5.75dB 0x2: -5.50dB 0x3: -5.25dB 0x18: 0dB (default) ...: ... (0.25dB steps) 0x2D: 5.25dB 0x2E: 5.50dB 0x2F: 5.75dB 0x30: 6.0dB 0x31 to 0x3F: Reserved

Playback Ramp Rate Configuration (0x2064)

BIT	7	6	5	4	3	2	1	0
Field	PB_SHDN_RMP_RATE[2:0]			PB_VOL_RMP_RATE[3:0]				PB_RMP_EN
Reset	0x2			0x2				0x1
Access Type	Write, Read			Write, Read				Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PB_SHDN_RMP_RATE	7:5	–	Selects the Ramp Rate for Playback Channel Disable	0x0: 1ms ramp rate 0x1: 2ms ramp rate 0x2: 4ms ramp rate 0x3: 8ms ramp rate 0x4: 16ms ramp rate 0x5: 32ms ramp rate 0x6: 64ms ramp rate 0x7: 128ms ramp rate
PB_VOL_RMP_RATE	4:1	–	Selects the Ramp Rate for Playback Channel Enable, Mute/Unmute, and Volume Changes	0x0: 1ms ramp rate 0x1: 2ms ramp rate 0x2: 4ms ramp rate 0x3: 8ms ramp rate 0x4: 16ms ramp rate 0x5: 32ms ramp rate 0x6: 64ms ramp rate 0x7: 128ms ramp rate 0x8: 256ms ramp rate 0x9: 512ms ramp rate 0xA: 1024ms ramp rate 0xB: 2048ms ramp rate 0xC to 0xF: Reserved
PB_RMP_EN	0	–	Enables Playback Channel Volume Ramping on Enable, Disable, Mute, and any Volume Change	0x0: Ramping disabled 0x1: Ramping enabled

Playback Volume Control (0x2065)

BIT	7	6	5	4	3	2	1	0
Field	–	PB_VOL[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read, Ext						

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PB_VOL	6:0	–	Sets the Digital Volume Level of the Playback Channel	0x0: 0dB 0x1: -0.5dB 0x2: -1.0dB 0x3: -1.5dB ...: ... (-0.5dB steps) 0x7C: -62.0dB 0x7D: -62.5dB 0x7E: -63.0dB 0x7F: -63.5dB

Playback Noise Gate Thresholds (0x2066)

BIT	7	6	5	4	3	2	1	0
Field	PB_NG_UNMUTE_THRESH[3:0]				PB_NG_MUTE_THRESH[3:0]			
Reset	0x3				0x2			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PB_NG_UNMUTE_THRESH	7:4	PB	Sets the threshold (in number of LSBs toggling) at which the noise gate block deactivates.	0x0: 1 LSB 0x1: 2 LSBs 0x2: 3 LSBs 0x3: 4 LSBs 0x4: 5 LSBs 0x5: 6 LSBs 0x6: 7 LSBs 0x7: 8 LSBs 0x8: 9 LSBs 0x9: 10 LSBs 0xA to 0xF: Reserved
PB_NG_MUTE_THRESH	3:0	PB	Sets the threshold (in number of LSBs toggling) at which the noise gate block activates.	0x0: 1 LSB 0x1: 2 LSBs 0x2: 3 LSBs 0x3: 4 LSBs 0x4: 5 LSBs 0x5: 6 LSBs 0x6: 7 LSBs 0x7: 8 LSBs 0x8: 9 LSBs 0x9 to 0xF: Reserved

Playback Noise Gate Control (0x2067)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	PB_NG_EN
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PB_NG_EN	0	PB	Enables the Playback Channel Noise Gate	0x0: Playback channel noise gate disabled. 0x1: Playback channel noise gate enabled.

Playback Amplifier Configuration (0x2069)

BIT	7	6	5	4	3	2	1	0
Field	–	PB_AMP_LOAD_OP_BIAS[1:0]		PB_AMP_PWM_SEL	PB_AMP_OCP_AUTORESTART_EN	PB_AMP_MODE[2:0]		
Reset	–	0x1		0b0	0x0	0x0		
Access Type	–	Write, Read		Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PB_AMP_LOAD_OP_BIAS	6:5	PB	Selects the Class AB Mode Amplifier Output Stage Bias. In low-power mode, increasing this value increases the capacitive load drive capability of the amplifier.	0x0: 20µA 0x1: 40µA 0x2: 60µA 0x3: 80µA
PB_AMP_PWM_SEL	4	PB	Selects the nominal PWM switching frequency of the playback amplifier when it is in a Class-D operating region. The nominal PWM switching frequency is dependent on whether the system is operating from a clock base that is a multiple of 48kHz or 44.1kHz.	0x0: PWM switching frequency is 341.333kHz (48kHz clock base) or 313.6kHz (44.1kHz clock base). 0x1: PWM switching frequency is 384kHz (48kHz Clock Base) or 352.8kHz (44.1kHz clock base).
PB_AMP_OCP_AUTORESTART_EN	3	PB	Controls whether or not the playback amplifier automatically restarts after an overcurrent protection fault condition.	0x0: Playback amplifier overcurrent protection recovery is in manual mode. 0x1: Playback amplifier overcurrent protection recovery is in auto mode.
PB_AMP_MODE	2:0	PB	Selects the Playback Amplifier Operating Mode. This control is used to restrict the amplifier operating supplies and modes. By default, based on the output signal level, the playback amplifier automatically operates from multiple supply voltage sources (AVDD1, AVDD2, and AVDD3), and transitions as needed between low signal Class-AB (AVDD2) and high/mid signal Class-D modes (AVDD1 and AVDD3).	0x0: Normal operation 0x1: Restricts amplifier operation to the low signal Class-AB (AVDD2) and mid signal Class-D (AVDD3) regions only. 0x2: Reserved 0x3: Reserved 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved

Playback Amplifier Falling Slew Rate Controls (0x206A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	PB_AMP_SLEW_FALL[1:0]	
Reset	–	–	–	–	–	–	0x2	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PB_AMP_SLEW_FALL	1:0	PB	Selects the Class-D Playback Amplifier Output Falling Edge Slew Rate	0x0: Class-D falling edge slew rate is 5ns. 0x1: Class-D falling edge slew rate is 3.25ns. 0x2: Class-D falling edge slew rate is 2.25ns. 0x3: Class-D falling edge slew rate is 1.25ns.

Playback Amplifier Rising Slew Rate Controls (0x206B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	PB_AMP_SLEW_RISE[1:0]	
Reset	–	–	–	–	–	–	0x2	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PB_AMP_SLEW_RISE	1:0	PB	Selects the Class-D Playback Amplifier Output Rising Edge Slew Rate	0x0: Class-D rising edge slew rate is 5ns. 0x1: Class-D rising edge slew rate is 3.25ns. 0x2: Class-D rising edge slew rate is 2.25ns. 0x3: Class-D rising edge slew rate is 1.25ns.

Playback Amplifier SSM Controls (0x206C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	PB_AMP_SSM_VAL[1:0]		PB_AMP_SSM_EN
Reset	–	–	–	–	–	0x0		0x0
Access Type	–	–	–	–	–	Write, Read		Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PB_AMP_SSM_VAL	2:1	EN	Selects the Value of the Clock Period Variation for the Class-D Amplifier when SSM Mode is Enabled	0x0: SSM mode clock period variation of ±1.3%. 0x1: SSM mode clock period variation of ±2.5%. 0x2: SSM mode clock period variation of ±3.7%. 0x3: SSM mode clock period variation of ±4.9%.
PB_AMP_SSM_EN	0	EN	Enables Clock Period Spread-Sprectrum Modulation (SSM) for the Class-D Amplifier	0x0: Class-D SSM mode disabled. 0x1: Class-D SSM mode enabled.

Playback Digital Mute Control (0x206E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	PB_VOL_MUTE
Reset	–	–	–	–	–	–	–	0x1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PB_VOL_MUTE	0	–	Applies a Digital Mute to the Playback Channel Audio Signal. If ramping on mute and unmute is enabled, the volume is ramped up/down at the selected volume ramp rate.	0x0: Playback channel is not muted. 0x1: Playback channel is muted.

Playback Enable (0x206F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	PB_EN
Reset	–	–	–	–	–	–	–	0x1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PB_EN	0	–	Enables the playback channel and the amplifier output when the device enters or is already in the audio state.	0x0: Playback channel disabled. 0x1: Playback channel enabled.

DMIC Interface Clock Drive Strength Configuration (0x2075)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DMIC3_DRV[1:0]		DMIC2_DRV[1:0]		DMIC1_DRV[1:0]	
Reset	–	–	0x1		0x1		0x1	
Access Type	–	–	Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DMIC3_DRV	5:4	DMIC	Configures the Drive Strength of the DMC3 Output	0x0: Reduced drive mode (2mA) 0x1: Normal drive mode (4mA) 0x2: High drive mode (6mA) 0x3: Highest drive mode (8mA)
DMIC2_DRV	3:2	DMIC	Configures the Drive Strength of the DMC2 Output	0x0: Reduced drive mode (2mA) 0x1: Normal drive mode (4mA) 0x2: High drive mode (6mA) 0x3: Highest drive mode (8mA)
DMIC1_DRV	1:0	DMIC	Configures the Drive Strength of the DMC1 Output	0x0: Reduced drive mode (2mA) 0x1: Normal drive mode (4mA) 0x2: High drive mode (6mA) 0x3: Highest drive mode (8mA)

DMIC Interface Clock Configuration (0x2076)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	DMIC_FRAME_SEL	DMIC_RATE[1:0]	
Reset	–	–	–	–	–	0x0	0x2	
Access Type	–	–	–	–	–	Write, Read	Write, Read	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DMIC_FRAME_SEL	2	DMIC	Selects whether a rising or falling clock edge is used to start digital microphone interface frames (Channel 0). If the falling clock edge is selected, the PDM data from each falling clock edge is internally phase aligned to the data from the next rising clock edge. If the rising edge is selected, this is reversed.	0x0: DMIC interface PDM frames (Channel 0) begin on falling clock edges. 0x1: DMIC interface PDM frames (Channel 0) begin on rising clock edges.
DMIC_RATE	1:0	DMIC	Selects the nominal output DMIC clock rate and input DMIC data sample rate for all DMIC interfaces. DMIC clock is internally derived from the PCM bit clock, and values shown are for PCM sample rates that are integer ratios to 48kHz/44.1kHz.	0x0: 768kHz/705.6kHz 0x1: 1.536MHz/1.4112MHz 0x2: 3.072MHz/2.8224MHz 0x3: Reserved

DMIC Interface Enables (0x2077)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	DMIC3_EN	DMIC2_EN	DMIC1_EN
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DMIC3_EN	2	–	Enables the clock output and data input on digital microphone interface receiver 3.	0x0: DMIC interface 3 disabled 0x1: DMIC interface 3 enabled
DMIC2_EN	1	–	Enables the clock output and data input on digital microphone interface receiver 2.	0x0: DMIC interface 2 disabled 0x1: DMIC interface 2 enabled
DMIC1_EN	0	–	Enables the clock output and data input on digital microphone interface receiver 1.	0x0: DMIC interface 1 disabled 0x1: DMIC interface 1 enabled

AMIC 1 Configuration 1 (0x2080)

BIT	7	6	5	4	3	2	1	0
Field	AMIC1_FAST_CHRG_FORCE	AMIC1_FAST_CHRG_BYPASS	AMIC1_PGA_HIZ_EN	AMIC1_PGA_GAIN[3:0]				AMIC1_PGA_RIN
Reset	0x0	0x0	0x0	0x2				0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMIC1_FAST_CHRG_FORCE	7	–	Turn on Fast Charge of Device. Use to introduce fast charge timed by host.	0x0: Normal mode, fast charge is only enabled during transition to active unless bypass is set. 0x1: Channel in fast charge mode.
AMIC1_FAST_CHRG_BYPASS	6	AMIC1	Bypasses the fast charge during the transition from software shutdown to active.	0x0: Channel fast charges during transition from software shutdown to active (regardless of the state of AMIC1_EN). 0x1: Fast charge is bypassed during transition from software shutdown to active.
AMIC1_PGA_HIZ_EN	5	AMIC1	If the analog microphone 1 record input is disabled (software shutdown state or AMIC1_EN = 0), this selects whether or not the inputs present normal or high (Hi-Z) input resistance. This has no effect when the analog microphone 1 record input is enabled (active state and AMIC1_EN = 1).	0x0: When the AMIC 1 PGA is disabled, the input common mode voltage is disabled and the inputs present normal input resistance. 0x1: When the AMIC 1 PGA is disabled, the inputs remain weakly biased and present high (Hi-Z) input resistance.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMIC1_PGA_GAIN	4:1	AMIC1	Controls the AMIC 1 Preamplifier Gain	0x0: -6dB Gain 0x1: -3dB Gain 0x2: 0dB Gain 0x3: 3dB Gain 0x4: 6dB Gain 0x5: 9dB Gain 0x6: 12dB Gain 0x7: 15dB Gain 0x8: 18dB Gain 0x9: 21dB Gain 0xA to 0xF: Reserved
AMIC1_PGA_RIN	0	AMIC1	Configures the Input Resistance of the Analog Microphone 1 PGA. The lower input resistance mode offers a noise advantage for cases where higher PGA gain is required, while higher input resistance in normal mode is best paired with high swing and/or high output impedance analog microphones.	0x0: Normal input resistance mode 0x1: Reduced input resistance mode

AMIC 1 Configuration 2 (0x2081)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	AMIC1_DRE_EN	AMIC1_DITH_EN
Reset	–	–	–	–	–	–	0x1	0x1
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMIC1_DRE_EN	1	AMIC1	Enables Dyanmic Range Extension (DRE) for the AMIC 1 ADC	0x0: DRE Disabled 0x1: DRE Enabled
AMIC1_DITH_EN	0	AMIC1	Enables Dither for the AMIC 1 ADC	0x0: Dither disabled 0x1: Dither enabled

AMIC 2 Configuration 1 (0x2083)

BIT	7	6	5	4	3	2	1	0
Field	AMIC2_FAST_CHRG_FORCE	AMIC2_FAST_CHRG_BYPASS	AMIC2_PGA_HIZ_EN	AMIC2_PGA_GAIN[3:0]				AMIC2_PGA_RIN
Reset	0x0	0x0	0x0	0x2				0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMIC2_FAST_CHRG_FORCE	7	–	Turn on Fast Charge of Device. Use to introduce fast charge timed by host.	0x0: Normal mode, fast charge is only enabled during transition to active unless bypass is set. 0x1: Channel in fast charge mode.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMIC2_FAST_CHRG_BYPASS	6	AMIC2	Bypasses the fast charge during the transition from software shutdown to active.	0x0: Channel fast charges during transition from software shutdown to active (regardless of the state of AMIC2_EN). 0x1: Fast charge is bypassed during transition from software shutdown to active.
AMIC2_PGA_HIZ_EN	5	AMIC2	If the analog microphone 2 record input is disabled (software shutdown state or AMIC2_EN = 0), this selects whether or not the inputs present normal or high (Hi-Z) input resistance. This has no effect when the analog microphone 2 record input is enabled (active state and AMIC2_EN = 1).	0x0: When the AMIC 2 PGA is disabled, the input common mode voltage is disabled and the inputs present normal input resistance. 0x1: When the AMIC 2 PGA is disabled, the inputs remain weakly biased and present high (Hi-Z) input resistance.
AMIC2_PGA_GAIN	4:1	AMIC2	Controls the AMIC 2 Preamplifier Gain	0x0: -6dB Gain 0x1: -3dB Gain 0x2: 0dB Gain 0x3: 3dB Gain 0x4: 6dB Gain 0x5: 9dB Gain 0x6: 12dB Gain 0x7: 15dB Gain 0x8: 18dB Gain 0x9: 21dB Gain 0xA to 0xF: Reserved
AMIC2_PGA_RIN	0	–	Configures the Input Resistance of the Analog Microphone 2 PGA. The lower input resistance mode offers a noise advantage for cases where higher PGA gain is required, while higher input resistance in normal mode is best paired with high swing and/or high output impedance analog microphones.	0x0: Normal input resistance mode. 0x1: Reduced input resistance mode.

AMIC 2 Configuration 2 (0x2084)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	AMIC2_DRE_EN	AMIC2_DITH_EN
Reset	–	–	–	–	–	–	0x1	0x1
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMIC2_DRE_EN	1	AMIC2	Enables Dyanmic Range Extension (DRE) for the AMIC 2 ADC	0x0: DRE disabled 0x1: DRE enabled
AMIC2_DITH_EN	0	AMIC2	Enables Dither for the AMIC 2 ADC	0x0: Dither disabled 0x1: Dither enabled

AMIC 3 Configuration 1 (0x2086)

BIT	7	6	5	4	3	2	1	0
Field	AMIC3_FAST_CHRG_FORCE	AMIC3_FAST_CHRG_BYPASS	AMIC3_PGA_HIZ_EN	AMIC3_PGA_GAIN[3:0]				AMIC3_PGA_RIN
Reset	0x0	0x0	0x0	0x2				0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMIC3_FAST_CHRG_FORCE	7	–	Turn on Fast Charge of Device. Use to introduce fast charge timed by host.	0x0: Normal mode, fast charge is only enabled during transition to active unless bypass is set. 0x1: Channel in fast charge mode.
AMIC3_FAST_CHRG_BYPASS	6	AMIC3	Bypasses the fast charge during the transition from software shutdown to active.	0x0: Channel fast charges during transition from software shutdown to active (regardless of the state of AMIC3_EN). 0x1: Fast charge is bypassed during transition from software shutdown to active.
AMIC3_PGA_HIZ_EN	5	AMIC3	If the analog microphone 3 record input is disabled (software shutdown state or AMIC3_EN = 0), this selects whether or not the inputs present normal or high (Hi-Z) input resistance. This has no effect when the analog microphone 3 record input is enabled (active state and AMIC3_EN = 1).	0x0: When the AMIC 3 PGA is disabled, the input common-mode voltage is disabled, and the inputs present normal input resistance. 0x1: When the AMIC 3 PGA is disabled, the inputs remain weakly biased and present high (Hi-Z) input resistance.
AMIC3_PGA_GAIN	4:1	AMIC3	Controls the AMIC 3 Preamplifier Gain	0x0: -6dB Gain 0x1: -3dB Gain 0x2: 0dB Gain 0x3: 3dB Gain 0x4: 6dB Gain 0x5: 9dB Gain 0x6: 12dB Gain 0x7: 15dB Gain 0x8: 18dB Gain 0x9: 21dB Gain 0xA to 0xF: Reserved
AMIC3_PGA_RIN	0	AMIC3	Configures the input resistance of the analog microphone 3 PGA. The lower input resistance mode offers a noise advantage for cases where higher PGA gain is required, while higher input resistance in normal mode is best paired with high swing and/or high output impedance analog microphones.	0x0: Normal input resistance mode. 0x1: Reduced input resistance mode.

AMIC 3 Configuration 2 (0x2087)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	AMIC3_DRE_EN	AMIC3_DITH_EN
Reset	–	–	–	–	–	–	0x1	0x1
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMIC3_DRE_EN	1	AMIC3	Enables Dyanmic Range Extension (DRE) for the AMIC 3 ADC	0x0: DRE disabled 0x1: DRE enabled
AMIC3_DITH_EN	0	AMIC3	Enables Dither for the AMIC 3 ADC	0x0: Dither disabled 0x1: Dither enabled

AMIC Power Down Controls (0x208A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	AMIC3_PD	AMIC2_PD	AMIC1_PD
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMIC3_PD	2	–	Powers Down the Analog Components of the AMIC 3 Input PGA and ADC	0x0: AMIC 3 analog active 0x1: AMIC 3 analog powered down
AMIC2_PD	1	–	Powers Down the Analog Components of the AMIC 2 Input PGA and ADC	0x0: AMIC 2 analog active 0x1: AMIC 2 analog powered down
AMIC1_PD	0	–	Powers Down the Analog Components of the AMIC 1 Input PGA and ADC	0x0: AMIC 1 analog active 0x1: AMIC 1 analog powered down

AMIC Bias Configuration (0x208B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	AMIC_BIAS_PD_EN	AMIC_BIAS_LP_MODE	AMIC_BIAS_SEL[2:0]		
Reset	–	–	–	0x0	0x0	0x5		
Access Type	–	–	–	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMIC_BIAS_PD_EN	4	MBIAS	Allows the analog microphone bias generator to quickly discharge the analog microphone bias voltage level.	0x0: Disabled 0x1: Enabled
AMIC_BIAS_LP_MODE	3	MBIAS	Selects whether the analog microphone bias generator operates in low noise (default) or low-power mode.	0x0: AMIC bias low-noise mode 0x1: AMIC bias low-power mode

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMIC_BIAS_SEL	2:0	–	Selects the analog microphone bias generator output voltage.	0x0: 1.2V Output voltage 0x1: 1.5V Output voltage 0x2: 1.8V Output voltage 0x3: 2V Output voltage 0x4: 2.25V Output voltage 0x5: 2.5V Output voltage 0x6: 2.75V Output voltage 0x7: 3V Output voltage

AMIC Bias Output Enables (0x208C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	AMIC_BIAS_OUT3	AMIC_BIAS_OUT2	AMIC_BIAS_EN
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMIC_BIAS_OUT3	2	–	If AMIC bias is enabled, this enables the MICBIAS3 output. If AMIC bias is disabled or this is disabled, the MICBIAS3 output is disabled.	0x0: MICBIAS3 output disabled 0x1: MICBIAS3 output enabled if analog microphone bias is also enabled.
AMIC_BIAS_OUT2	1	–	If AMIC bias is enabled, this enables the MICBIAS2 output. If AMIC bias is disabled or this is disabled, the MICBIAS2 output is disabled.	0x0: MICBIAS2 output disabled 0x1: MICBIAS2 output enabled if analog microphone bias is also enabled.
AMIC_BIAS_EN	0	–	When enabled, the analog microphone bias generator is active. Microphone bias voltage is always output on MICBIAS1, and is optionally (if enabled) output on MICBIAS2 and MICBIAS3. If disabled, all microphone bias outputs are disabled.	0x0: Analog microphone bias is disabled. 0x1: Analog microphone bias enabled, and MICBIAS1 output enabled.

AMIC Input Configuration (0x208D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	AMIC_CT_SEL[1:0]	
Reset	–	–	–	–	–	–	0x1	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMIC_CT_SEL	1:0	EN	Selects the duration of the AMIC input coupling capacitance precharge time during AMIC input channel start up. This changes the expected duration of the device turn on time.	0x0: C_{IN} ≤ 1µF (3.7ms turn on time) 0x1: C_{IN} ≤ 2.2µF (5.2ms turn on time) 0x2: C_{IN} ≤ 4.7µF (9.2ms turn on time) 0x3: C_{IN} ≤ 10µF (17.2ms turn on time)

AMIC Power Mode Select (0x208E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	AMIC3_LP_MODE	AMIC2_LP_MODE	AMIC1_LP_MODE
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMIC3_LP_MODE	2	EN	Enables AMIC 3 Input Low-Power Mode	0x0: High-performance mode 0x1: Low-power mode
AMIC2_LP_MODE	1	EN	Enables AMIC 2 Input Low-Power Mode	0x0: High-performance mode 0x1: Low-power mode
AMIC1_LP_MODE	0	EN	Enables AMIC 1 Input Low-Power Mode	0x0: High-performance mode 0x1: Low-power mode

AMIC Enables (0x208F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	AMIC3_EN	AMIC2_EN	AMIC1_EN
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMIC3_EN	2	–	Enables the AMIC 3 Input PGA and ADC. This may be preset prior to exiting software shutdown or toggled dynamically in full function mode (with propoer sequencing). Has no effect in playback only mode.	0x0: AMIC 3 input disabled 0x1: AMIC 3 input enabled
AMIC2_EN	1	–	Enables the AMIC 2 Input PGA and ADC. This may be preset prior to exiting software shutdown or toggled dynamically in full function mode (with propoer sequencing). Has no effect in playback only mode.	0x0: AMIC 2 input disabled 0x1: AMIC 2 input enabled
AMIC1_EN	0	–	Enables the AMIC 1 Input PGA and ADC. This may be preset prior to exiting software shutdown or toggled dynamically in full function mode (with proper sequencing). Has no effect in playback only mode.	0x0: AMIC 1 input disabled 0x1: AMIC 1 input enabled

Record Channel 1 Configuration 1 (0x20A0)

BIT	7	6	5	4	3	2	1	0
Field	REC1_DELAY[3:0]				REC1_INVERT	REC1_DCBLK[1:0]		REC1_DCBLK_EN
Reset	0x0				0x0	0x0		0x1
Access Type	Write, Read				Write, Read	Write, Read		Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
REC1_DELAY	7:4	REC1	Adds Delay to Record Channel 1 Data. Delay is added in terms of number of samples at the internal DSP sample rate (DSP_SR) with a range from 0 to 7.5 samples with a 0.5 sample step size. The only exception occurs when the record channel sample rate (PCM_REC_SR) is set to 32kHz and the DSP sample rate (DSP_SR) is set to 96kHz. In this case, the maximum delay is limited to 3.5 samples (all settings above this are limited to this value).	0x0: No additional delay. 0x1: Add a 0.5 sample delay. 0x2: Add a 1 sample delay. 0x3: Add a 1.5 sample delay. 0x4 to 0xC: ... (0.5 Sample Increments) 0xD: Add a 6.5 sample delay. 0xE: Add a 7 sample delay. 0xF: Add a 7.5 sample delay.
REC1_INVERT	3	REC1	Inverts the Record Channel 1 Data	0x0: Non-inverted record channel 1 data 0x1: Inverted record channel 1 data
REC1_DCBLK	2:1	REC1	Sets the Record Channel 1 DC Blocking Filter Corner Frequency. The DC blocking corner frequency scales with record sample rate from 8kHz to 48kHz.	0x0: Record channel 1 DC blocking corner frequency scales from 0.312Hz at f_S = 8kHz to a maximum of 1.872Hz at f_S = 48kHz. 0x1: Record channel 1 blocking corner frequency scales from 2.496Hz at f_S = 8kHz to a maximum of 14.976Hz at f_S = 48kHz. 0x2: Reserved 0x3: Reserved
REC1_DCBLK_EN	0	REC1	Enables the Record Channel 1 DC Blocking Filter	0x0: Record channel 1 DC blocking filter disabled. 0x1: Record channel 1 DC blocking filter enabled.

Record Channel 1 Configuration 2 (0x20A1)

BIT	7	6	5	4	3	2	1	0
Field	REC1_GAIN[4:0]					REC1_SEL[2:0]		
Reset	0x0					0x0		
Access Type	Write, Read					Write, Read		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
REC1_GAIN	7:3	REC1	Record Channel 1 Digital Gain Correction. Typically needed when digital microphone inputs are used.	0x0: +0dB Gain 0x1: +1dB Gain 0x2: +2dB Gain 0x3: +3dB Gain 0x4 to 0x1C: ... 0x1D: +29dB Gain 0x1E: +30dB Gain 0x1F: +31dB Gain

BITFIELD	BITS	RES	DESCRIPTION	DECODE
REC1_SEL	2:0	REC1	Selects whether the source data for record channel 1 is taken from AMIC ADC 1 or a selected DMIC interface and channel.	0x0: Record channel 1 accepts data from AMIC ADC 1. 0x1: Record channel 1 accepts data from DMIC interface 1 channel 0. 0x2: Record channel 1 accepts data from DMIC interface 1 channel 1. 0x3: Record channel 1 accepts data from DMIC interface 2 channel 0. 0x4: Record channel 1 accepts data from DMIC interface 2 channel 1. 0x5: Record channel 1 accepts data from DMIC interface 3 channel 0. 0x6: Record channel 1 accepts data from DMIC interface 3 channel 1. 0x7: Reserved

Record Channel 1 Digital Volume Control (0x20A2)

BIT	7	6	5	4	3	2	1	0
Field	–	REC1_VOL[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	RES	DESCRIPTION	DECODE
REC1_VOL	6:0	REC1	Sets the Digital Volume Level of Record Channel 1	0x0: 0dB 0x1: -0.5dB 0x2: -1.0dB 0x3: -1.5dB ...: ... (-0.5dB steps) 0x7C: -62.0dB 0x7D: -62.5dB 0x7E: -63.0dB 0x7F: -63.5dB

Record Channel 2 Configuration 1 (0x20A4)

BIT	7	6	5	4	3	2	1	0
Field	REC2_DELAY[3:0]				REC2_INVERT	REC2_DCBLK[1:0]		REC2_DCBLK_EN
Reset	0x0				0x0	0x0		0x1
Access Type	Write, Read				Write, Read	Write, Read		Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
REC2_DELAY	7:4	REC2	Adds Delay to Record Channel 2 Data. Delay is added in terms of number of samples at the internal DSP sample rate (DSP_SR) with a range from 0 to 7.5 samples with a 0.5 sample step size. The only exception occurs when the record channel sample rate (PCM_REC_SR) is set to 32kHz and the DSP sample rate (DSP_SR) is set to 96kHz. In this case, the maximum delay is limited to 3.5 samples (all settings above this are limited to this value).	0x0: No additional delay. 0x1: Add a 0.5 sample delay. 0x2: Add a 1 sample delay. 0x3: Add a 1.5 sample delay. 0x4 to 0xC: ... (0.5 sample increments) 0xD: Add a 6.5 sample delay. 0xE: Add a 7 sample delay. 0xF: Add a 7.5 sample delay.
REC2_INVERT	3	REC2	Inverts the Record Channel 2 Data	0x0: Non-inverted record channel 2 data 0x1: Inverted record channel 2 data
REC2_DCBLK	2:1	REC2	Sets the Record Channel 2 DC Blocking Filter Corner Frequency. The DC blocking corner frequency scales with record sample rate from 8kHz to 48kHz.	0x0: Record channel 2 DC blocking corner frequency scales from 0.312Hz at f_S = 8kHz to a maximum of 1.872Hz at f_S = 48kHz. 0x1: Record channel 2 blocking corner frequency scales from 2.496Hz at f_S = 8kHz to a maximum of 14.976Hz at f_S = 48kHz. 0x2: Reserved 0x3: Reserved
REC2_DCBLK_EN	0	REC2	Enables the Record Channel 2 DC Blocking Filter	0x0: Record channel 2 DC blocking filter disabled. 0x1: Record channel 2 DC blocking filter enabled.

Record Channel 2 Configuration 2 (0x20A5)

BIT	7	6	5	4	3	2	1	0
Field	REC2_GAIN[4:0]					REC2_SEL[2:0]		
Reset	0x0					0x0		
Access Type	Write, Read					Write, Read		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
REC2_GAIN	7:3	REC2	Record Channel 2 Digital Gain Correction. Typically needed when digital microphone inputs are used.	0x0: +0dB Gain 0x1: +1dB Gain 0x2: +2dB Gain 0x3: +3dB Gain 0x4 to 0x1C: ... 0x1D: +29dB Gain 0x1E: +30dB Gain 0x1F: +31dB Gain

BITFIELD	BITS	RES	DESCRIPTION	DECODE
REC2_SEL	2:0	REC1	Selects whether the source data for record channel 2 is taken from AMIC ADC 2 or a selected DMIC interface and channel.	0x0: Record channel 2 accepts data from AMIC ADC 2. 0x1: Record channel 2 accepts data from DMIC interface 1 channel 0. 0x2: Record channel 2 accepts data from DMIC interface 1 channel. 0x3: Record channel 2 accepts data from DMIC interface 2 channel 0. 0x4: Record channel 2 accepts data from DMIC interface 2 channel 1. 0x5: Record channel 2 accepts data from DMIC interface 3 channel 0. 0x6: Record channel 2 accepts data from DMIC interface 3 channel 1. 0x7: Reserved

Record Channel 2 Digital Volume (0x20A6)

BIT	7	6	5	4	3	2	1	0
Field	–	REC2_VOL[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	RES	DESCRIPTION	DECODE
REC2_VOL	6:0	REC2	Sets the Digital Volume Level of Record Channel 2	0x0: 0dB 0x1: -0.5dB 0x2: -1.0dB 0x3: -1.5dB ...: ... (-0.5dB steps) 0x7C: -62.0dB 0x7D: -62.5dB 0x7E: -63.0dB 0x7F: -63.5dB

Record Channel 3 Configuration 1 (0x20A8)

BIT	7	6	5	4	3	2	1	0
Field	REC3_DELAY[3:0]				REC3_INVERT	REC3_DCBLK[1:0]		REC3_DCBLK_EN
Reset	0x0				0x0	0x0		0x1
Access Type	Write, Read				Write, Read	Write, Read		Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
REC3_DELAY	7:4	REC3	Adds Delay to Record Channel 3 Data. Delay is added in terms of number of samples at the internal DSP sample rate (DSP_SR) with a range from 0 to 7.5 samples with a 0.5 sample step size. The only exception occurs when the record channel sample rate (PCM_REC_SR) is set to 32kHz and the DSP sample rate (DSP_SR) is set to 96kHz. In this case, the maximum delay is limited to 3.5 samples (all settings above this are limited to this value).	0x0: No additional delay. 0x1: Add a 0.5 sample delay. 0x2: Add a 1 sample delay. 0x3: Add a 1.5 sample delay. 0x4 to 0xC: ... (0.5 sample Increments) 0xD: Add a 6.5 sample delay. 0xE: Add a 7 sample delay. 0xF: Add a 7.5 sample delay.
REC3_INVERT	3	REC3	Inverts the Record Channel 3 Data	0x0: Non-inverted record channel 3 data. 0x1: Inverted record channel 3 data.
REC3_DCBLK	2:1	REC3	Sets the Record Channel 3 DC Blocking Filter Corner Frequency. The DC blocking corner frequency scales with record sample rate from 8kHz to 48kHz.	0x0: Record channel 3 DC blocking corner Frequency Scales from 0.312Hz at f_S = 8kHz to a Maximum of 1.872Hz at f_S = 48kHz. 0x1: Record channel 3 blocking corner frequency scales from 2.496Hz at f_S = 8kHz to a maximum of 14.976Hz at f_S = 48kHz. 0x2: Reserved 0x3: Reserved
REC3_DCBLK_EN	0	REC3	Enables the Record Channel 3 DC Blocking Filter	0x0: Record channel 3 DC blocking filter disabled. 0x1: Record channel 3 DC blocking filter enabled.

Record Channel 3 Configuration 2 (0x20A9)

BIT	7	6	5	4	3	2	1	0
Field	REC3_GAIN[4:0]					REC3_SEL[2:0]		
Reset	0x0					0x0		
Access Type	Write, Read					Write, Read		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
REC3_GAIN	7:3	REC3	Record Channel 3 Digital Gain Correction. Typically needed when digital microphone inputs are used.	0x0: +0dB Gain 0x1: +1dB Gain 0x2: +2dB Gain 0x3: +3dB Gain 0x4 to 0x1C: ... 0x1D: +29dB Gain 0x1E: +30dB Gain 0x1F: +31dB Gain

BITFIELD	BITS	RES	DESCRIPTION	DECODE
REC3_SEL	2:0	REC3	Selects whether the source data for record channel 3 is taken from AMIC ADC 3 or a selected DMIC interface and channel.	0x0: Record channel 3 accepts data from AMIC ADC 3. 0x1: Record channel 3 accepts data from DMIC interface 1 channel 0. 0x2: Record channel 3 accepts data from DMIC interface 1 channel 1. 0x3: Record channel 3 accepts data from DMIC interface 2 channel 0. 0x4: Record channel 3 accepts data from DMIC interface 2 channel 1. 0x5: Record channel 3 accepts data from DMIC interface 3 channel 0. 0x6: Record channel 3 accepts data from DMIC interface 3 channel 1. 0x7: Reserved

Record Channel 3 Digital Volume (0x20AA)

BIT	7	6	5	4	3	2	1	0
Field	–	REC3_VOL[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	RES	DESCRIPTION	DECODE
REC3_VOL	6:0	REC3	Sets the Digital Volume Level of Record Channel 3	0x0: 0dB 0x1: -0.5dB 0x2: -1.0dB 0x3: -1.5dB ...: ... (-0.5dB steps) 0x7C: -62.0dB 0x7D: -62.5dB 0x7E: -63.0dB 0x7F: -63.5dB

Record Channel 4 Configuration 1 (0x20AC)

BIT	7	6	5	4	3	2	1	0
Field	REC4_DELAY[3:0]				REC4_INVERT	–	–	–
Reset	0x0				0x0	–	–	–
Access Type	Write, Read				Write, Read	–	–	–

BITFIELD	BITS	RES	DESCRIPTION	DECODE
REC4_DELAY	7:4	REC4	Adds Delay to Record Channel 4 Data. Delay is added in terms of number of samples at the internal DSP sample rate (DSP_SR) with a range from 0 to 7.5 samples with a 0.5 sample step size. The only exception occurs when the record channel sample rate (PCM_REC_SR) is set to 32kHz and the DSP sample rate (DSP_SR) is set to 96kHz. In this case, the maximum delay is limited to 3.5 samples (all settings above this are limited to this value).	0x0: No additional delay. 0x1: Add a 0.5 sample delay. 0x2: Add a 1 sample delay. 0x3: Add a 1.5 sample delay. 0x4 to 0xC: ... (0.5 sample increments) 0xD: Add a 6.5 sample delay. 0xE: Add a 7 sample delay. 0xF: Add a 7.5 sample delay.
REC4_INVERT	3	REC4	Inverts the Record Channel 4 Data	0x0: Non-inverted record channel 4 data. 0x1: Inverted record channel 4 data.

Record Channel Enables (0x20AF)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	REC4_PCM_EN	REC3_PCM_EN	REC2_PCM_EN	REC1_PCM_EN
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read, Pulse

BITFIELD	BITS	RES	DESCRIPTION	DECODE
REC4_PCM_EN	3	–	Enables PCM record channel 4 when the device enters or is already in the active state. When enabled, the PCM record channel 4 data is assigned to the PCM data output channel/slot selected with the PCM_REC4_SLOT bit field. PCM record channel 4 has a fixed input source (no input select control), and is used to monitor the playback channel output digital data.	0x0: PCM record channel 4 disabled. 0x1: PCM record channel 4 enabled.
REC3_PCM_EN	2	–	Enables PCM record channel 3 when the device enters or is already in the active state. When enabled, the PCM record channel 3 data is assigned to the PCM data output channel/slot selected with the PCM_REC3_SLOT bit field.	0x0: PCM record channel 3 disabled. 0x1: PCM record channel 3 enabled.
REC2_PCM_EN	1	–	Enables PCM record channel 2 when the device enters or is already in the active state. When enabled, the PCM record channel 2 data is assigned to the PCM data output channel/slot selected with the PCM_REC2_SLOT bit field.	0x0: PCM record channel 2 disabled. 0x1: PCM record channel 2 enabled.
REC1_PCM_EN	0	–	Enables PCM record channel 1 when the device enters or is already in the active state. When enabled, the PCM record channel 1 data is assigned to the PCM data output channel/slot selected with the PCM_REC1_SLOT bit field.	0x0: PCM record channel 1 disabled. 0x1: PCM record channel 1 enabled.

Digital Filter Channel 1 Bank A Configuration (0x20B0)

BIT	7	6	5	4	3	2	1	0
Field	–	DF1_GAIN_BKA[2:0]			DF1_BQ_BKA_EN[3:0]			
Reset	–	0x0			0x0			
Access Type	–	Write, Read			Write, Read, Ext			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF1_GAIN_BKA	6:4	–	Sets the digital gain offset for digital filter channel 1 bank A. Can be changed anytime this bank is inactive.	0x0: 0dB 0x1: +6dB 0x2: +12dB 0x3: +18dB 0x4: +24dB 0x5: +30dB 0x6: +36dB 0x7: +42dB
DF1_BQ_BKA_EN	3:0	–	Enable control for the digital filter channel 1 bank A biquad filter bands. Can be changed anytime this bank is inactive. Bands are incrementally enabled in series, and this control selects the number of enabled bands when bank A is active.	0x0: DF1 biquad filter fully disabled. 0x1: DF1 biquad filter band 1 enabled. 0x2: DF1 biquad filter bands 1 and 2 enabled. 0x3: DF1 biquad filter bands 1 to 3 enabled. 0x3 to 0xA: ... 0xB: DF1 biquad filter bands 1 to 11 enabled. 0xC: DF1 biquad filter bands 1 to 12 enabled. 0xD to 0xF: Reserved

Digital Filter Channel 1 Bank A Volume (0x20B1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DF1_VOL_BKA[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read, Ext					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF1_VOL_BKA	5:0	–	Sets the digital volume level of digital filter channel 1 bank A. Can be changed at any time—even while the bank is active. If ramping is enabled, it occurs on all volume changes.	0x0: 0dB 0x1: -0.5dB 0x2: -1.0dB 0x3: -1.5dB ...: ... (-0.5dB steps) 0x3C: -30.0dB 0x3D: -30.5dB 0x3E: -31.0dB 0x3F: -31.5dB

Digital Filter Channel 1 Bank B Configuration (0x20B2)

BIT	7	6	5	4	3	2	1	0
Field	–	DF1_GAIN_BKB[2:0]			DF1_BQ_BKB_EN[3:0]			
Reset	–	0x0			0x0			
Access Type	–	Write, Read			Write, Read			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF1_GAIN_BKB	6:4	–	Sets the digital gain offset for digital filter channel 1 bank B. Can be changed anytime this bank is inactive.	0x0: 0dB 0x1: +6dB 0x2: +12dB 0x3: +18dB 0x4: +24dB 0x5: +30dB 0x6: +36dB 0x7: +42dB
DF1_BQ_BKB_EN	3:0	–	Enable control for the digital filter channel 1 bank B biquad filter bands. Can be changed anytime this bank is inactive. Bands are incrementally enabled in series, and this control selects the number of enabled bands when bank B is active.	0x0: DF1 biquad filter fully disabled. 0x1: DF1 biquad filter band 1 enabled. 0x2: DF1 biquad filter bands 1 and 2 enabled. 0x3: DF1 biquad filter bands 1 to 3 enabled. 0x3 to 0xA: ... 0xB: DF1 biquad filter bands 1 to 11 enabled. 0xC: DF1 biquad filter bands 1 to 12 enabled. 0xD to 0xF: Reserved

Digital Filter Channel 1 Bank B Volume (0x20B3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DF1_VOL_BKB[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read, Ext					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF1_VOL_BKB	5:0	–	Sets the digital volume level of digital filter channel 1 bank B. Can be changed at any time—even while the bank is active. If ramping is enabled, it occurs on all volume changes.	0x0: 0dB 0x1: -0.5dB 0x2: -1.0dB 0x3: -1.5dB ...: ... (-0.5dB steps) 0x3C: -30.0dB 0x3D: -30.5dB 0x3E: -31.0dB 0x3F: -31.5dB

Digital Filter Channel 1 Ramp Configuration (0x20B4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	DF1_VOL_RMP_RATE[3:0]				DF1_VOL_RMP_EN
Reset	–	–	–	0x7				0x1
Access Type	–	–	–	Write, Read				Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF1_VOL_RMP_RATE	4:1	–	Selects the ramp rate for digital filter channel 1 on enable/disable, mute/unmute, and volume changes.	0x0: 4ms ramp rate 0x1: 8ms ramp rate 0x2: 16ms ramp rate 0x3: 32ms ramp rate 0x4: 64ms ramp rate 0x5: 128ms ramp rate 0x6: 256ms ramp rate 0x7: 512ms ramp rate 0x8: 1024ms ramp rate 0x9: 2048ms ramp rate 0xA to 0xF: Reserved
DF1_VOL_RMP_EN	0	–	Enables digital filter channel 1 ramping on enable, disable, mute, and any volume change.	0x0: Ramping disabled 0x1: Ramping enabled

Digital Filter Channel 1 Configuration (0x20B5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DF1_DCBLK[1:0]		DF1_DCBLK_EN	DF1_ULTRA_EN
Reset	–	–	–	–	0x0		0x1	0x0
Access Type	–	–	–	–	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF1_DCBLK	3:2	DF1	Sets the digital filter channel 1 DC blocking filter corner frequency. The selected corner frequency is dependent on the configured digital filter channel sample rate (DSP_SR).	0x0: DF1 DC blocking corner frequency is set to either 3.744Hz (DSP_SR = 96kHz) or 1.872Hz (DSP_SR = 192kHz/384Hz). 0x1: DF1 DC blocking corner frequency is set to either 14.976Hz (DSP_SR = 96kHz) or 7.488Hz (DSP_SR = 192kHz/384kHz). 0x2: DF1 DC blocking corner frequency is set to either 29.952Hz (DSP_SR = 96kHz) or 14.976Hz (DSP_SR = 192kHz/384kHz). 0x3: DF1 DC blocking corner frequency is set to either 59.904Hz (DSP_SR = 96kHz) or 29.952Hz (DSP_SR = 192kHz/384kHz).
DF1_DCBLK_EN	1	DF1	Enables the Digital Filter Channel 1 DC Blocking Filter	0x0: DC blocking filter disabled. 0x1: DC blocking filter enabled.
DF1_ULTRA_EN	0	DF1	Enables the Digital Filter Channel 1 Ultrasound Filter	0x0: Ultrasound filter disabled. 0x1: Ultrasound filter enabled.

Digital Filter Channel 1 DRC Attack Configuration 1 (0x20B8)

BIT	7	6	5	4	3	2	1	0
Field	DF1_DRC_ATK_WF[15:8]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION
DF1_DRC_ATK_WF	7:0	DF1	Sets the value of the DRC attack weighting factor (α_{ATK}, often called a forgetting factor) used to configure the desired DRC attack time constant. When the signal level is increasing, α_{ATK} is used in the running RMS signal level calculations to set the weighted ratio of the current to the previous RMS signal level calculation.

Digital Filter Channel 1 DRC Attack Configuration 2 (0x20B9)

BIT	7	6	5	4	3	2	1	0
Field	DF1_DRC_ATK_WF[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION
DF1_DRC_ATK_WF	7:0	DF1	Sets the value of the DRC attack weighting factor (α_{ATK}, often called a forgetting factor) used to configure the desired DRC attack time constant. When the signal level is increasing, α_{ATK} is used in the running RMS signal level calculations to set the weighted ratio of the current to the previous RMS signal level calculation.

Digital Filter Channel 1 DRC Release Configuration 1 (0x20BA)

BIT	7	6	5	4	3	2	1	0
Field	DF1_DRC_RLS_WF[15:8]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION
DF1_DRC_RLS_WF	7:0	DF1	Sets the value of the DRC attack weighting factor (α_{RLS}, often called a forgetting factor) used to configure the desired DRC release time constant. When the signal level is decreasing, α_{RLS} is used in the running RMS signal level calculations to set the weighted ratio of the current to the previous RMS signal level calculation.

Digital Filter Channel 1 DRC Release Configuration 2 (0x20BB)

BIT	7	6	5	4	3	2	1	0
Field	DF1_DRC_RLS_WF[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION
DF1_DRC_RLS_WF	7:0	DF1	Sets the value of the DRC attack weighting factor (α_{RLS}, often called a forgetting factor) used to configure the desired DRC release time constant. When the signal level is decreasing, α_{RLS} is used in the running RMS signal level calculations to set the weighted ratio of the current to the previous RMS signal level calculation.

Digital Filter Channel 1 DRC Threshold (0x20BC)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DF1_DRC_THR[5:0]					
Reset	–	–	0x1					
Access Type	–	–	Write, Read					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF1_DRC_THR	5:0	DF1	Sets the digital filter channel 1 DRC threshold (relative to full-scale).	0x0: Reserved 0x1: DRC threshold is 0dBFS. 0x2: DRC threshold is -1dBFS. 0x3 to 0x3C: ... (-1dBFS steps) 0x3D: DRC threshold is -60dBFS. 0x3E: DRC threshold is -61dBFS. 0x3F: DRC threshold is -62dBFS.

Digital Filter Channel 1 DRC Enable (0x20BD)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DF1_DRC_INST_RLS	DF1_DRC_INST_ATK	DF1_DRC_CMP[2:0]			DF1_DRC_EN
Reset	–	–	0x0	0x0	0x0			0x0
Access Type	–	–	Write, Read	Write, Read	Write, Read			Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF1_DRC_INST_RLS	5	DF1	Enables digital filter channel 1 DRC instant release mode. When enabled, the value of the programmed DRC release weighting factor (α_{RLS}) is ignored, and the DRC release time is instead instant.	0x0: DRC instant release mode disabled. 0x1: DRC instant release Mode enabled.
DF1_DRC_INST_ATK	4	DF1	Enables digital filter channel 1 DRC instant attack mode. When enabled, the value of the programmed DRC attack weighting factor (α_{ATK}) is ignored, and the DRC attack time is instead instant.	0x0: DRC instant attack mode disabled. 0x1: DRC instant attack mode enabled.
DF1_DRC_CMP	3:1	DF1	Sets the digital filter channel 1 DRC compression ratio (in dB).	0x0: Compression ratio is 2:1. 0x1: Compression ratio is 5:1. 0x2: Compression ratio is 10:1. 0x3: Compression ratio is 20:1. 0x4: Compression ratio is 30:1. 0x5: Compression ratio is 40:1. 0x6: Compression ratio is 60:1. 0x7: Compression ratio is ∞:1.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF1_DRC_EN	0	DF1	Enables the digital filter channel 1 DRC.	0x0: DRC Disabled 0x1: DRC Enabled

Digital Filter Channel 2 Bank A Enable (0x20C0)

BIT	7	6	5	4	3	2	1	0
Field	–	DF2_GAIN_BKA[2:0]			DF2_BQ_BKA_EN[3:0]			
Reset	–	0x0			0x0			
Access Type	–	Write, Read			Write, Read			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF2_GAIN_BKA	6:4	–	Sets the digital gain offset for digital filter channel 2 bank A. Can be changed anytime this bank is inactive.	0x0: 0dB 0x1: +6dB 0x2: +12dB 0x3: +18dB 0x4: +24dB 0x5: +30dB 0x6: +36dB 0x7: +42dB
DF2_BQ_BKA_EN	3:0	–	Enable control for the digital filter channel 2 bank A biquad filter bands. Bands are incrementally enabled in series, and this control selects the number of enabled bands when bank A is active.	0x0: DF2 biquad filter fully disabled. 0x1: DF2 biquad filter band 1 enabled. 0x2: DF2 biquad filter bands 1 and 2 enabled. 0x3: DF2 biquad filter bands 1 to 3 enabled. 0x3 to 0xA: ... 0xB: DF2 biquad filter bands 1 to 11 enabled. 0xC: DF2 biquad filter bands 1 to 12 enabled. 0xD to 0xF: Reserved

Digital Filter Channel 2 Bank A Volume (0x20C1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DF2_VOL_BKA[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read, Ext					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF2_VOL_BKA	5:0	–	Sets the digital volume level of digital filter channel 1 Bank A. Can be changed at any time - even while the bank is active. If ramping is enabled, it occurs on all volume changes.	0x0: 0dB 0x1: -0.5dB 0x2: -1.0dB 0x3: -1.5dB ...: ... (-0.5dB steps) 0x3C: -30.0dB 0x3D: -30.5dB 0x3E: -31.0dB 0x3F: -31.5dB

Digital Filter Channel 2 Biquad Bank B Enable (0x20C2)

BIT	7	6	5	4	3	2	1	0
Field	–	DF2_GAIN_BKB[2:0]			DF2_BQ_BKB_EN[3:0]			
Reset	–	0x0			0x0			
Access Type	–	Write, Read			Write, Read			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF2_GAIN_BKB	6:4	–	Sets the digital gain offset for digital filter channel 2 bank B. Can be changed anytime this bank is inactive.	0x0: 0dB 0x1: +6dB 0x2: +12dB 0x3: +18dB 0x4: +24dB 0x5: +30dB 0x6: +36dB 0x7: +42dB
DF2_BQ_BKB_EN	3:0	–	Enable control for the digital filter channel 2 bank B biquad filter bands. Bands are incrementally enabled in series, and this control selects the number of enabled bands when bank B is active.	0x0: DF2 biquad filter fully disabled. 0x1: DF2 biquad filter band 1 enabled. 0x2: DF2 biquad filter bands 1 and 2 enabled. 0x3: DF2 biquad filter bands 1 to 3 enabled. 0x3 to 0xA: ... 0xB: DF2 biquad filter bands 1 to 11 enabled. 0xC: DF2 biquad filter bands 1 to 12 enabled. 0xD to 0xF: Reserved

Digital Filter Channel 2 Bank B Volume (0x20C3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DF2_VOL_BKB[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read, Ext					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF2_VOL_BKB	5:0	–	Sets the digital volume level of digital filter channel 1 Bank B. Can be changed at any time—even while the bank is active. If ramping is enabled, it occurs on all volume changes.	0x0: 0dB 0x1: -0.5dB 0x2: -1.0dB 0x3: -1.5dB ...: ... (-0.5dB steps) 0x3C: -30.0dB 0x3D: -30.5dB 0x3E: -31.0dB 0x3F: -31.5dB

Digital Filter Channel 2 Ramp Configuration (0x20C4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	DF2_VOL_RMP_RATE[3:0]				DF2_VOL_RMP_EN
Reset	–	–	–	0x7				0x1
Access Type	–	–	–	Write, Read				Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF2_VOL_RMP_RATE	4:1	–	Selects the ramp rate for digital filter channel 2 on enable/disable, mute/unmute, and volume changes.	0x0: 4ms ramp rate 0x1: 8ms ramp rate 0x2: 16ms ramp rate 0x3: 32ms ramp rate 0x4: 64ms ramp rate 0x5: 128ms ramp rate 0x6: 256ms ramp rate 0x7: 512ms ramp rate 0x8: 1024ms ramp rate 0x9: 2048ms ramp rate 0xA to 0xF: Reserved
DF2_VOL_RMP_EN	0	–	Enables digital filter channel 2 ramping on enable, disable, mute, and any volume change.	0x0: Ramping disabled 0x1: Ramping enabled

Digital Filter Channel 2 Configuration (0x20C5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DF2_DCBLK[1:0]		DF2_DCBLK_EN	DF2_ULTRA_EN
Reset	–	–	–	–	0x0		0x1	0x0
Access Type	–	–	–	–	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF2_DCBLK	3:2	DF2	Sets the digital filter channel 2 DC blocking filter corner frequency. The selected corner frequency is dependent on the configured digital filter channel sample rate (DSP_SR).	0x0: DF2 DC blocking corner frequency is set to either 3.744Hz (DSP_SR = 96kHz) or 1.872Hz (DSP_SR = 192kHz/384Hz). 0x1: DF2 DC blocking corner frequency is set to either 14.976Hz (DSP_SR = 96kHz) or 7.488Hz (DSP_SR = 192kHz/384kHz). 0x2: DF2 DC blocking corner frequency is set to either 29.952Hz (DSP_SR = 96kHz) or 14.976Hz (DSP_SR = 192kHz/384kHz). 0x3: DF2 DC blocking corner frequency is set to either 59.904Hz (DSP_SR = 96kHz) or 29.952Hz (DSP_SR = 192kHz/384kHz).
DF2_DCBLK_EN	1	DF2	Enables the digital filter channel 2 DC blocking filter.	0x0: DC blocking filter disabled. 0x1: DC blocking filter enabled.
DF2_ULTRA_EN	0	DF2	Enables the digital filter channel 2 ultrasound filter.	0x0: Ultrasound filter disabled. 0x1: Ultrasound filter enabled.

Digital Filter Channel 2 DRC Attack Configuration 1 (0x20C8)

BIT	7	6	5	4	3	2	1	0
Field	DF2_DRC_ATK_WF[15:8]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION
DF2_DRC_ATK_WF	7:0	DF2	Sets the value of the DRC attack weighting factor (α_{ATK}, often called a forgetting factor) used to configure the desired DRC attack time constant. When the signal level is increasing, α_{ATK} is used in the running RMS signal level calculations to set the weighted ratio of the current to the previous RMS signal level calculation.

Digital Filter Channel 2 DRC Attack Configuration 2 (0x20C9)

BIT	7	6	5	4	3	2	1	0
Field	DF2_DRC_ATK_WF[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION
DF2_DRC_ATK_WF	7:0	DF2	Sets the value of the DRC attack weighting factor (α_{ATK}, often called a forgetting factor) used to configure the desired DRC attack time constant. When the signal level is increasing, α_{ATK} is used in the running RMS signal level calculations to set the weighted ratio of the current to the previous RMS signal level calculation.

Digital Filter Channel 2 DRC Release Configuration 1 (0x20CA)

BIT	7	6	5	4	3	2	1	0
Field	DF2_DRC_RLS_WF[15:8]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION
DF2_DRC_RLS_WF	7:0	DF2	Sets the value of the DRC attack weighting factor (α_{RLS}, often called a forgetting factor) used to configure the desired DRC release time constant. When the signal level is decreasing, α_{RLS} is used in the running RMS signal level calculations to set the weighted ratio of the current to the previous RMS signal level calculation.

Digital Filter Channel 2 DRC Release Configuration 2 (0x20CB)

BIT	7	6	5	4	3	2	1	0
Field	DF2_DRC_RLS_WF[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION
DF2_DRC_RLS_WF	7:0	DF2	Sets the value of the DRC attack weighting factor (α_{RLS}, often called a forgetting factor) used to configure the desired DRC release time constant. When the signal level is decreasing, α_{RLS} is used in the running RMS signal level calculations to set the weighted ratio of the current to the previous RMS signal level calculation.

Digital Filter Channel 2 DRC Threshold (0x20CC)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DF2_DRC_THR[5:0]					
Reset	–	–	0x1					
Access Type	–	–	Write, Read					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF2_DRC_THR	5:0	DF2	Sets the digital filter channel 2 DRC threshold (relative to full-scale).	0x0: Reserved 0x1: DRC threshold is 0dBFS. 0x2: DRC threshold is -1dBFS. 0x3 to 0x3C: ... (-1dBFS steps) 0x3D: DRC threshold is -60dBFS. 0x3E: DRC threshold is -61dBFS. 0x3F: DRC threshold is -62dBFS.

Digital Filter Channel 2 DRC Enable (0x20CD)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DF2_DRC_INST_RLS	DF2_DRC_INST_ATK	DF2_DRC_CMP[2:0]			DF2_DRC_EN
Reset	–	–	0x0	0x0	0x0			0x0
Access Type	–	–	Write, Read	Write, Read	Write, Read			Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF2_DRC_INST_RLS	5	DF2	Enables digital filter channel 2 DRC instant release mode. When enabled, the value of the programmed DRC release weighting factor (α_{RLS}) is ignored, and the DRC release time is instead instant.	0x0: DRC instant release mode disabled. 0x1: DRC instant release mode enabled.
DF2_DRC_INST_ATK	4	DF2	Enables digital filter channel 2 DRC instant attack mode. When enabled, the value of the programmed DRC attack weighting factor (α_{ATK}) is ignored, and the DRC attack time is instead instant.	0x0: DRC instant attack mode disabled. 0x1: DRC instant attack mode enabled.
DF2_DRC_CMP	3:1	DF2	Sets the digital filter channel 2 DRC compression ratio (in dB).	0x0: Compression ratio is 2:1. 0x1: Compression ratio is 5:1. 0x2: Compression ratio is 10:1. 0x3: Compression ratio is 20:1. 0x4: Compression ratio is 30:1. 0x5: Compression ratio is 40:1. 0x6: Compression ratio is 60:1. 0x7: Compression ratio is ∞:1.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF2_DRC_EN	0	DF2	Enables the digital filter channel 2 DRC.	0x0: DRC Disabled 0x1: DRC Enabled

Playback Compensation Channel Bank A Biquad Enable (0x20D0)

BIT	7	6	5	4	3	2	1	0
Field	–	PBC_GAIN_BKA[2:0]			PBC_BQ_BKA_EN[3:0]			
Reset	–	0x0			0x0			
Access Type	–	Write, Read			Write, Read			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PBC_GAIN_BKA	6:4	–	Sets the digital gain offset for the playback compensation channel bank A. Can be changed anytime this bank is inactive.	0x0: 0dB 0x1: +6dB 0x2: +12dB 0x3: +18dB 0x4: +24dB 0x5: +30dB 0x6: +36dB 0x7: +42dB
PBC_BQ_BKA_EN	3:0	–	Enable control for the playback compensation channel bank A biquad filter bands. Bands are incrementally enabled in series, and this control selects the number of enabled bands when bank A is active.	0x0: Playback compensation biquad filter fully disabled. 0x1: Playback compensation biquad filter band 1 enabled. 0x2: Playback compensation biquad filter bands 1 and 2 enabled. 0x3: Playback compensation biquad filter bands 1 to 3 enabled. 0x3 to 0x8: ... 0x9: Playback compensation biquad filter bands 1 to 9 enabled. 0xA: Playback compensation biquad filter bands 1 to 10 enabled. 0xB to 0xF: Reserved

Playback Compensation Channel Bank A Volume (0x20D1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PBC_VOL_BKA[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read, Ext					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PBC_VOL_BKA	5:0	–	Sets the digital volume level of the playback compensation channel bank A. Can be changed at any time—even while the bank is active. If ramping is enabled, it occurs on all volume changes.	0x0: 0dB 0x1: -0.5dB 0x2: -1.0dBdB 0x3: -1.5dB ...: ... (-0.5dB steps) 0x3C: -30.0dB 0x3D: -30.5dB 0x3E: -31.0dB 0x3F: -31.5dB

Playback Compensation Channel Bank B Biquad Enable (0x20D2)

BIT	7	6	5	4	3	2	1	0
Field	–	PBC_GAIN_BKB[2:0]			PBC_BQ_BKB_EN[3:0]			
Reset	–	0x0			0x0			
Access Type	–	Write, Read			Write, Read			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PBC_GAIN_BKB	6:4	–	Sets the digital gain offset for the playback compensation channel bank B. Can be changed anytime this bank is inactive.	0x0: 0dB 0x1: +6dB 0x2: +12dB 0x3: +18dB 0x4: +24dB 0x5: +30dB 0x6: +36dB 0x7: +42dB
PBC_BQ_BKB_EN	3:0	–	Enable control for the playback compensation channel bank B biquad filter bands. Bands are incrementally enabled in series, and this control selects the number of enabled bands when bank B is active.	0x0: Playback compensation biquad filter fully disabled. 0x1: Playback compensation biquad filter band 1 enabled. 0x2: Playback compensation biquad filter bands 1 and 2 enabled. 0x3: Playback compensation biquad filter bands 1 to 3 enabled. 0x3 to 0x8: ... 0x9: Playback compensation biquad filter bands 1 to 9 enabled. 0xA: Playback compensation biquad filter bands 1 to 10 enabled. 0xB to 0xF: Reserved

Playback Compensation Channel Bank B Volume (0x20D3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PBC_VOL_BKB[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read, Ext					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PBC_VOL_BKB	5:0	–	Sets the digital volume level of the playback compensation channel bank B. Can be changed at any time—even while the bank is active. If ramping is enabled, it occurs on all volume changes.	0x0: 0dB 0x1: -0.5dB 0x2: -1.0dBdB 0x3: -1.5dB ...: ... (-0.5dB steps) 0x3C: -30.0dB 0x3D: -30.5dB 0x3E: -31.0dB 0x3F: -31.5dB

Playback Compensation Channel Ramp Configuration (0x20D4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	PBC_VOL_RMP_RATE[3:0]				PBC_VOL_RMP_EN
Reset	–	–	–	0x7				0x1
Access Type	–	–	–	Write, Read				Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PBC_VOL_RMP_RATE	4:1	–	Selects the ramp rate for the playback compensation channel on enable/disable, mute/unmute, and volume changes.	0x0: 4ms ramp rate 0x1: 8ms ramp rate 0x2: 16ms ramp rate 0x3: 32ms ramp rate 0x4: 64ms ramp rate 0x5: 128ms ramp rate 0x6: 256ms ramp rate 0x7: 512ms ramp rate 0x8: 1024ms ramp rate 0x9: 2048ms ramp rate 0xA to 0xF: Reserved
PBC_VOL_RMP_EN	0	–	Enables playback compensation channel ramping on enable, disable, mute, and any volume change.	0x0: Ramping disabled 0x1: Ramping enabled

Digital Filter Channel Configuration (0x20DC)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	DF2_SEL	DF1_SEL
Reset	–	–	–	–	–	–	0x0	0x0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DF2_SEL	1	DF2	Selects the microphone input channel data source for digital filter channel 2.	0x0: Digital fIlter channel 2 input data source is microphone input channel 2. 0x1: Digital fIlter channel 2 input data source is microphone input channel 3.
DF1_SEL	0	FFEN	Selects the input data source for digital filter channel 1.	0x0: Digital fIlter channel 1 input data source is microphone input channel 1. 0x1: Digital fIlter channel 1 input data source is microphone input channel 3.

Digital Filter Channel Biquad Bank Select (0x20DD)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	PBC_BQ_BK_SEL	DF2_BQ_BK_SEL	DF1_BQ_BK_SEL
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–	Write, Read, Pulse	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PBC_BQ_BK_SEL	2	–	Selects the active biquad coefficient bank for the playback compensation channel. When the channel is enabled, it powers up using the selected biquad bank (if the biquad filter for that bank is enabled). If this is changed while the channel is active, the channel transitions between the active and inactive bank at the selected ramp rate (if ramping is enabled).	0x0: Selects biquad coefficient bank A. 0x1: Selects biquad coefficient bank B.
DF2_BQ_BK_SEL	1	–	Selects the active biquad coefficient bank for digital filter channel 2. When the channel is enabled, it powers up using the selected biquad bank (if the biquad filter for that bank is enabled). If this is changed while the channel is active, the channel transitions between the active and inactive bank at the selected ramp rate (if ramping is enabled).	0x0: Selects biquad coefficient bank A. 0x1: Selects biquad coefficient bank B.
DF1_BQ_BK_SEL	0	–	Selects the active biquad coefficient bank for digital filter channel 1. When the channel is enabled, it powers up using the selected biquad bank (if the biquad filter for that bank is enabled). If this is changed while the channel is active, the channel transitions between the active and inactive bank at the selected ramp rate (if ramping is enabled).	0x0: Selects biquad coefficient bank A. 0x1: Selects biquad coefficient bank B.

Digital Filter Channel Mute Controls (0x20DE)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	PBC_VOL_MUTE	DF2_VOL_MUTE	DF1_VOL_MUTE
Reset	–	–	–	–	–	0x1	0x1	0x1
Access Type	–	–	–	–	–	Write, Read, Pulse	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PBC_VOL_MUTE	2	–	Applies a digital mute to the playback compensation channel. If ramping on mute and unmute is enabled, the volume is ramped up/down at the selected mute ramp rate.	0x0: Playback compensation channel is not muted. 0x1: Playback compensation channel is muted.
DF2_VOL_MUTE	1	–	Applies a digital mute to digital filter channel 2. If ramping on mute and unmute is enabled, the volume is ramped up/down at the selected mute ramp rate.	0x0: Digital filter channel 2 is not muted. 0x1: Digital filter channel 2 is muted.
DF1_VOL_MUTE	0	–	Applies a digital mute to digital filter channel 1. If ramping on mute and unmute is enabled, the volume is ramped up/down at the selected mute ramp rate.	0x0: Digital filter channel 1 is not muted. 0x1: Digital filter channel 1 is muted.

Digital Filter Channel Enables (0x20DF)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	PBC_EN	DF2_EN	DF1_EN
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read, Pulse

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PBC_EN	2	–	Enables the playback compensation channel (when the device is in the audio state).	0x0: Playaback compensation channel disabled. 0x1: Playaback compensation channel enabled.
DF2_EN	1	–	Enables digital filter channel 2 (when the device is in the audio state).	0x0: Digital filter channel 2 disabled. 0x1: Digital filter channel 2 enabled.
DF1_EN	0	–	Enables digital filter channel 1 (when the device is in the audio state).	0x0: Digital filter channel 1 disabled. 0x1: Digital filter channel 1 enabled.

Clock Monitor Configuration (0x20F1)

BIT	7	6	5	4	3	2	1	0
Field	–	CMON_BSELTOL[2:0]			CMON_ERRTOL[2:0]			CMON_AUTORESTART_EN
Reset	–	0x0			0x0			0x1
Access Type	–	Write, Read			Write, Read			Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
CMON_BSELTOL	6:4	EN	Sets the number of frames with incorrect (or correct) clock ratio (BCLKs per LRCLK) required to trigger (or recover from) a clock framing error.	0x0: Trigger after 1 incorrect LRCLK frame, and recover after 1 correct LRCLK frame. 0x1: Trigger after 2 incorrect LRCLK frames, and recover after 16 correct LRCLK frames. 0x2: Trigger after 3 incorrect LRCLK frames, and recover after 24 correct LRCLK frames. 0x3: Trigger after 4 incorrect LRCLK frames, and recover after 32 correct LRCLK frames. 0x4: Trigger after 5 incorrect LRCLK frames, and recover after 40 correct LRCLK frames. 0x5: Trigger after 6 incorrect LRCLK frames, and recover after 48 correct LRCLK frames. 0x6: Trigger after 7 incorrect LRCLK frames, and recover after 56 correct LRCLK frames. 0x7: Trigger after 8 incorrect LRCLK frames, and recover after 64 correct LRCLK frames.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
CMON_ERRTOL	3:1	EN	Selects the number of incorrect (or correct) LRCLk periods needed to trigger (or recover from) a frame clock (LRCLK) frequency error.	0x0: Trigger after 1 incorrect LRCLK frame, and recover after 1 correct LRCLK frame. 0x1: Trigger after 2 incorrect LRCLK frames, and recover after 16 correct LRCLK frames. 0x2: Trigger after 3 incorrect LRCLK frames, and recover after 24 correct LRCLK frames. 0x3: Trigger after 4 incorrect LRCLK frames, and recover after 32 correct LRCLK frames. 0x4: Trigger after 5 incorrect LRCLK frames, and recover after 40 correct LRCLK frames. 0x5: Trigger after 6 incorrect LRCLK frames, and recover after 48 correct LRCLK frames. 0x6: Trigger after 7 incorrect LRCLK frames, and recover after 56 correct LRCLK frames. 0x7: Trigger after 8 incorrect LRCLK frames, and recover after 64 correct LRCLK frames.
CMON_AUTORESTART_EN	0	EN	Controls whether or not the device can automatically recover from a clock error. If enabled, the device resumes audio record and/or playback once the clock monitor detects valid clocking (after audio was disabled due to a clock error).	0x0: Clock monitor is in manual mode. 0x1: Clock monitor is in auto mode.

Clock Monitor Enable (0x20F2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	CMON_EN
Reset	–	–	–	–	–	–	–	0x1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
CMON_EN	0	EN	Enables the PCM interface bit clock and frame clock monitor.	0x0: Clock monitor disabled. 0x1: Clock monitor enabled.

Data Monitor Configuration (0x20F4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DMON_MAG_THRES[1:0]		DMON_STUCK_THRES[1:0]		DMON_DURATION[1:0]	
Reset	–	–	0x0		0x0		0x0	
Access Type	–	–	Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DMON_MAG_THRES	5:4	EN	Sets the data magnitude error threshold that the input PCM data amplitude level is compared against. If the input signal is above this threshold for longer than the DMON_DURATION, a data monitor error is asserted.	0x0: Sets the data magnitude error threshold to -30.1030dBFS (5-bits). 0x1: Sets the data magnitude error threshold to -24.0824dBFS (4-bits). 0x2: Sets the data magnitude error threshold to -18.0618.1030dBFS (3-bits). 0x3: Sets the data magnitude error threshold to -12.0412dBFS (2-bits).
DMON_STUCK_THRES	3:2	EN	Sets the data stuck error threshold that the input PCM data amplitude level is compared against. If the input signal is stuck at the same value above this threshold for longer than the DMON_DURATION, a data monitor error is asserted.	0x0: Sets the data stuck error threshold to -90.3090dBFS (15-bits). 0x1: Sets the data stuck error threshold to -78.2678dBFS (13-bits). 0x2: Sets the data stuck error threshold to -66.2266dBFS (11-bits). 0x3: Sets the data stuck error threshold to -54.1854dBFS (9-bits).
DMON_DURATION	1:0	EN	Sets the time duration over which the data monitor must consecutively detect erroneous input PCM data (DIN) before asserting a data monitor magnitude or stuck error.	0x0: Error duration must exceed 64ms. 0x1: Error duration must exceed 256ms. 0x2: Error duration must exceed 1.024s. 0x3: Error duration must exceed 4.096s.

Data Monitor Enables (0x20F5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	DMON_MAG_EN	DMON_STUCK_EN
Reset	–	–	–	–	–	–	0x1	0x1
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DMON_MAG_EN	1	EN	Enables the data monitor to detect PCM input data magnitude errors. The data monitor is fully disabled when both data magnitude and stuck error detection is disabled.	0x0: Data monitor magnitude error detection disabled. 0x1: Data monitor magnitude error detection enabled.
DMON_STUCK_EN	0	EN	Enables the data monitor to detect PCM input data stuck errors. The data monitor is fully disabled when both data magnitude and stuck error detection is disabled.	0x0: Data monitor stuck error detection disabled. 0x1: Data monitor stuck error detection enabled.

System Level Configuration (0x20FE)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	FLL_ERR_AUTORESTART_EN	DSP_SR[1:0]	
Reset	–	–	–	–	–	0x0	0x1	
Access Type	–	–	–	–	–	Write, Read	Write, Read	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
FLL_ERR_AUTORESTART_EN	2	EN	Controls whether or not the device attempts to automatically recover from an FLL lock error. If disabled, the device is placed in the software shutdown state on FLL lock errors. If enabled, the device automatically returns to the audio state once FLL lock is restored.	0x0: FLL lock error recovery is in manual mode. 0x1: FLL lock error recovery is in automatic mode.
DSP_SR	1:0	EN	Selects the sample rate at which the core internal device DSP and digital filter channels run. The precise rate is based upon the sample rate (LRCLK rate) selected for the PCM interface and playback channel (PCM_PB_SR), and is a multiple of the same clock base (48kHz or 44.1kHz clock base ratio).	0x0: Internal DSP sample rate is 96kHz (for a 48kHz clock base) or 88.2kHz (for a 44.1kHz clock base). 0x1: Internal DSP sample rate is 192kHz (for a 48kHz clock base) or 176.4kHz (for a 44.1kHz clock base). 0x2: Internal DSP sample rate is 384kHz (for a 48kHz clock base) or 352.8kHz (for a 44.1kHz clock base). 0x3: Reserved

Device System Level Enables (0x20FF)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	AUDIO_EN
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read, Ext

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AUDIO_EN	0	–	Global audio enable is used to place the device into software shutdown, or to allow the device to exit software shutdown (if all other conditions are met). In software shutdown, all internal blocks are disabled except for the I^2C control interface, the device register contents, and any currently active fault modes.	0x0: Device is held in software shutdown. 0x1: Device is not held in software shutdown.

Device ID MSB (0x28FD)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[15:8]							
Reset	0x80							
Access Type	Read Only							

BITFIELD	BITS	RES	DESCRIPTION
DEV_ID	7:0	–	Upper two digits of the device identification number.

Device ID LSB (0x28FE)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[7:0]							
Reset	0x50							
Access Type	Read Only							

BITFIELD	BITS	RES	DESCRIPTION
DEV_ID	7:0	–	Lower two digits of the device identification number.

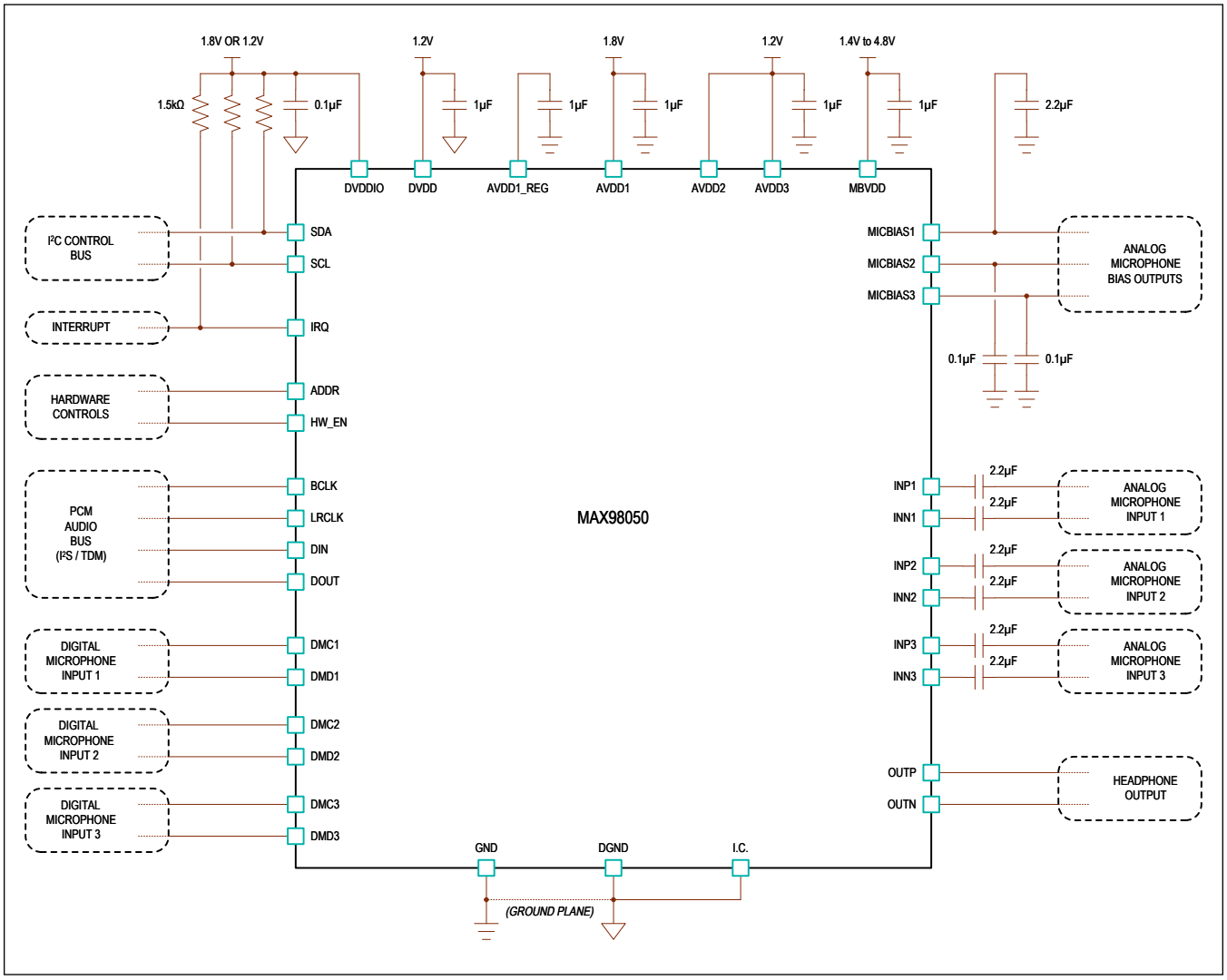
Revision ID (0x28FF)

BIT	7	6	5	4	3	2	1	0
Field	REV_ID[7:0]							
Reset	0x41							
Access Type	Read Only							

BITFIELD	BITS	RES	DESCRIPTION
REV_ID	7:0	–	Contains the current device revision identification number. Updated for every device revision.

Typical Application Circuits

Typical Use Case with PCM Mode Record and Playback



Ordering Information

Part Number	Temperature Range	Pin-Package
MAX98050ENX+	-40°C to +85°C	36-WLP
MAX98050ENX+T	-40°C to +85°C	36-WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/20	Initial release	—

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