EVALUATION KIT AVAILABLE

MAX98304

Mono 3.2W Class D Amplifier

General Description

The MAX98304 mono 3.2W Class D amplifier provides Class AB audio performance with Class D efficiency. This device offers five selectable gain settings (0dB, 3dB, 6dB, 9dB, and 12dB) set by a single gain-select input (GAIN).

Active emissions-limiting, edge-rate, and overshoot control circuitry greatly reduces EMI. A filterless spread-spectrum modulation scheme eliminates the need for output filtering found in traditional Class D devices. These features reduce application component count.

The IC's 0.95mA at 3.7V (1.2mA at 5V) quiescent current extends battery life in portable applications.

The IC is available in a 9-bump (1.0mm x 1.0mm) WLP with 0.3mm pitch that is specified over the extended -40°C to +85°C temperature range.

Applications

Notebook and Netbook Computers

Cellular Phones

Tablets

MP3 Players

Portable Audio Players

VoIP Phones

Features

- **Low Quiescent Current: 0.95mA at 3.7V**
- **Spread Spectrum and Active Emissions Limiting**
- **Five Pin-Selectable Gains**
- **19µV$_{RMS}$ Ultra-Low Noise**
- **90dB PSRR**
- **Click-and-Pop Suppression**
- **Thermal and Overcurrent Protection**
- **Low-Current Shutdown Mode**
- **1.0mm x 1.0mm, 9-Bump WLP (0.3mm Pitch) Space-Saving Package**

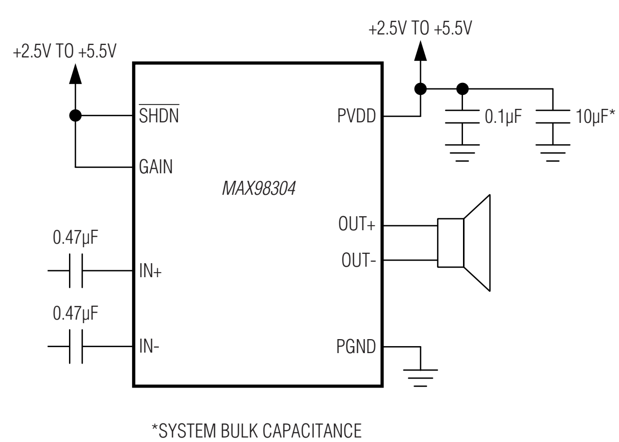
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX98304EWL+	-40°C to +85°C	9 WLP	AIR

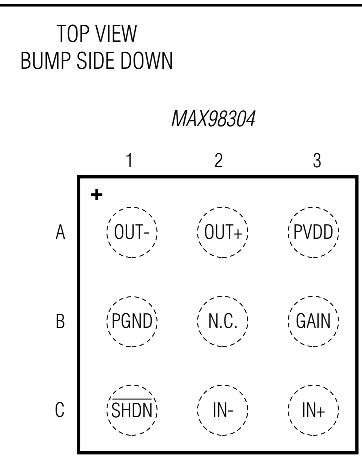
+Denotes a lead(Pb)-free/RoHS-compliant package.

Visit www.maximintegrated.com/products/patents for product patent marking information.

Typical Application Circuit



Bump Configuration



WLP (1mm x 1mm x 0.64mm 0.3mm PITCH)

ABSOLUTE MAXIMUM RATINGS

PVDD, IN+, IN-, $\overline{SHDN}$, GAIN to PGND..................-0.3V to +6V
All Other Pins to PGND ....-0.3V to (V_{PVDD} + 0.3V)
Continuous Current Into/Out of PVDD, PGND, OUT_... ±750mA
Continuous Input Current (all other pins)........................ ±20mA
Duration of Short Circuit Between
OUT_ and PVDD, PGND ....Continuous
OUT+ and OUT- ....Continuous

Continuous Power Dissipation (T_A = +70°C) for Multilayer Board
9-Bump WLP (derate 10.6mW/°C) 848mW
Junction Temperature ....+150°C
Operating Temperature Range.......................... -40°C to +85°C
Storage Temperature Range............................ -65°C to +150°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{PVDD} = $V_{\overline{SHDN}}$ = 5.0V, V_{PGND} = 0V, A_V = 12dB (GAIN = PGND), R_L = ∞, R_L connected between OUT+ to OUT-, AC measurement bandwidth 20Hz to 22kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	PVDD	Inferred from PSRR test		2.5		5.5	V
Undervoltage Lockout	UVLO	PVDD falling		1.5	1.8	2.2	V
Quiescent Supply Current	I_{DD}	T_A = +25°C			1.2	1.8	mA
		V_{PVDD} = 3.7V			0.95		
Shutdown Supply Current	I_{SHDN}	$V_{\overline{SHDN}}$ = 0V, T_A = +25°C			< 0.1	10	µA
Turn-On Time	t_{ON}				3.4	10	ms
Bias Voltage	V_{BIAS}				V_{PVDD} /2		V
Input Resistance	R_{IN}	T_A = +25°C, single-ended	A_V = 12dB	45	70		kΩ
			A_V = 9dB	64	100		
			A_V = 6dB	90	140		
			A_V = 3dB	128	200		
			A_V = 0dB	180	280		
Voltage Gain	A_V	Connect GAIN to PGND		11.5	12	12.5	dB
		Connect GAIN to PGND through 100kΩ ±5%		8.5	9	9.5	
		Connect GAIN to PVDD		5.5	6	6.5	
		Connect GAIN to PVDD through 100kΩ ±5%		2.5	3	3.5	
		GAIN unconnected		-0.5	0	+0.5	
Output Offset Voltage	V_{OS}	T_A = +25°C (Note 3)			±1	±4.5	mV
Click and Pop	K_{CP}	Peak voltage, A-weighted, 32 samples per second, R_L = 8Ω (Notes 3, 4)	Into shutdown		-74		dBV
			Out of shutdown		-60		
Common-Mode Rejection Ratio	CMRR	f_{IN} = 1kHz, input referred			80		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{PVDD} = $V_{\overline{SHDN}}$ = 5.0V, V_{PGND} = 0V, A_V = 12dB (GAIN = PGND), R_L = ∞, R_L connected between OUT+ to OUT-, AC measurement bandwidth 20Hz to 22kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio (Note 3)	PSRR	V_{PVDD} = 2.5V to 5.5V, T_A = +25°C		72	90		dB
		V_{RIPPLE} = 200mV_{P-P}	f = 217Hz		80		
			f = 1kHz		84		
			f = 20kHz		84		
Output Power	P_{OUT}	THD+N = 10%, f = 1kHz, R_L = 4Ω + 33µH	V_{PVDD} = 5.0V		3.2		W
			V_{PVDD} = 4.2V		2.2		
			V_{PVDD} = 3.7V		1.7		
		THD+N = 1%, f = 1kHz, R_L = 4Ω + 33µH	V_{PVDD} = 5.0V		2.6		
			V_{PVDD} = 4.2V		1.8		
			V_{PVDD} = 3.7V		1.4		
		THD+N = 10%, f = 1kHz, R_L = 8Ω + 68µH	V_{PVDD} = 5.0V		1.8		
			V_{PVDD} = 4.2V		1.2		
			V_{PVDD} = 3.7V		0.96		
		THD+N = 1%, f = 1kHz, R_L = 8Ω + 68µH	V_{PVDD} = 5.0V		1.4		
			V_{PVDD} = 4.2V		1		
			V_{PVDD} = 3.7V		0.8		
Total Harmonic Distortion Plus Noise	THD+N	f_{IN} = 1kHz	R_L = 4Ω, P_{OUT} = 1W		0.03	0.1	%
			R_L = 8Ω, P_{OUT} = 0.7W		0.03		
Oscillator Frequency	f_{OSC}				300		kHz
Spread-Spectrum Bandwidth					±12.5		kHz
Efficiency	η	P_{OUT} = 1.75W, R_L = 8Ω			93		%
Noise	V_N	A-weighted (Note 3)	A_V = 12dB		31		µV_{RMS}
			A_V = 9dB		26		
			A_V = 6dB		23		
			A_V = 3dB		21		
			A_V = 0dB		19		
Output Current Limit	I_{LIM}				2.8		A
Thermal Shutdown Level					155		°C
Thermal Shutdown Hysteresis					15		°C
DIGITAL INPUT ($\overline{SHDN}$)							
Input-Voltage High	V_{INH}	V_{PVDD} = 2.5V to 5.5V		1.4			V
Input-Voltage Low	V_{INL}	V_{PVDD} = 2.5V to 5.5V				0.4	V
Input Leakage Current		T_A = +25°C				±1	µA

Note 1: This device is 100% production tested at +25°C. All temperature limits are guaranteed by design.

Note 2: Testing performed with a resistive load in series with an inductor to simulate an actual speaker load. For R_L = 4Ω, L = 33µH. For R_L = 8Ω, L = 68µH.

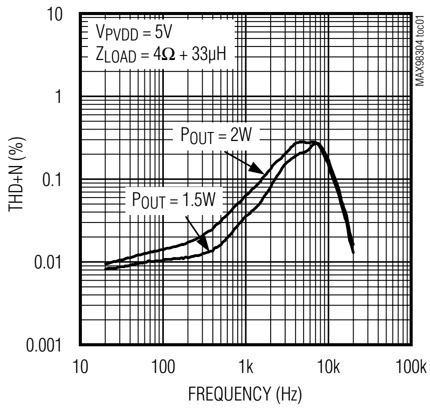
Note 3: Amplifier inputs AC-coupled to ground.

Note 4: Mode transitions controlled by $\overline{SHDN}$.

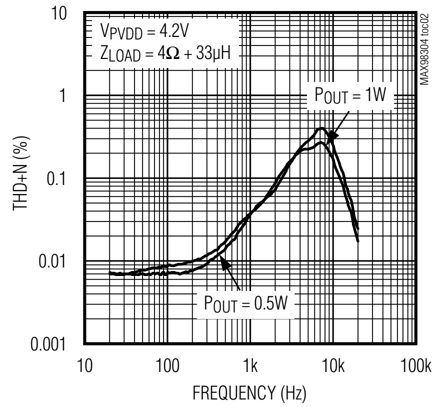
Typical Operating Characteristics

($V_{PVDD} = V_{\overline{SHDN}} = 5.0V$, $V_{PGND} = 0V$, $A_V = 6dB$, $R_L = \infty$, R_L connected between OUT+ to OUT-, AC measurement bandwidth 20Hz to 22kHz, $T_A = +25°C$, unless otherwise noted.)

TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



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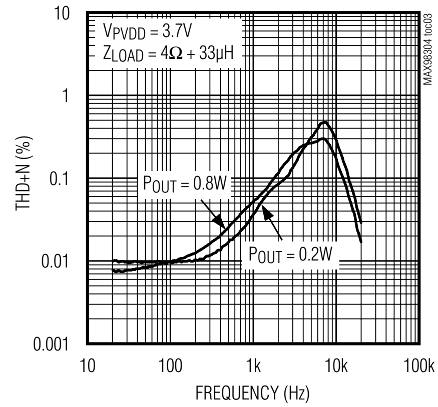

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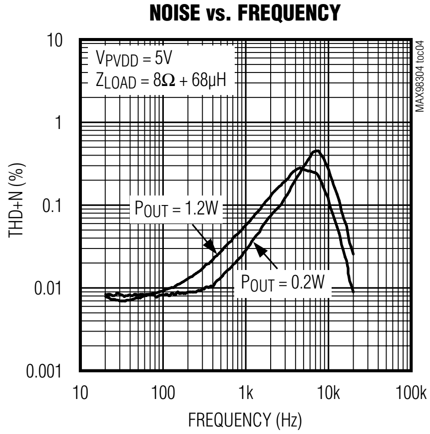
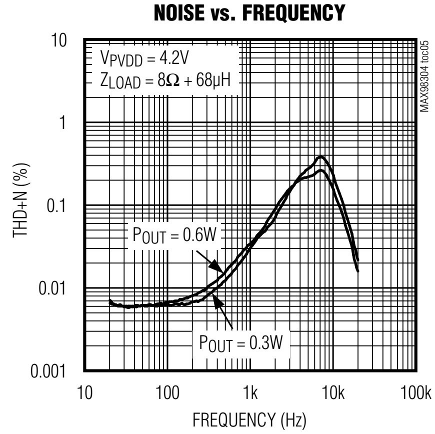
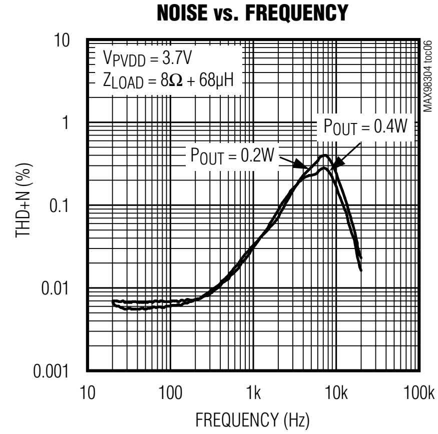


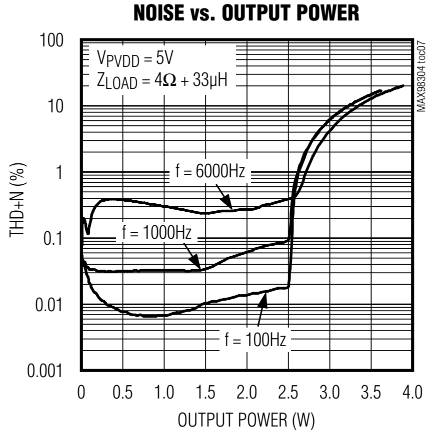
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



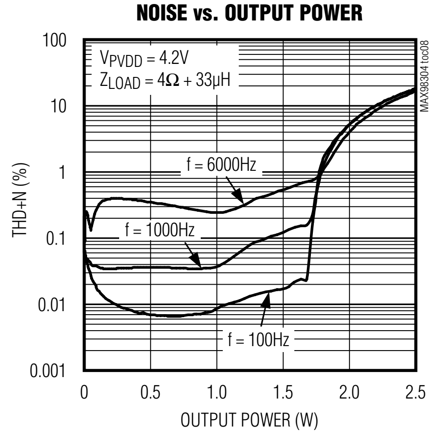
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



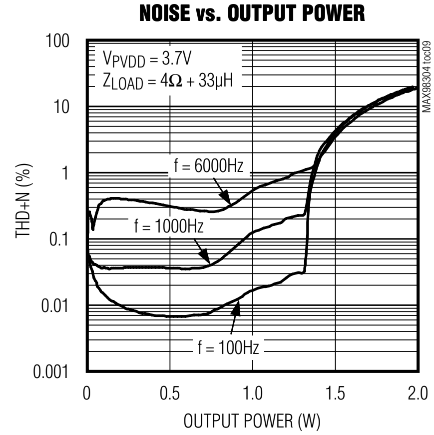
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



Typical Operating Characteristics (continued)

($V_{PVDD} = V_{\overline{SHDN}}$ = 5.0V, V_{PGND} = 0V, A_V = 6dB, $R_L = \infty$, R_L connected between OUT+ to OUT-, AC measurement bandwidth 20Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

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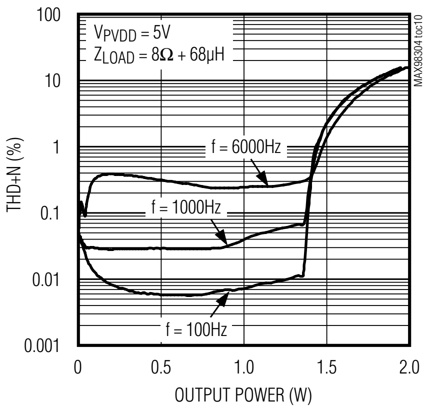
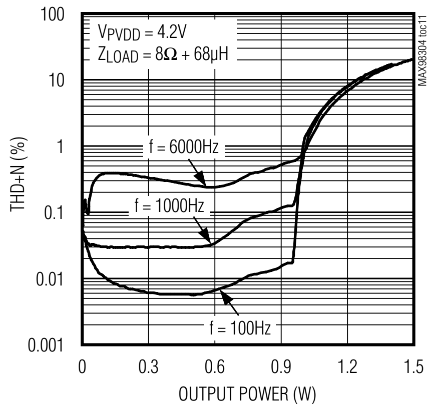
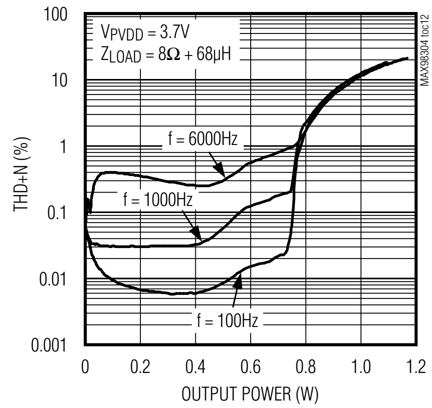


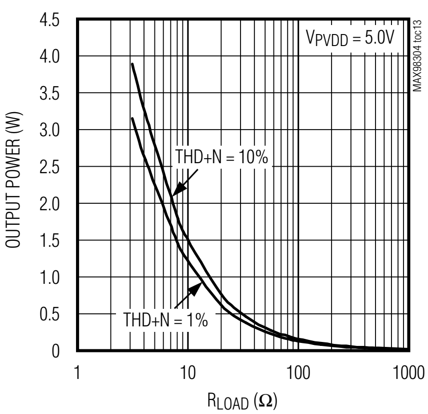
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



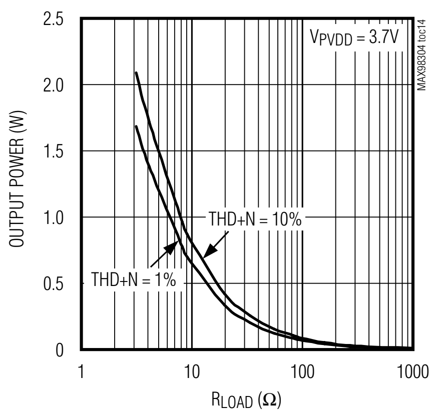
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



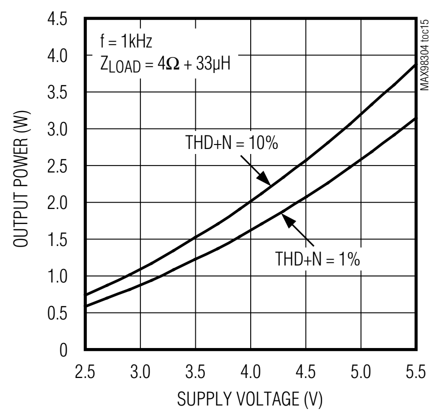
OUTPUT POWER vs. LOAD RESISTANCE



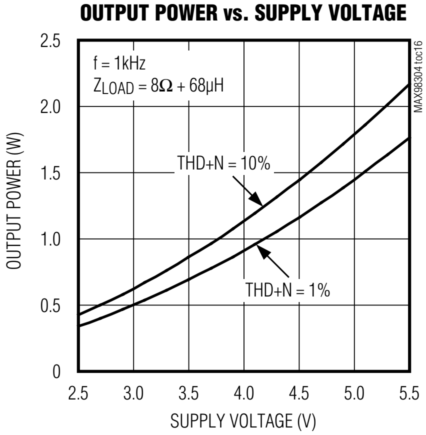
OUTPUT POWER vs. LOAD RESISTANCE



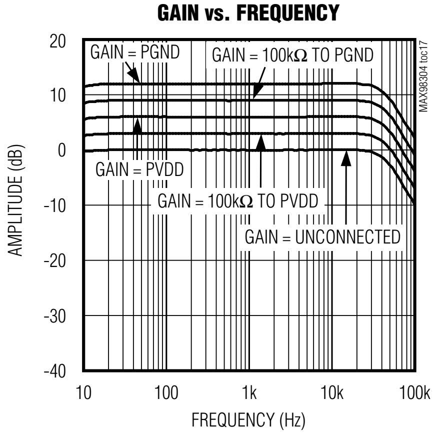
OUTPUT POWER vs. SUPPLY VOLTAGE



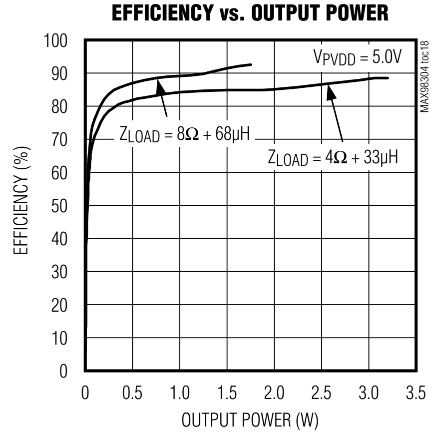
OUTPUT POWER vs. SUPPLY VOLTAGE



GAIN vs. FREQUENCY



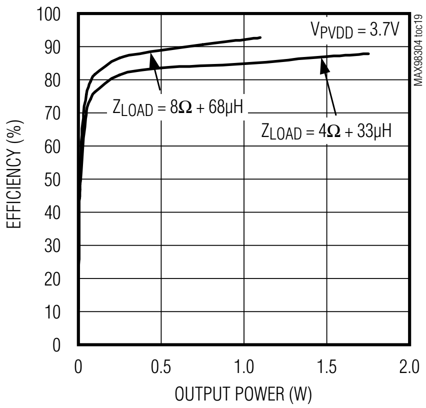
EFFICIENCY vs. OUTPUT POWER



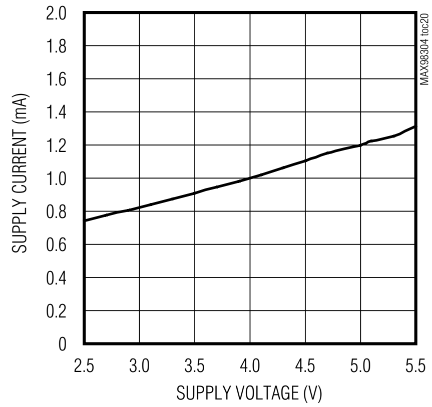
Typical Operating Characteristics (continued)

($V_{PVDD} = V_{\overline{SHDN}} = 5.0V$, $V_{PGND} = 0V$, $A_V = 6dB$, $R_L = \infty$, R_L connected between OUT+ to OUT-, AC measurement bandwidth 20Hz to 22kHz, $T_A = +25°C$, unless otherwise noted.)

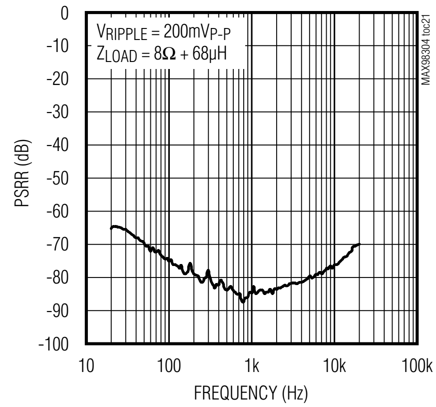
EFFICIENCY vs. OUTPUT POWER



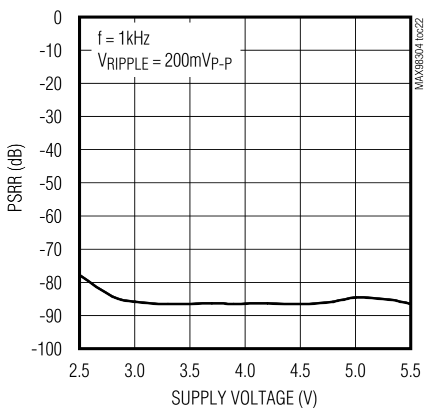
SUPPLY CURRENT vs. SUPPLY VOLTAGE



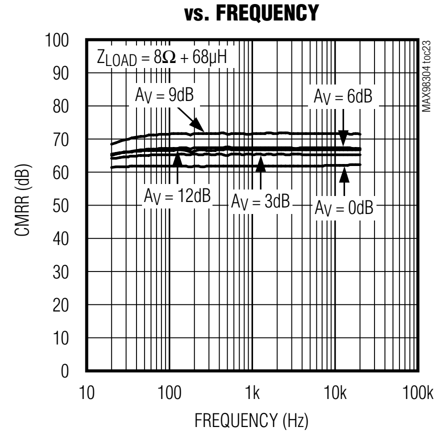
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



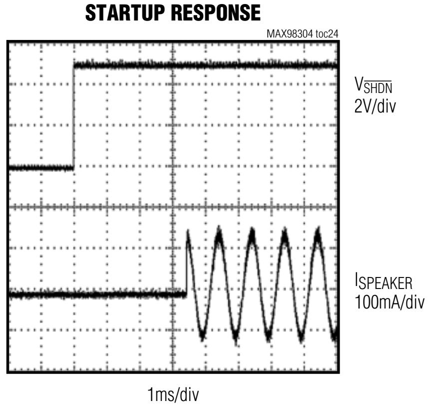
POWER-SUPPLY REJECTION RATIO vs. SUPPLY VOLTAGE



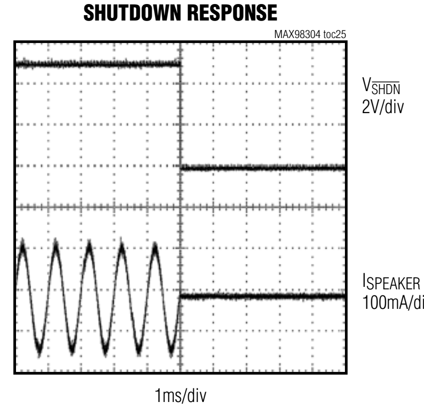
COMMON-MODE REJECTION RATIO vs. FREQUENCY



STARTUP RESPONSE



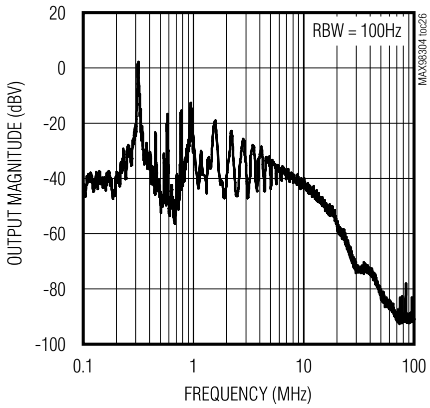
SHUTDOWN RESPONSE



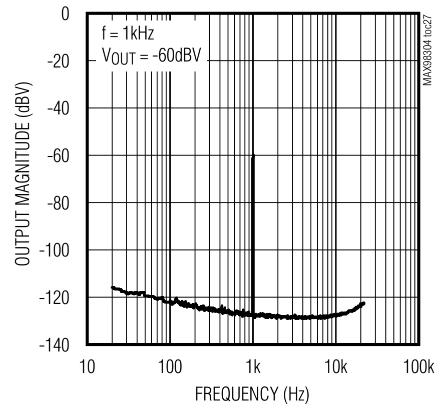
Typical Operating Characteristics (continued)

($V_{PVDD} = V_{\overline{SHDN}} = 5.0V$, $V_{PGND} = 0V$, $A_V = 6dB$, $R_L = \infty$, R_L connected between OUT+ to OUT-, AC measurement bandwidth 20Hz to 22kHz, $T_A = +25°C$, unless otherwise noted.)

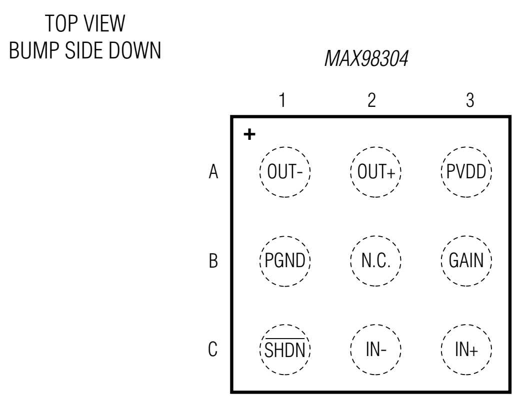
WIDEBAND vs. FREQUENCY



IN-BAND vs. FREQUENCY



Bump Configuration



WLP
(1mm x 1mm x 0.64mm
0.3mm PITCH)

Bump Description

BUMP	NAME	FUNCTION
A1	OUT-	Negative Speaker Output
A2	OUT+	Positive Speaker Output
A3	PVDD	Power Supply. Bypass PVDD to PGND with 0.1µF ll 10µF.
B1	PGND	Ground
B2	N.C.	No Connection. Can be left unconnected, or connected to PGND.
B3	GAIN	Gain Select. See Table 1 for GAIN settings.
C1	$\overline{SHDN}$	Active-Low Shutdown Input. Drive $\overline{SHDN}$ low to place the device in shutdown.
C2	IN-	Inverting Audio Input
C3	IN+	Noninverting Audio Input

Detailed Description

The MAX98304 features low quiescent current, a low-power shutdown mode, comprehensive click-and-pop suppression, and excellent RF immunity.

The device offers Class AB audio performance with Class D efficiency in a minimal board-space solution.

The Class D amplifier features spread-spectrum modulation, edge-rate, and overshoot control circuitry that offers significant improvements to switch-mode amplifier radiated emissions.

The amplifier features click-and-pop suppression that reduces audible transients on startup and shutdown. The amplifier includes thermal overload and short-circuit protection.

Class D Speaker Amplifier

The filterless Class D amplifier offers much higher efficiency than Class AB amplifiers. The high efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. Any power loss associated with the Class D output stage is mostly due to the I^2R loss of the MOSFET on-resistance and quiescent current overhead.

Ultra-Low EMI Filterless Output Stage

Traditional Class D amplifiers require the use of external LC filters, or shielding, to meet EN55022B electromagnetic-interference (EMI) regulation standards. Maxim's patented active emissions-limiting edge-rate control circuitry and spread-spectrum modulation reduces EMI emissions, while maintaining up to 93% efficiency.

Maxim's patented spread-spectrum modulation mode flattens wideband spectral components, while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency. The IC's spread-spectrum modulator randomly varies the switching frequency by ±12.5kHz around the center frequency (300kHz). Above 10MHz, the wideband spectrum looks like noise for EMI purposes (Figure 1).

Speaker Current Limit

If the output current of the speaker amplifier exceeds the current limit (2.8A typ), the IC disables the outputs for approximately 100µs. At the end of 100µs, the outputs are reenabled. If the fault condition still exists, the IC continues to disable and reenable the outputs until the fault condition is removed.

Selectable Gain

The IC offers five programmable gain selections through a single gain input (GAIN).

Table 1. Gain Control Configuration

GAIN PIN	MAXIMUM GAIN (dB)
Connect to PGND	12
Connect to PGND through 100kΩ ±5% resistor	9
Connect to PVDD	6
Connect to PVDD through 100kΩ ±5% resistor	3
Unconnected	0

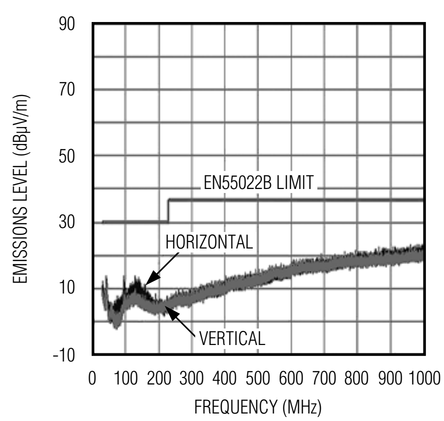


Figure 1. EMI with 60cm of Speaker Cable and No Output Filtering

Shutdown

The IC features a low-power shutdown mode, drawing less than 0.1µA (typ) of supply current. Drive $\overline{SHDN}$ low to put the IC into shutdown.

Click-and-Pop Suppression

The IC speaker amplifier features Maxim's comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces any audible transient sources internal to the device. When entering shutdown, the differential speaker outputs ramp down to PGND quickly and simultaneously.

Applications Information

Filterless Class D Operation

Traditional Class D amplifiers require an output filter. The filter adds cost, size, and decreases efficiency and THD+N performance. The IC's filterless modulation scheme does not require an output filter.

Because the switching frequency of the IC is well beyond the bandwidth of most speakers, voice coil movement due to the switching frequency is very small. Use a speaker with a series inductance > 10µH. Typical 8Ω speakers exhibit series inductances in the 20µH to 100µH range.

Component Selection

Power-Supply Input (PVDD)

PVDD powers the speaker amplifier. PVDD ranges from 2.5V to 5.5V. Bypass PVDD with a 0.1µF and 10µF capacitor to PGND. Apply additional bulk capacitance at the device if long input traces between PVDD and the power source are used.

Input Filtering

The input-coupling capacitor (C_{IN}), in conjunction with the amplifier's internal input resistance (R_{IN}), forms a high-pass filter that removes the DC bias from the incoming signal. These capacitors allow the amplifier to bias the signal to an optimum DC level.

Assuming zero source impedance C_{IN} is:

$$C_{IN} = \frac{2\pi \times R_{IN}}{f_{-3dB}} [\mu F]$$

where f_{-3dB} is the -3dB corner frequency and R_{IN} is the input resistance shown in the *Electrical Characteristics* table. Use capacitors with adequately low voltage-coefficient for best low-frequency THD performance.

Layout and Grounding

Proper layout and grounding are essential for optimum performance. Good grounding improves audio performance and prevents switching noise from coupling into the audio signal.

Use wide, low-resistance output traces. As the load impedance decreases, the current drawn from the device increases. At higher current, the resistance of the output traces decreases the power delivered to the load. For example, if 2W is delivered from the device output to a 4Ω load through 100mΩ of total speaker trace, 1.904W is being delivered to the speaker. If power is delivered through 10mΩ of total speaker trace, 1.99W is being delivered to the speaker. Wide output, supply, and ground traces also improve the power dissipation of the device.

The IC is inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on top or bottom PCB planes.

WLP Applications Information

For the latest application details on WLP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to Application Note 1891: *Wafer-level packaging (WLP) and its applications*. Figure 2 shows the dimensions of the WLP balls used on the IC.

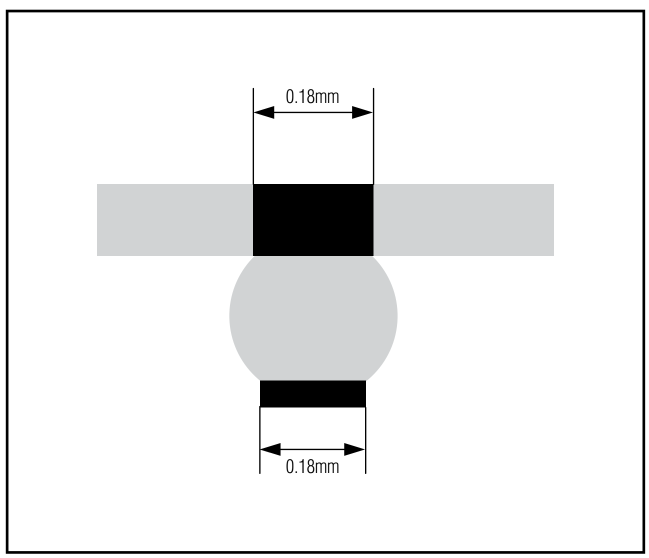
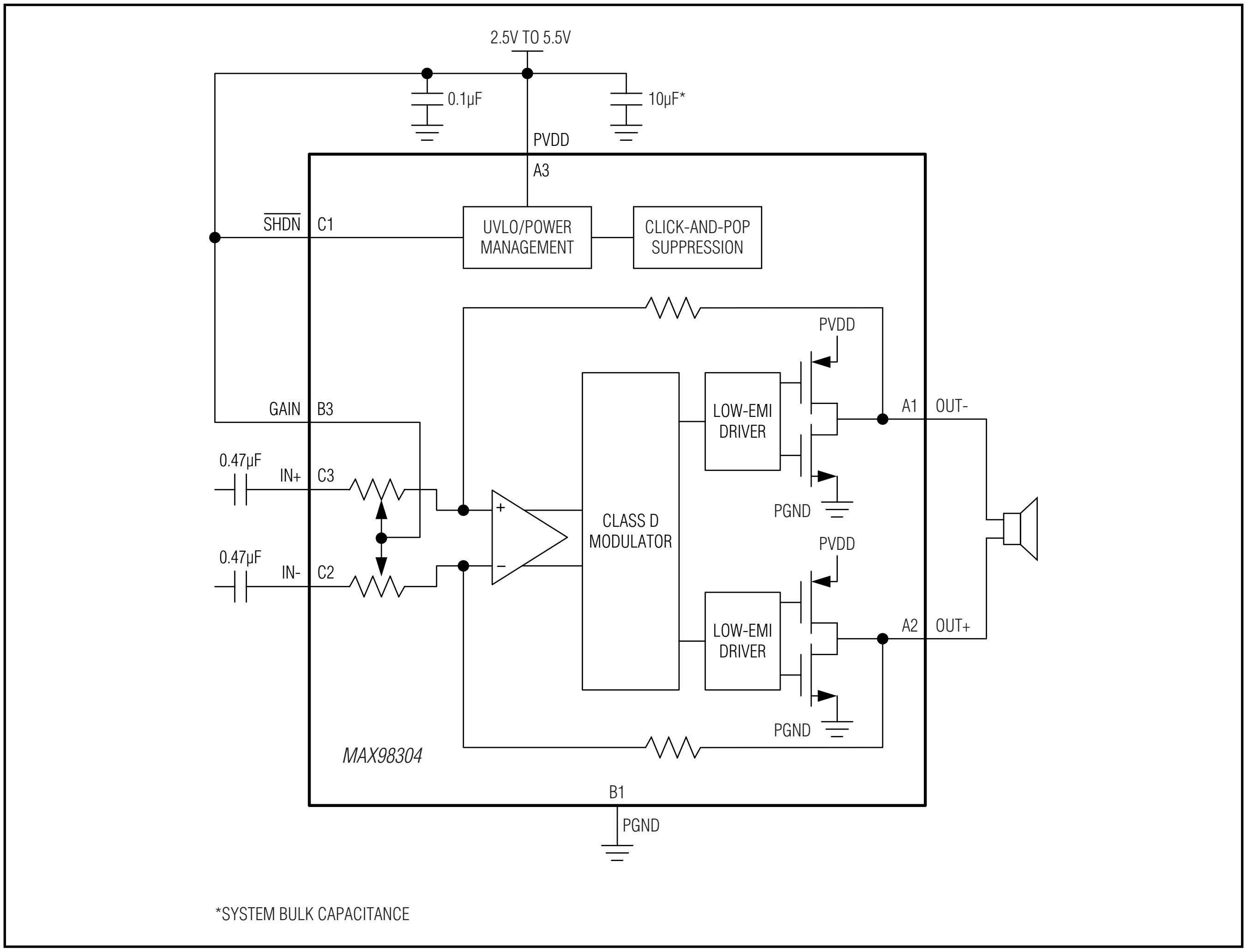


Figure 2. MAX98304 WLP Ball Dimensions

Functional Diagram



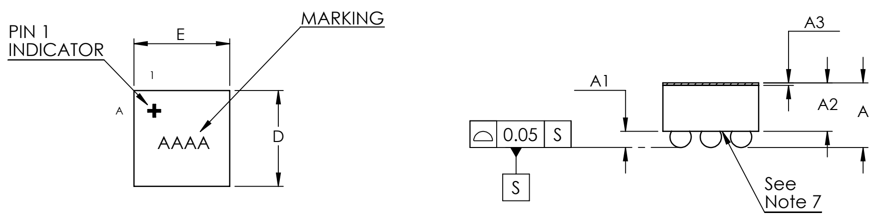
Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns, go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
9 WLP	W91D1+1	21-0486	—

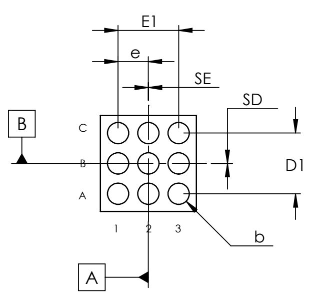


TOP VIEW

SIDE VIEW

COMMON DIMENSIONS		
A	0.64	±0.05
A1	0.16	±0.03
A2	0.48	REF
A3	0.025	BASIC
b	0.21	±0.03
D1	0.60	BASIC
E1	0.60	BASIC
e	0.30	BASIC
SD	0.00	BASIC
SE	0.00	BASIC

PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W91D1+1	0.95	0.98	0.95	0.98	NONE



BOTTOM VIEW

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

-DRAWING NOT TO SCALE-

TITLE	PACKAGE OUTLINE 9 BUMPS, WLP PKG. 0.3mm PITCH		
APPROVAL	DOCUMENT CONTROL NO. 21-0486	REV. B	1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/10	Initial release	—

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