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MAXM15068

7.5V to 60V, 200mA Himalaya uSLIC Step-Down Power Module

General Description

The Himalaya series of voltage regulator ICs and power modules enable cooler, smaller, and simpler power-supply solutions. The MAXM15068 is a high-efficiency, synchronous step-down DC-DC module with integrated controller, MOSFETs, compensation components, and inductor that operates over a wide input-voltage range. The module operates from 7.5V to 60V input and delivers up to 200mA output current over a programmable output voltage from 5V to 12V. The module significantly reduces design complexity, manufacturing risks, and offers a true plug and play power/supply solution, reducing time-to-market.

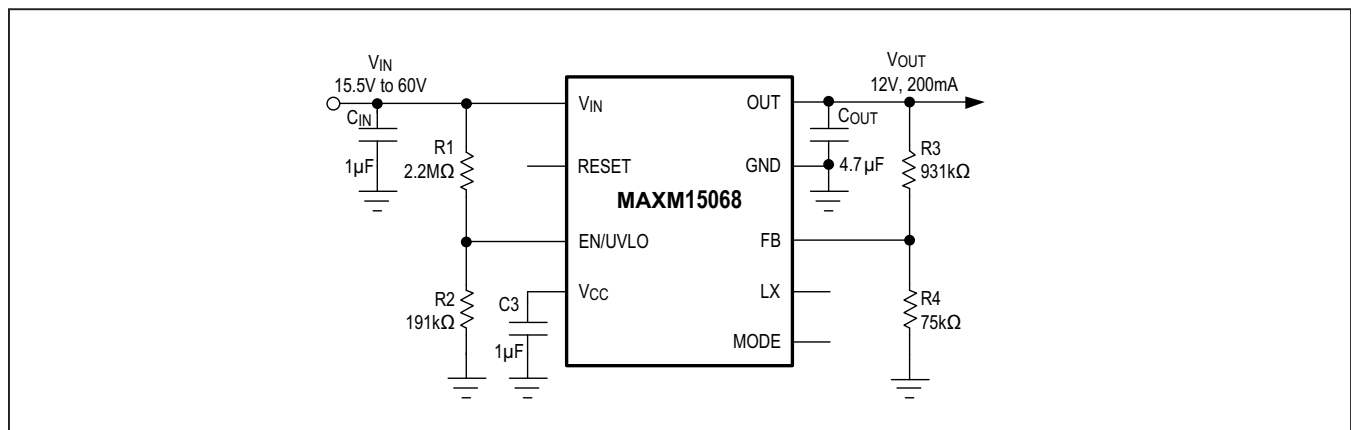
The MAXM15068 employs peak-current-mode control architecture. To reduce input inrush current, the device offers a fixed 3.75ms soft-start time.

The MAXM15068 module is available in a low profile, compact 10-pin, 2.6mm × 3mm × 1.5mm, uSLIC™ package.

Applications

- Industrial Sensors and Process Control
- 4-20mA Current-Loop Powered Sensors
- LDO Replacement
- HVAC and Building Control
- Battery-Powered Equipment
- General Purpose Point-of-Load

Typical Application Circuit



Benefits and Features

- Easy to Use
 - Wide 7.5V to 60V Input Range
 - Adjustable 5V to 12V Output
 - ±1.44% Feedback Accuracy
 - Up to 200mA Output-Current
 - Internally Compensated
 - All Ceramic Capacitors
- High Efficiency
 - Selectable PWM- or PFM-Mode of Operation
 - Shutdown Current as Low as 2.2µA (typ)
- Flexible Design
 - Internal Soft-Start and Prebias Startup
 - Open-Drain Power Good Output (RESET Pin)
 - Programmable EN/UVLO Threshold
- Robust Operation
 - Hiccup Overcurrent Protection
 - Overtemperature Protection
 - -40°C to +125°C Ambient Operating Temperature/
-40°C to +150°C Junction Temperature
- Rugged
 - Complies with CISPR22 (EN55022) Class B Conducted and Radiated Emissions
 - Passes Drop, Shock, and Vibration Standards: JESD22-B103, B104, B111

Ordering Information appears at end of data sheet.

uSLIC is a trademark of Maxim Integrated Products, Inc.

Absolute Maximum Ratings

V _{IN} , EN/UVLO to GND	-0.3V to 70V	Junction Temperature (Note 1).....	+150°C
LX, OUT and GND	-0.3V to (V _{IN} + 0.3V)	Storage Temperature Range	-55°C to +125°C
V _{CC} , FB, RESET to GND.....	-0.3V to 6V	Lead Temperature (soldering, 10s)	+260°C
MODE to GND.....	-0.3V to (V _{CC} + 0.3V)	Soldering Temperature (reflow)	+260°C
Output Short-Circuit Duration	Continuous		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 10-PIN uSLIC	
Package Code	M102A3+2
Outline Number	21-100094
Land Pattern Number	90-100027
THERMAL RESISTANCE, FOUR-LAYER BOARD (Note 2)	
Junction-to-Ambient (θ _{JA})	41.5°C/W

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Note 2: Package thermal resistances are measured on an evaluation board with natural convection.

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

($V_{IN} = V_{EN/UVLO} = 24V$, $V_{GND} = 0V$, $C_{VCC} = 1\mu F$, $FB = 1V$, $LX = MODE = \overline{RESET} = OUT = \text{unconnected}$; $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$. All voltages are referenced to GND, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})						
Input-Voltage Range	V_{IN}		7.5		60	V
Input-Shutdown Current	I_{IN-SH}	$V_{EN/UVLO} = 0V$, shutdown mode		2.2	4	μA
Input-Supply Current	I_{Q-PFM}	MODE = unconnected, FB = $1.03 \times V_{FB-REG}$		90	160	μA
	I_{Q-PWM}	Normal switching mode, MODE = 0		3.4		mA
ENABLE/UVLO ($EN/UVLO$)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.19	1.215	1.28	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.06	1.09	1.16	
EN/UVLO Input leakage-Current	$I_{EN/UVLO}$	$T_A = +25^\circ C$	-100		+100	nA
LDO (V_{CC})						
V_{CC} Output-Voltage Range	V_{CC}	$7.5V < V_{IN} < 60V$, $0mA < I_{VCC} < 10mA$	4.75	5	5.25	V
V_{CC} Current Limit	$I_{VCC-MAX}$	$V_{CC} = 4.3V$	13	30	50	mA
V_{CC} UVLO	V_{CC-UVR}	V_{CC} rising	4.05	4.18	4.3	V
	V_{CC-UVF}	V_{CC} falling	3.7	3.8	3.95	
SOFT-START (SS)						
Soft-Start Time	t_{SS}		3.5	3.75	4	ms
FEEDBACK (FB)						
FB-Regulation Voltage	V_{FB-REG}	MODE = GND	0.887	0.9	0.913	V
		MODE = unconnected	0.887	0.915	0.936	
FB-Leakage Current	I_{FB}		-100	-25		nA
TIMING						
Switching Frequency	f_{SW}		515	550	585	kHz
FB Undervoltage Trip Level to Cause Hiccup			62.5	64.5	66.5	%
Hiccup Timeout				120		ms
Minimum On-Time	t_{ON-MIN}			90	120	ns
Maximum Duty Cycle	D_{MAX}	FB = $0.98 \times V_{FB-REG}$	89	91.4	94	%

Electrical Characteristics (continued)

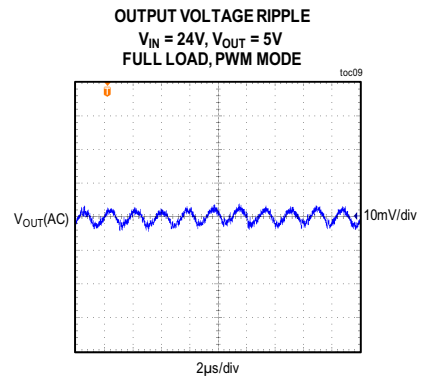
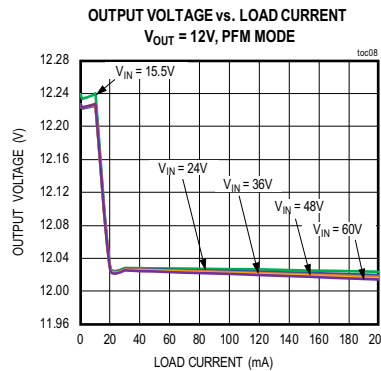
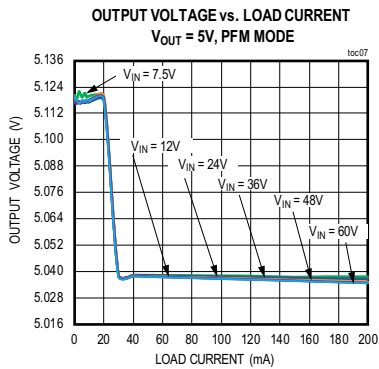
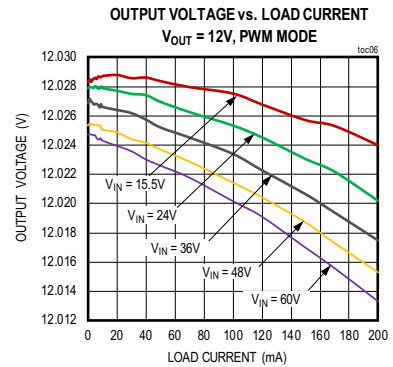
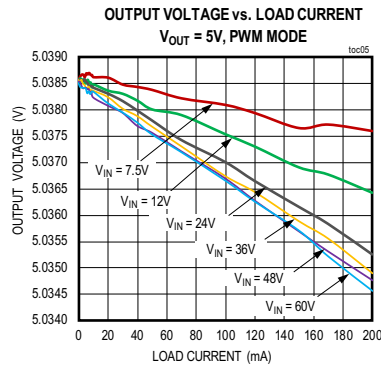
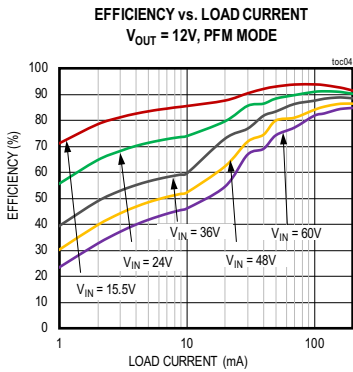
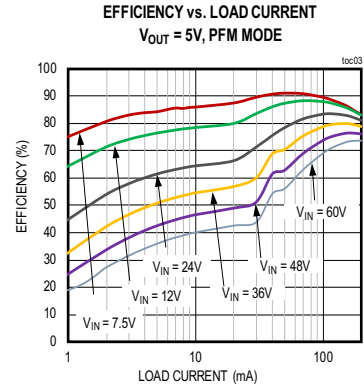
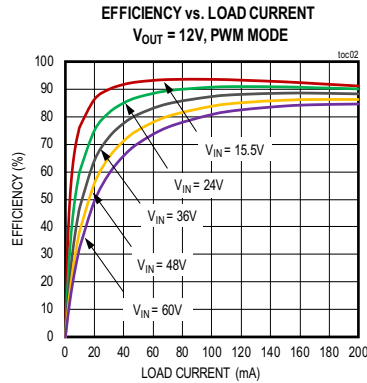
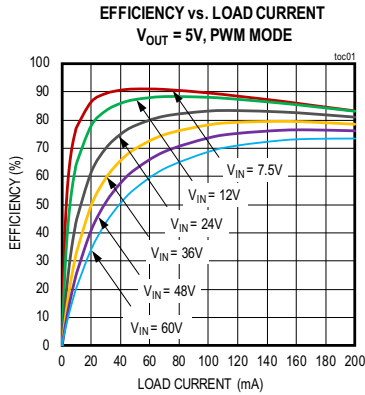
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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET						
FB Threshold for \overline{RESET} Rising		FB rising	93.5	95.5	97.5	%
FB Threshold for \overline{RESET} Falling		FB falling	90	92	94	%
\overline{RESET} Delay After FB Reaches 95% Regulation				1.9		ms
\overline{RESET} Output Level Low		$I_{\overline{RESET}} = 5mA$			0.2	V
\overline{RESET} Output Leakage Current		$V_{\overline{RESET}} = 5.5V$, $T_A = +25^\circ C$			0.1	μA
MODE						
MODE Internal Pullup Resistor				500		k Ω
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold		Temperature rising		166		$^\circ C$
Thermal-Shutdown Hysteresis				10		$^\circ C$

Note 3: Electrical specifications are production tested at $T_A = +25^\circ C$. Specifications over the entire operating temperature range are guaranteed by design and characterization.

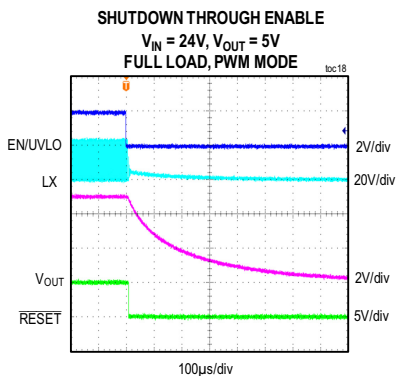
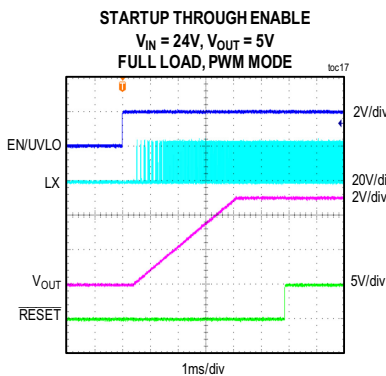
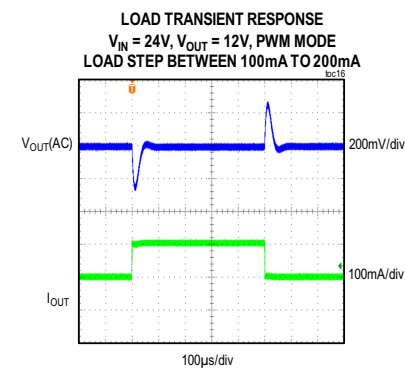
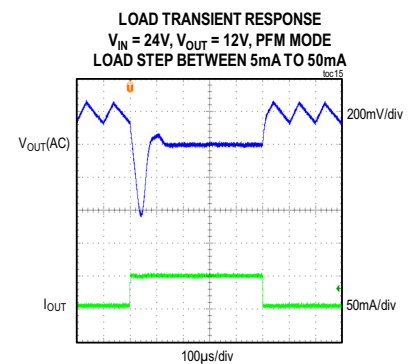
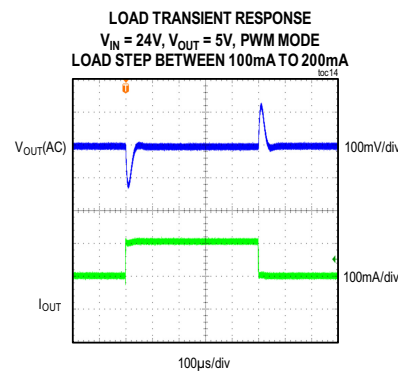
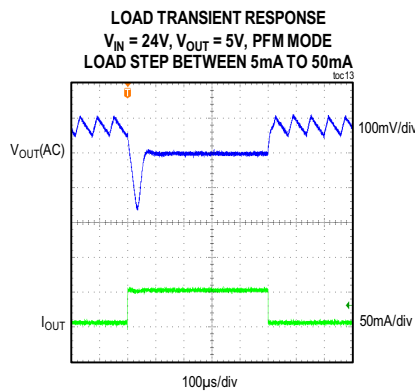
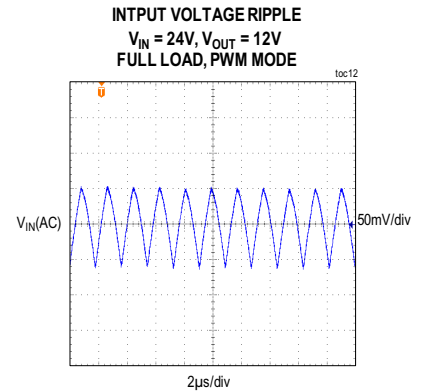
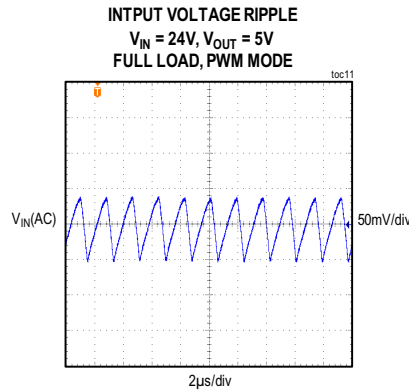
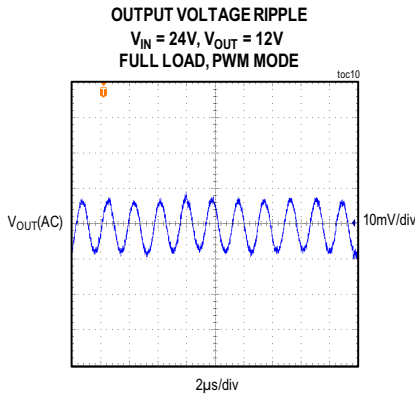
Typical Operating Characteristics

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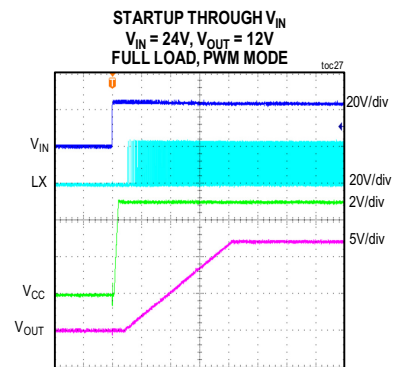
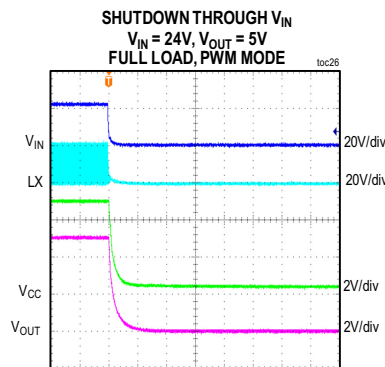
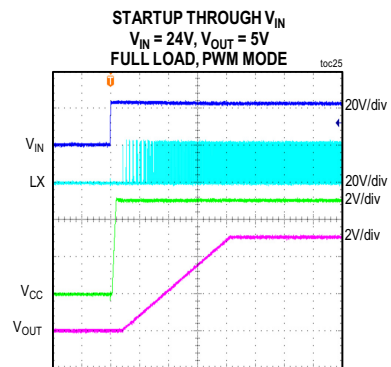
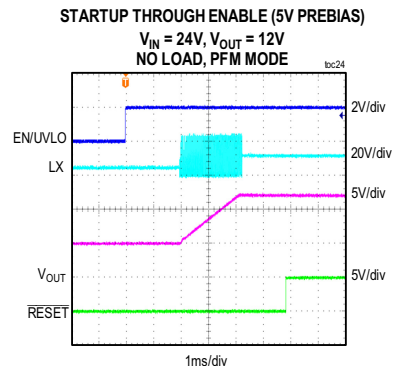
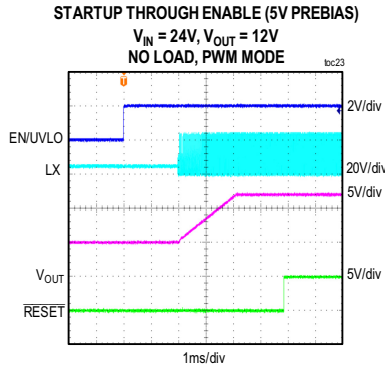
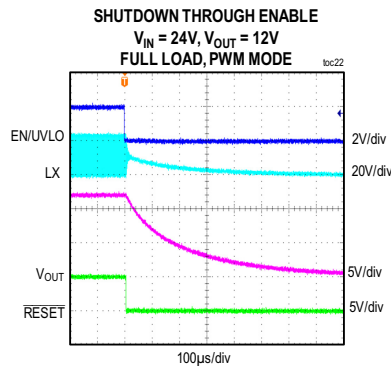
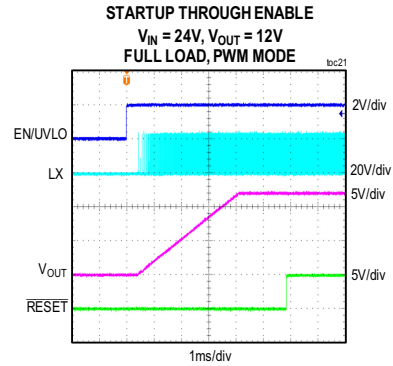
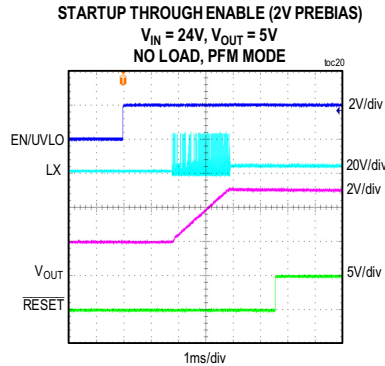
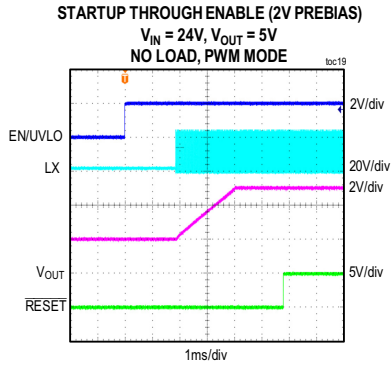
Typical Operating Characteristics (continued)

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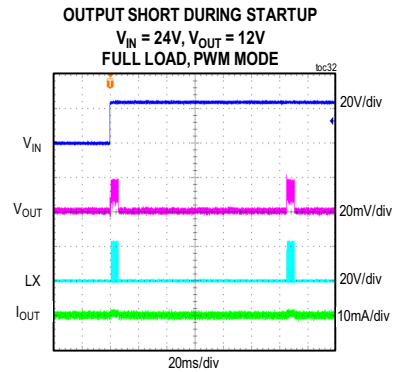
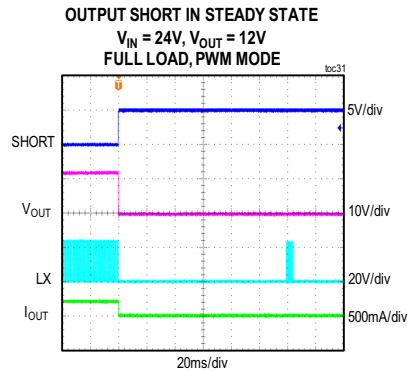
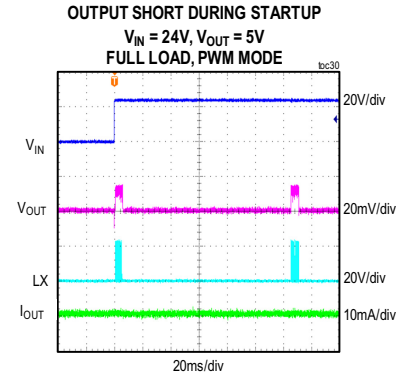
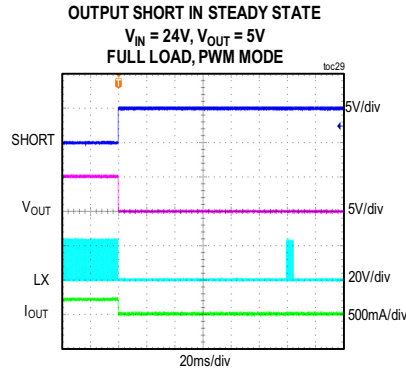
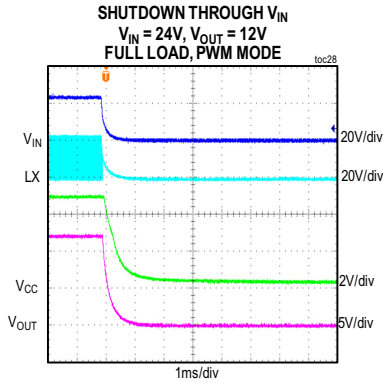
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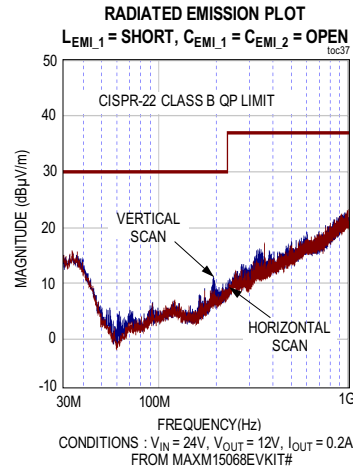
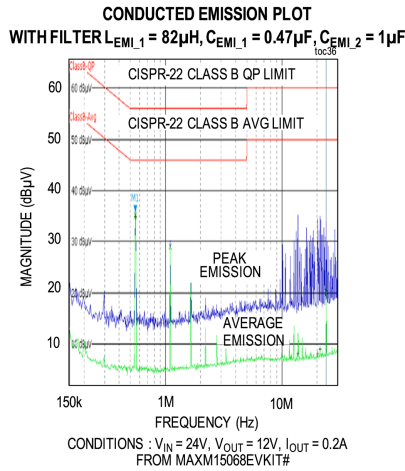
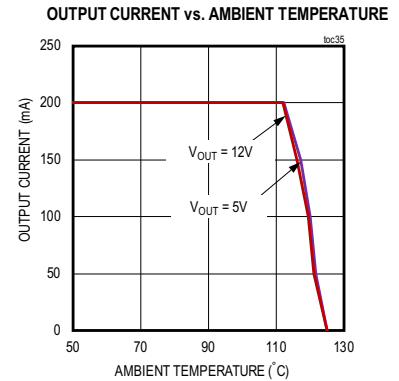
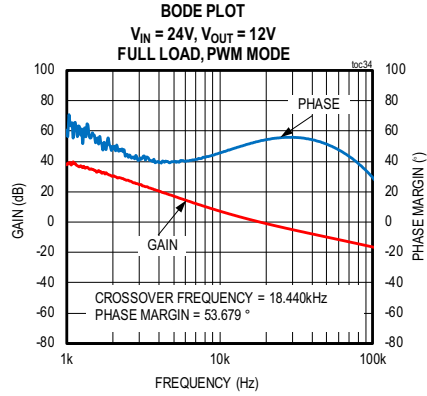
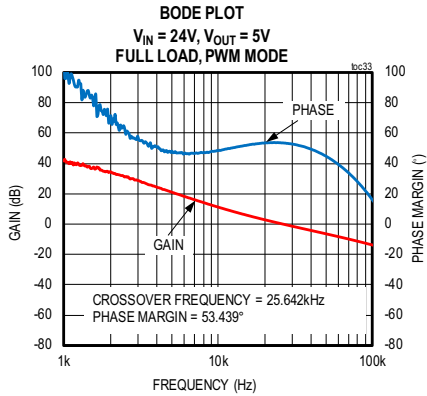
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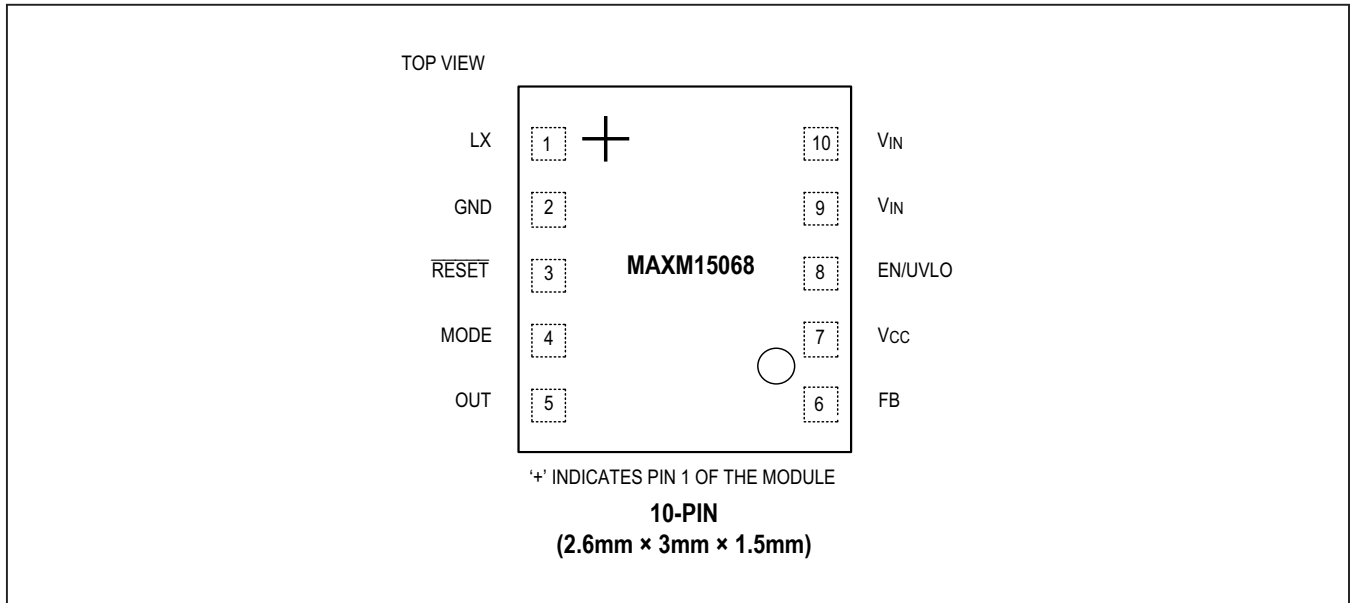


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Pin Configuration

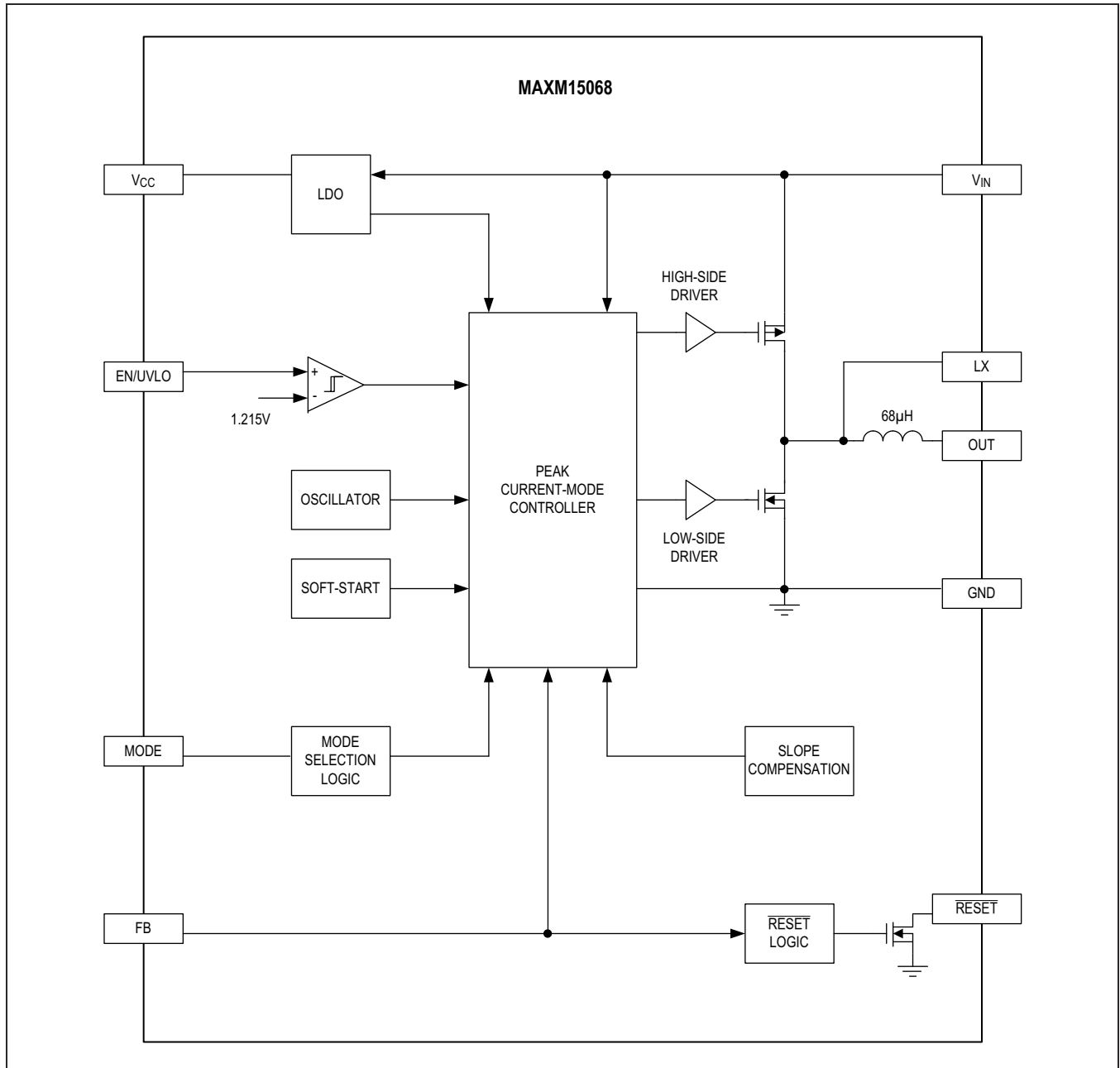


Pin Description

PIN	NAME	FUNCTION
1	LX	Switching Node of the Inductor. No external connection to this pin.
2	GND	Ground Pin. Connect GND to the ground plane. See the PCB Layout Guidelines section for more details. Refer to the MAXM15068 EV kit for a sample layout.
3	RESET	Open-Drain Power Good Output. Pull up RESET to an external power supply with an external resistor. RESET goes low if FB drops below 92% of its set value. RESET goes high impedance 1.9ms after FB rises above 95.5% of its set value. See the Electrical Characteristics table for threshold values.
4	MODE	PFM/PWM Mode-Selection Input. Connect MODE to GND to enable fixed-frequency PWM operation at all loads. Leave MODE unconnected for PFM operation at light load.
5	OUT	Module Output Pin. Connect a capacitor from OUT to GND. See PCB Layout Guidelines section for more details.
6	FB	Output Feedback Connection. Connect FB to a resistor-divider between OUT and GND to set the output voltage.
7	VCC	Internal LDO Power Output. Bypass VCC to GND with a minimum 1µF ceramic capacitor.
8	EN/UVLO	Active-High, Enable/Undervoltage-Detection Input. Pull EN/UVLO to GND to disable the module output. Connect EN/UVLO to VIN for always-on operation. Connect a resistor-divider between VIN, EN/UVLO, and GND to program the input voltage at which the module turns on.
9,10	VIN	Power-Supply Input. Connect the VIN pins together. Decouple to GND with a capacitor; place the capacitor close to the VIN and GND pins. See Table 1 for more details.

Functional Diagram

Internal Diagram



Detailed Description

The MAXM15068 module is a high-voltage, synchronous step-down DC-DC module with integrated MOSFETs and inductor, that operates over a wide 7.5V to 60V input voltage range. The module delivers output current up to 200mA over a programmable output-voltage range of 5V to 12V. When EN/UVLO and V_{CC} UVLO are ascertained, an internal power-up sequence ramps up the error-amplifier reference, resulting in an output-voltage soft-start.

The FB pin monitors the output voltage through a resistor-divider. The RESET pin transitions to a high-impedance state 1.9ms after the output voltage reaches 95.5% of regulation. The device selects either PFM or forced-PWM mode depending on the state of the MODE pin at power-up. By pulling the EN/UVLO pin to low, the device enters shutdown mode and consumes only 2.2 μ A (typ) of standby current.

The module uses an internally compensated, fixed-frequency, current-mode control scheme. On the rising edge of an internal clock, the high-side pMOSFET turns on. An internal error amplifier compares the feedback voltage to a fixed internal reference voltage and generates an error voltage. The error voltage is compared to a sum of the current-sense voltage and a slope-compensation voltage by a PWM comparator to set the on-time. During the on-time of the pMOSFET, the inductor current ramps up. For the remainder of the switching period (off-time), the pMOSFET is kept off and the low-side nMOSFET turns on. During the off-time, the inductor releases the stored energy as the inductor current ramps down, providing current to the output. Under overload conditions, the cycle-by-cycle current-limit feature limits the inductor peak current by turning off the high-side pMOSFET and turning on the low-side nMOSFET.

Mode Selection (MODE)

The logic state of the MODE pin is latched after V_{CC} and EN/UVLO voltages exceed respective UVLO rising thresholds and all internal voltages are ready to allow LX switching. If the MODE pin is unconnected at power-up, the part operates in PFM mode at light loads. If the MODE pin is grounded at power-up, the part operates in constant-frequency PWM mode at all loads. State changes on the MODE pin are ignored during normal operation.

PWM Mode

In PWM mode, the module output current is allowed to go negative. PWM mode is useful in frequency sensitive applications and provides fixed switching frequency operation at all loads.

PFM Mode

PFM mode disables negative output current from the module, and skips pulses at light loads for better efficiency. In PFM mode, the module output current is forced to a fixed peak of 60mA in every clock cycle until the output voltage rises to 102.3% of the nominal value. Once the output voltage reaches 102.3% of the nominal value, the high-side switch is turned off and the low-side switch is turned on. Once the module output current hits zero cross, LX goes to a high-impedance state and the module enters hibernate operation until the load current discharges the output voltage to 101.1% of the nominal value. Most of the internal blocks are turned off in hibernate operation to save quiescent current. When the output voltage falls below 101.1% of the nominal value, the module comes out of hibernate operation, turns on all internal blocks, and commences the process of delivering pulses of energy until the output voltage reaches 102.3% of the nominal value. The module naturally comes out of PFM mode and serves load requirements when the module output demands more than 60mA peak. At light loads, PFM mode gives higher efficiency compared to PWM mode because of lower quiescent current drawn from supply.

Internal 5V Regulator

An internal regulator provides a 5V nominal supply to power the internal functions and to drive the power MOSFETs. The output of the linear regulator (V_{CC}) should be bypassed with a 1 μ F ceramic capacitor to GND. An undervoltage lockout circuit disables the buck converter when V_{CC} falls below 3.8V (typ). The 400mV, V_{CC} -UVLO hysteresis prevents chattering on power-up and power-down.

Enable/Undervoltage Lockout (EN/UVLO), Soft-Start

When EN/UVLO voltage is above 1.215V (typ), the device's internal error-amplifier reference voltage starts to ramp up. The duration of the soft-start ramp is 3.75ms (typ), allowing a smooth increase of the output voltage. Driving EN/UVLO low disables both power MOSFETs, as well as other internal circuitry, and reduces V_{IN} quiescent current to below 2.2 μ A. EN/UVLO can be used as an input-voltage UVLO adjustment input. An external voltage-divider between V_{IN} and EN/UVLO to GND adjusts the input voltage at which the device turns on or turns off. If input UVLO programming is not desired, connect EN/UVLO to V_{IN} (see the [Electrical Characteristics](#) table for EN/UVLO rising and falling threshold voltages).

RESET Output (RESET)

The device includes an open-drain $\overline{\text{RESET}}$ output to monitor the output voltage. $\overline{\text{RESET}}$ goes high impedance 1.9ms after the output rises above 95.5% of its nominal set value and pulls low when the output voltage falls below 92% of the set nominal regulated voltage. $\overline{\text{RESET}}$ asserts low during the hiccup timeout period.

Startup into a Prebiased Output

The device is capable of soft-start into a prebiased output, without discharging the output capacitor in both the PFM and forced-PWM modes. Such a feature is useful in applications where digital integrated circuits with multiple rails are powered.

Overcurrent Protection (OCP)/Hiccup Mode

The device is provided with a robust overcurrent protection (OCP) scheme that protects the device under overload and output short-circuit conditions. When overcurrent is detected or if the FB node goes below 64.5% of its nominal regulation threshold, the device enters hiccup mode of operation. In hiccup mode, the device is protected by suspending switching for a hiccup timeout period of 120ms (typ). Once the hiccup timeout period expires, soft-start is attempted again. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions. The device exits hiccup mode if the overcurrent condition is removed or if V_{IN} or EN/UVLO is cycled.

Thermal Overload Protection

Thermal overload protection limits the total power dissipation in the device. When the junction temperature exceeds +166°C, an on-chip thermal sensor shuts down the device, turns off the internal power MOSFETs, allowing the device to cool down. The thermal sensor turns the device on after the junction temperature cools by 10°C.

Applications Information

Input Voltage Range

The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{\text{IN(MIN)}} = \frac{V_{\text{OUT}} + (I_{\text{OUT}} \times 5.1)}{D_{\text{MAX}}} + (I_{\text{OUT}} \times 1.8) + 0.4$$

$$V_{\text{IN(MAX)}} = \frac{V_{\text{OUT}}}{t_{\text{ON(MIN)}} \times f_{\text{SW}}}$$

where:

V_{OUT} = Steady-state output voltage,

I_{OUT} = Maximum load current,

f_{SW} = Worst-case switching frequency (585 kHz),

D_{MAX} = Maximum duty cycle (0.89),

$t_{\text{ON(MIN)}}$ = Worst-case minimum controllable switch on-time (120ns).

Selection of Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the converter's switching.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{\text{RMS}} = I_{\text{OUT(MAX)}} \times \frac{\sqrt{V_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}})}}{V_{\text{IN}}}$$

where $I_{\text{OUT(MAX)}}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{\text{IN}} = 2 \times V_{\text{OUT}}$). So,

$$I_{\text{RMS(MAX)}} = \frac{I_{\text{OUT(MAX)}}}{2}$$

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{\text{IN}} = \frac{I_{\text{OUT(MAX)}} \times D_{\text{MAX}} \times (1 - D_{\text{MAX}})}{f_{\text{SW}} \times \Delta V_{\text{IN}}}$$

where:

D_{MAX} = Maximum duty cycle (0.89),

f_{SW} = Switching frequency,

ΔV_{IN} = Allowable input-voltage ripple.

Selection of Output Capacitor

Small ceramic X7R-grade capacitors are sufficient and recommended for output-voltage generation. The output capacitor has two functions. It provides smooth voltage, stores sufficient energy to support the output voltage under load transient conditions, and stabilizes the device’s internal control loop. Usually the output capacitor is sized to support a step load of 50% of the maximum output current in the application, such that the output-voltage deviation is less than 3%. Required output capacitance can be calculated from the following equation:

$$C_{OUT} = \frac{30}{V_{OUT}}$$

where C_{OUT} is the output capacitance in μF and V_{OUT} is the output voltage. Derating of ceramic capacitors with DC-voltage must be considered while selecting the output capacitor.

Setting the Input Undervoltage-Lockout Level

The device offers an adjustable input undervoltage lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from V_{IN} to GND (see [Figure 1](#)). Connect the center node of the divider to EN/UVLO.

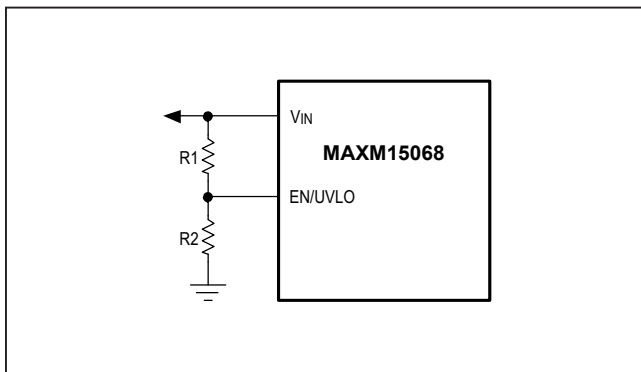


Figure 1. Adjustable EN/UVLO Network

Choose R1 to be 2.2M Ω (max), and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.215}{(V_{INU} - 1.215)}$$

where V_{INU} is the voltage at which the device is required to turn on.

If the EN/UVLO pin is driven from an external signal source, a series resistance of minimum 1k Ω is recommended to be placed between the signal source output and the EN/UVLO pin to reduce voltage ringing on the line.

Output Voltage Setting

The MAXM15068 typical output voltage can be programmed from 5V to 12V. Set the output voltage by connecting a resistor-divider from output to FB to GND (see [Figure 2](#)).

Choose R4 to be less than or equal to 75k Ω and calculate R3 with the following equation:

$$R3 = R4 \times \left(\frac{V_{OUT}}{0.9} - 1 \right)$$

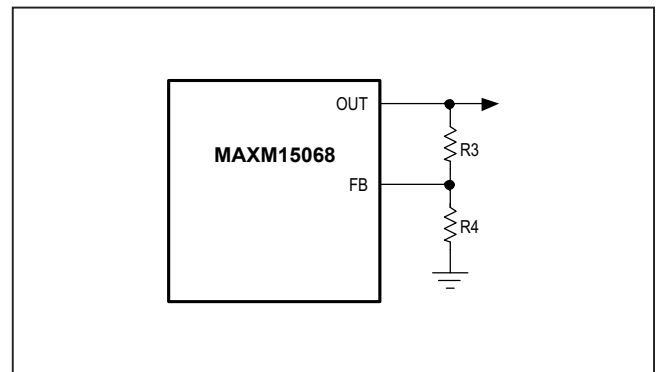


Figure 2. Setting the Output Voltage

Table 1. Selection of Components

$V_{IN(MIN)}$ (V)	$V_{IN(MAX)}$ (V)	V_{OUT} (V)	C_{IN}	C_{OUT}	R3 (k Ω)	R4 (k Ω)
7.5	60	5	1 x 1 μF 1206 100V (TAIYO YUDEN HMK316B7105KLH)	1 x 10 μF 0805 16V (MURATA GRM21BZ71C106KE15)	348	75
15.5	60	12	1 x 1 μF 1206 100V (TAIYO YUDEN HMK316B7105KLH)	1 x 4.7 μF 0805 25V (MURATA GRM21BZ71E475KE15)	931	75

Power Dissipation

To operate in high ambient temperature, the device output current needs to be derated. See the [Typical Operating Characteristics](#) section for the derating curves to use as a guide.

PCB Layout Guidelines

Use the following guidelines for good PCB layout:

- Keep the input capacitors as close as possible to the V_{IN} and GND pins.

- Keep the output capacitors as close as possible to the OUT and GND pins.
- Keep the resistive feedback dividers as close as possible to the FB pin.
- Keep the power traces and load connections short. Refer to EV kit layout for first-pass success.

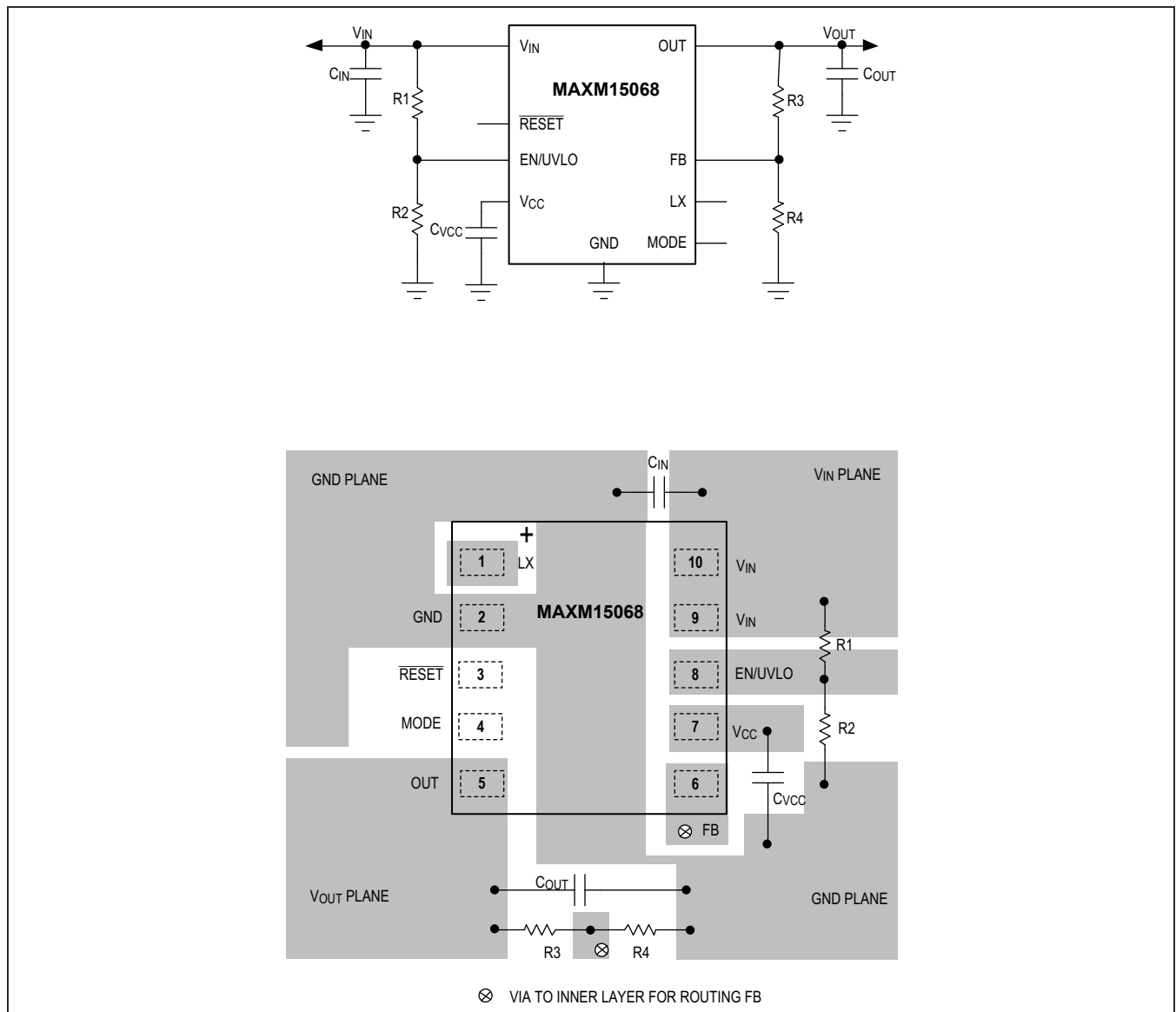
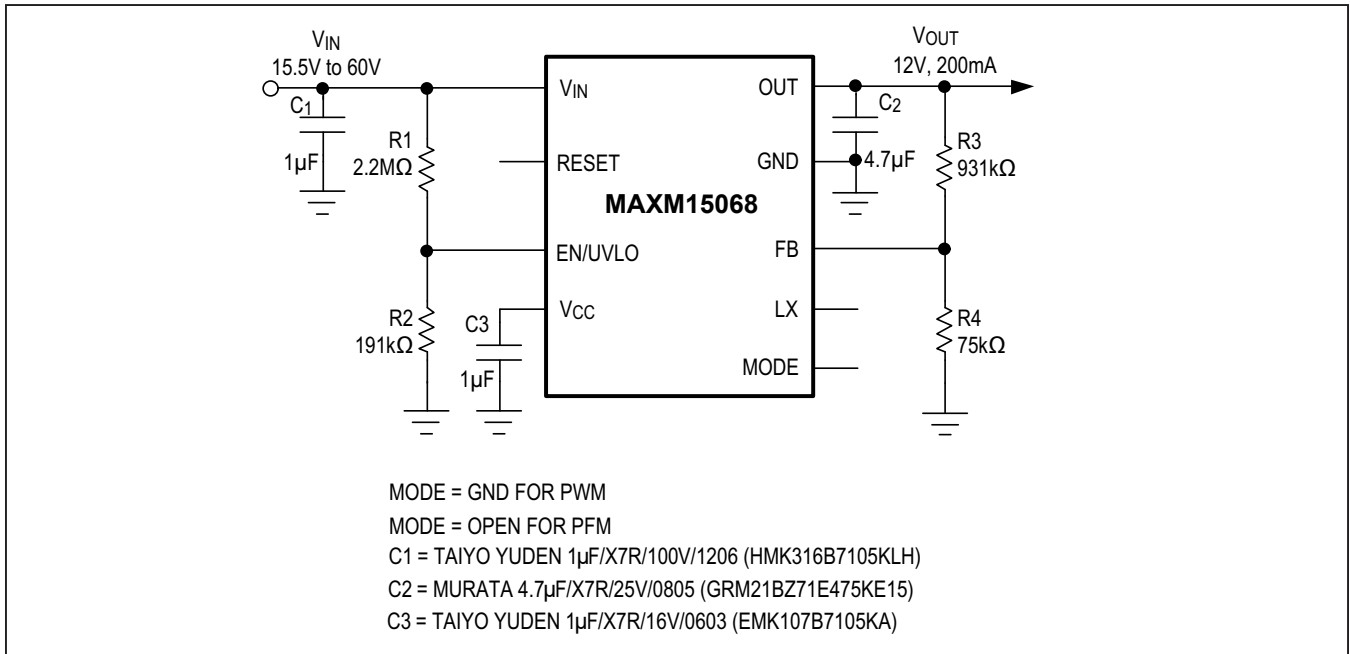


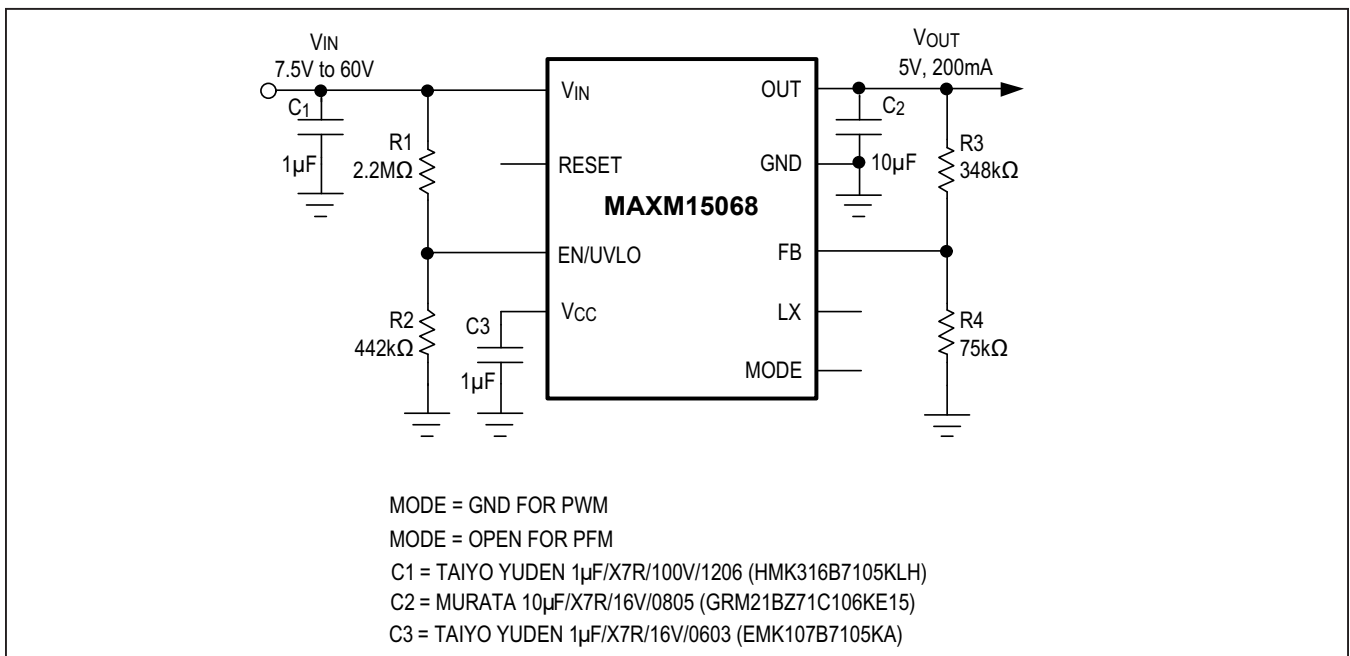
Figure 3. Layout Guidelines

Typical Application Circuits

Typical Application Circuit for 12V Output



Typical Application Circuit for 5V Output



MAXM15068

7.5V to 60V, 200mA Himalaya uSLIC
Step-Down Power Module

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAXM15068AMB+	-40°C to +125°C	10-pin uSLIC
MAXM15068AMB+T	-40°C to +125°C	10-pin uSLIC

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

MAXM15068

7.5V to 60V, 200mA Himalaya uSLIC
Step-Down Power Module

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/19	Initial release	—

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