Data Sheet

LMV321

General Purpose, Rail-to-Rail Output Amplifier
Rail-to-Rail Amplifiers

FEATURES

- 130µA supply current
- 1MHz gain bandwidth
- Input voltage range with 5V supply: -0.2V to 4.2V
- Output voltage range with 5V supply: 0.065V to 4.99V
- >1V/µs slew rate
- No crossover distortion
- Fully specified at 2.7V and 5V supplies
- LMV321: Pb-free TSOT-5

APPLICATIONS

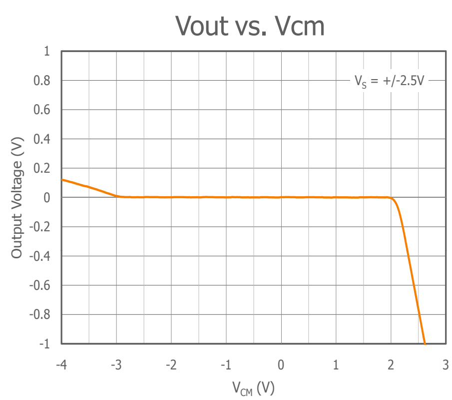
- Portable/battery-powered applications
- Mobile communications, cell phones, pagers
- ADC buffer
- Active filters
- Portable test instruments
- Signal conditioning
- Medical Equipment
- Portable medical instrumentation

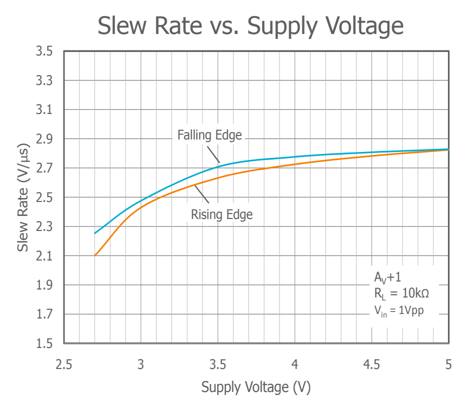
General Description

The LMV321 is a single channel, low cost, voltage feedback amplifier. The LMV321 consumes only 130µA of supply current and is designed to operate from a supply range of 2.7V to 5.5V (±1.35 to ±2.75). The input voltage range extends 200mV below the negative rail and 800mV below the positive rail.

The LMV321 is fabricated on a CMOS process. It offers 1MHz gain bandwidth product and >1V/µs slew rate. The combination of low power, low supply voltage operation, and rail-to-rail performance make the LMV321 well suited for battery-powered systems. The LMV321 is packaged in the space saving TSOT-5 package. TSOT-5 package is pin compatible with the SOT23-5 package.

Typical Performance Examples



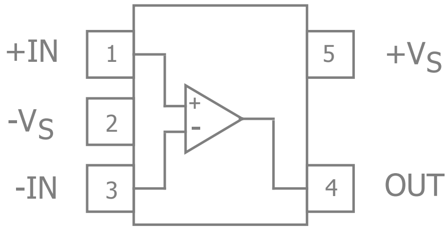


Ordering Information

Part Number	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
LMV321IST5X	TSOT-5	Yes	Yes	-40°C to +85°C	Reel

Moisture sensitivity level for all parts is MSL-1.

LMV321 Pin Configuration



LMV321 Pin Assignments[1]

Pin No.	Pin Name	Description
1	+IN	Positive input
2	$-V_S$	Negative supply
3	-IN	Negative input
4	OUT	Output
5	$+V_S$	Positive supply

Notes:
1.Pin compatible to SOT23-5.

Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage		7	V
Input Voltage Range	$-V_S$-0.4V	$+V_S$	V
Continuous Output Current	Output is protected against momentary short circuit		

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
5-Lead TSOT		221		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	TSOT-5
Human Body Model (HBM)	2kV
Charged Device Model (CDM)	2kV

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	2.7		5.5	V

Electrical Characteristics at +2.7V

T_A = 25°C, V_S = +2.7V, R_f = R_g =10 KΩ, R_L = 10kΩ to V_S/2, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DC Performance						
V_{IO}	Input Offset Voltage			1.7	7	mV
dV_{IO}	Average Drift			5		µV/°C
I_b	Input Bias Current			<1	250	nA
I_{OS}	Input Offset Current			<1	50	nA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.7V	50	63		dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V, V_O=1V, V_{CM}=1V	50	60		dB
CMIR	Common Mode Input Range	For V_{CM} ≤ 50 dB	0	-0.2		V
				1.9	1.7	V
V_{OUT}	Output Voltage Swing	R_L = 10kΩ to V_S / 2	V^+ -100	V^+ -10		mV
				60	180	mV
I_S	Supply Current			110	170	µA
AC Performance						
GBWP	Gain Bandwidth Product	C_L=200 pF		1		MHz
Φ_m	Phase Margin			60		°
G_m	Gain Margin			10		dB
e_n	Input Voltage Noise	f = 1kHz		46		nV/√Hz

Notes:
Min max specifications are guaranteed by testing, design, or characterization

Electrical Characteristics at +5V

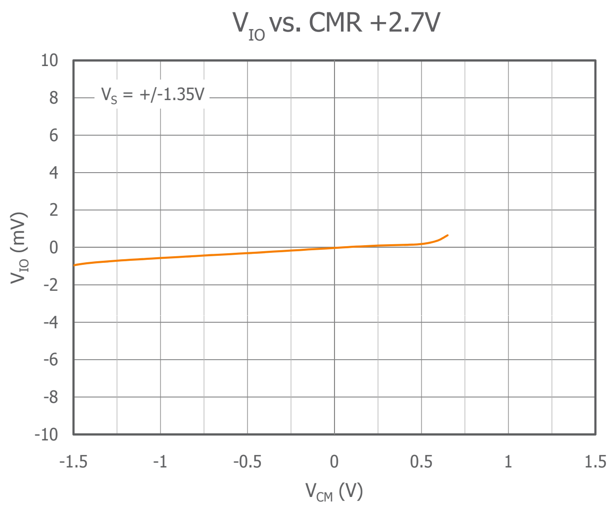
T_A = 25°C, V_S = +5V, R_f = R_g =10kΩ, R_L = 10kΩ to V_S/2, G = 2; unless otherwise noted. **Boldface** limits apply at the temperature extremes.

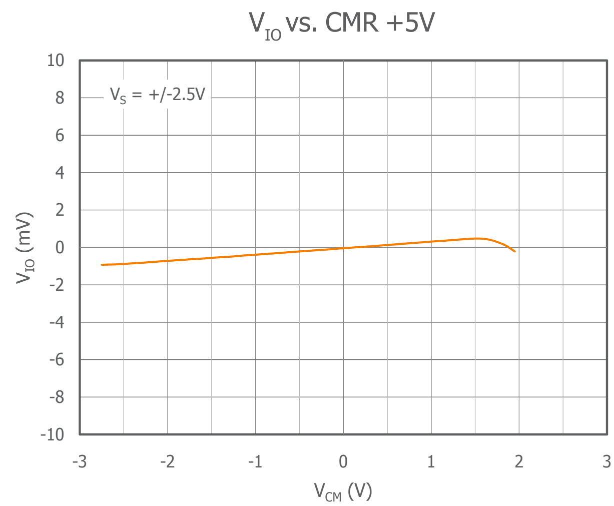
Symbol	Parameter	Conditions	Min	Typ	Max	Units
DC Performance						
V_{IO}	Input Offset Voltage			1.7	7 **9**	mV
dV_{IO}	Average Drift			5		μV/°C
I_b	Input Bias Current			<1	250 **500**	nA
I_{OS}	Input Offset Current			<1	50 **150**	nA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 4V	50	65		dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V, V_O=1V, V_{CM}=1V	50	60		dB
CMIR	Common Mode Input Range	For V_{CM} ≤ 50 dB	0	-0.2		V
				4.2	4	V
A_{OL}	Open-Loop Gain	R_L = 2kΩ	15 **10**	100		V/mV
V_{OUT}	Output Voltage Swing	R_L = 2kΩ to V_S / 2	V^+-300 **V^+-400**	V^+-40		mV
				120	300 **400**	mV
		R_L = 10kΩ to V_S / 2	V^+-100 **V^+-200**	V^+-10		mV
				65	180 **280**	mV
I_{SC}	Short Circuit Output Current	Sourcing V_O=0V	5	60		mA
		Sinking V_O=5V	10	160		mA
I_S	Supply Current			130	250 **350**	μA
AC Performance						
SR	Slew Rate			>1		V/μs
GBWP	Gain Bandwidth Product	C_L=200 pF		1		MHz
Φ_m	Phase Margin			60		°
G_m	Gain Margin			10		dB
e_n	Input Voltage Noise	f = 1kHz		39		nV/√Hz

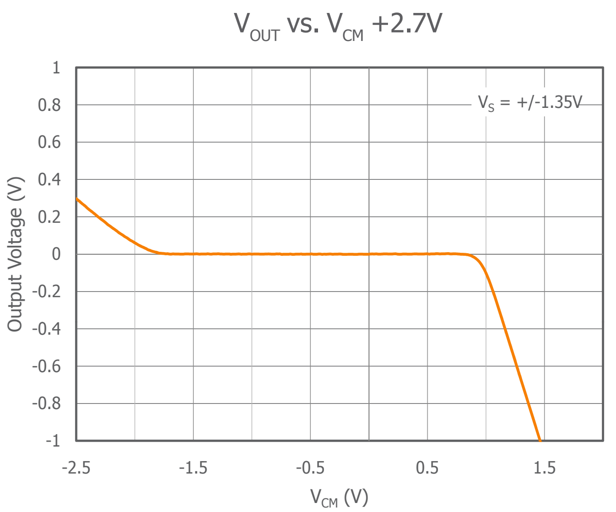
Notes:
Min max specifications are guaranteed by testing, design, or characterization

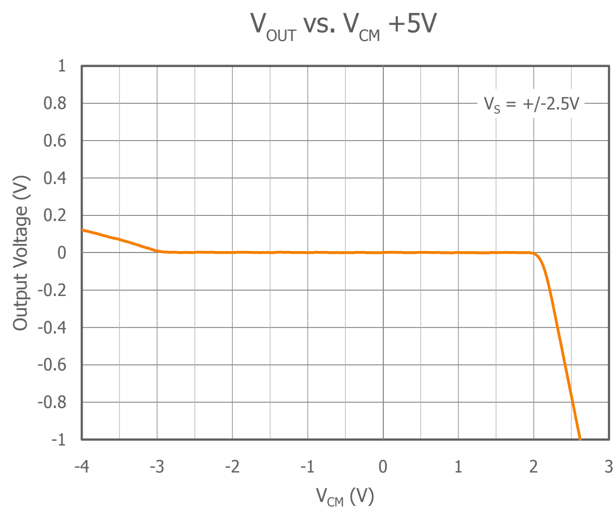
Typical Performance Characteristics at +5V - Continued

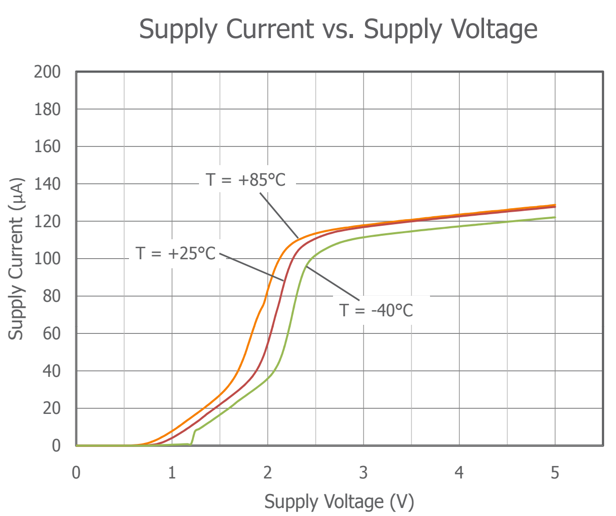
T_A = 25°C, V_S = +5V, R_f = R_g =10kΩ, R_L = 10kΩ to V_S/2, G = 2; unless otherwise noted.

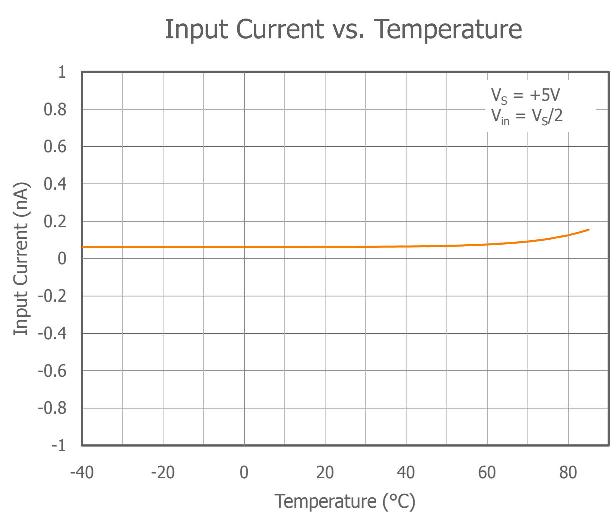








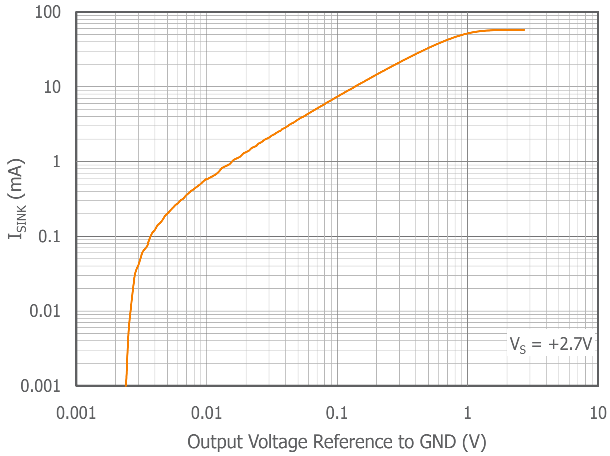




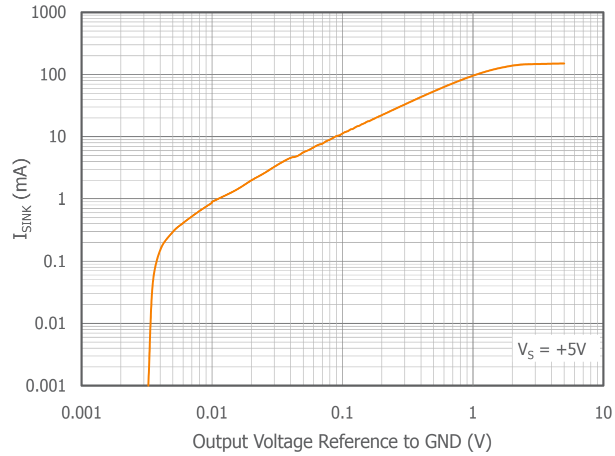
Typical Performance Characteristics at +5V - Continued

T_A = 25°C, V_S = +5V, R_f = R_g =10kΩ, R_L = 10kΩ to V_S/2, G = 2; unless otherwise noted.

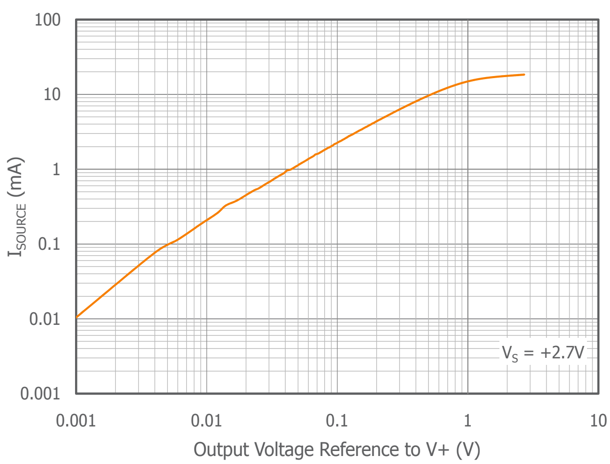
Sinking Current vs. Output Voltage +2.7V



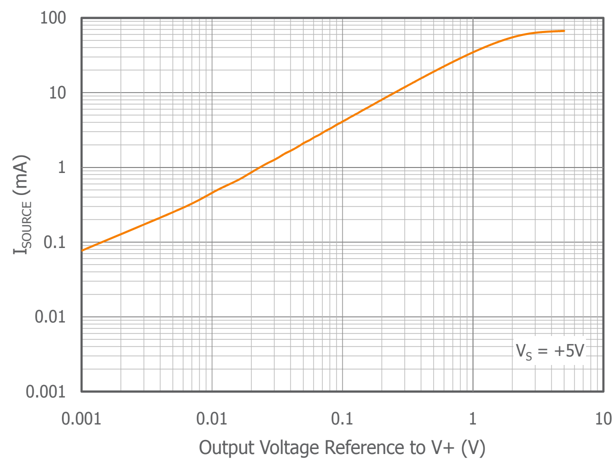
Sinking Current vs. Output Voltage +5V



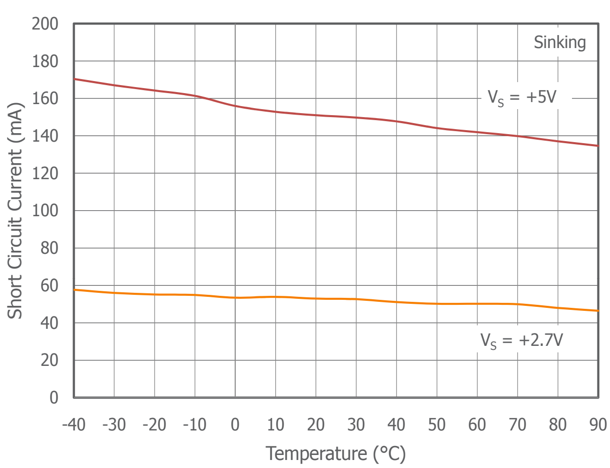
Sourcing Current vs. Output Voltage +2.7V



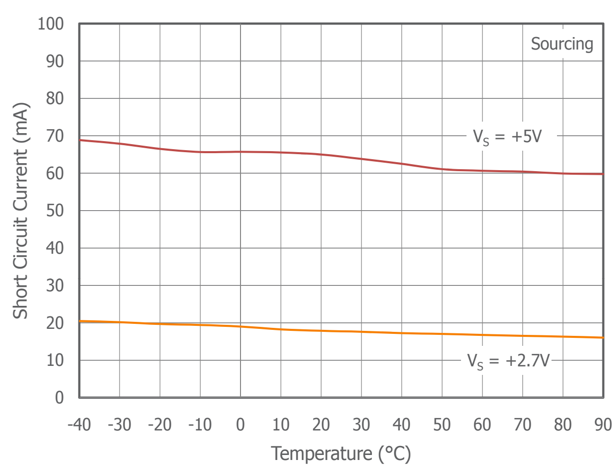
Sourcing Current vs. Output Voltage +5V



Short Circuit Current vs. Temperature (Sinking)

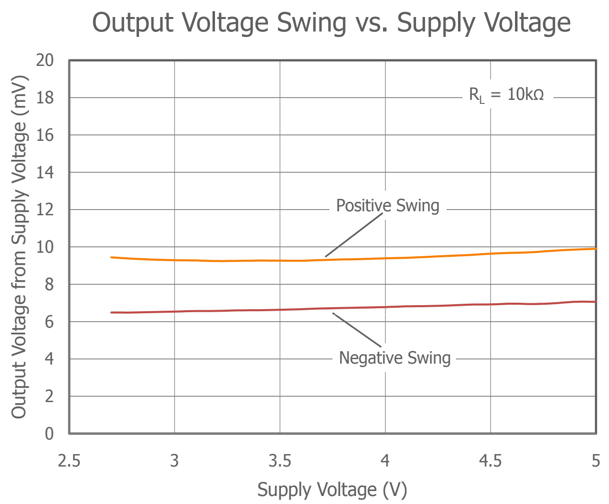


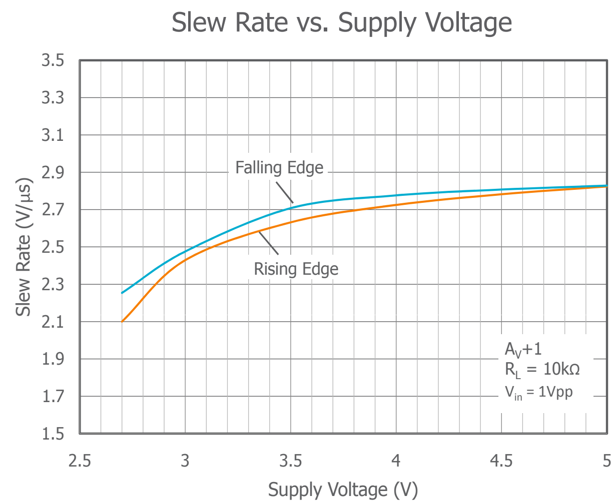
Short Circuit Current vs. Temperature (Sourcing)

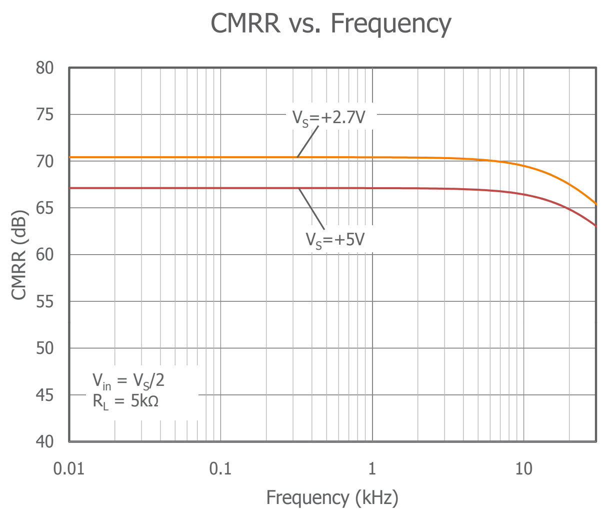


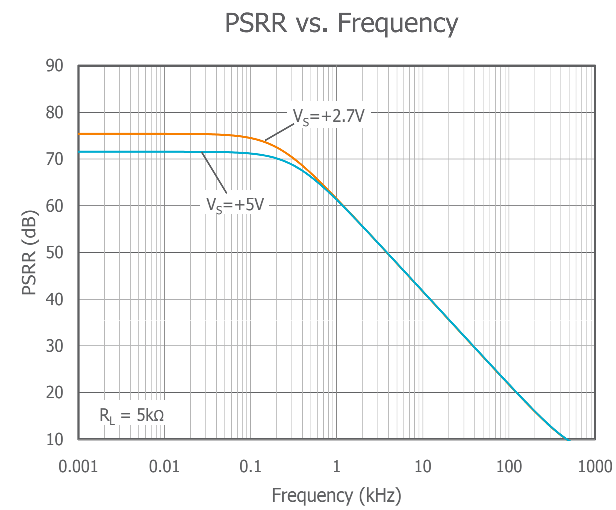
Typical Performance Characteristics at +5V - Continued

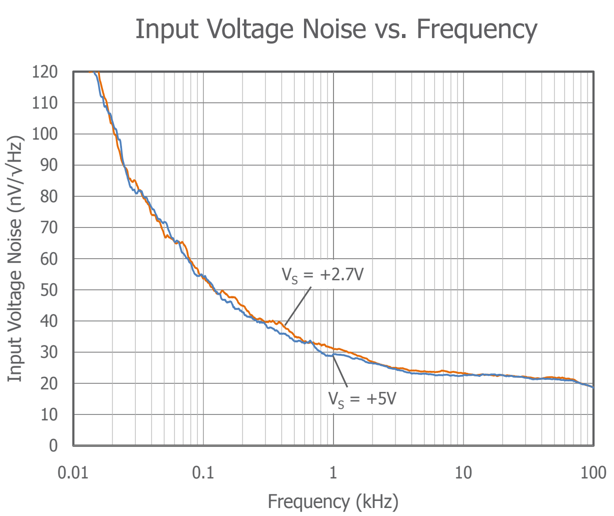
T_A = 25°C, V_S = +5V, R_f = R_g =10kΩ, R_L = 10kΩ to V_S/2, G = 2; unless otherwise noted.

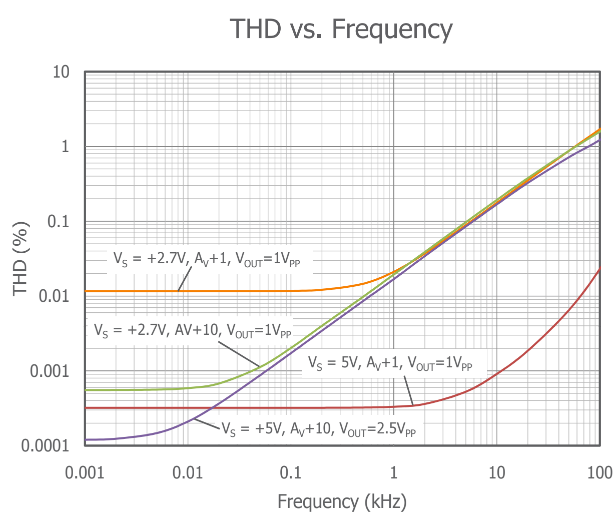








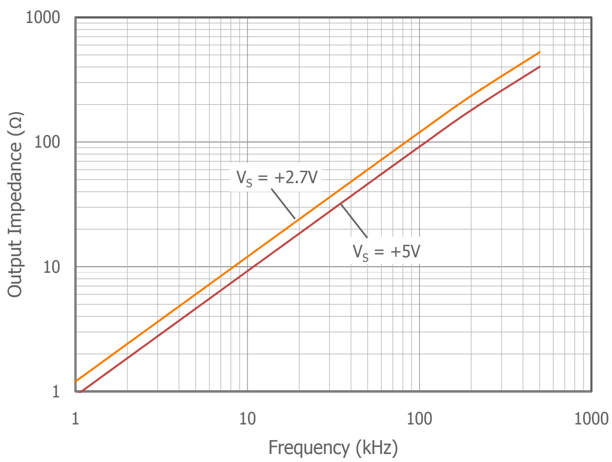




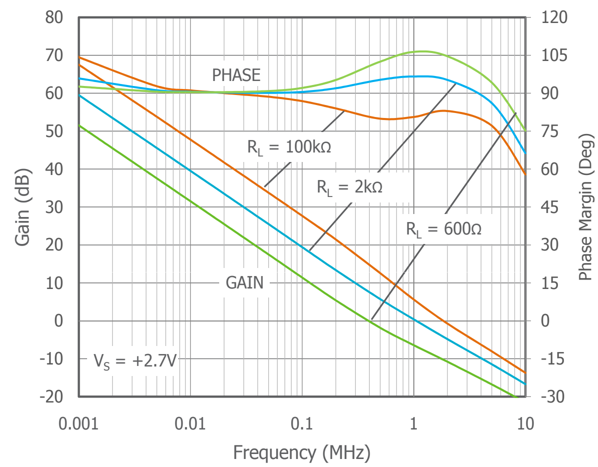
Typical Performance Characteristics at +5V - Continued

T_A = 25°C, V_S = +5V, R_f = R_g =10kΩ, R_L = 10kΩ to V_S/2, G = 2; unless otherwise noted.

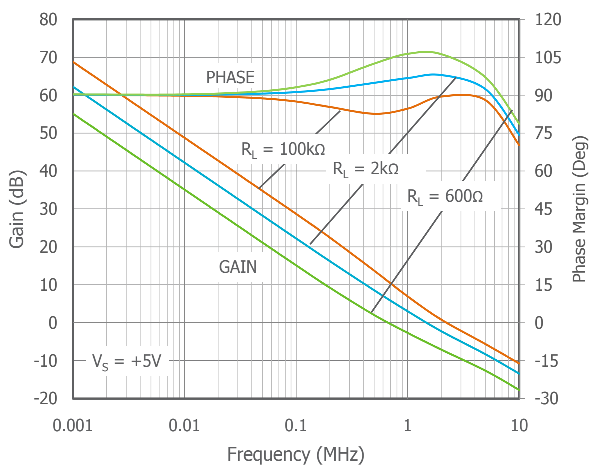
Open Loop Output Impedance vs. Frequency



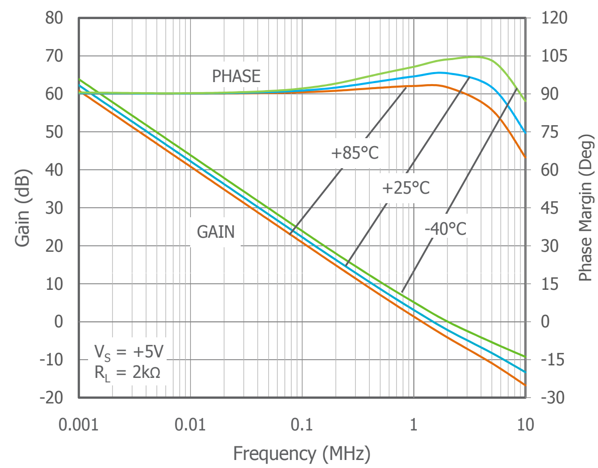
Open Loop Frequency Response +2.7V



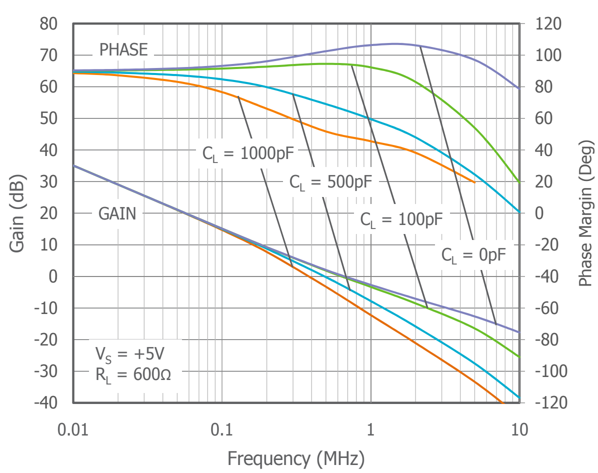
Open Loop Frequency Response 5V



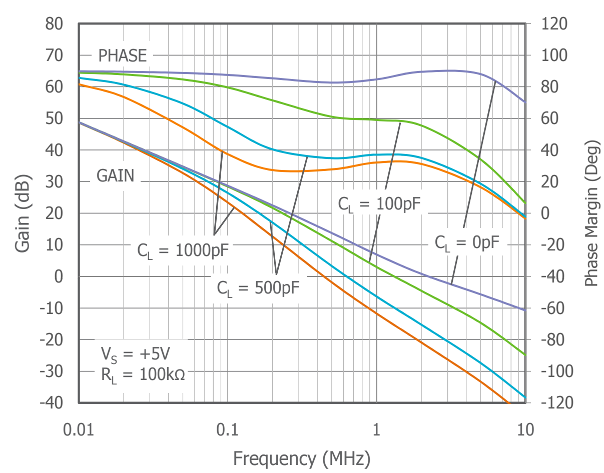
Open Loop Frequency Response vs. Temperature



Gain and Phase vs. Capacitive Load R_L=600Ω



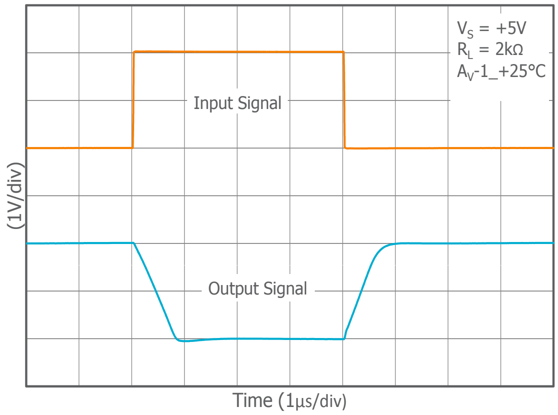
Gain and Phase vs. Capacitive Load R_L=100kΩ



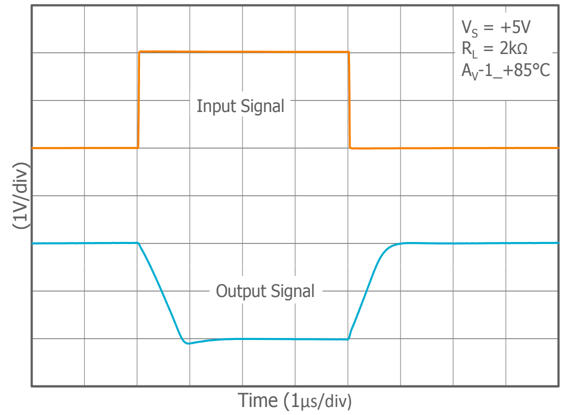
Typical Performance Characteristics at +5V - Continued

T_A = 25°C, V_S = +5V, R_f = R_g =10kΩ, R_L = 10kΩ to V_S/2, G = 2; unless otherwise noted.

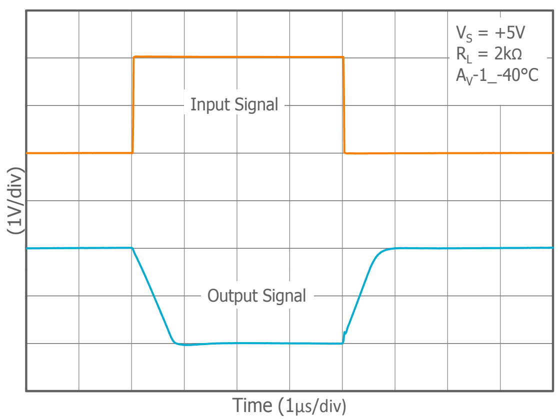
Inverting Large Signal Pulse Response



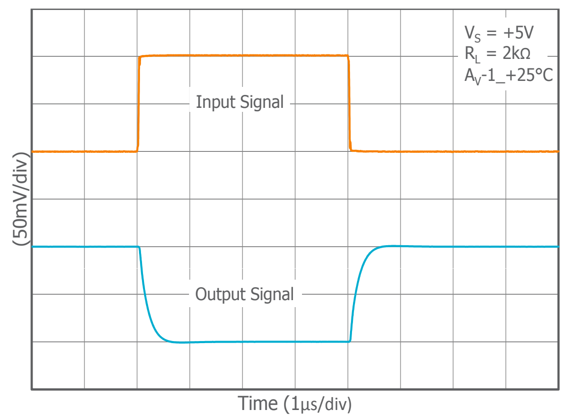
Inverting Large Signal Pulse Response



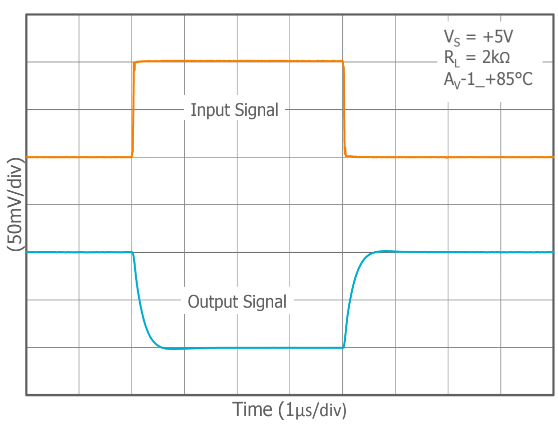
Inverting Large Signal Pulse Response



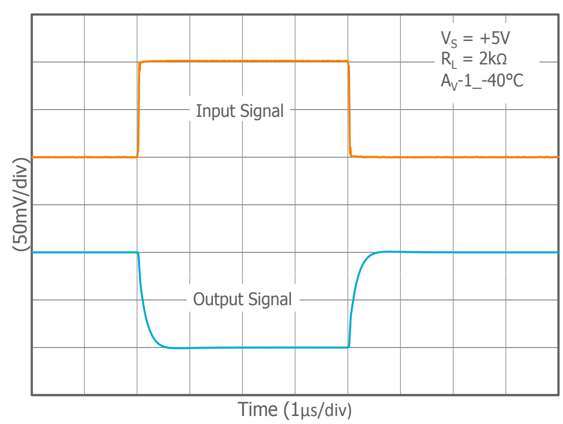
Inverting Small Signal Pulse Response



Inverting Small Signal Pulse Response



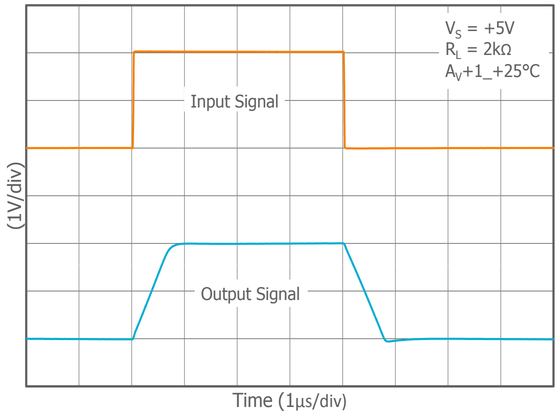
Inverting Small Signal Pulse Response



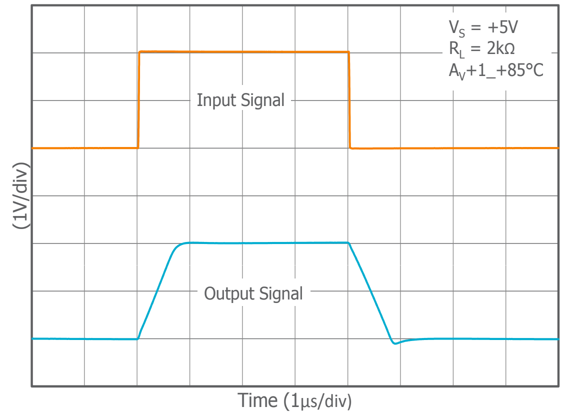
Typical Performance Characteristics at +5V - Continued

T_A = 25°C, V_S = +5V, R_f = R_g =10kΩ, R_L = 10kΩ to V_S/2, G = 2; unless otherwise noted.

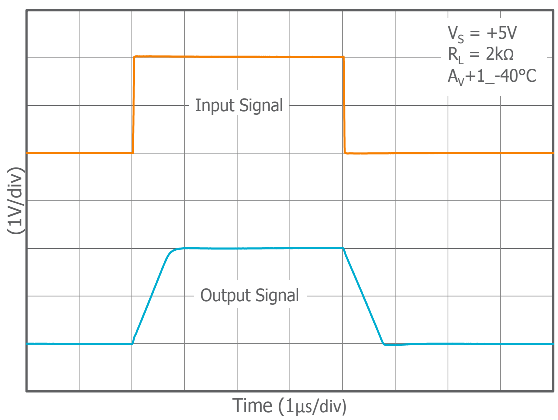
Non-Inverting Large Signal Pulse Response



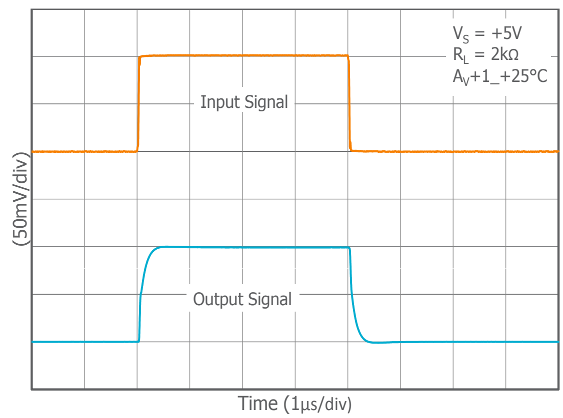
Non-Inverting Large Signal Pulse Response



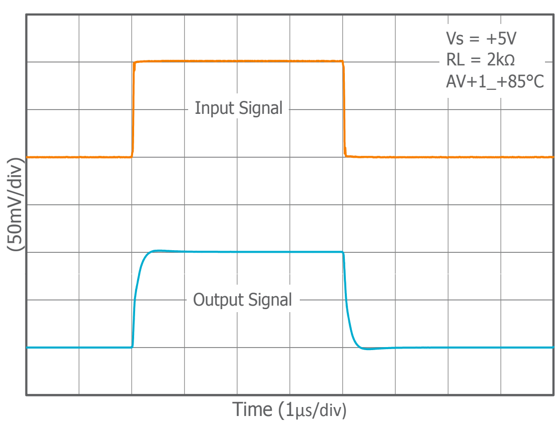
Non-Inverting Large Signal Pulse Response



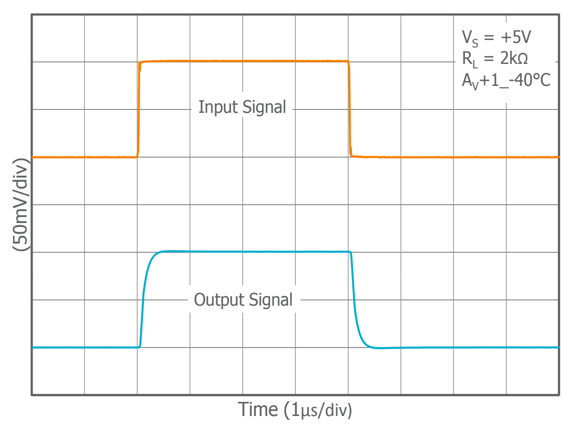
Non-Inverting Small Signal Pulse Response



Non-Inverting Small Signal Pulse Response



Non-Inverting Small Signal Pulse Response



Application Information

General Description

The LMV321 is a single supply, general purpose, voltage-feedback amplifier fabricated on a CMOS process. The LMV321 offers 1MHz gain bandwidth product, >1V/µs slew rate, and only 130µA supply current. It features a rail-to-rail output stage and is unity gain stable.

The common mode input range extends to 200mV below ground and to 800mV below Vs. Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct. The output will stay at the rail during this overdrive condition.

The output stage is short circuit protected and offers "soft" saturation protection that improves recovery time.Figures 1, 2, and 3 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations. Figure 4 shows the typical non-inverting gain circuit for single supply applications

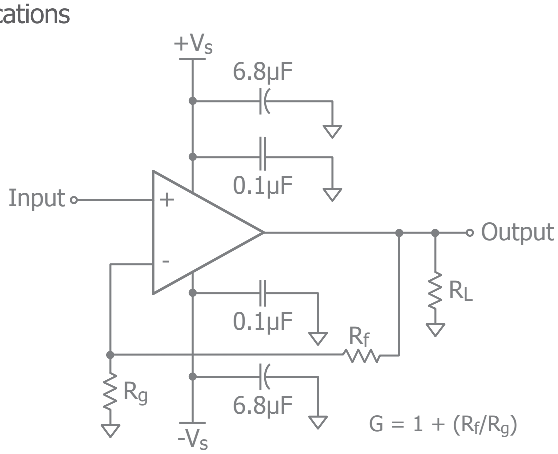


Figure 1. Typical Non-Inverting Gain Circuit

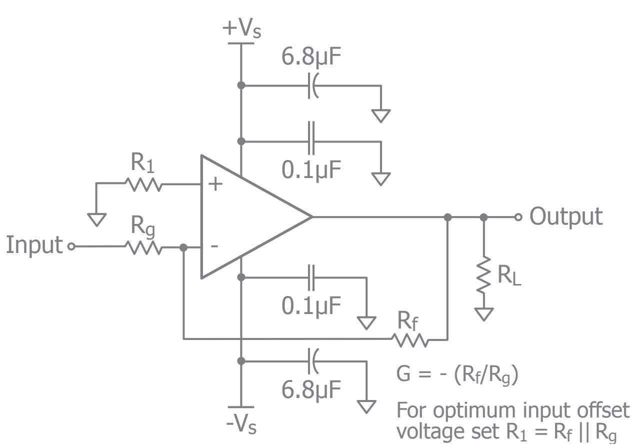


Figure 2. Typical Inverting Gain Circuit

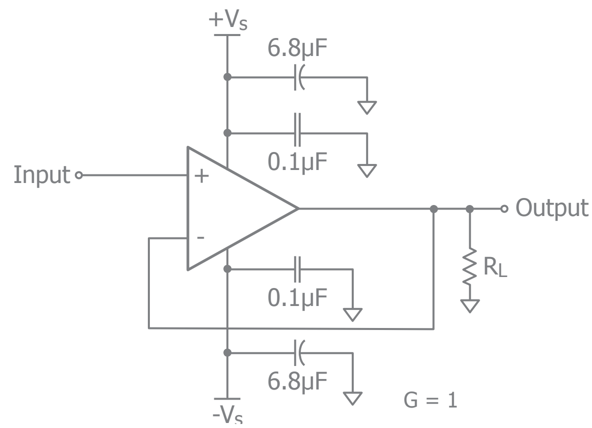


Figure 3. Unity Gain Circuit

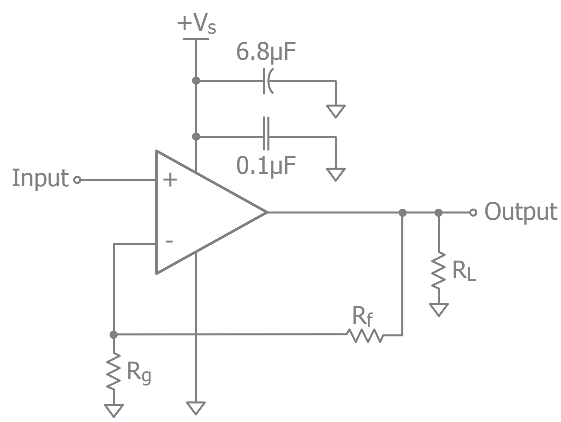


Figure 4. Single Supply Non-Inverting Gain Circuit

Power Dissipation

Power dissipation should not be a factor when operating under the stated 2kΩ load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond it's intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value Theta$_{JA}$ (Θ_{JA}) is used along with the total die power dissipation.

$$T_{Junction} = T_{Ambient} + (\Theta_{JA} \times P_D)$$

Where $T_{Ambient}$ is the temperature of the working environment.

In order to determine P_D, the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{supply} - P_{load}$$

Supply power is calculated by the standard power equation.

$$P_{supply} = V_{supply} \times I_{RMS\ supply}$$

$$V_{supply} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{load} = ((V_{LOAD})_{RMS}{}^2)/Rload_{eff}$$

The effective load resistor ($Rload_{eff}$) will need to include the effect of the feedback network. For instance,

$Rload_{eff}$ in Figure 3 would be calculated as:

$$R_L \parallel (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$$P_D = P_{Quiescent} + P_{Dynamic} - P_{Load}$$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{Supply}. Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{LOAD})_{RMS} = V_{PEAK} / \sqrt{2}$$

$$(I_{LOAD})_{RMS} = (V_{LOAD})_{RMS} / Rload_{eff}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{DYNAMIC} = (V_{S+} - V_{LOAD})_{RMS} \times (I_{LOAD})_{RMS}$$

Assuming the load is referenced in the middle of the power rails or $V_{supply}/2$.

The LMV321 is short circuit protected. However, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions.

Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S, between the amplifier and the load to help improve stability and settling performance. Refer to Figure 5.

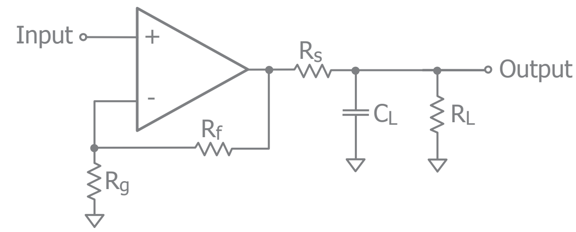


Figure 5. Addition of R_S for Driving Capacitive Loads

For a given load capacitance, adjust R_S to optimize the tradeoff between settling time and bandwidth. In general, reducing R_S will increase bandwidth at the expense of additional overshoot and ringing.

Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies, based on whether the input or output is overdriven and by how much the range is exceeded. The LMV321 and will typically recover in less than 5us from an overdrive condition. Figure 6 shows the LMV321 in an overdriven condition.

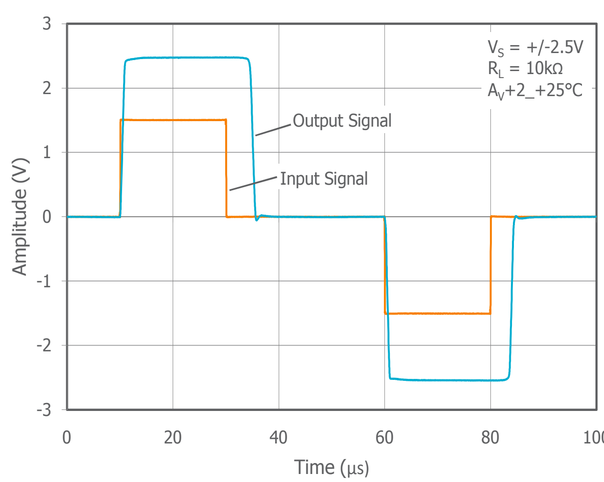


Figure 6. Overdrive Recovery

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. CADEKA has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8μF and 0.1μF ceramic capacitors for power supply decoupling

- Place the 6.8μF capacitor within 0.75 inches of the power pin
- Place the 0.1μF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 7-9. These evaluation boards are built for dual supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.

2. Use C3 (6.8uF) and C4 (0.1uF), if the -VS pin of the amplifier is not directly connected to the ground plane.

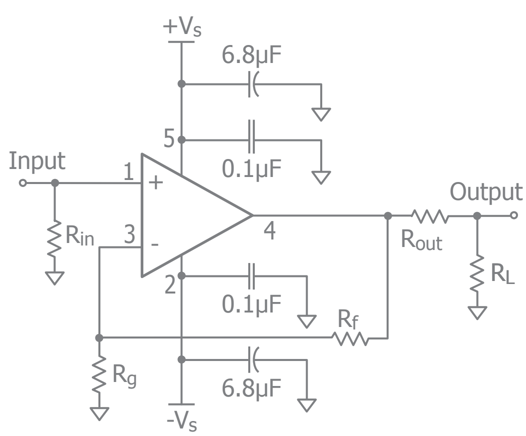


Figure 7. CEB004 Schematic

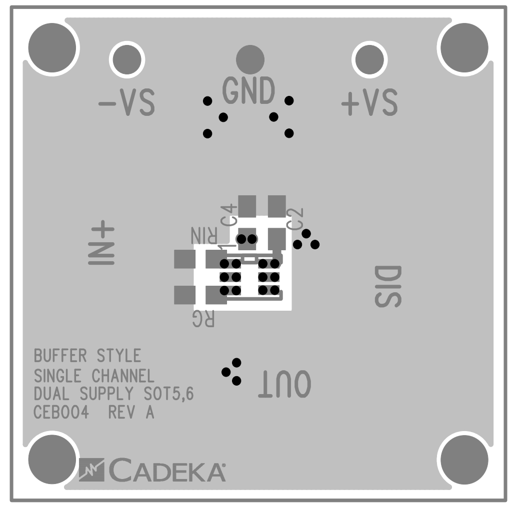


Figure 8. CEB004 Top View

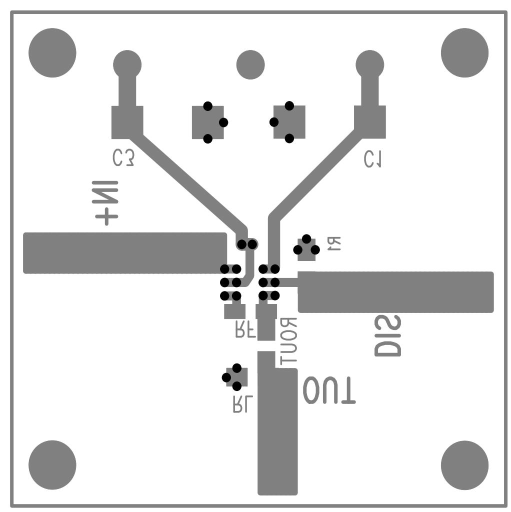
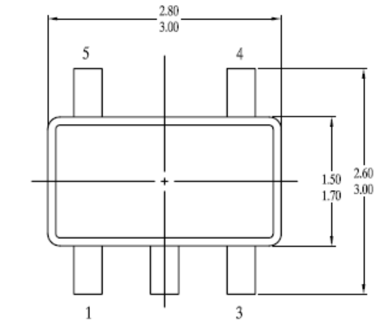


Figure 9. CEB004 Bottom View

Mechanical Dimensions

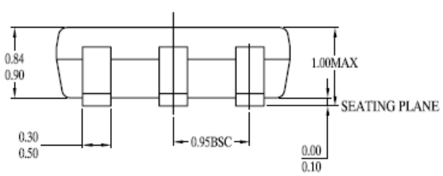
TSOT-5 Package



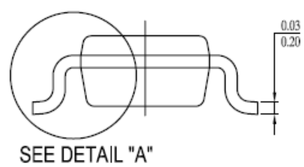
TOP VIEW

NOTE:

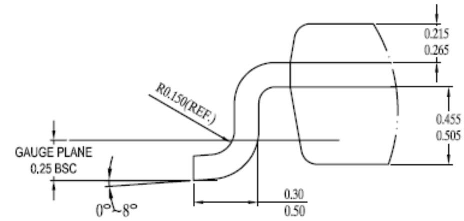
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE INTERLEAD FALSH OR PROTRUSION
3. PACKAGE WIDTH DOES NOTINCLUDE INTERLEAD FALSH OR PROTRUSION.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5. DRAWING CONFROMS TO JEDEC MO-193, VARIATION AA.
6. DRAWING IS NOT TO SCALE.



FRONT VIEW



SIDE VIEW



DETAIL "A"

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