

## General Description

The MxL7213 is a dual channel, 13A step-down power module. It includes a wide 4.5V to 16V input voltage range and supports two outputs each with an output voltage range of 0.6V to 5.3V, set by a single external resistor. The MxL7213 requires just a few input and output capacitors, which simplifies design and shortens time-to-market. The module supplies either two 13A outputs, a single 26A or up to 100A when paralleled with additional MxL7213 modules. Attention to thermal design, component selection and internal construction results in higher efficiency and extended operating range relative to devices with the same industry standard pinout.

The complete switch mode DC/DC power supply integrates the control, drivers, bootstrap diodes, bootstrap capacitors, inductors, MOSFETs and HF bypass capacitors in a single package for point-of-load conversions.

The MxL7213 includes a temperature diode that enables device temperature monitoring. It also has an adjustable switching frequency and utilizes a peak current mode architecture which allows fast line and load transient response.

A host of protection features, including overcurrent, over-temperature, short-circuit and UVLO, help this module achieve safe operation under abnormal operating conditions.

The MxL7213 is available in two space saving, RoHS compliant and thermally enhanced packages: a 15mm x 15mm x 4.41mm LGA package and a 15mm x 15mm x 5.01mm BGA package.

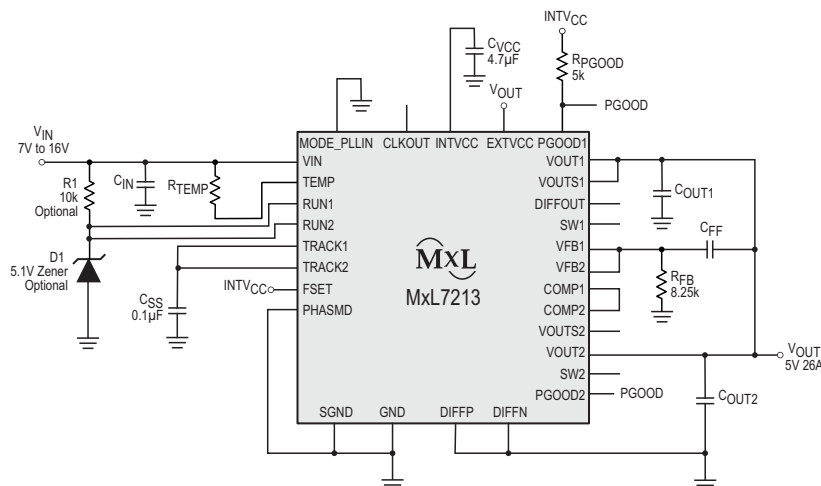
## Features

- Dual 13A or single 26A output
- Input voltage range: 4.5V to 16V
- Output voltage range: 0.6V to 5.3V
- Multiphase current sharing with multiple MxL7213s for up to 100A output
- Frequency synchronization
- Higher efficiency than competitive devices with the same industry standard pinout
- Differential remote sense amplifier
- Peak current mode architecture for fast transient response
- Adjustable switching frequency (250kHz to 780kHz)
- Overcurrent protection
- Output overvoltage protection
- Internal temperature monitor and thermal shutdown protection
- Thermally enhanced packages:
  - 15mm x 15mm x 4.41mm LGA package
  - 15mm x 15mm x 5.01mm BGA package

## Applications

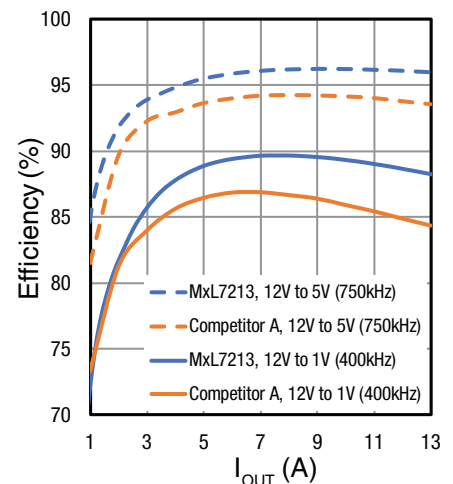
- Telecom and Networking Equipment
- Industrial Equipment
- Test Equipment

## Typical Application



**Figure 1: Typical Application: 26A, 5V Output DC/DC Power Module**

Ordering Information - [page 34](#)



**Figure 2: Efficiency Advantage vs. Competition**

## Revision History

| Document No. | Release Date | Change Description  |
|--------------|--------------|---|
| 074DSR01     | 4/1/19       | Initial release.  |
| 074DSR02     | 5/16/19      | Remove stray line from Recommended PCB Layout. Correct number of phases sentence under Multiphase Operation and current source and external lock sentences under Frequency Selection and Phase-Lock Loop. Correct SGND to GND in INTVCC pin description. Changed $TC_{VTEMP}$ to $-2.2\text{mV}/^\circ\text{C}$ . |
| 074DSR03     | 9/19/19      | Update efficiency, power loss, and de-rating graphs. Removed output voltage noise graph. Update compensation section, thermal resistances, and capacitor table. $V_{OUT}$ maximum changed to 16V. Update ordering information.  |

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## Specifications

### Absolute Maximum Ratings

**Important:** The stresses above what is listed under Table 1 may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed under Table 1 or any other conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above what is listed under Table 3 for extended periods of time may affect device reliability. Solder reflow profile is specified in the IPC/JEDEC J-STD-020C standard.

**Table 1: Absolute Maximum Ratings**

| Parameter                                       | Minimum | Maximum                   | Units |
|---|---------|---------------------------|-------|
| $V_{IN}$  | -0.3    | 18                        | V     |
| $V_{SW1}, V_{SW2}$                              | -1      | 23                        | V     |
| PGOOD1, PGOOD2, COMP1, COMP2                    | -0.3    | 6                         | V     |
| INTV <sub>CC</sub> , EXTV <sub>CC</sub>         | -0.3    | 6                         | V     |
| MODE/PLLIN, f <sub>SET</sub> , TRACK1, TRACK2   | -0.3    | INTV <sub>CC</sub>        | V     |
| DIFFOUT   | -0.3    | INTV <sub>CC</sub> - 1.1V | V     |
| PHASMD  | -0.3    | INTV <sub>CC</sub>        | V     |
| $V_{OUT1}, V_{OUT2}, V_{OUTS1}, V_{OUTS2}$      | -0.3    | 6                         | V     |
| DIFFP, DIFFN                                    | -0.3    | INTV <sub>CC</sub>        | V     |
| RUN1, RUN2, V <sub>FB1</sub> , V <sub>FB2</sub> | -0.3    | INTV <sub>CC</sub>        | V     |
| INTV <sub>CC</sub> Peak Output Current          |         | 100                       | mA    |
| Storage Temperature Range                       | -65     | 150                       | °C    |
| Peak Package Body Temperature                   |         | 245                       | °C    |

### ESD Ratings

**Table 2: ESD Ratings**

| Parameter                  | Minimum | Maximum | Units |
|----------------------------|---------|---------|-------|
| HBM (Human Body Model)     |         | 2k      | V     |
| CDM (Charged Device Model) |         | 500     | V     |



## Operating Conditions

**Table 3: Operating Conditions**

| Parameter   | Minimum | Typical | Maximum     | Units |
|---|---------|---------|-------------|-------|
| $V_{IN}$  | 4.5     |         | 16          | V     |
| $INTV_{CC}$   | 4.5     |         | 5.5         | V     |
| $EXTV_{CC}$   | 4.7     |         | 6           | V     |
| PGOOD   | 0       |         | $INTV_{CC}$ | V     |
| Switching Frequency   | 250     |         | 780         | kHz   |
| Junction Temperature Range ( $T_J$ )  | -40     |         | 125         | °C    |
| Thermal Resistance from Junction to Ambient ( $\Theta_{JA}$ )                     |         | 7       |             | °C/W  |
| Thermal Resistance from Junction to Bottom of Module Case ( $\Theta_{JCbottom}$ ) |         | 1.5     |             | °C/W  |
| Thermal Resistance from Junction to Top of Module Case ( $\Theta_{JCtop}$ )       |         | 3.86    |             | °C/W  |

## Electrical Characteristics

Specifications are for Operating Junction Temperature of  $T_J = 25^\circ\text{C}$  only; limits applying over the full Operating Junction Temperature range are denoted by a ". Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$  and are provided for reference purposes only. Unless otherwise indicated,  $V_{IN} = 12\text{V}$  and  $V_{RUN1}, V_{RUN2} = 5\text{V}$ . Per [Figure 20](#).

**Table 4: Electrical Characteristics**

| Symbol   | Parameter                                      | Conditions   | • | Min   | Typ   | Max   | Units            |
|--|--|--|---|-------|-------|-------|------------------|
| DC Specifications  |  |  |   |       |       |       |                  |
| $V_{IN(DC)}$   | Input DC voltage                               |  | • | 4.5   |       | 16    | V                |
| $V_{OUT1(RANGE)}$<br>$V_{OUT2(RANGE)}$                               | Output DC range                                | $V_{IN} = 5.5\text{V to }16.0\text{V}$   | • | 0.6   |       | 5.3   | V                |
| $V_{OUT1(DC)}$<br>$V_{OUT2(DC)}$                                     | $V_{OUT}$ total variation with line and load   | $C_{IN} = 22\ \mu\text{F} \times 3$<br>$C_{OUT} = 100\ \mu\text{F} \times 1$ Ceramic, 220 $\mu\text{F}$ POSCAP,<br>MODE_PLLIN = GND<br>$V_{IN} = 12\text{V}, V_{OUT} = 1.5\text{V}$                              | • | 1.477 | 1.5   | 1.523 | V                |
| Input Specifications   |  |  |   |       |       |       |                  |
| $V_{RUN1}, V_{RUN2}$   | RUN pin on/off threshold                       | RUN rising   |   | 1.1   | 1.25  | 1.40  | V                |
| $V_{RUN1HYS}, V_{RUN2HYS}$   | RUN pin ON hysteresis                          |  |   |       | 170   |       | mV               |
| $I_{INRUSH(VIN)}$  | Input inrush current at start-up               | $I_{OUT} = 0\text{A}, C_{IN} = 3 \times 22\ \mu\text{F}, C_{SS} = 0.01\ \mu\text{F},$<br>$C_{OUT} = 3 \times 100\ \mu\text{F}, V_{OUT1} = 1.5\text{V},$<br>$V_{OUT2} = 1.5\text{V}, V_{IN} = 12\text{V}$         |   |       | 0.5   |       | A                |
| $I_{Q(VIN)}$   | Input supply bias current                      | $V_{IN} = 12\text{V}, V_{OUT} = 1.5\text{V},$<br>pulse-skipping mode   |   |       | 5     |       | mA               |
|  |  | $V_{IN} = 12\text{V}, V_{OUT} = 1.5\text{V},$ switching CCM  |   |       | 85    |       |                  |
|  |  | Shutdown, RUN = 0, $V_{IN} = 12\text{V}$   |   |       | 50    |       | $\mu\text{A}$    |
| $I_{S(VIN)}$   | Input supply current                           | $V_{IN} = 5\text{V}, V_{OUT} = 1.5\text{V}, I_{OUT} = 13\text{A}$  |   |       | 4.34  |       | A                |
|  |  | $V_{IN} = 12\text{V}, V_{OUT} = 1.5\text{V}, I_{OUT} = 13\text{A}$   |   |       | 1.82  |       |                  |
| Output Specifications  |  |  |   |       |       |       |                  |
| $I_{OUT1(DC)}, I_{OUT2(DC)}$   | Output continuous current range <sup>(1)</sup> | $V_{IN} = 12\text{V}, V_{OUT} = 1.5\text{V}$   |   | 0     |       | 13    | A                |
| $\Delta V_{OUT1(LINE)}/V_{OUT1}$<br>$\Delta V_{OUT2(LINE)}/V_{OUT2}$ | Line regulation accuracy                       | $V_{OUT} = 1.5\text{V}, V_{IN}$ from 4.75V to 16V<br>$I_{OUT} = 0\text{A}$ for each output   | • |       | 0.016 | 0.025 | %/V              |
| $\Delta V_{OUT1(LOAD)}/V_{OUT1}$<br>$\Delta V_{OUT2(LOAD)}/V_{OUT2}$ | Load regulation accuracy <sup>(1)</sup>        | $V_{OUT} = 1.5\text{V}, 0\text{A to }13\text{A}, V_{IN} = 12\text{V}$  | • |       | 0.35  | 0.5   | $\pm\%$          |
| $V_{OUT1(AC)}, V_{OUT2(AC)}$   | Output ripple voltage                          | For each output; $I_{OUT} = 0\text{A},$<br>$C_{OUT} = 100\ \mu\text{F} \times 3 / \text{X7R} / \text{ceramic},$<br>470 $\mu\text{F}$ POSCAP, $V_{IN} = 12\text{V}, V_{OUT} = 1.5\text{V},$<br>frequency = 400kHz |   |       | 26    |       | mV <sub>PP</sub> |
| $f_S$ (each channel)   | Output ripple voltage frequency <sup>(2)</sup> | $V_{IN} = 12\text{V}, V_{OUT} = 1.5\text{V}, f_{SET} = 1.25\text{V}$   |   |       | 500   |       | kHz              |
| $f_{SYNC}$ (each channel)  | SYNC capture range                             |  |   | 400   |       | 780   | kHz              |

**Table 4: (Continued) Electrical Characteristics**

| Symbol   | Parameter  | Conditions  | • | Min   | Typ   | Max     | Units      |
|--|--|---|---|-------|-------|---------|------------|
| $\Delta V_{OUT1START}$<br>$\Delta V_{OUT2START}$ | Turn-on overshoot  | $C_{OUT} = 100\mu F / X5R / \text{ceramic}, 470\mu F$<br>POSCAP, $V_{OUT} = 1.5V$ , $I_{OUT} = 0A$ ,<br>$V_{IN} = 12V$<br>Each channel                              |   |       | 10    |         | mV         |
| $t_{START1}$ , $t_{START2}$                      | Turn-on time   | $C_{OUT} = 100\mu F / X5R / \text{ceramic},$<br>470 $\mu F$ POSCAP, No load,<br>TRACK/SS with 0.01 $\mu F$ to GND, $V_{IN} = 12V$<br>Each channel                   |   |       | 4.8   |         | ms         |
| $\Delta V_{OUT1(LS)}$<br>$\Delta V_{OUT2(LS)}$   | Peak deviation for<br>dynamic load   | Load: 0% to 50% to 0% of full load<br>$C_{OUT} = 22\mu F \times 3 / X5R / \text{ceramic},$<br>470 $\mu F$ POSCAP, $V_{IN} = 12V$ , $V_{OUT} = 1.5V$<br>Each channel |   |       | 30    |         | mV         |
| $t_{SETTLE1}$ , $t_{SETTLE2}$                    | Settling time for<br>dynamic load step                                     | Load: 0% to 50% to 0% of full load,<br>$V_{IN} = 12V$ , $C_{OUT} = 100\mu F, 470\mu F$ POSCAP<br>Each channel   |   |       | 20    |         | $\mu s$    |
| $I_{OUT1(PK)}$<br>$I_{OUT2(PK)}$                 | Output current limit   | $V_{IN} = 12V$ , $V_{OUT} = 1.5V$<br>Each channel   |   |       | 20    |         | A          |
| <b>Control Section</b>                           |  |   |   |       |       |         |            |
| $V_{FB1}$ , $V_{FB2}$                            | Voltage at $V_{FB}$ pins   | $I_{OUT} = 0A$ , $V_{OUT} = 1.5V$   | • | 0.594 | 0.600 | 0.606   | V          |
| $I_{FB}$   | Current at $V_{FB}$ pins   |   |   |       | -5    | -20     | nA         |
| $V_{OVL}$  | Feedback overvoltage<br>lockout  |   | • | 0.64  | 0.66  | 0.68    | V          |
| TRACK1 (I),<br>TRACK2 (I)                        | Track pin soft-start<br>pull-up current                                    | TRACK1 (I), TRACK2 (I) start at 0V  |   | 1.1   | 1.25  | 1.4     | $\mu A$    |
| UVLO   | Undervoltage lockout   | $V_{IN}$ falling  |   |       | 3.66  |         | V          |
|  |  | $V_{IN}$ rising   |   |       | 4.25  |         | V          |
| UVLO Hysteresis                                  |  |   |   |       | 600   |         | mV         |
| $t_{ON(MIN)}$                                    | Minimum on-time  |   |   |       | 90    |         | ns         |
| $R_{FBHI1}$ , $R_{FBHI2}$                        | Resistor between<br>$V_{OUTS1}$ , $V_{OUTS2}$ and<br>$V_{FB1}$ , $V_{FB2}$ | Each output   |   | 60.05 | 60.4  | 60.75   | k $\Omega$ |
| $V_{PGOOD1 LOW}$ ,<br>$V_{PGOOD2 LOW}$           | PGOOD voltage low  | $I_{PGOOD} = 2mA$   |   |       | 35    | 50      | mV         |
| $I_{PGOOD}$                                      | PGOOD leakage<br>current   | $V_{PGOOD} = 5V$  |   |       |       | $\pm 5$ | $\mu A$    |
| $V_{PGOOD}$                                      | PGOOD trip level   | $V_{FB}$ with respect to set output voltage<br>$V_{FB}$ ramping negative  |   |       | -10   |         | %          |
|  |  | $V_{FB}$ with respect to set output voltage<br>$V_{FB}$ ramping positive  |   |       | 10    |         |            |
| <b>INTV<sub>CC</sub> Linear Regulator</b>        |  |   |   |       |       |         |            |
| $V_{INTVCC}$                                     | Internal $V_{CC}$ voltage  | $6V < V_{IN} < 16V$   |   | 4.8   | 5     | 5.2     | V          |
| $V_{INTVCC}$<br>Load Regulation                  | INTV <sub>CC</sub> load<br>regulation                                      | $I_{CC} = 0mA$ to 50mA  |   |       | 1     | 2       | %          |

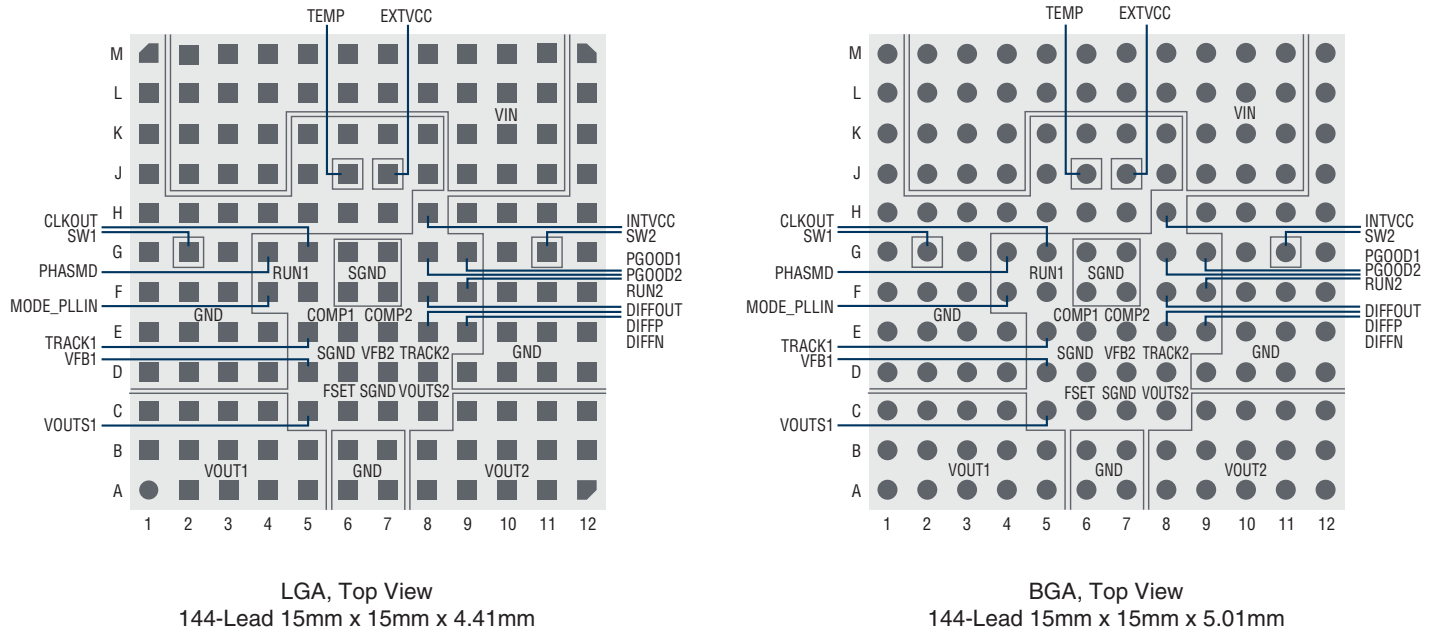
**Table 4: (Continued) Electrical Characteristics**

| Symbol                           | Parameter                              | Conditions   | • | Min                      | Typ   | Max | Units |
|----------------------------------|--|--|---|--------------------------|-------|-----|-------|
| $V_{EXTVCC}$                     | EXTV <sub>CC</sub> switchover voltage  | EXTV <sub>CC</sub> ramping positive                                      | • | 4.5                      | 4.7   |     | V     |
| $V_{EXTVCC(DROP)}$               | EXTV <sub>CC</sub> dropout             | $I_{CC} = 20\text{mA}$ , $V_{EXTVCC} = 5\text{V}$                        |   |                          | 19    | 50  | mV    |
| $V_{EXTVCC(HYST)}$               | EXTV <sub>CC</sub> hysteresis          |  |   |                          | 156   |     | mV    |
| Oscillator and Phase-Locked Loop |  |  |   |                          |       |     |       |
| Frequency Nominal                | Nominal frequency                      | FSET = 1.2V  |   | 450                      | 500   | 550 | kHz   |
| Frequency Low                    | Lowest frequency                       | FSET = 0V  |   | 210                      | 250   | 290 | kHz   |
| Frequency High                   | Highest frequency                      | FSET > 2.4V, up to INTV <sub>CC</sub>                                    |   | 700                      | 780   | 860 | kHz   |
| $I_{FSET}$                       | Frequency set current                  |  |   | 9                        | 10    | 11  | μA    |
| $f_{SYNC}$                       | SYNC capture range                     | Each channel   |   | 250                      |       | 780 | kHz   |
| $R_{MODE\_PLLIN}$                | MODE_PLLIN input resistance            |  |   |                          | 250   |     | kΩ    |
| CLKOUT                           | Phase (relative to V <sub>OUT1</sub> ) | PHASMD = GND   |   |                          | 60    |     | Deg   |
|                                  |  | PHASMD = float   |   |                          | 90    |     | Deg   |
|                                  |  | PHASMD = INTV <sub>CC</sub>  |   |                          | 120   |     | Deg   |
| CLK High                         | Clock High output voltage              |  | 2 |                          |       | V   |       |
| CLK Low                          | Clock Low output voltage               |  |   |                          | 0.2   | V   |       |
| Differential Amplifier           |  |  |   |                          |       |     |       |
| $A_V$                            | Gain                                   |  |   |                          | 1     |     | V/V   |
| $R_{IN}$                         | Input resistance                       | Measured at DIFFP Input  |   |                          | 80    |     | kΩ    |
| $V_{OS}$                         | Input offset voltage                   | $V_{DIFFP} = V_{DIFFOUT} = 1.5\text{V}$ , $I_{DIFFOUT} = 100\mu\text{A}$ |   |                          |       | 2   | mV    |
| PSRR                             | Power Supply Rejection Ratio           | $5\text{V} < V_{IN} < 16\text{V}$  |   |                          | 90    |     | dB    |
| $I_{CL}$                         | Maximum Output current                 |  |   |                          | 3     |     | mA    |
| $V_{DIFFOUT(MAX)}$               | Maximum output voltage                 | $I_{DIFFOUT} = 300\mu\text{A}$   |   | INTV <sub>CC</sub> - 1.4 |       |     | V     |
| GBW                              | Gain Bandwidth Product                 |  |   |                          | 3     |     | MHz   |
| $V_{TEMP}$                       | Diode Connected PNP                    | $I = 100\mu\text{A}$   |   |                          | 0.636 |     | V     |
| $TC_{VTEMP}$                     | Temperature Coefficient                |  | • |                          | -2.2  |     | mV/°C |
| OT                               | Thermal shutdown threshold             | Rising temperature   |   |                          | 145   |     | °C    |
|                                  | Thermal hysteresis                     |  |   |                          | 15    |     | °C    |

1. See output current derating curves for different  $V_{IN}$ ,  $V_{OUT}$  and  $T_A$ .
2. The switching frequency is programmable from 250kHz to 780kHz.

## Pin Information

### Pin Configuration



**Figure 3: Pin Configuration**

### Pin Description

**Table 5: Pin Description**

| Pin Number   | Pin Name | Description  |
|--|----------|--|
| A1, A2, A3, A4, A5,<br>B1, B2, B3, B4, B5,<br>C1, C2, C3, C4   | VOUT1    | Output of the channel 1 power stage. Connect the corresponding output load from the VOUT1 pins to the PGND pins. Direct output decoupling capacitance from VOUT1 to PGND is recommended. |
| A6, A7, B6, B7,<br>D1, D2, D3, D4,<br>D9, D10, D11, D12,<br>E1, E2, E3, E4,<br>E10, E11, E12,<br>F1, F2, F3,<br>F10, F11, F12,<br>G1, G3, G10, G12,<br>H1, H2, H3, H4, H5, H6,<br>H7, H9, H10, H11, H12,<br>J1, J5, J8, J12,<br>K1, K5, K6, K7, K8, K12,<br>L1, L12, M1, M12 | GND      | Ground for the power stage. Connect to the application's power ground plane.   |
| A8, A9, A10, A11, A12,<br>B8, B9, B10, B11, B12,<br>C9, C10, C11, C12  | VOUT2    | Output of the channel 2 power stage. Connect the corresponding output load from the VOUT2 pins to the PGND pins. Direct output decoupling capacitance from VOUT2 to PGND is recommended. |

**Table 5: Pin Description (Continued)**

| Pin Number             | Pin Name          | Description   |
|------------------------|-------------------|---|
| C5, C8                 | VOUTS1,<br>VOUTS2 | These pins are connected internally to the top of the feedback resistor for each output. Connect this pin directly to its specific output or to DIFFOUT when using the remote sense amplifier. When paralleling modules, connect one of the VOUTS pins to DIFFOUT when remote sensing or directly to VOUT when not remote sensing. These pins must be connected to either DIFFOUT or VOUT. This connection provides the feedback path and cannot be left open.  |
| C6                     | FSET              | This pin is used to set the operating frequency via two methods: <ul style="list-style-type: none"> <li>▪ Connect a resistor from this pin to ground</li> <li>▪ Drive this pin with a DC voltage</li> </ul> This pin sources a 10 $\mu$ A current. See <a href="#">Figure 24</a> for frequency of operation vs. FSET voltage.   |
| C7, D6, G6, G7, F6, F7 | SGND              | Ground pin for all analog signals and low power circuits. Connect to GND in one place. See layout guidelines in <a href="#">Figure 40</a> .   |
| D5, D7                 | VFB1, VFB2        | Feedback input to the negative side of the error amplifier for each channel. These pins are each internally connected to VOUTS1 and VOUTS2 via a precision 60.4k $\Omega$ resistor. Vary each output voltage by adding a feedback resistor from VFB to SGND. Tie VFB1 and VFB2 together for parallel operation.   |
| E5, D8                 | TRACK1,<br>TRACK2 | Soft-Start and Output Voltage Tracking pins. Each channel has a 1.25 $\mu$ A pull-up current source. When one channel is configured as a master, adding a capacitor from this pin to ground sets a soft-start ramp rate. The other channel can be set up as the slave and have the master output applied through a voltage divider to the slave's output TRACK pin. For coincidental tracking, this voltage divider is equal to the slave's output feedback divider.  |
| E6, E7                 | COMP1,<br>COMP2   | Current control threshold and error amplifier compensation point for each channel. The current comparator threshold increases with this control voltage. The MxL7213 is internally compensated, however a feed-forward $C_{FF}$ is frequently required (see <a href="#">Table 11</a> ). $R_{COMP}$ and $C_{COMP}$ may be required for certain operating conditions (see <a href="#">Figure 20</a> ). When paralleling both channels, connect the COMP1 and COMP2 pins together.   |
| E8                     | DIFFP             | This pin is the remote sense amplifier's positive input and is connected to the output voltage's remote sense point. If the remote sense amplifier is not used, connect this pin to SGND.<br><br><b>Important:</b> The differential amplifier cannot be used for outputs > 3.3V.  |
| E9                     | DIFFN             | This pin is the remote sense amplifier's negative input and is connected to the remote sense point GND. If the remote sense amplifier is not used, connect this pin to SGND.<br><br><b>Important:</b> The differential amplifier cannot be used for outputs >3.3V.  |
| F4                     | MODE_PLLIN        | Selects between Forced Continuous Mode or Pulse-Skipping Mode and provides the external synchronization input to the Phase Detector Pin. There are three connection options: <ol style="list-style-type: none"> <li>1. Connect this pin to SGND to force both channels into Forced Continuous Mode.</li> <li>2. Connect this pin to INTVCC or leave it floating to enable Pulse-Skipping Mode.</li> <li>3. Connect this pin to an external clock to force both channels into Forced Continuous Mode that are synchronized to the external clock.</li> </ol> |
| F5, F9                 | RUN1, RUN2        | The RUN1 and RUN2 pins enable and disable the module's two channels: <ul style="list-style-type: none"> <li>▪ A voltage above 1.4V will turn on the related channel.</li> <li>▪ A voltage below 1.1V will turn off the related channel.</li> </ul> Each RUN pin has a 1 $\mu$ A pull-up current; once the RUN pin reaches ~1.25V, an additional 4.5 $\mu$ A pull-up current is added to the RUN pin.  |
| F8                     | DIFFOUT           | Output of the internal remote sense amplifier. If remote sensing on channel 1, connect to VOUTS1. If remote sensing on channel 2, connect to VOUTS2. When paralleling modules, connect one of the VOUTS pins to DIFFOUT when remote sensing.<br><br><b>Important:</b> The differential amplifier cannot be used for outputs >3.3V.  |

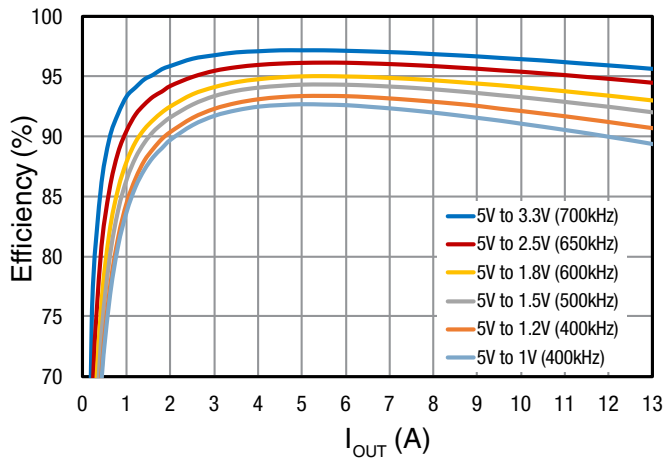
**Table 5: Pin Description (Continued)**

| Pin Number   | Pin Name       | Description  |
|--|----------------|--|
| G2, G11  | SW1, SW2       | Use these pins to access the switching node of each channel. An RC snubber can be connected to reduce switch node ringing. Otherwise, leave these pins floating.   |
| G4   | PHASMD         | This pin selects the CLKOUT phase as follows: <ul style="list-style-type: none"> <li>■ Connect to SGND for 60 degrees</li> <li>■ Connect to INTVCC for 120 degrees</li> <li>■ Leave floating for 90 degrees</li> </ul>   |
| G5   | CLKOUT         | This is the clock output. Its phase is set with the PHASMD pin. It is also used during Multiphase Operation. Refer to the Application Section on <b>Multiphase Operation</b> for more details.   |
| G9, G8   | PGOOD1, PGOOD2 | Power Good outputs. This open-drain output is pulled low when the $V_{OUT}$ of its respective channel is more than $\pm 10\%$ outside regulation.  |
| H8   | INTVCC         | Internal 5V Regulator Output. This voltage powers the control circuits and internal gate driver. Decouple to GND with a $4.7\mu\text{F}$ ceramic capacitor. INTVCC is activated when either RUN1 or RUN2 is activated.   |
| J6   | TEMP           | The internal temperature sensing diode monitors the temperature change with voltage change on $V_{BE}$ . Connect to VIN through a resistor to limit the current to $100\mu\text{A}$ .<br>$R = (V_{IN} - 0.6\text{V}) / 100\mu\text{A}$   |
| J7   | EXTVCC         | External power input that is enabled through a switch to INTVCC whenever EXTVCC is $>4.7\text{V}$ . Do not exceed 6V on this input. Connect this pin to $V_{IN}$ when operating $V_{IN}$ on 5V. An efficiency increase that is a function of $(V_{IN} - \text{INTVCC})$ multiplied by the power MOSFET driver current occurs when the feature is used. $V_{IN}$ must be applied before EXTVCC, and EXTVCC must be removed before $V_{IN}$ . To increase efficiency, a 5V output can be tied to this pin. |
| M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, L2, L3, L4, L5, L6, L7, L8, L9, L10, L11, J2, J3, J4, J9, J10, J11, K2, K3, K4, K9, K10, K11 | VIN            | Power input pins. Connect input voltage from these pins to GND. Direct input decoupling capacitance from VIN to GND is recommended.  |

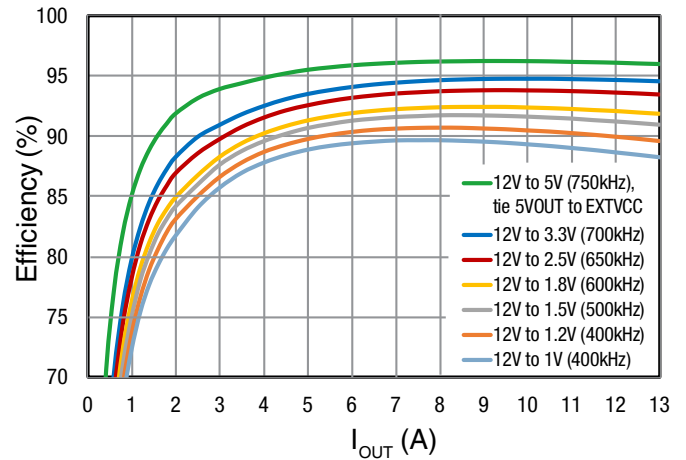
1. Use test points to monitor signal pin connections.

# Typical Performance Characteristics

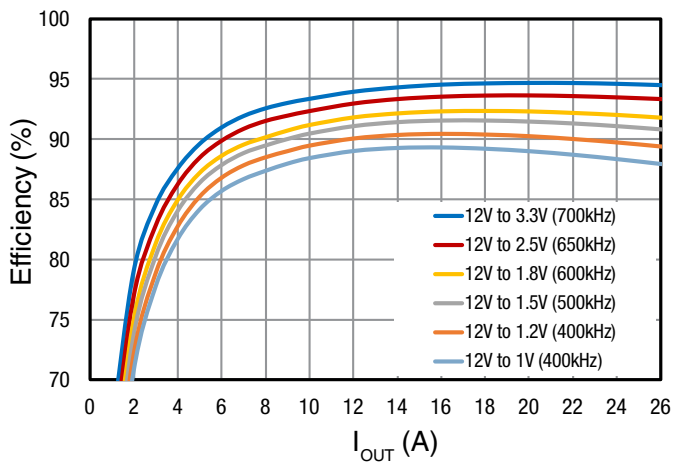
See Figure 20 for typical application schematic.



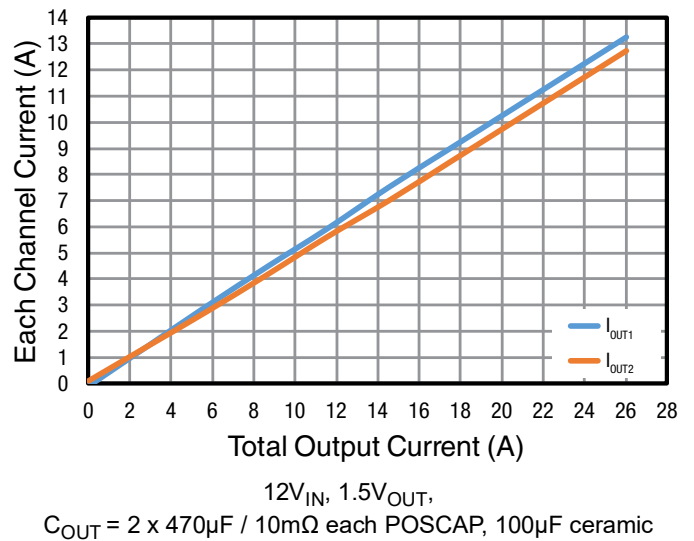
**Figure 4: Efficiency: Single Phase,  $V_{IN} = 5V$**



**Figure 5: Efficiency: Single Phase,  $V_{IN} = 12V$**



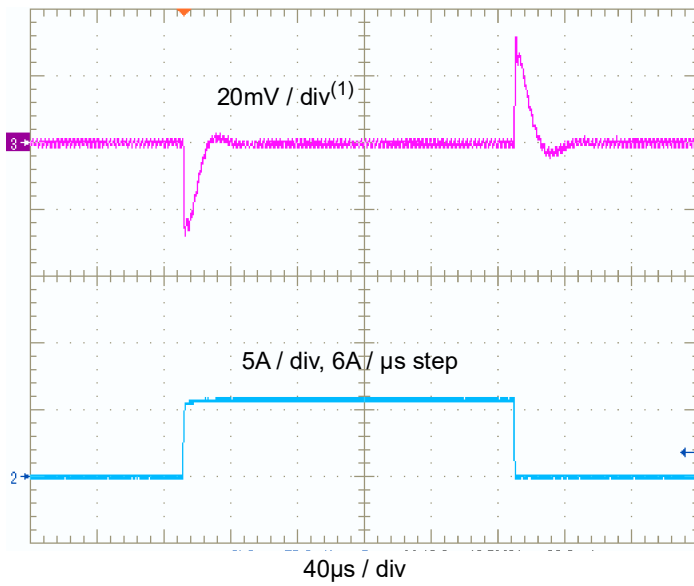
**Figure 6: Efficiency: Dual Phase,  $V_{IN} = 12V$**



**Figure 7: Output Current Sharing**

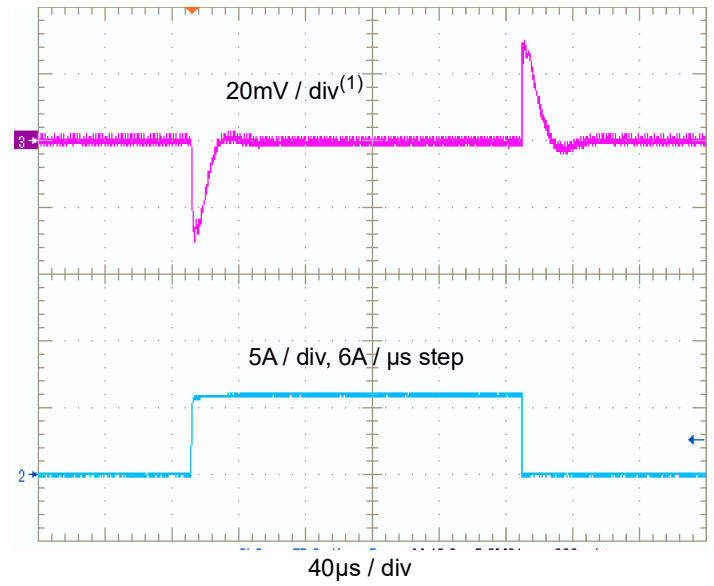


See Figure 20 for typical application schematic.



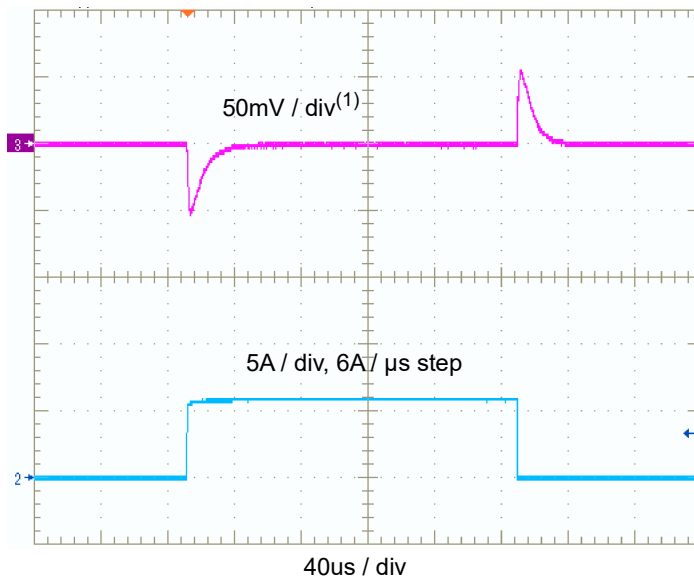
$C_{OUT}$ : 2 x 470 $\mu$ F / 10m $\Omega$  each POSCAP, 100 $\mu$ F ceramic;  
 $C_{FF}$  = 180pF

**Figure 8: 12V to 1V Load Step Response**



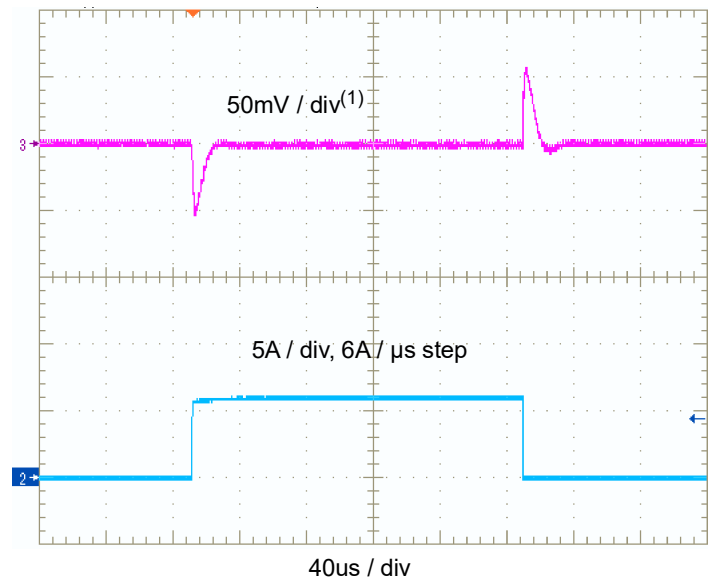
$C_{OUT}$ : 2 x 470 $\mu$ F / 10m $\Omega$  each POSCAP, 100 $\mu$ F ceramic;  
 $C_{FF}$  = 180pF

**Figure 9: 12V to 1.2V Load Step Response**



$C_{OUT}$ : 220 $\mu$ F / 9m $\Omega$  POSCAP, 100 $\mu$ F ceramic;  $C_{FF}$  = 100pF,

**Figure 10: 12V to 1.5V Load Step Response**

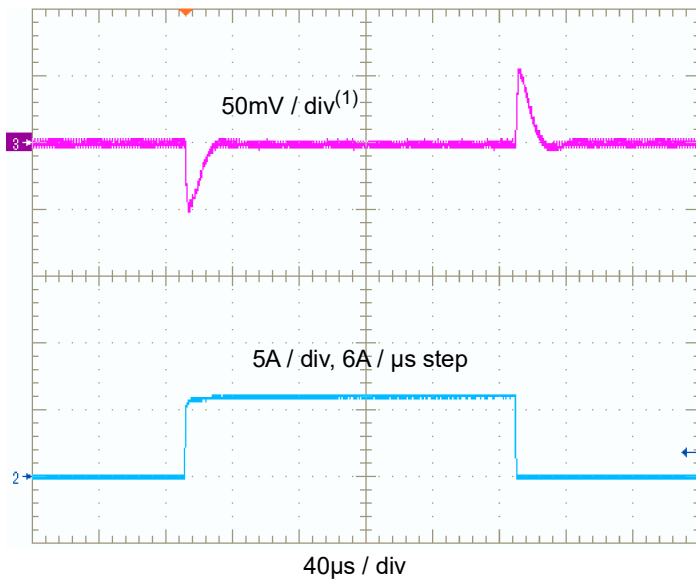


$C_{OUT}$ : 220 $\mu$ F / 9m $\Omega$  POSCAP, 100 $\mu$ F ceramic;  $C_{FF}$  = 47pF

**Figure 11: 12V to 1.8V Load Step Response**

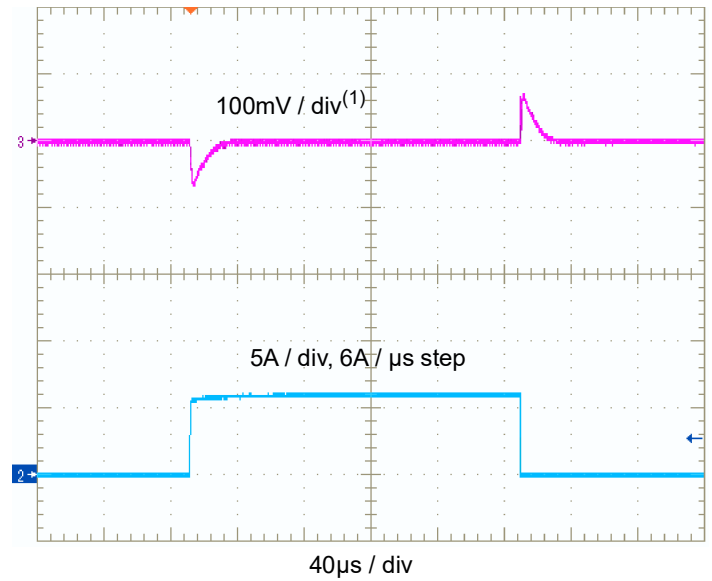
1. Waveform averaged to remove high frequency ripple.

See [Figure 20](#) for typical application schematic.



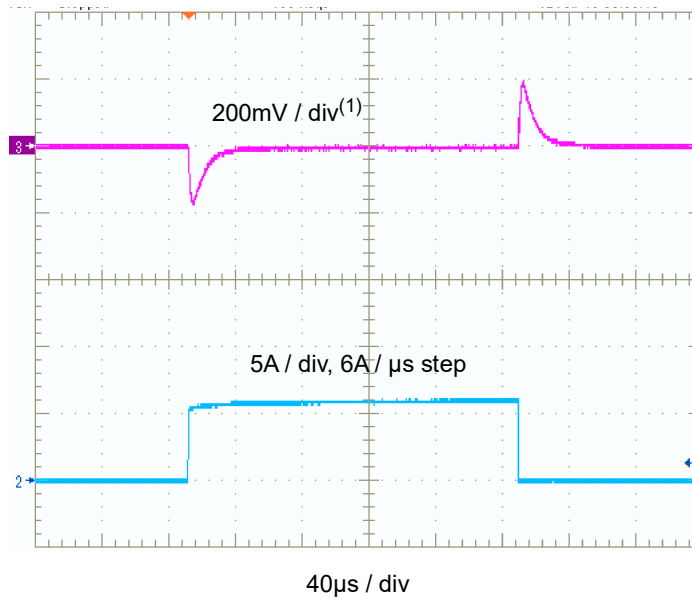
$C_{OUT}$ : 220 $\mu$ F / 9m $\Omega$  POSCAP, 100 $\mu$ F ceramic

**Figure 12: 12V to 2.5V Load Step Response**



$C_{OUT}$ : 100 $\mu$ F / 18m $\Omega$  POSCAP, 100 $\mu$ F ceramic;  $C_{FF}$  = 47pF

**Figure 13: 12V to 3.3V Load Step Response**

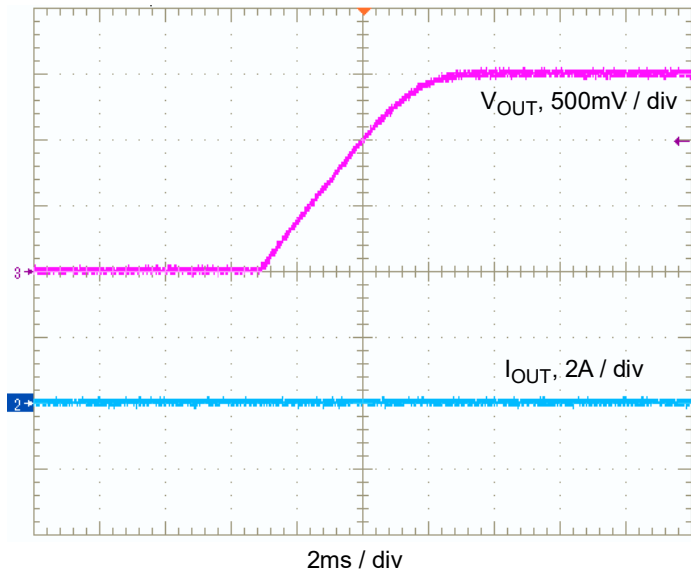


$C_{OUT}$ : 100 $\mu$ F ceramic;  $C_{FF}$  = 22pF

**Figure 14: 12V to 5V Load Step Response**

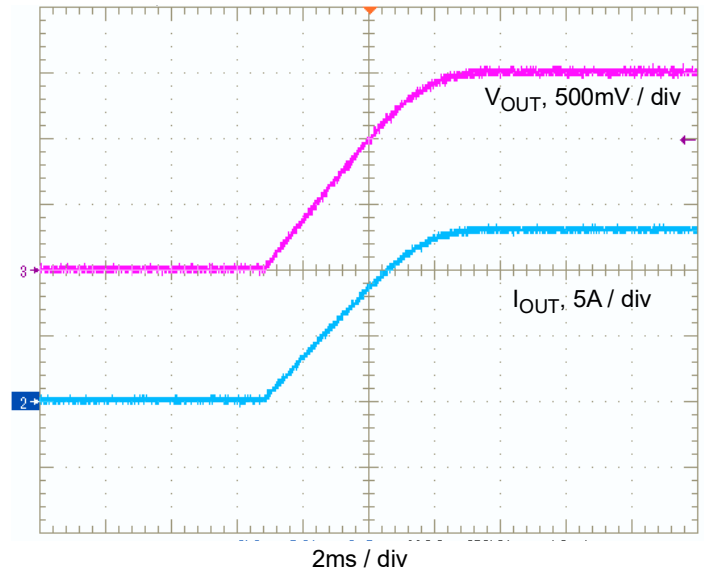
1. Waveform averaged to remove high frequency ripple.

See Figure 20 for typical application schematic.



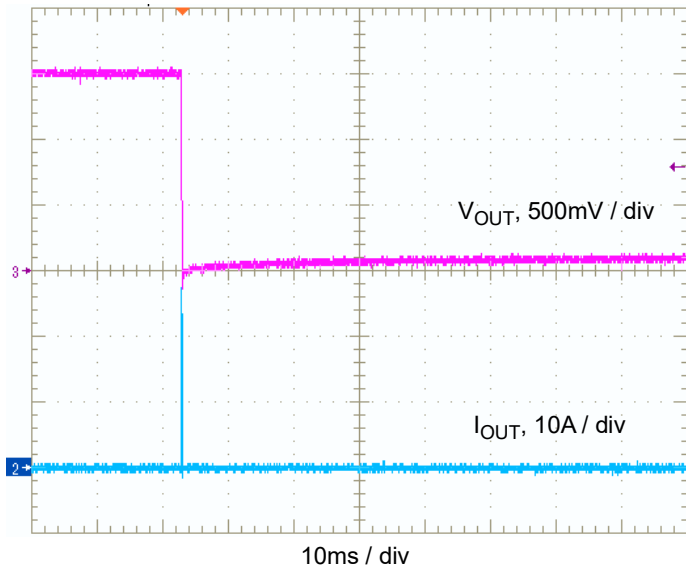
12V<sub>IN</sub>, 1.5V<sub>OUT</sub>, soft-start capacitor = 0.01μF,  
C<sub>OUT</sub> = 2 x 470μF / 10mΩ each POSCAP, 100μF ceramic,  
use RUN pin to control start-up

**Figure 15: Single Phase Start-Up,  
12V to 1.5V, No Load**



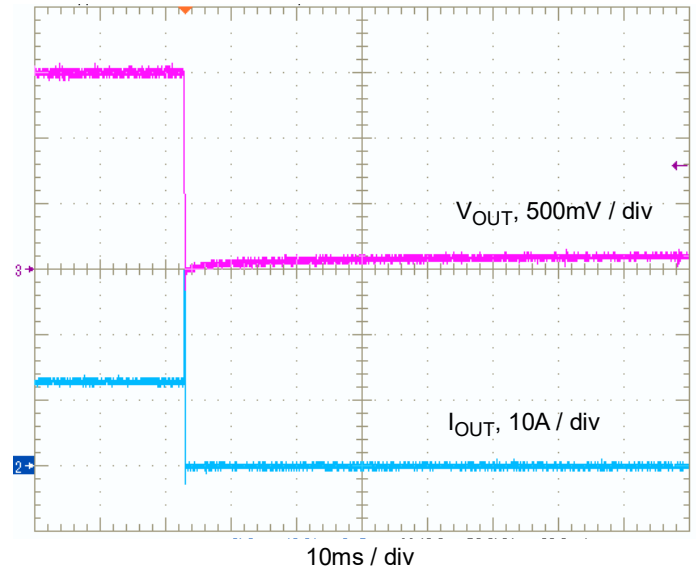
12V<sub>IN</sub>, 1.5V<sub>OUT</sub>, soft-start capacitor = 0.01μF,  
C<sub>OUT</sub> = 2 x 470μF / 10mΩ each POSCAP, 100μF ceramic,  
use RUN pin to control start-up

**Figure 16: Single Phase Start-Up,  
12V to 1.5V, 13A Load**



12V<sub>IN</sub>, 1.5V<sub>OUT</sub>, soft-start capacitor = 0.01μF,  
C<sub>OUT</sub> = 2 x 470μF / 10mΩ each POSCAP, 100μF ceramic

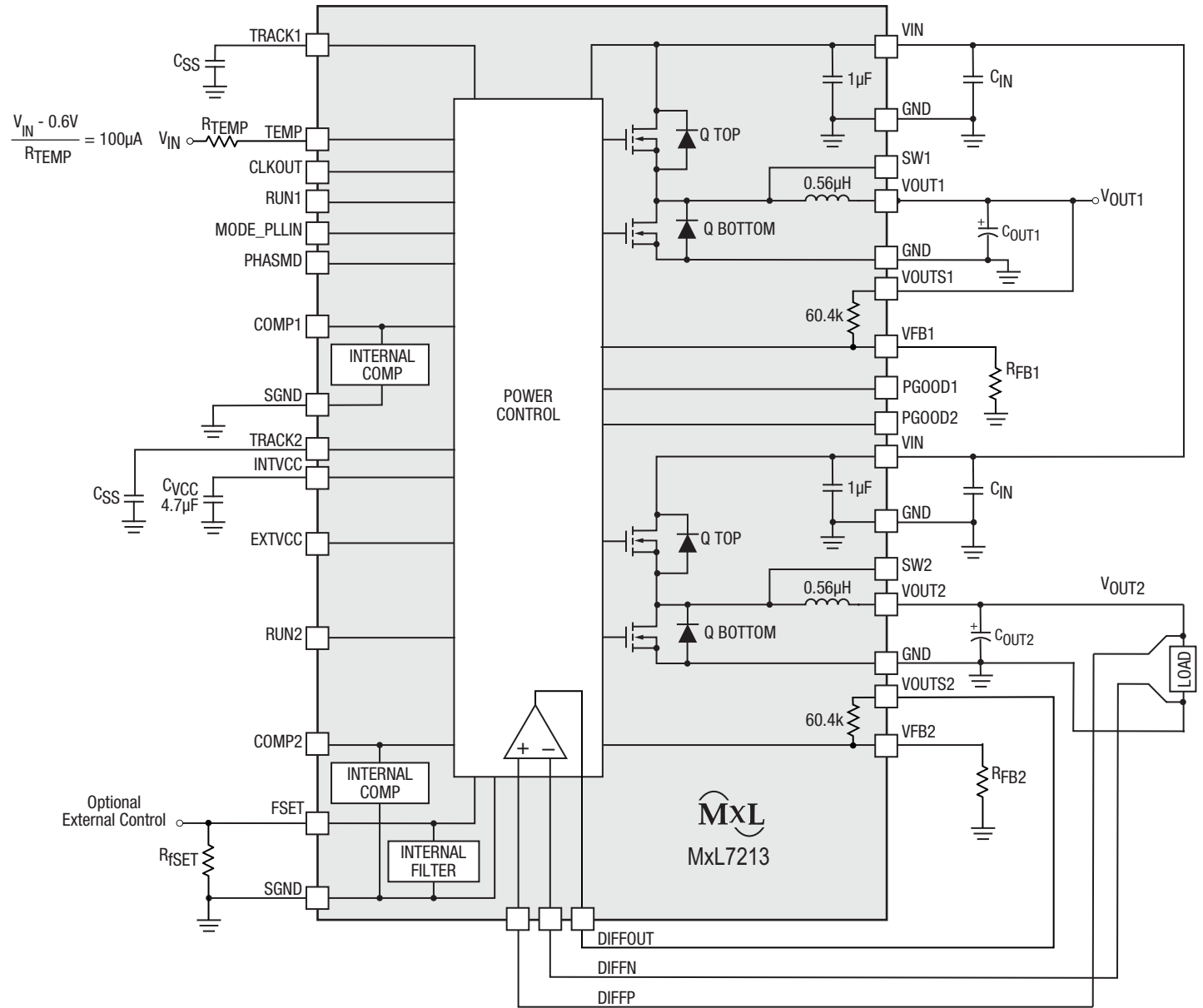
**Figure 17: Short-Circuit, 12V to 1.5V, 0A Load**



12V<sub>IN</sub>, 1.5V<sub>OUT</sub>, soft-start capacitor = 0.01μF,  
C<sub>OUT</sub> = 2 x 470μF / 10mΩ each POSCAP, 100μF ceramic

**Figure 18: Short-Circuit, 12V to 1.5V, 13A Load**

# Functional Block Diagram



**Figure 19: Functional Block Diagram**

## Operation

### Power Module Description

The MxL7213 is a dual-channel, standalone, synchronous step-down power module that provides two 13A outputs or one 26A output. This power module has a continuous input voltage range of 4.5V to 16V and has been optimized for 12V conversions. It provides precisely regulated output voltages from 0.6V to 5.3V that are set by a single external resistor. See typical application schematic in [Figure 20](#).

The module employs a constant frequency, peak current mode control loop architecture. It also has an internal feedback loop compensation. These features ensure the MxL7213 has sufficient stability margins as well as good transient performance over a wide range of output capacitors, including low ESR ceramic capacitors.

The peak current mode control supports cycle-by-cycle fast current limit and current limit hiccup in overcurrent or output short circuit conditions. The open-drain PGOOD outputs are pulled low when the output voltage exceeds  $\pm 10\%$  of its set point. Once the output voltage exceeds  $+10\%$ , the high side MOSFET is kept off while the low side MOSFET turns on, clamping the output voltage. The overvoltage and undervoltage detection are referenced to the feedback pin.

The RUN1 and RUN2 pins enable and disable the module's two channels. Pulling a RUN pin below 1.1V forces the respective regulator into shutdown mode and turns off both the high side and low side MOSFETs. The TRACK pins are used for either programming the output voltage ramp and voltage tracking during start-up, or for soft-starting the channels.

The MxL7213 includes a differential remote sense amplifier (with a gain of +1). This amplifier can be used to accurately sense the voltage at the load point on one of the module's two outputs or on a single parallel output.

The switching frequency is programmed from 250kHz to 780kHz using an external resistor on the FSET pin. For noise sensitive applications, the module can be synchronized to an external clock.

The MxL7213 module can be configured to current share between channels. It can also be set to current share between modules (multiphase or ganged operation). Using the MODE\_PLLIN, PHASMD and CLKOUT pins, multiphase operation of up to 8 phases is possible with multiple MxL7213s running in parallel.

Using the the MODE\_PLLIN pin to operate in pulse-skipping mode results in high efficiency performance at

light loads. This light load feature extends battery life.

The EXTVCC pin allows an external 5V supply to power the module and reduce the power dissipation in the internal 5V LDO. EXTVCC has a threshold of 4.7V for activation and a max rating of 6V. It must sequence on after  $V_{IN}$  and sequence off before  $V_{IN}$ .

Monitor the internal die temperature by using the TEMP pin. Pull the anode up to  $V_{IN}$  through an external resistor to set the bias current in the diode. Thermal simulation has shown that the thermal monitor on the controller die is within  $5^{\circ}\text{C}$  of the MOSFETs.

## Applications Information

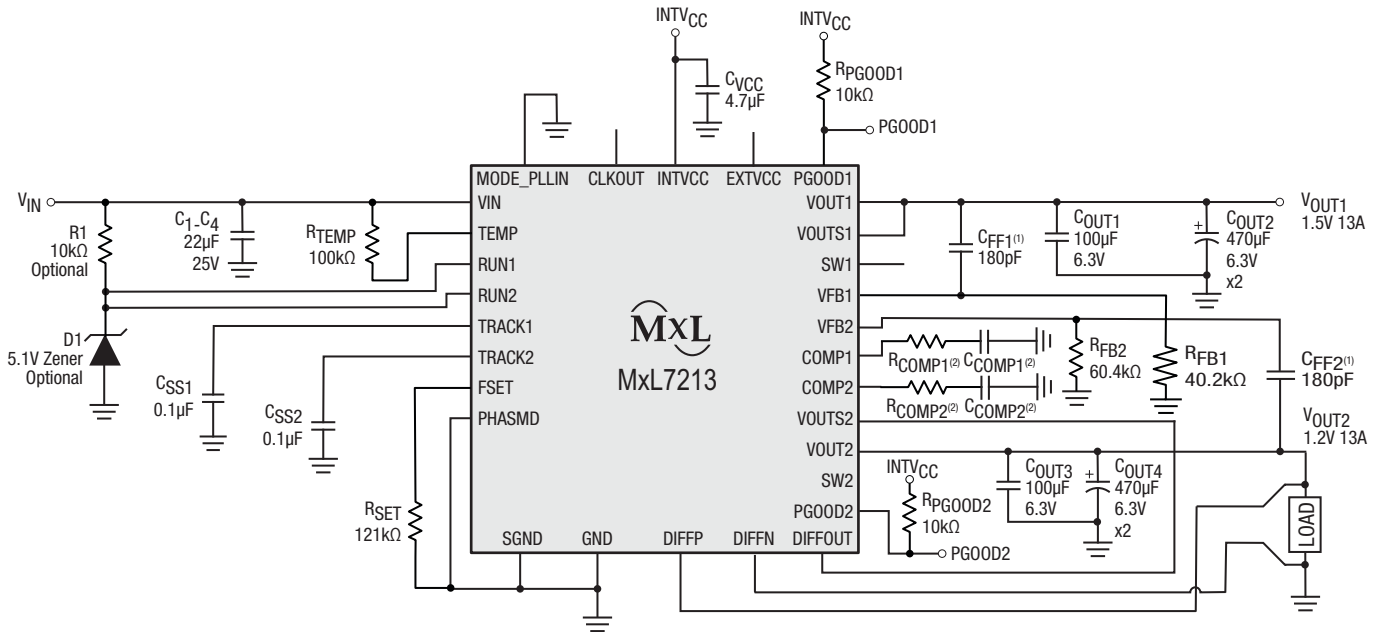
### Typical Application Circuit

The typical MxL7213 application circuit is shown in [Figure 20](#). External component selection is primarily determined by the maximum load current and output voltage. Refer to [Table 11](#) for a selection of various design solutions. Additional information about selecting external compensation components can be found in the [Stability and Compensation](#) section.

### $V_{IN}$ to $V_{OUT}$ Step-Down Ratios

For a given input voltage, there are limitations to the maximum possible  $V_{IN}$  and  $V_{OUT}$  stepdown ratios.

The MxL7213 has a maximum duty cycle of 90% at 500kHz, meaning the maximum output voltage will be approximately  $0.9 \times V_{IN}$ . When running at high duty cycle, output current can be limited by the power dissipation in the high-side MOSFET. The minimum output voltage from a given input is controlled by the minimum on-time which is 90ns. The minimum output voltage is  $V_{IN} \times f_{SW}(\text{MHz}) \times 0.09\mu\text{s}$ . To get a lower output voltage, reduce the switching frequency.



1. See Table 11.
2. May be necessary for certain operating conditions.

**Figure 20: Typical 5V<sub>IN</sub> to 16V<sub>IN</sub>, 1.5V and 1.2V Outputs**

## Output Voltage Programming

The PWM controller has an internal 0.6V reference. A resistor  $R_{FB}$  between the VFB and SGND pins programs the output voltage. A 60.4kΩ internal feedback resistor is connected from VOUTS1 to VFB1 and from VOUTS2 to VFB2, as illustrated in the functional block diagram.

$R_{FB}$  values for corresponding standard  $V_{OUT}$  values are shown in Table 6. Use the following equation to determine the  $R_{FB}$  value for other  $V_{OUT}$  levels:

$$V_{OUT} = \frac{0.6 \times (60.4 + R_{FB})}{R_{FB}}$$

When paralleling multiple channels and devices, a common  $R_{FB}$  resistor may be used. Select the  $R_{FB}$  as explained above. Note that VFB pins have an  $I_{FB}$  max of 20nA per channel. To reduce  $V_{OUT}$  error due to  $I_{FB}$ , use an additional  $R_{FB}$  and connect corresponding VOUTS to VOUT as shown in Figure 21.

When paralleling multiple channels and devices:

- Tie all COMP pins together for current sharing between the phases.

- Tie the TRACK pins together and use a single soft-start capacitor to soft-start the regulator.
- Increase the soft-start current parameter by the number of paralleled channels when solving the soft-start equation. (Refer to the **Soft Start and Output Voltage Tracking** section).

**Table 6: VFB Resistor Table vs. Various Output Voltages**

| $V_{OUT}$ | 0.6V | 1.0V  | 1.2V  | 1.5V  | 1.8V  | 2.5V  | 3.3V  | 5V    |
|-----------|------|-------|-------|-------|-------|-------|-------|-------|
| $R_{FB}$  | Open | 90.9k | 60.4k | 40.2k | 30.2k | 19.1k | 13.3k | 8.25k |

## Input Capacitors

Connect the MxL7213 to a low impedance DC source. Use four 22µF ceramic input capacitors to reduce RMS ripple current on the regulator input.

A bulk input capacitor is required if the source impedance is high or the source capacitance is low. For additional bulk input capacitance, use a surface mount 47µF to 100µF aluminum electrolytic bulk capacitor.

## Output Capacitors

The bulk output capacitors, denoted as  $C_{OUT}$ , need to have low enough effective series resistance (ESR) to meet output voltage ripple and transient requirements. The MxL7213 can use low ESR tantalum capacitors, low ESR polymer capacitors, ceramic capacitors or a combination for  $C_{OUT}$ . Refer to [Table 11](#) for  $C_{OUT}$  recommendations that optimize performance for different output voltages.

## Pulse-Skipping Mode Operation

Pulse-skipping mode enables the module to skip cycles at light loads which reduces switching losses and increases efficiency at low to intermediate currents. To enable this mode, connect the  $MODE\_PLLIN$  pin to the  $INTVCC$  pin.

## Forced Continuous Operation

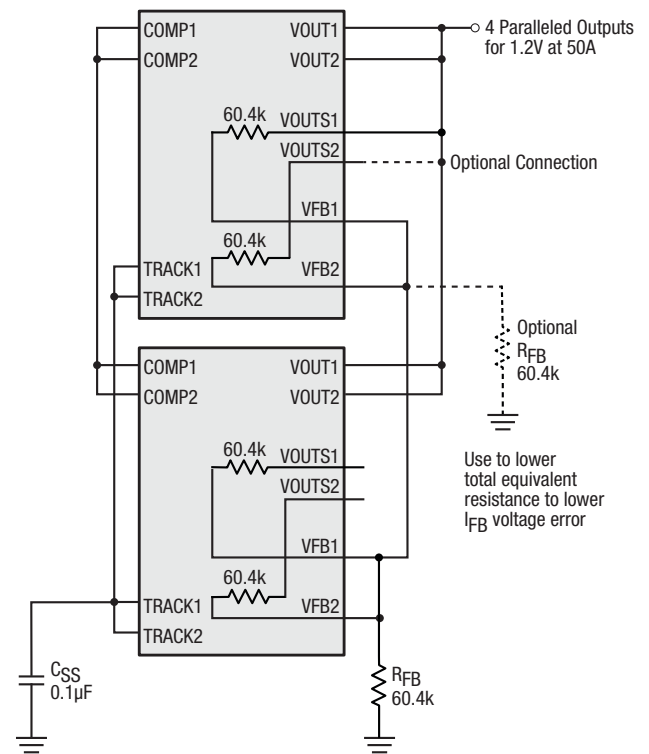
Forced continuous operation is recommended when fixed frequency is more important than light load efficiency, and when the lowest output ripple is desired. To enable this mode, connect the  $MODE\_PLLIN$  pin to GND.

## Multiphase Operation

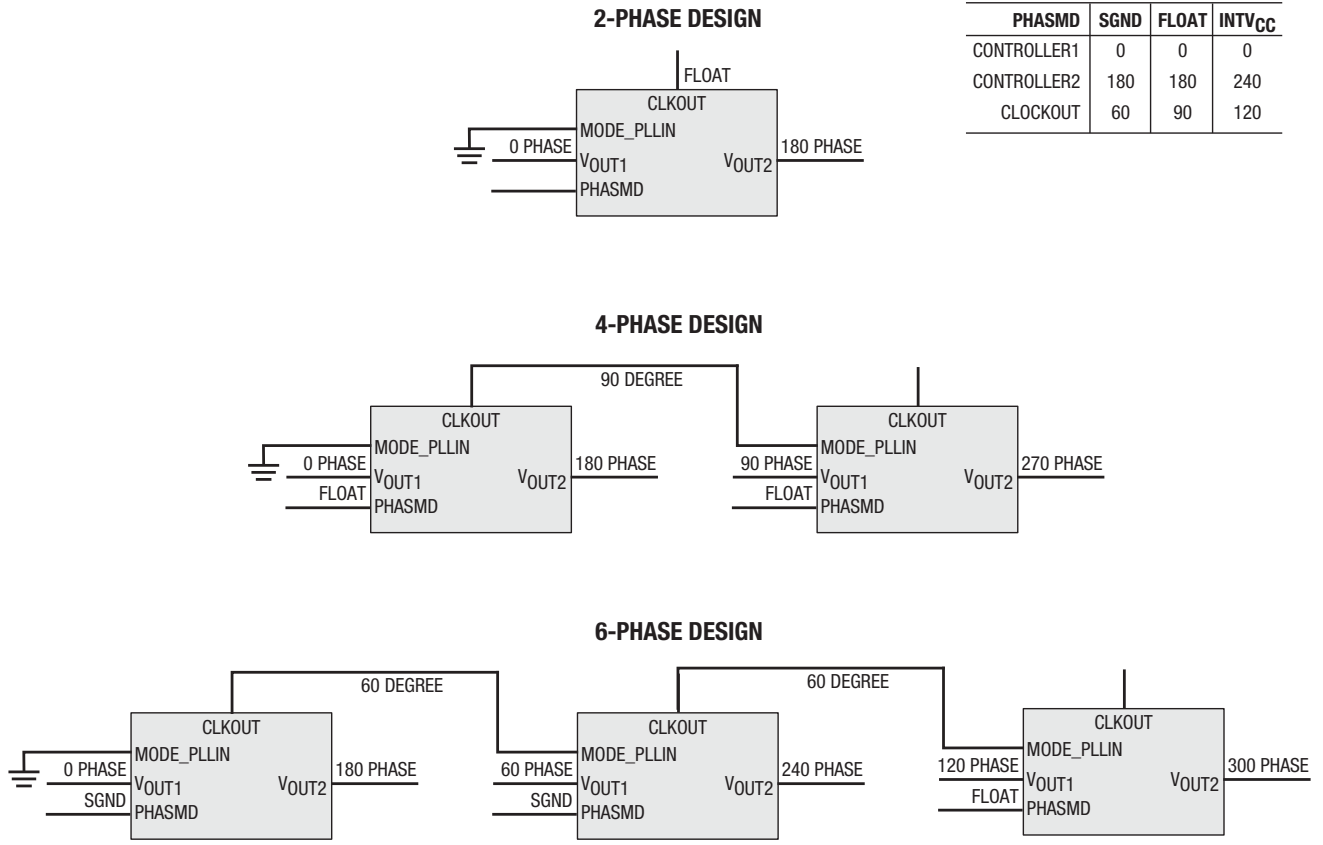
Multiphase operation is used to achieve output currents greater than 13A. It can be used with both MxL7213 channels to achieve one 26A output. It can also be used by paralleling multiple MxL7213s and running them out of phase to attain one single high current output, up to 100A. Ripple current in both the input and output capacitors is substantially lower using a multiphase design when the number of phases multiplied by the output voltage is less than the input voltage. Input RMS ripple current and output ripple amplitude is reduced by the number of phases used while the effective ripple frequency is multiplied by the number of phases used. The MxL7213 is a peak current mode controlled device which results in very good current sharing between parallel modules and balances the thermal loading.

Up to 8 phases can be paralleled by using each MxL7213 channel's  $PHASMD$ ,  $MODE\_PLLIN$  and  $CLKOUT$  pins. When the  $CLKOUT$  pin is connected to the following stage's  $MODE\_PLLIN$  pin, the frequency and the phase of both devices are locked. Phase difference can be obtained between  $MODE\_PLLIN$  and  $CLKOUT$  of 120 degrees, 60 degrees or 90 degrees respectively by connecting the  $PHASMD$  pin to  $INTVCC$ ,  $SGND$  or left floating. [Figure 21](#)

shows an example of parallel operation and [Figure 22](#) shows examples of 2-phase, 4-phase and 6-phase designs.



**Figure 21: 4-Phase Parallel Configuration**

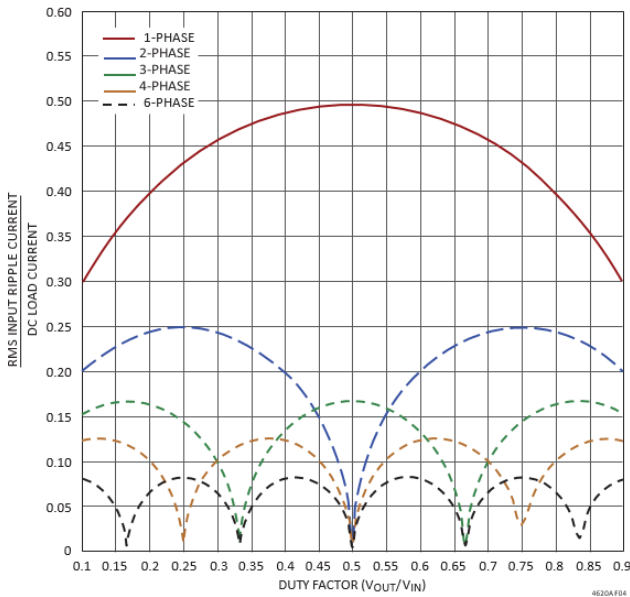


**Figure 22: Examples of 2-Phase, 4-Phase and 6-Phase Operation with PHASMD Table**



## Input RMS Ripple Current Cancellation

Figure 23 illustrates the RMS ripple current reduction that is expected as a function of the number of interleaved phases.



**Figure 23:** Normalized Input RMS Ripple Current vs. Duty Cycle, One to Six Phases

## Frequency Selection and Phase-Lock Loop

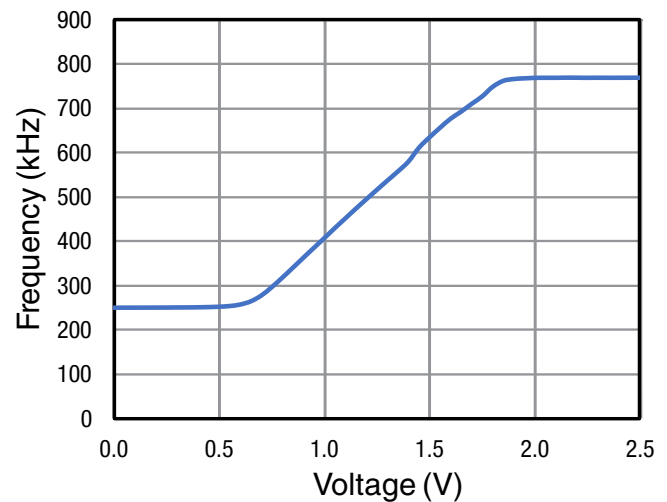
To increase efficiency, the MxL7213 works over a range of frequencies. For lower output voltages or duty cycles, lower frequencies are recommended to lower MOSFET switching losses and improve efficiency. For higher output voltages or duty cycles, higher frequencies are recommended to limit inductor ripple current. Refer to the efficiency graphs and their operating frequency conditions. When selecting an operating frequency, keep the highest output voltage in mind.

Use an external resistor between the FSET pin and SGND to set the switching frequency. An accurate 10 $\mu$ A current source into the resistor sets a voltage that programs the frequency. Alternately, a DC voltage can be applied to FSET to program the frequency. Figure 24 illustrates the operating frequency versus FSET pin voltage.

An external clock with a frequency range of 250kHz to 780kHz and a voltage range of 0V to INTV<sub>CC</sub> can be connected to the MODE\_PLLIN pin. The high level threshold of the clock input is 1.6V and the low level threshold of the clock input is 1V.

The MxL7213 integrates the PLL loop filter components. Ensure that the initial switching frequency is set with an external resistor before locking to an external clock. Both regulators will operate in continuous mode while being synchronized to an external clock signal.

The PLL phase detector output charges and discharges the internal filter network with a pair of complementary current sources. When an external clock is connected, an internal switch disconnects the external FSET frequency resistor. The switching frequency then locks to the incoming external clock. If no external clock is connected, then the internal switch is on, which connects the external FSET frequency set resistor.



**Figure 24:** Operating Frequency vs. FSET Pin Voltage

## Minimum On-Time

Minimum On-Time  $t_{ON(MIN)}$  is the shortest time the controller can turn on the high-side MOSFET of either channel. Approaching this time may be more of an issue in low duty cycle applications. Use the following equation to make sure the on-time is above this minimum:

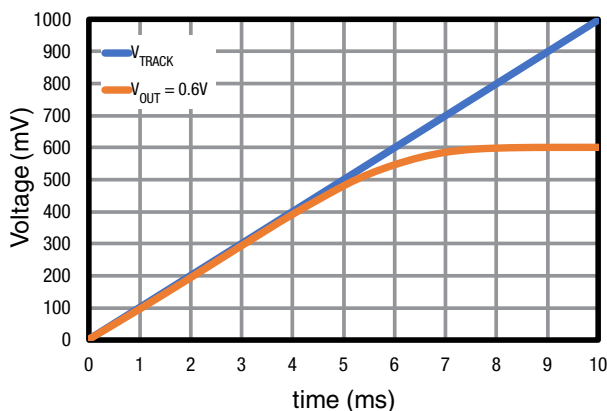
$$\frac{V_{OUT}}{V_{IN} \times FREQ} > t_{ON(MIN)}$$

If the on-time falls below this minimum, the channel will start to skip cycles. In this case, the output voltage continues to regulate, however output ripple increases. Lowering the switching frequency increases on-time. Minimum on-time specified in the electrical characteristics is 90ns.

## Soft Start and Output Voltage Tracking

A capacitor  $C_{SS}$  can be connected from the TRACK pin to ground to implement soft start. The TRACK pin is charged by a  $1.25\mu\text{A}$  current source up to the reference voltage and then on to  $INTV_{CC}$ . The MxL7213 has a smooth transition from TRACK to  $V_{OUT}$  as shown in [Figure 25](#). If the RUN pin is below 1.2V, the TRACK pin is pulled low. The following equation can be used to calculate soft-start time, defined as when PGOOD asserts:

$$t_{SOFTSTART} = \left( \frac{C_{SS}}{1.25\mu\text{A}} \right) \times 0.65V$$

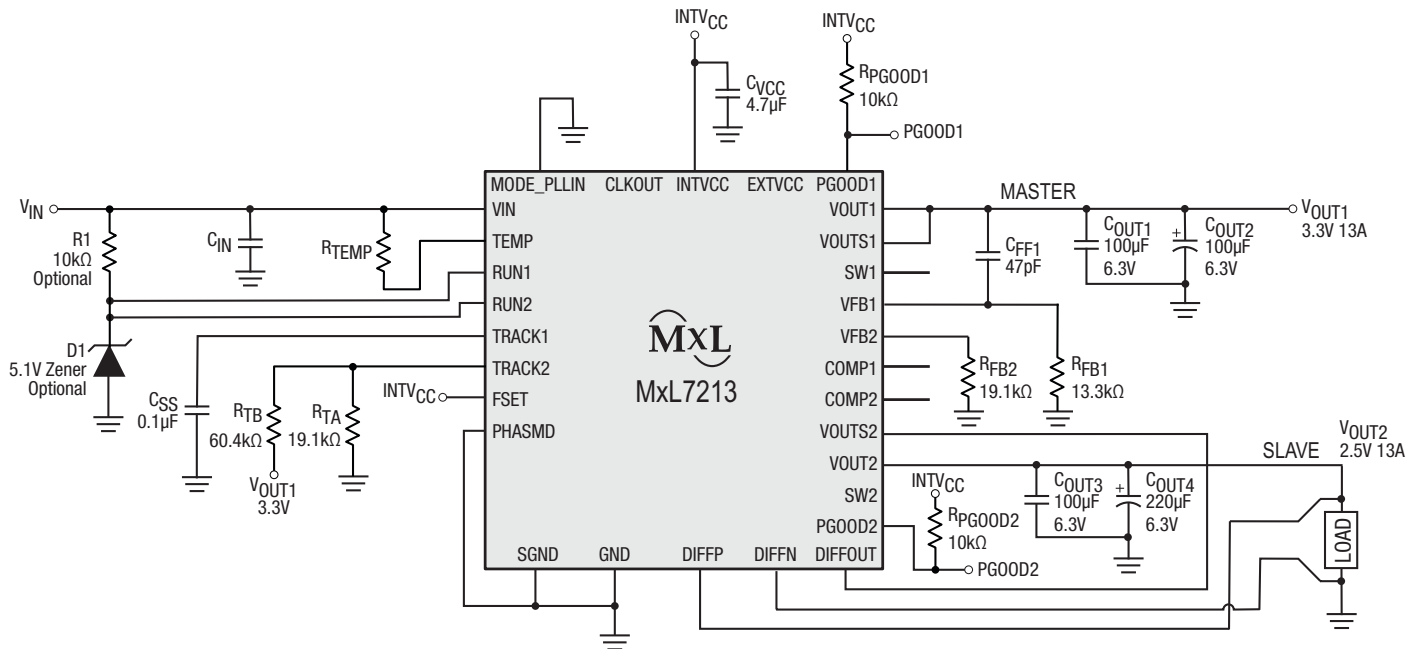


**Figure 25:**  $V_{OUT}$  and  $V_{TRACK}$  versus Time

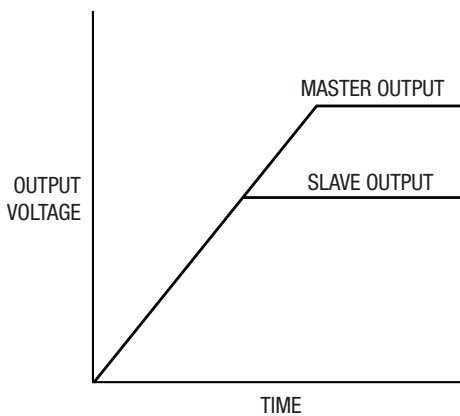
The MODE\_PLLIN pin selects between forced continuous mode or pulse-skipping mode during steady-state operation. Regardless of the mode selected, the module channels will always start in pulse-skipping mode up to  $TRACK = 0.5V$ . Between  $TRACK = 0.5V$  and  $0.54V$ , it will operate in forced continuous mode. Once  $TRACK > 0.54V$ , it will follow the selected mode.

The TRACK pins can be used to externally program the output voltage tracking. The output may be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider to implement coincident tracking. Note that each MxL7213 channel has an internal accurate  $60.4k\Omega$  for the top feedback resistor. Refer to the equation below, which is applicable for  $V_{TRACK(SLAVE)} < 0.8V$ . An example of coincident tracking is shown in [Figure 26](#).

$$V_{OUT(SLAVE)} = \left( 1 + \frac{60.4k}{R_{TA}} \right) \times V_{TRACK(SLAVE)}$$



**Figure 26: Example of Output Tracking Application Circuit**



**Figure 27: Output Coincident Tracking Waveform**

The ramping voltage is applied to the track pin of the slave. Since the same resistor values are used to divide down the output of the master and to set the output of the slave, the slave tracks with the master coincidentally until its final value it achieved. The master continues from the slave's regulation point to its final value. In [Figure 26](#),  $R_{TA}$  is equal to  $R_{FB2}$  for coincident tracking.

Ratiometric power up can be implemented by tying the TRACK pins together and connecting a capacitor from TRACK to ground. For existing designs where this is not

possible, populate  $R_{TA}$  with the same capacitor as the master's TRACK capacitor and do not populate  $R_{TB}$ . Capacitors with 10% accuracy are recommended.

## Power Good

Each channel's open drain PGOOD pin can be used to monitor if its respective  $V_{OUT}$  is outside  $\pm 10\%$  of the set point. The PGOOD pin is pulled low when the output of either channel is outside the monitoring window, the RUN pin is below its threshold (1.25V), or the MxL7213 is in the soft start or tracking phase. The PGOOD pin will flag power good immediately when both VFB pins are within the monitoring window. Note that there is an internal 20 $\mu$ s delay when VFB voltage goes out of the monitoring window.

If desired, a pull up resistor can be connected from the PGOOD pins to a supply voltage with a maximum level of  $\leq 6$ V.

## Stability and Compensation

The MxL7213 is internally compensated across the range of all input and output voltages so additional compensation is not typically required. [Table 11](#) covers most application requirements.

For low output capacitance or low output voltage applications, sometimes a reasonable loop bandwidth and improved phase margin can be obtained by adding a series R-C circuit between the COMP pin and SGND.

## Additional Compensation Information

When the loop gain crosses 0dB at a slope steeper than -20dB / decade, the phase margin sometimes can be inadequate. This is when a small  $C_{FF}$  capacitor may offer some help. This  $C_{FF}$  capacitor is connected between the VOUTS and FB pins and is in parallel with the 60.4k $\Omega$  internal upper feedback resistor. The  $C_{FF}$ , together with the upper and lower feedback resistors, form a lead compensation network that inserts a "Zero" in the loop at a frequency followed by a "Pole" at a higher frequency. This gives the loop a phase boost mainly between the Zero and Pole frequencies.

$C_{FF}$ , in conjunction with the upper 60.4k feedback resistor located inside the module, creates a feedback "Zero" ( $F_z$ ).

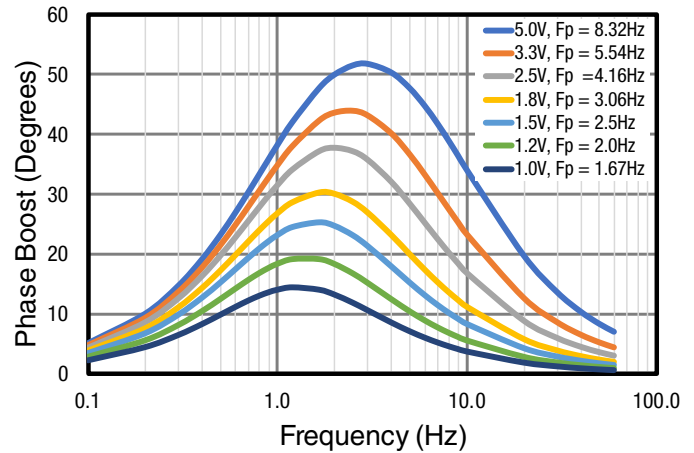
$$F_z = \frac{1}{2 \times \pi \times 60400 \times C_{FF}}$$

This added zero makes it easier for high frequency signals to pass from the output back to the FB pin which helps boost the loop's phase margin.

The "Pole" in the lead compensation network can be calculated as:

$$F_p = \frac{60400 + R_{FB}}{2\pi \times 60400 \times R_{FB} \times C_{FF}}$$

For maximum effect,  $C_{FF}$  should be selected to place the peak of the phase boost right at the crossover frequency. [Figure 28](#) shows the available phase boost normalized to the  $F_z$  frequency of 1.



**Figure 28:  $C_{FF}$  Phase Boost vs. Frequency  $F_z$  Normalized to 1**

As a starting point, calculate  $C_{FF}$  from the following equation, where  $F_{CO}$  is the crossover frequency.

$$C_{FF} = \frac{1}{2 \times \pi \times 60400 \times F_{CO}}$$

Since the addition of a  $C_{FF}$  also brings about a gain boost, the final crossover frequency will increase somewhat. So it may take several iterations to achieve the highest phase margin.

## Enabling the Channels

The RUN1 and RUN2 pins enable and disable the module's two channels. If either channel is activated using a run pin, then INTVCC is activated. The typical enable threshold of the RUN pins is 1.25V, with a hysteresis of 150mV and a maximum of 1.4V. For 5V operation, they can be pulled up to  $V_{IN}$ . For higher than 5V operation, a 10k $\Omega$  to 100k $\Omega$  resistor and 5V Zener diode can be used to enable the channels.

Alternately, the RUN pins can be left floating and the channels will turn on upon application of  $V_{IN}$ . For output voltage sequencing applications, the RUN pins can be connected to another channel's or device's PGOOD pins.

When using paralleled mode, connect the RUN pins together and use a single control. See [Figure 20](#).

## INTV<sub>CC</sub> and EXTV<sub>CC</sub>

The VIN input voltage powers an internal 5V low dropout regulator. The regulator output (INTVCC) provides voltage to the control circuitry of the module. Alternatively, the EXTVCC pin allows an external 5V supply to be used to eliminate the 5V LDO power dissipation in power sensitive applications.

## Differential Remote Sense Amplifier

For output voltages ≤3.3V, the MxL7213’s differential remote sense amplifier can be used to accurately sense voltages at the load. This is particularly useful in high current load conditions. The DIFFP and DIFFN pins must be connected properly to the remote load point, and the DIFFOUT pin must be connected to the corresponding VOUTS1 or VOUTS2 pin.

## SW Pins

Use the SW pins to monitor the switching node of each channel. These pins are generally used for testing or monitoring. During normal operation, these pins should be unconnected and left floating. However, in conjunction with an external series R-C snubber circuit, these pins can be used to dampen ringing on the switch node which may be caused by LC parasitics in the switched current paths.

## Temperature Monitoring (TEMP)

An internal temperature sensing diode / PNP transistor is used to monitor its V<sub>BE</sub> voltage over temperature, thus serving as a temperature monitor. Its forward voltage and temperature coefficient are shown in the electrical characteristics section and plotted in Figure 29. It is connected to VIN through a pullup resistor R<sub>TEMP</sub> to limit the current to 100µA. It is recommended to set a 60µA minimum current in applications where V<sub>IN</sub> varies over a wide range. See Figure 30 for an example on how to use this feature.

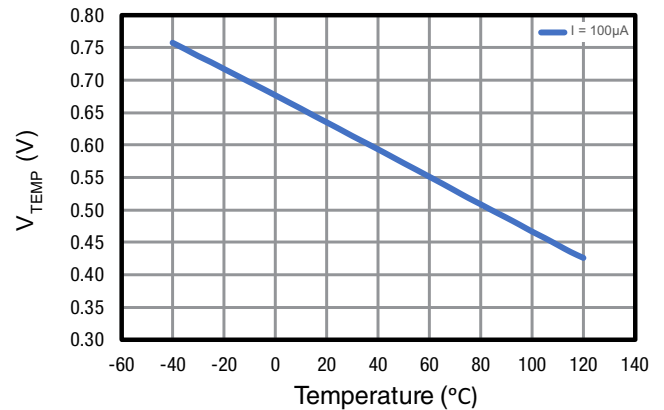


Figure 29: Diode Voltage vs. Temperature

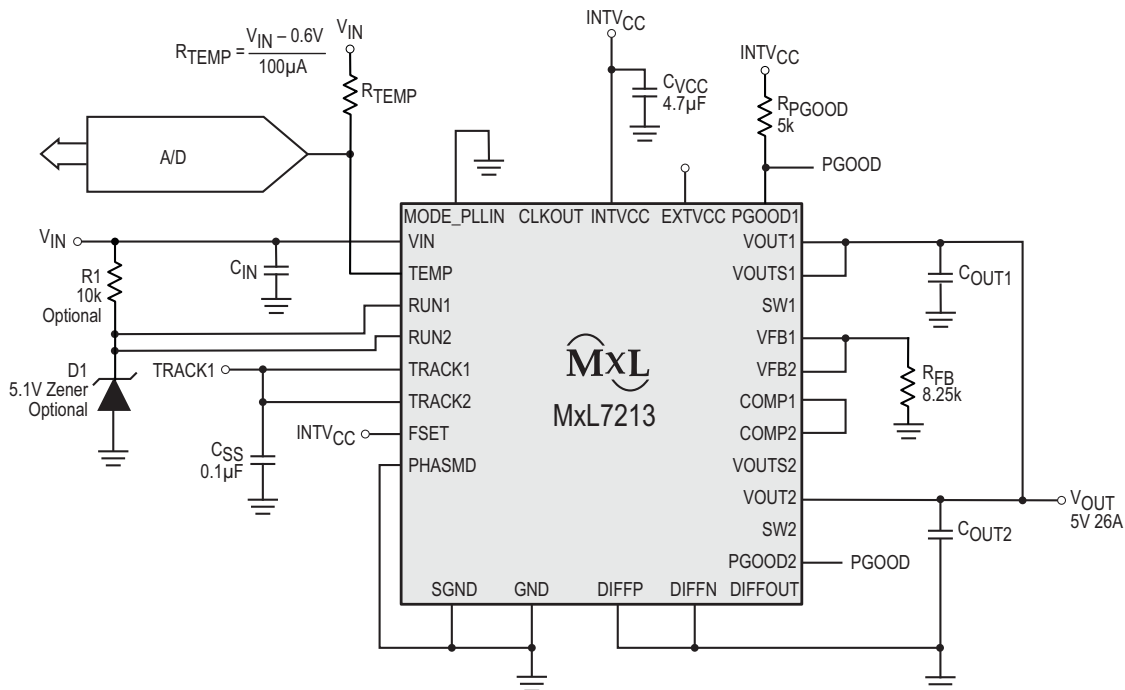


Figure 30: 2-Phase, 5V at 26A with Temperature Monitoring

## Fault Protection

The MxL7213 modules support overcurrent, output overvoltage, and overtemperature protection.

The overcurrent triggers at a nominal load of 20A. Overcurrent during four consecutive switching cycles initiates a hiccup mode. During hiccup, the high-side and low-side MOSFETs are turned off for 100ms. A soft start is attempted following the hiccup. If the overcurrent persists, the hiccup will continue.

The overvoltage triggers when the output voltage is 10% above set-point and the high-side MOSFET is kept off while the low-side MOSFET turns on, clamping the output voltage.

The overtemperature triggers at 145°C and turns off the two MOSFETs. When the temperature cools down below 130°C, the module soft-starts.

A fuse or circuit breaker should be selected to limit the current to the regulator during overvoltage in case of an internal top MOSFET fault. If the internal top MOSFET fails, then turning it off will not resolve the overvoltage, thus the internal bottom MOSFET will turn on indefinitely trying to protect the load. Under this fault condition, the input voltage will source very large currents to ground through the failed internal top MOSFET and enabled internal bottom MOSFET. This can cause excessive heat and board damage depending on how much power the input voltage can deliver to this system. A fuse or circuit breaker can be used as a secondary fault protector in this situation.

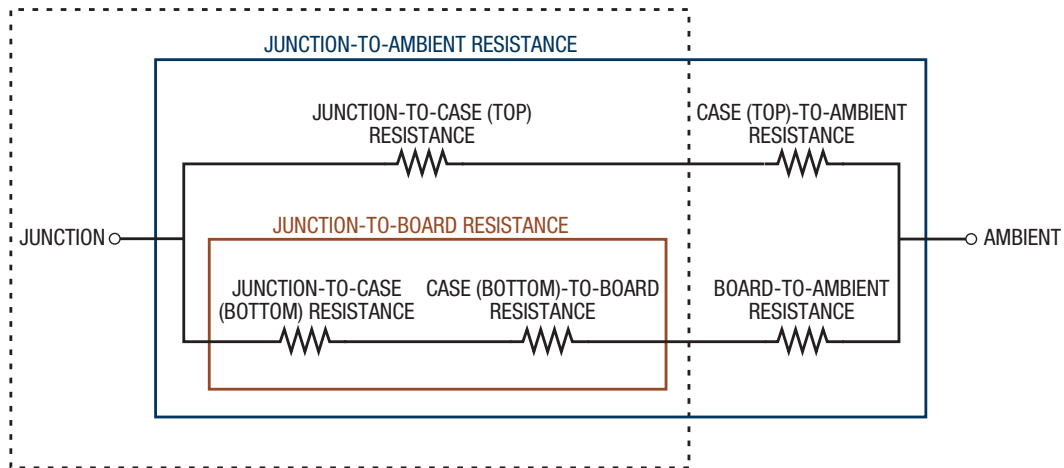
## Thermal Considerations and Output Current Derating

The design of the MxL7213 module removes heat from the bottom side of the package effectively. Thermal resistance from the bottom substrate material to the printed circuit board is very low.

Proper thermal design is critical in controlling device temperatures and in achieving robust designs. There are many factors that affect the thermal performance. One key factor is the temperature rise of the devices in the package, which is a function of the thermal resistances of the devices inside the package and the power being dissipated. The thermal resistances of the MxL7213 are shown in the “Operating Ratings” section of this datasheet. The JEDEC  $\Theta_{JA}$  thermal resistance provided is based on tests that comply with the JESD51-2A “Integrated Circuit Thermal Test Method Environmental Conditions – Natural Convection” standard. JESD51 is a group of standards whose intent is to provide comparative data based on a standard test condition which includes a defined board construction. Since the actual board design in the final application will be different from the board defined in the standard, the thermal resistances in the final design may be different from those shown.

Figure 33, Figure 34, Figure 36, Figure 37 and Figure 39 show output current derating versus ambient temperature for various  $V_{IN}$  and  $V_{OUT}$  ( $V_{IN} / V_{OUT}$ ) ratios with 0, 200, and 400 LFM of airflow. The total package power dissipation ( $P_{PKG}$ ) is dependent on the final application and is the sum of the losses for the two channels. The power losses for a channel will depend mainly on the input voltage, output voltage, and output current. Figure 32, Figure 35 and Figure 38 show the power losses for input voltages of 5V and 12V and for  $V_{OUT}$  voltages of 1V, 2.5V, and 5.0V respectively ( $V_{IN} / V_{OUT}$ ).

## Power Derating



**Figure 31:** Graphical Representation of Thermal Coefficients

**Table 7:**  $\theta_{JA}$  and Derating Curves Corresponding to 1.0V Output

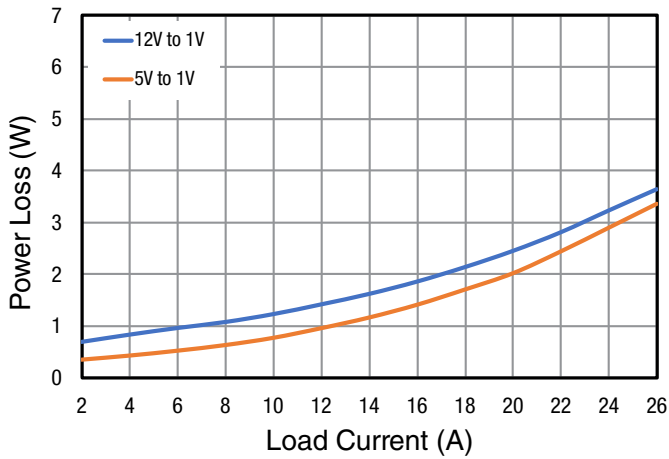
| Derating Curve       | $V_{IN}$ (V) | Power Loss Curve | Airflow (LFM) | LGA $\theta_{JA}$ ( $^{\circ}\text{C}/\text{W}$ ) | BGA $\theta_{JA}$ ( $^{\circ}\text{C}/\text{W}$ ) |
|----------------------|--------------|------------------|---------------|---|---|
| Figure 33, Figure 34 | 5, 12        | Figure 32        | 0             | 7   | 7   |
| Figure 33, Figure 34 | 5, 12        | Figure 32        | 200           | 5.5   | 5.5   |
| Figure 33, Figure 34 | 5, 12        | Figure 32        | 400           | 5   | 5   |

**Table 8:**  $\theta_{JA}$  and Derating Curves Corresponding to 2.5V Output

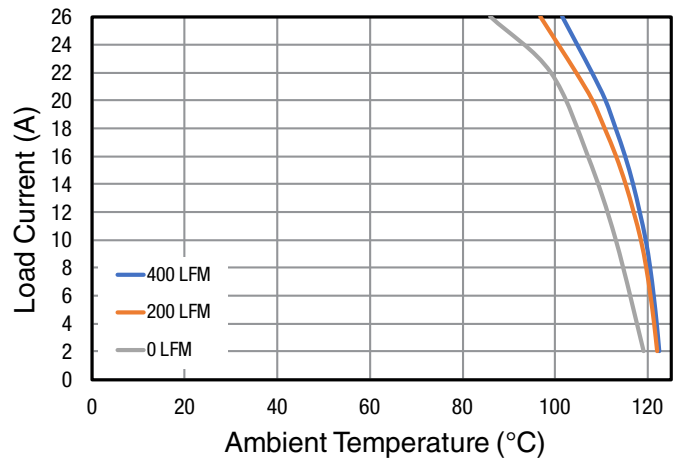
| Derating Curve       | $V_{IN}$ (V) | Power Loss Curve | Airflow (LFM) | LGA $\theta_{JA}$ ( $^{\circ}\text{C}/\text{W}$ ) | BGA $\theta_{JA}$ ( $^{\circ}\text{C}/\text{W}$ ) |
|----------------------|--------------|------------------|---------------|---|---|
| Figure 36, Figure 37 | 5, 12        | Figure 35        | 0             | 7   | 7   |
| Figure 36, Figure 37 | 5, 12        | Figure 35        | 200           | 6   | 6   |
| Figure 36, Figure 37 | 5, 12        | Figure 35        | 400           | 4.5   | 4.5   |

**Table 9:**  $\theta_{JA}$  and Derating Curves Corresponding to 5V Output

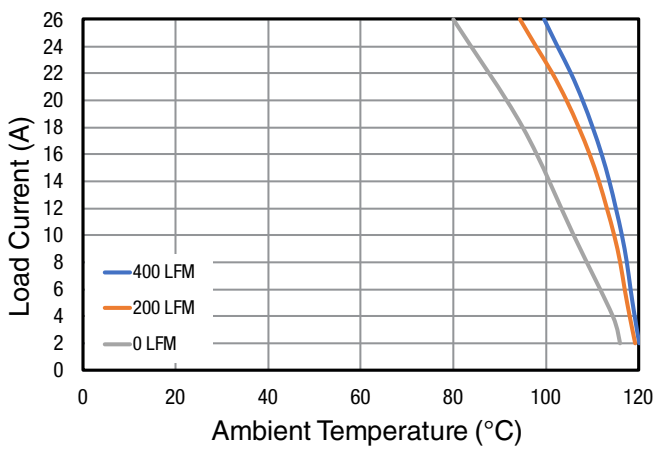
| Derating Curve | $V_{IN}$ (V) | Power Loss Curve | Airflow (LFM) | LGA $\theta_{JA}$ ( $^{\circ}\text{C}/\text{W}$ ) | BGA $\theta_{JA}$ ( $^{\circ}\text{C}/\text{W}$ ) |
|----------------|--------------|------------------|---------------|---|---|
| Figure 39      | 12           | Figure 38        | 0             | 7   | 7   |
| Figure 39      | 12           | Figure 38        | 200           | 6   | 6   |
| Figure 39      | 12           | Figure 38        | 400           | 4.5   | 4.5   |



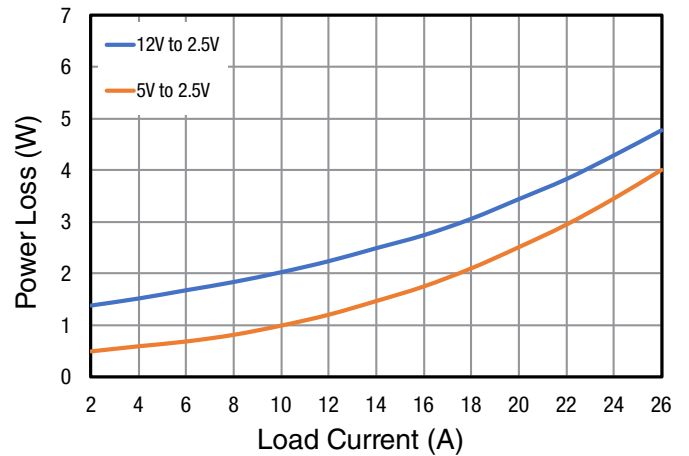
**Figure 32: Power Loss,  $V_{OUT} = 1.0V$**



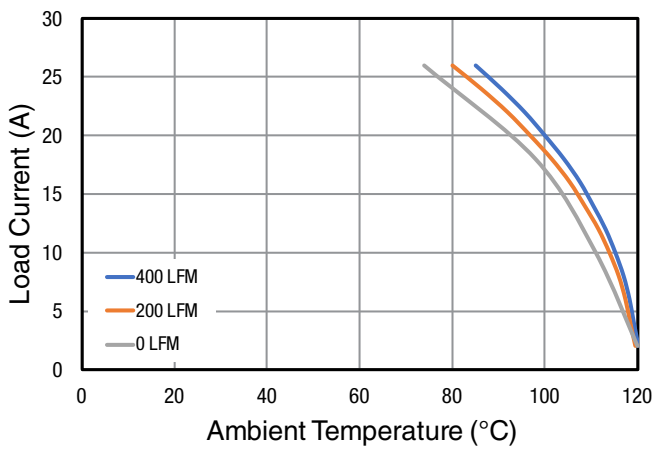
**Figure 33: Current Derating,  $V_{IN} = 5V, V_{OUT} = 1.0V$**



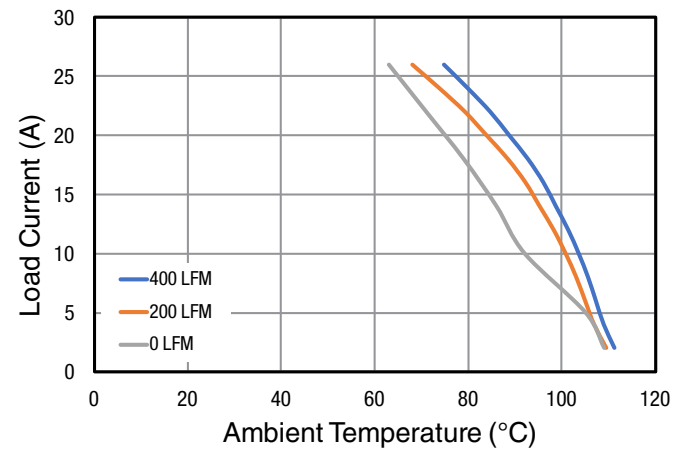
**Figure 34: Current Derating,  $V_{IN} = 12V, V_{OUT} = 1.0V$**



**Figure 35: Power Loss,  $V_{OUT} = 2.5V$**

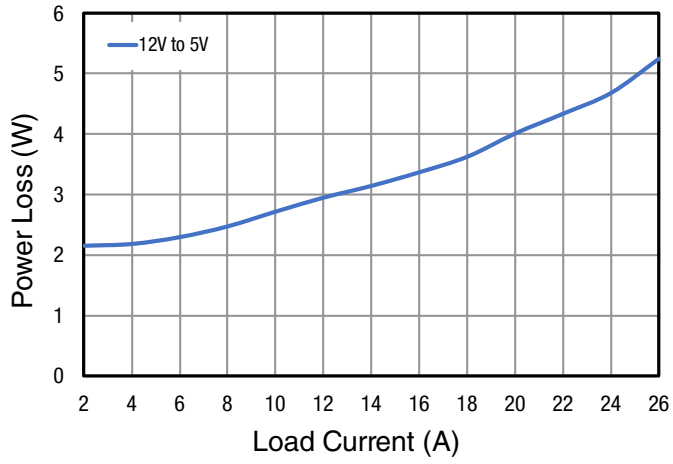


**Figure 36: Current Derating,  $V_{IN} = 5V, V_{OUT} = 2.5V$**

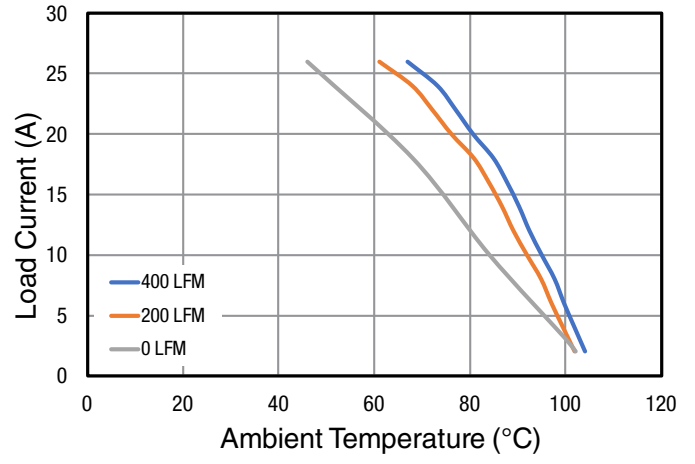


**Figure 37: Current Derating,  $V_{IN} = 12V, V_{OUT} = 2.5V$**





**Figure 38: Power Loss,  $V_{OUT} = 5V$**



**Figure 39: Current Derating,  $V_{IN} = 12V$ ,  $V_{OUT} = 5V$**

**Table 10: Capacitors Used for Output Voltage Response Matrix**

| Vendor                                 | Value       | Part Number        | ESR (mΩ) |
|--|-------------|--------------------|----------|
| Murata, C <sub>OUT1</sub> Ceramic      | 100μF, 6.3V | GRM32ER60J107ME20L | ~2       |
| Taiyo Yuden, C <sub>OUT1</sub> Ceramic | 100μF, 6.3V | JMK325BJ107MY      | ~2       |
| Panasonic POSCAP, C <sub>OUT2</sub>    | 470μF, 6.3V | 6TPF470MAH         | 10       |
| Panasonic POSCAP, C <sub>OUT2</sub>    | 220μF, 6.3V | 6TPF220ML          | 12       |
| Panasonic POSCAP, C <sub>OUT2</sub>    | 220μF, 2.5V | 2R5TPE220M9        | 9        |
| Panasonic POSCAP, C <sub>OUT2</sub>    | 100μF, 6.3V | 6TPE100MI          | 18       |
| Nichicon, C <sub>IN</sub> Bulk         | 150μF, 25V  | UCD1E151MNL1GS     |          |

**Table 11: Output Voltage Response vs. Component Matrix**

| V <sub>OUT</sub> (V) | C <sub>IN</sub> (CERAMIC) (μF) | C <sub>IN</sub> <sup>(1)</sup> (BULK) (μF) | C <sub>OUT1</sub> (CERAMIC) (μF) | C <sub>OUT2</sub> (BULK) (μF) | C <sub>FF</sub> (pF) | V <sub>IN</sub> (V) | DROOP (mV) | P-P DEVIATION at 6A LOAD STEP (mV) | Recovery Time (μs) | LOAD STEP (A/μs) | R <sub>FB</sub> (kΩ) | FREQ (kHz) |
|----------------------|--------------------------------|--|----------------------------------|-------------------------------|----------------------|---------------------|------------|------------------------------------|--------------------|------------------|----------------------|------------|
| 1                    | 3 x 22                         | 150  | 100                              | 2 x 470                       | 180                  | 5                   | 27         | 54                                 | 15                 | 6                | 90.9                 | 400        |
| 1                    | 3 x 22                         | 150  | 100                              | 2 x 470                       | 180                  | 12                  | 26         | 56                                 | 15                 | 6                | 90.9                 | 400        |
| 1                    | 3 x 22                         | 150  | 3 x 100                          | 470                           | 180                  | 12                  | 40         | 81                                 | 17                 | 6                | 90.9                 | 400        |
| 1.2                  | 3 x 22                         | 150  | 3 x 100                          | 470                           | 180                  | 12                  | 39         | 79                                 | 15                 | 6                | 60.4                 | 500        |
| 1.2                  | 3 x 22                         | 150  | 100                              | 2 x 470                       | 180                  | 5                   | 28         | 57                                 | 16                 | 6                | 60.4                 | 500        |
| 1.2                  | 3 x 22                         | 150  | 100                              | 2 x 470                       | 180                  | 12                  | 28         | 56                                 | 16                 | 6                | 60.4                 | 500        |
| 1.5                  | 3 x 22                         | 150  | 100                              | 2 x 470                       | 180                  | 5                   | 26         | 53                                 | 21                 | 6                | 40.2                 | 550        |
| 1.5                  | 3 x 22                         | 150  | 100                              | 2 x 470                       | 180                  | 12                  | 25         | 52                                 | 21                 | 6                | 40.2                 | 550        |
| 1.5                  | 3 x 22                         | 150  | 100                              | 220                           | 100                  | 12                  | 51         | 104                                | 22                 | 6                | 40.2                 | 550        |
| 1.8                  | 3 x 22                         | 150  | 100                              | 220                           | 47                   | 12                  | 51         | 106                                | 14                 | 6                | 30.2                 | 600        |
| 1.8                  | 3 x 22                         | 150  | 100                              | 220                           | 47                   | 5                   | 54         | 110                                | 14                 | 6                | 30.2                 | 600        |
| 2.5                  | 3 x 22                         | 150  | 100                              | 220                           |                      | 12                  | 47         | 100                                | 20                 | 6                | 19.1                 | 650        |
| 2.5                  | 3 x 22                         | 150  | 3 x 100                          |                               | 62                   | 12                  | 73         | 155                                | 25                 | 6                | 19.1                 | 650        |
| 3.3                  | 3 x 22                         | 150  | 100                              | 100                           | 47                   | 12                  | 65         | 134                                | 20                 | 6                | 13.3                 | 700        |
| 3.3                  | 3 x 22                         | 150  | 2 x 100                          |                               | 47                   | 12                  | 96         | 198                                | 25                 | 6                | 13.3                 | 700        |
| 5                    | 3 x 22                         | 150  | 100                              |                               | 22                   | 12                  | 172        | 356                                | 25                 | 6                | 8.25                 | 750        |
| 5                    | 3 x 22                         | 150  |                                  | 100                           |                      | 12                  | 126        | 260                                | 15                 | 6                | 8.25                 | 750        |

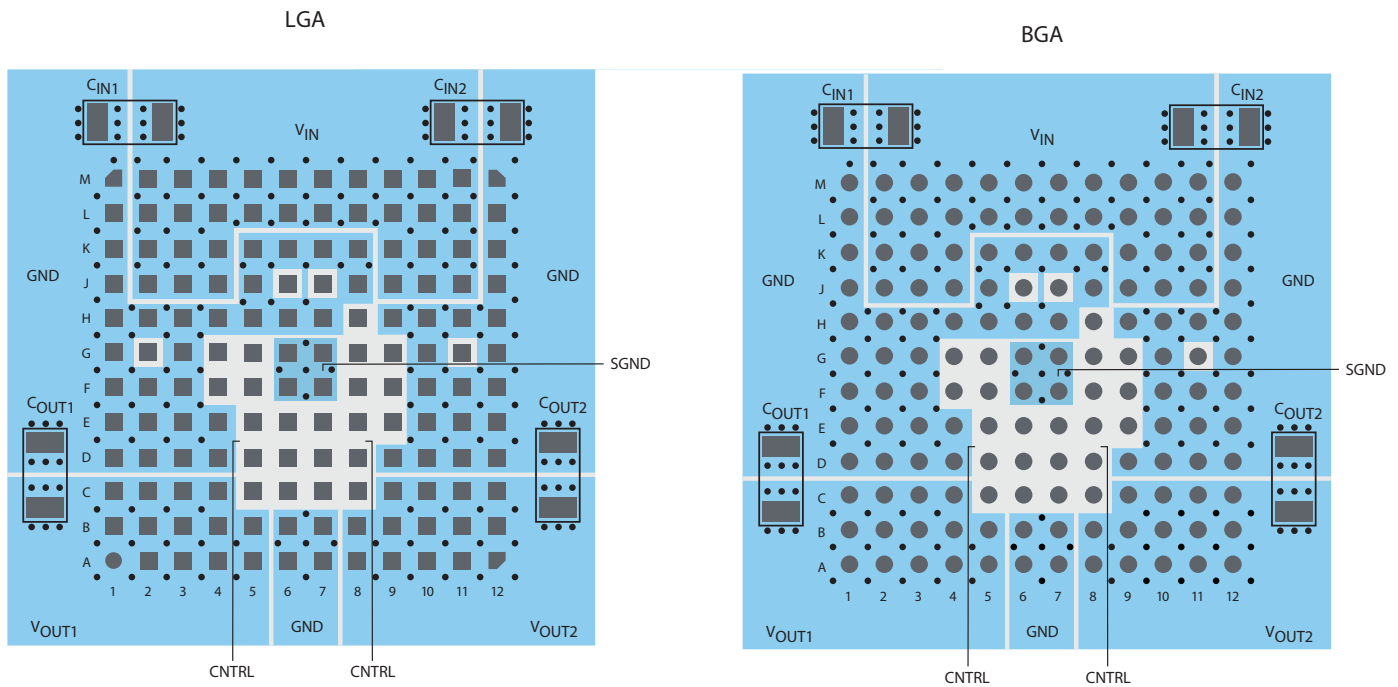
1. Bulk capacitance is optional if V<sub>IN</sub> has very low input impedance.

## Layout Guidelines and Example

The MxL7213's high level of integration simplifies PCB board design. However, some layout considerations are still recommended for optimal electrical and thermal performance.

- Use large PCB copper areas for high current paths, including VIN, VOUT1 and VOUT2 and GND to minimize conduction loss and thermal stress in the PCB.
- Use a dedicated power ground layer, placed under the MxL7213.
- Use multiple vias to interconnect the top layer and other power layers to minimize via conduction loss and module thermal stress.
- Cap or plate over any vias that are directly placed on the pad.
- Use a separated SGND ground copper area for components that are connected to the signal pins. The SGND to GND should be connected underneath the module.
- Place high frequency ceramic input and output capacitors next to the VIN, VOUT and PGND pins to minimize high frequency noise.
- When paralleling modules, connect the VFB, VOUT and COMP pins together closely with an internal layer. For soft-start mode, the TRACK pins may be tied together via a common capacitor.
- Test points can be brought out for monitoring the signal pins.

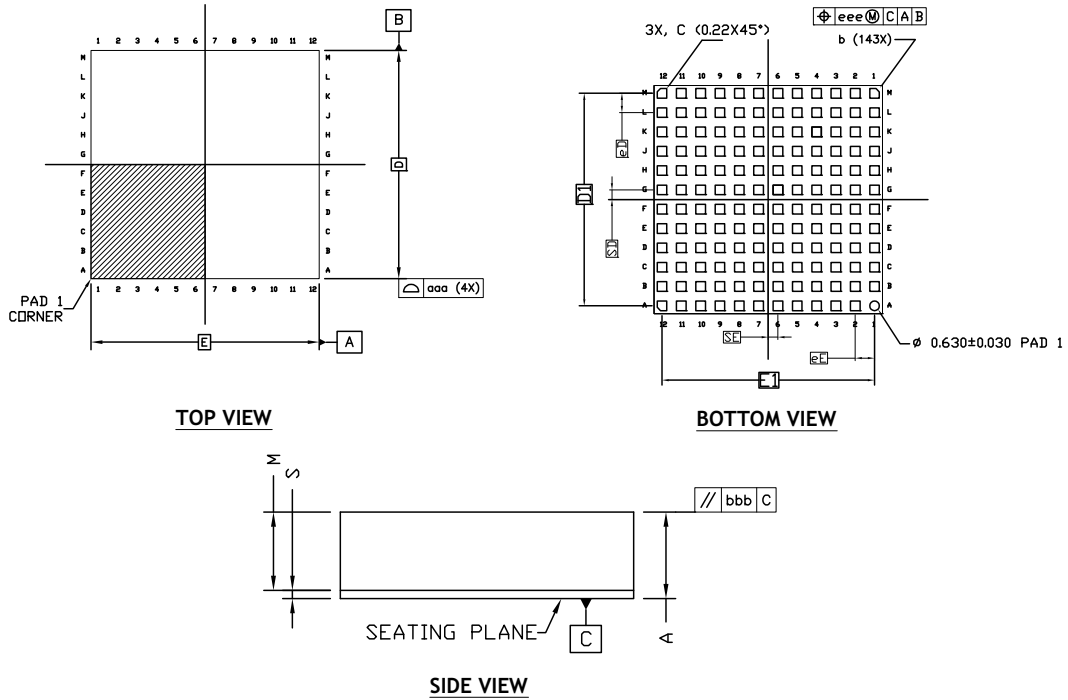
An example layout for the top PCB layer is recommended for both LGA and BGA packages in [Figure 40](#).



**Figure 40: Recommended PCB Layout**

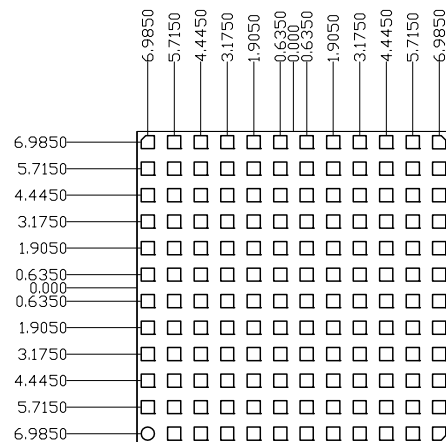
# Mechanical Dimensions

## 15mm x 15mm x 4.41mm LGA



|  | Symbol | Common Dimensions |
|--|--------|-------------------|
| Package :                                  |        | SIPLGA            |
| Body Size:                                 | X      | E 15.000          |
|  | Y      | D 15.000          |
| LGA Pad Pitch :                            | X      | eE 1.270          |
|  | Y      | eD 1.270          |
| Total Thickness :                          | A      | 4.410±0.10        |
| Mold Thickness :                           | M      | 4.000±0.05        |
| Substrate Thickness :                      | S      | 0.410±0.05        |
| LGA Pad Size :                             | b      | SO 0.630±0.030    |
| Stand Off :                                | A1     | N/A               |
| Ball Width :                               |        | N/A               |
| Package Edge Tolerance :                   | aaa    | 0.150             |
| Mold Flatness :                            | bbb    | 0.100             |
| Coplanarity:                               | ddd    | N/A               |
| LGA Pad Offset (Land) :                    | eee    | 0.050             |
| Ball Offset (Ball) :                       | fff    | N/A               |
| LGA Pad Count :                            | n      | 144               |
| Edge LGA Pad Center to Center :            | X      | E1 13.970         |
|  | Y      | D1 13.970         |
| Center Plg To Adjacent Center Of LGA Pad : | SE     | 0.635             |
|  | SD     | 0.635             |

**TERMINAL DETAILS**



**PAD LOCATION**

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

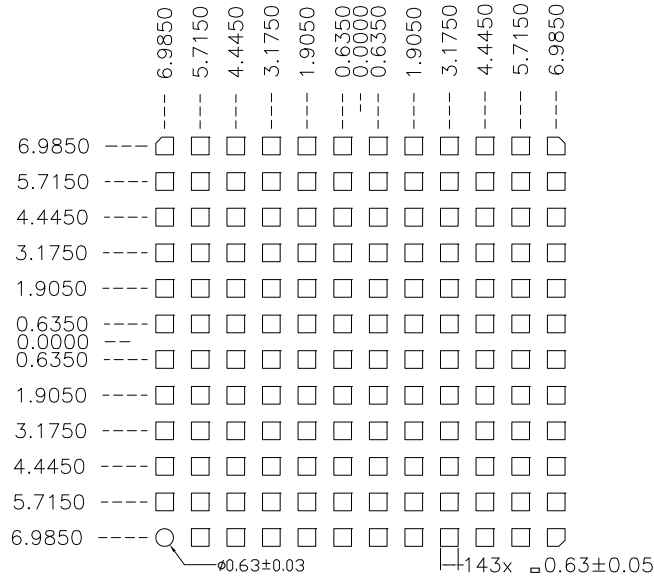
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Revision: B

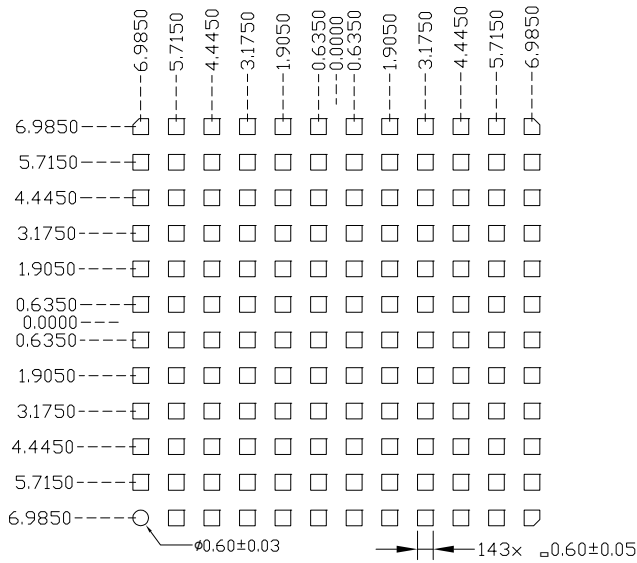
**Figure 41: Mechanical Dimensions, LGA**

# Recommended Land Pattern and Stencil

## 15mm x 15mm x 4.41mm LGA



**TYPICAL RECOMMENDED LAND PATTERN**



**TYPICAL RECOMMENDED STENCIL**

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

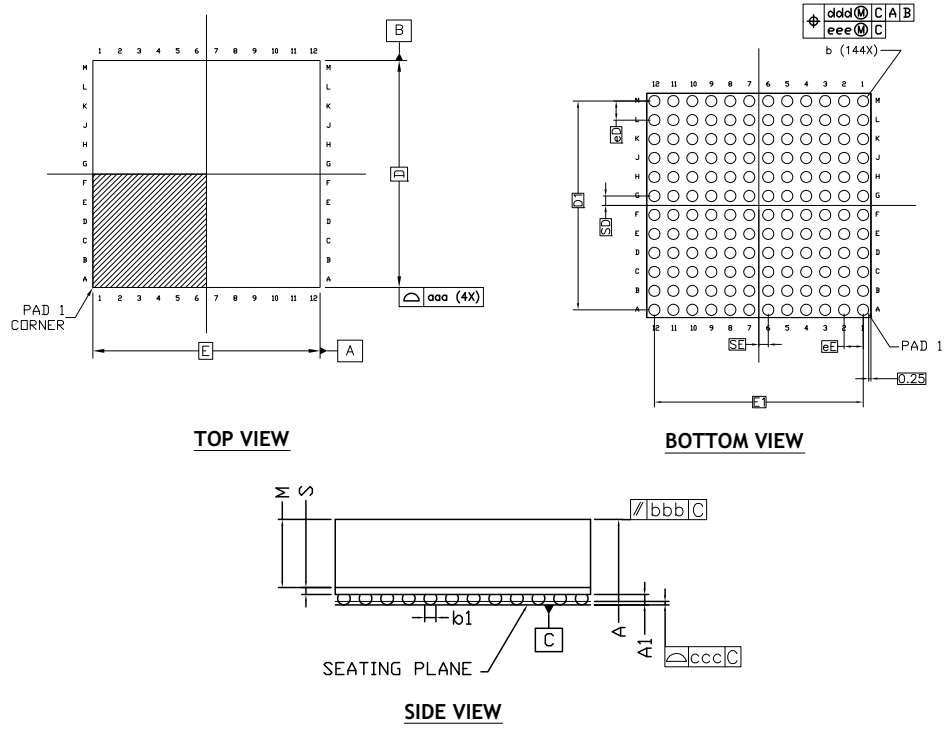
Drawing No.: POD-0000083

Revision: B

**Figure 42: Recommended Land Pattern and Stencil, LGA**

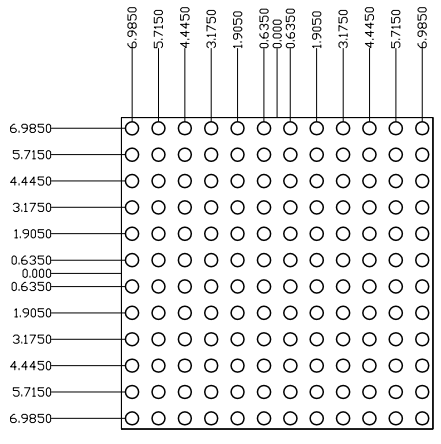
# Mechanical Dimensions

## 15mm x 15mm x 5.01mm BGA



|   | Symbol | Common Dimensions |
|---|--------|-------------------|
| Package :                                   |        | SIPBGA            |
| Body Size:                                  | X      | E 15.000          |
|   | Y      | D 15.000          |
| Ball Pitch :                                | X      | eE 1.270          |
|   | Y      | eD 1.270          |
| Total Thickness :                           | A      | 5.010±0.20        |
| Mold Thickness :                            | M      | 4.000±0.05        |
| Substrate Thickness :                       | S      | 0.410±0.05        |
| Ball Diameter (Before reflow) :             | b      | 0.750±0.150       |
| Stand Off :                                 | A1     | 0.500 ~ 0.700     |
| Ball Width (After reflow) :                 | b1     | 0.600 ~ 0.660     |
| Package Edge Tolerance :                    | aaa    | 0.150             |
| Mold Flatness :                             | bbb    | 0.100             |
| Coplanarity:                                | ccc    | 0.200             |
| Ball Offset (Package) :                     | ddd    | 0.300             |
| Ball Offset (Ball) :                        | eee    | 0.150             |
| Ball Count :                                | n      | 144               |
| Edge Ball Center to Center :                | X      | E1 13.970         |
|   | Y      | D1 13.970         |
| Center Pkg To Adjacent Center Of Ball Pod : | SE     | 0.635             |
|   | SD     | 0.635             |

**TERMINAL DETAILS**



**PAD LOCATION**

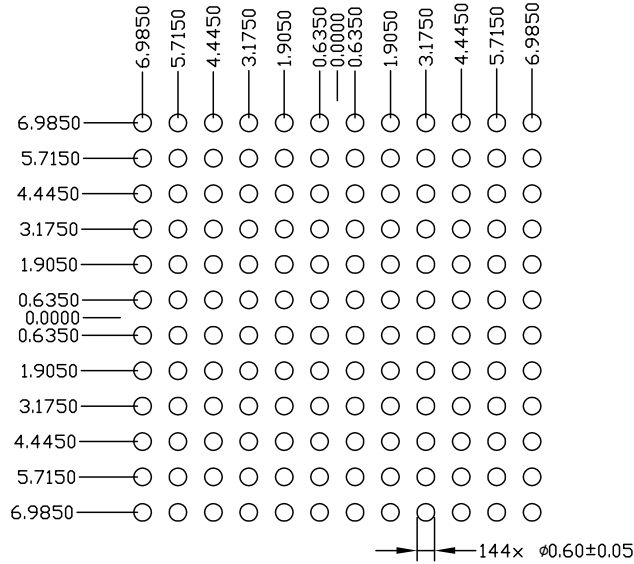
NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

Drawing No.: POD-00000084  
Revision: B

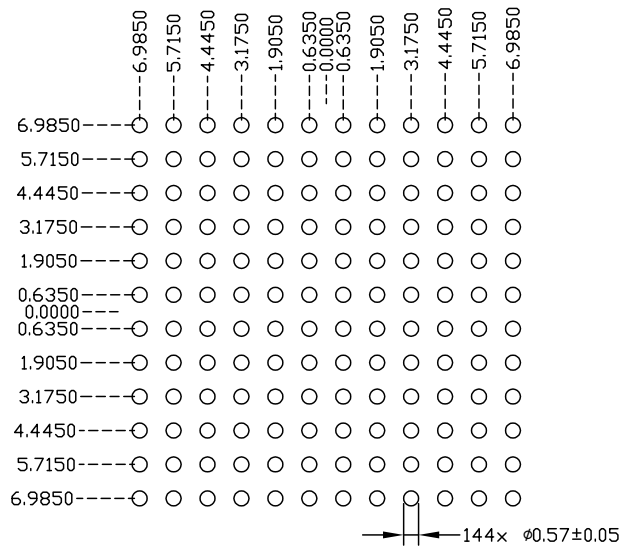
**Figure 43: Mechanical Dimensions, BGA**

# Recommended Land Pattern and Stencil

## 15mm x 15mm x 5.01mm BGA



**TYPICAL RECOMMENDED LAND PATTERN**



**TYPICAL RECOMMENDED STENCIL**

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

Drawing No.: POD-0000084

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**Figure 44: Recommended Land Pattern and Stencil, BGA**

## MxL7213 Component Pinout

**Table 12: MxL7213 Component Pinout**

| Pin ID | Function | Pin ID | Function | Pin ID | Function | Pin ID | Function | Pin ID | Function | Pin ID | Function   |
|--------|----------|--------|----------|--------|----------|--------|----------|--------|----------|--------|------------|
| A1     | VOUT1    | B1     | VOUT1    | C1     | VOUT1    | D1     | GND      | E1     | GND      | F1     | GND        |
| A2     | VOUT1    | B2     | VOUT1    | C2     | VOUT1    | D2     | GND      | E2     | GND      | F2     | GND        |
| A3     | VOUT1    | B3     | VOUT1    | C3     | VOUT1    | D3     | GND      | E3     | GND      | F3     | GND        |
| A4     | VOUT1    | B4     | VOUT1    | C4     | VOUT1    | D4     | GND      | E4     | GND      | F4     | MODE_PLLIN |
| A5     | VOUT1    | B5     | VOUT1    | C5     | VOU1S1   | D5     | VFB1     | E5     | TRACK1   | F5     | RUN1       |
| A6     | GND      | B6     | GND      | C6     | FSET     | D6     | SGND     | E6     | COMP1    | F6     | SGND       |
| A7     | GND      | B7     | GND      | C7     | SGND     | D7     | VFB2     | E7     | COMP2    | F7     | SGND       |
| A8     | VOUT2    | B8     | VOUT2    | C8     | VOU2S2   | D8     | TRACK2   | E8     | DIFFP    | F8     | DIFFOUT    |
| A9     | VOUT2    | B9     | VOUT2    | C9     | VOUT2    | D9     | GND      | E9     | DIFFN    | F9     | RUN2       |
| A10    | VOUT2    | B10    | VOUT2    | C10    | VOUT2    | D10    | GND      | E10    | GND      | F10    | GND        |
| A11    | VOUT2    | B11    | VOUT2    | C11    | VOUT2    | D11    | GND      | E11    | GND      | F11    | GND        |
| A12    | VOUT2    | B12    | VOUT2    | C12    | VOUT2    | D12    | GND      | E12    | GND      | F12    | GND        |
| G1     | GND      | H1     | GND      | J1     | GND      | K1     | GND      | L1     | GND      | M1     | GND        |
| G2     | SW1      | H2     | GND      | J2     | VIN      | K2     | VIN      | L2     | VIN      | M2     | VIN        |
| G3     | GND      | H3     | GND      | J3     | VIN      | K3     | VIN      | L3     | VIN      | M3     | VIN        |
| G4     | PHASMD   | H4     | GND      | J4     | VIN      | K4     | VIN      | L4     | VIN      | M4     | VIN        |
| G5     | CLKOUT   | H5     | GND      | J5     | GND      | K5     | GND      | L5     | VIN      | M5     | VIN        |
| G6     | SGND     | H6     | GND      | J6     | TEMP     | K6     | GND      | L6     | VIN      | M6     | VIN        |
| G7     | SGND     | H7     | GND      | J7     | EXTVCC   | K7     | GND      | L7     | VIN      | M7     | VIN        |
| G8     | PGOOD2   | H8     | INTVCC   | J8     | GND      | K8     | GND      | L8     | VIN      | M8     | VIN        |
| G9     | PGOOD1   | H9     | GND      | J9     | VIN      | K9     | VIN      | L9     | VIN      | M9     | VIN        |
| G10    | GND      | H10    | GND      | J10    | VIN      | K10    | VIN      | L10    | VIN      | M10    | VIN        |
| G11    | SW2      | H11    | GND      | J11    | VIN      | K11    | VIN      | L11    | VIN      | M11    | VIN        |
| G12    | GND      | H12    | GND      | J12    | GND      | K12    | GND      | L12    | GND      | M12    | GND        |



## Ordering Information

**Table 13: Ordering Information<sup>(1)</sup>**

| Ordering Part Number | Operating Temperature Range             | MSL Rating | Lead-Free          | Package      | Packaging Method |
|----------------------|---|------------|--------------------|--------------|------------------|
| MxL7213-AYA-T        | -40°C ≤ T <sub>J</sub> ≤ 125°C          | 3          | Yes <sup>(2)</sup> | LGA144 15x15 | Tray             |
| MxL7213-ABA-T        |   |            |                    | BGA144 15x15 |                  |
| MxL7213-EVK-1        | MxL7213 LGA Power Module Dual-Phase EVK |            |                    |              |                  |
| MxL7213-EVK-3        | MxL7213 BGA Power Module Dual-Phase EVK |            |                    |              |                  |

1. Refer to [www.maxlinear.com/MxL7213](http://www.maxlinear.com/MxL7213) for most up-to-date Ordering Information.
2. Visit [www.maxlinear.com](http://www.maxlinear.com) for additional information on Environmental Rating.



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