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MxL7213
13A Dual Phase
EVB User Manual

Revision History

Document No.	Release Date	Change Description
000UMR02	4/23/19	Initial Release
000UMR03	8/29/19	References changed to reflect board revision. **Added** ■ EVB Mode Selection section.
000UMR04	9/19/19	**Update** ■ BOM and ordering information.
000UMR05	10/15/20	**Update** ■ VOUT and GND test pin numbers in Quick Start Up and connections in Figure 1. ■ Schematic (R1, R16, C13, C36, C37 values) to match BOM. ■ Board photo.

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Introduction

The MxL7213 evaluation board provides a platform to evaluate the features and performance of the MxL7213. The MxL7213 is a dual 13A Power Module optimized for powering Telecom, Networking and Industrial equipment. This manual covers the 13A Dual Phase BGA and LGA Evaluation Boards.

Quick EVB Set Up and Start Up

Factory Settings

In addition to utilizing the 4.5V to 16V input voltage range and dual 13A maximum load current rating capabilities of the MxL7213 Power Module, the Evaluation Board has been set up with the factory default configurations shown below for quick set up and operation. **Do not exceed the EVB maximum load current rating.**

The factory default configuration (Table 2) for the MxL7213 Evaluation Board is:

- V_{OUT1} = 3.3V ±1.5%
- V_{OUT2} = 5.0V ±1.5%
- 750kHz Switching Frequency
- CCM mode. For other modes, see Jumper J44 MODE.
- Run is enabled for both channels. See Jumpers J30 RUN1 and J29 RUN2.
- Soft-start is selected for both channels. See Jumper J26 TRACK1 SEL and Jumper J25 TRACK2 SEL.
- CLKOUT phase is 90 degrees, see Jumper J45 PHASMD.
- Differential remote sense amplifier monitoring V_{OUT1}

Quick Start Up

To quickly see the regulator in operation:

1. Use the factory settings and default configuration. If other settings or components are desired, apply them before the next steps and see Set-Up Options for more.
2. Connect a turned-off power supply that is within a V_{IN} specification of 4.5V to 16V, (12V typical) to VIN and GND with short, thick leads. Use test pins VIN+ and VIN- to monitor VIN and GND respectively. See locations in Figure 1.
3. For the channel 1 output, connect an electronic load initially set to 0A, that will be no more than the above maximum I_{OUT} (13A), to VOUT1 and GND with short / thick leads. Use test pins VOUT1 (J52) and VOUT_GND (J60) to monitor VOUT1 and GND respectively. See locations in Figure 1.
4. For the channel 2 output, connect an electronic load initially set to 0A, that will be no more than the above maximum I_{OUT} (13A), to VOUT2 and GND with short, thick leads. Use test pins VOUT2 (J53) and VOUT2_GND (J61) to monitor VOUT2 and GND respectively. See locations in Figure 1.
5. Turn on the power supply and check V_{OUT} of both channels. The EVB will power up and (factory default) regulate the channel 1 output at 3.3V ±1.5% (3.251V to 3.349V) and channel 2 output at 5.0V ±1.5% (4.925V to 5.075V). Output ripple should be measured across the output capacitors for each channel: C8 for VOUT1 and C22 for VOUT2. Test points J52 and J53 can be used to monitor the ripple for VOUT1 and VOUT2, respectively.
6. Set or vary the load (do not exceed the maximum I_{OUT}) and check V_{OUT} and other desired performance levels such as regulation and efficiency.

See Configuration and I/O Interfaces and Load Transient Circuit for more on testing and monitoring. For Single Rail Dual Phase 26A Operation and to vary V_{OUT} see MxL7213 EVB Mode Selection.

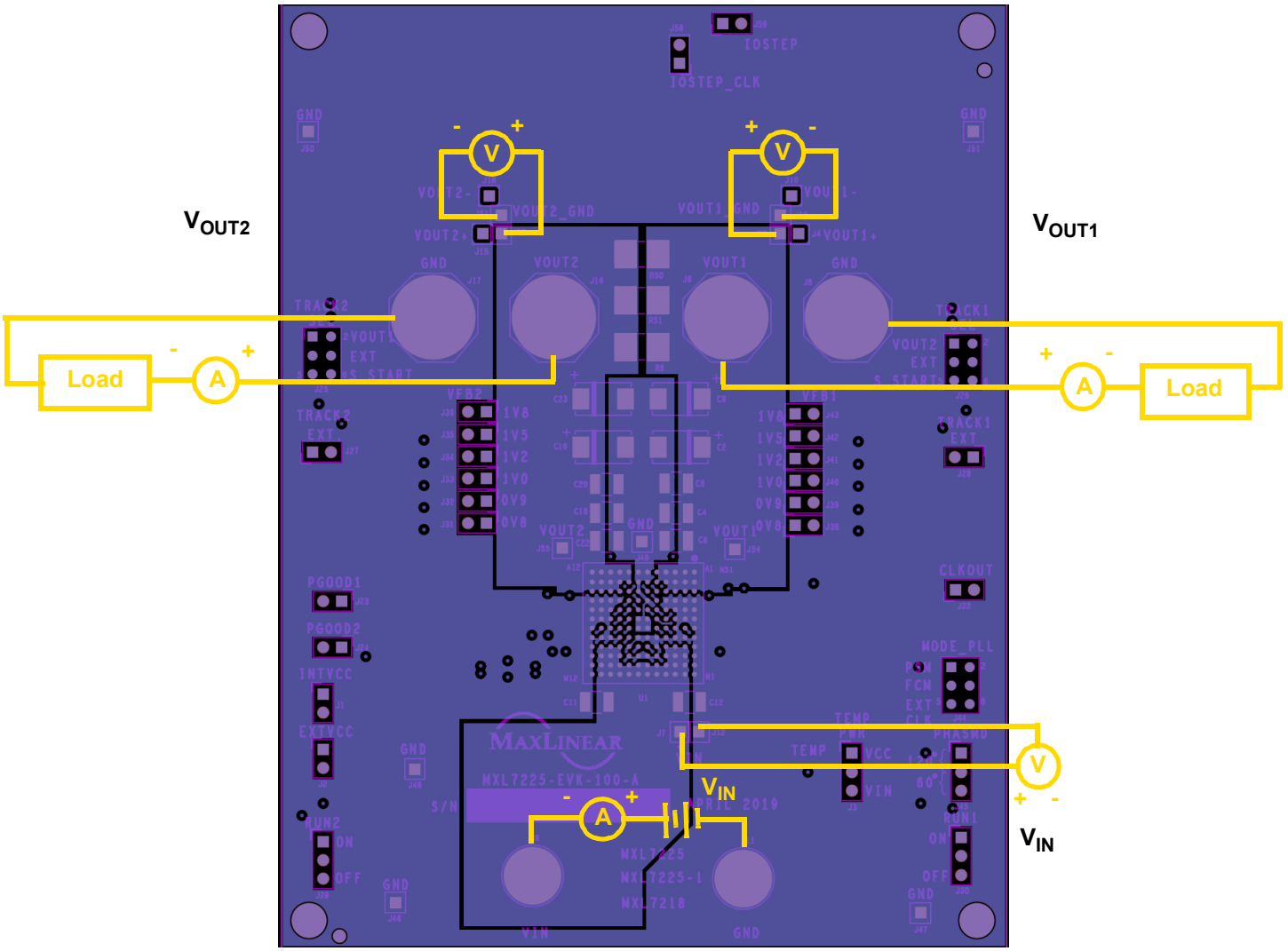


Figure 1: Monitoring V_{IN} and V_{OUT}

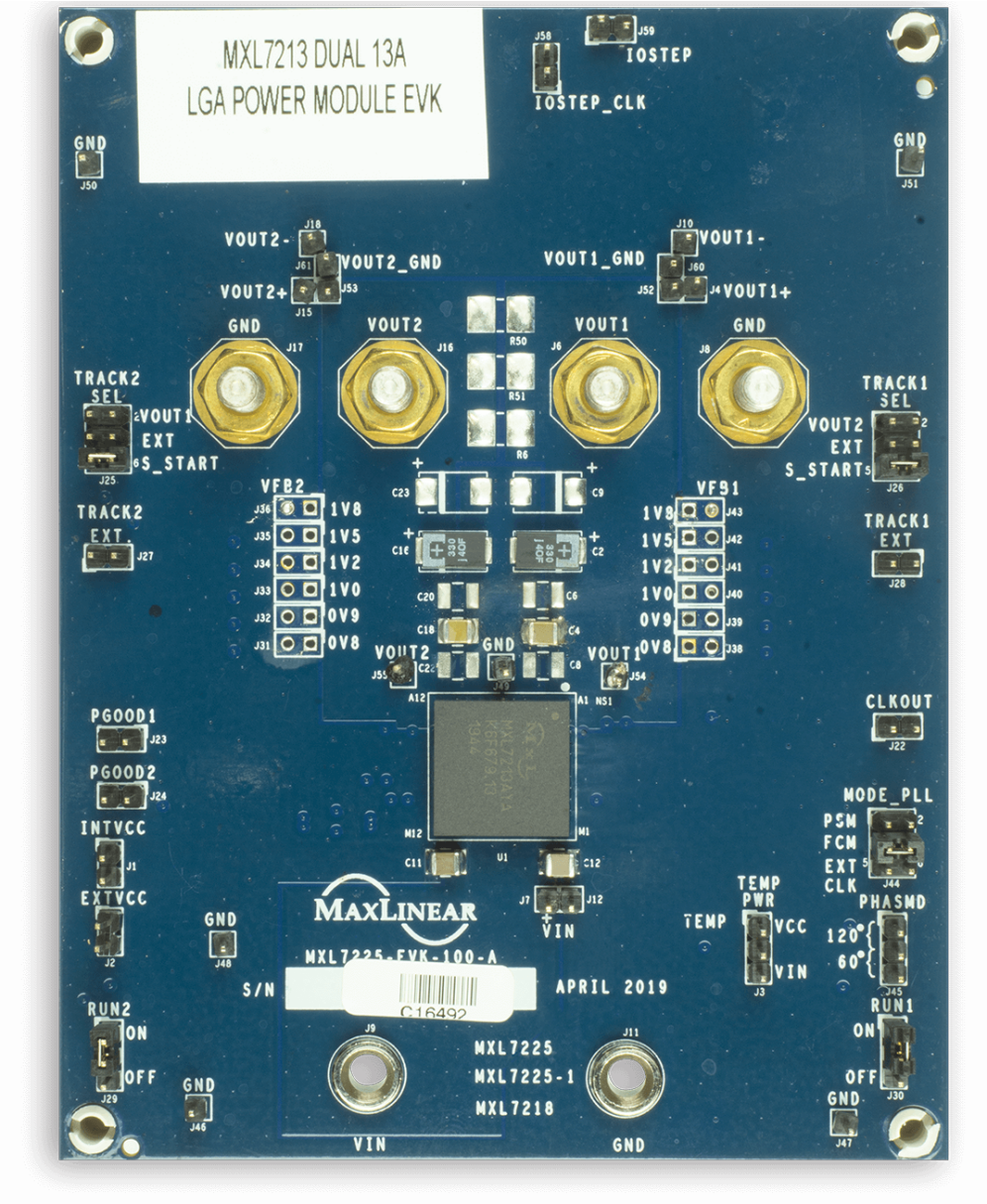


Figure 2: Top View of MxL7213 13A Dual Phase EVB

Reference Documentation

Please refer to the MxL7213 Data Sheet for additional information about the MxL7213, including efficiency curves for this configuration with V_{IN} = 12V. The datasheet also includes a full list of IC features, pinout, pin descriptions, typical performance characteristics and external component calculations. This manual is meant to be used in conjunction with the datasheet.

This manual provides EVB schematics, PCB layout and bill of materials that can be utilized to assist in your board design. The schematics are also available on the MxL7213 product page.

Ordering Information

Table 1: Evaluation Board Ordering Part Number(1)

Power Module	Evaluation Board	Description
MxL7213-AYA-T	MxL7213-EVK-1	MxL7213 LGA Power Module Dual-Phase EVB
MxL7213-ABA-T	MxL7213-EVK-3	MxL7213 BGA Power Module Dual-Phase EVB

1. Refer to www.maxlinear.com/MxL7213 for most up-to-date Ordering Information.

Evaluation Board Overview

The block diagram shown in Figure 3 illustrates the connection points for the VIN, VOUT1, VOUT2, TRACK, MODE_PLL and RUN pins.

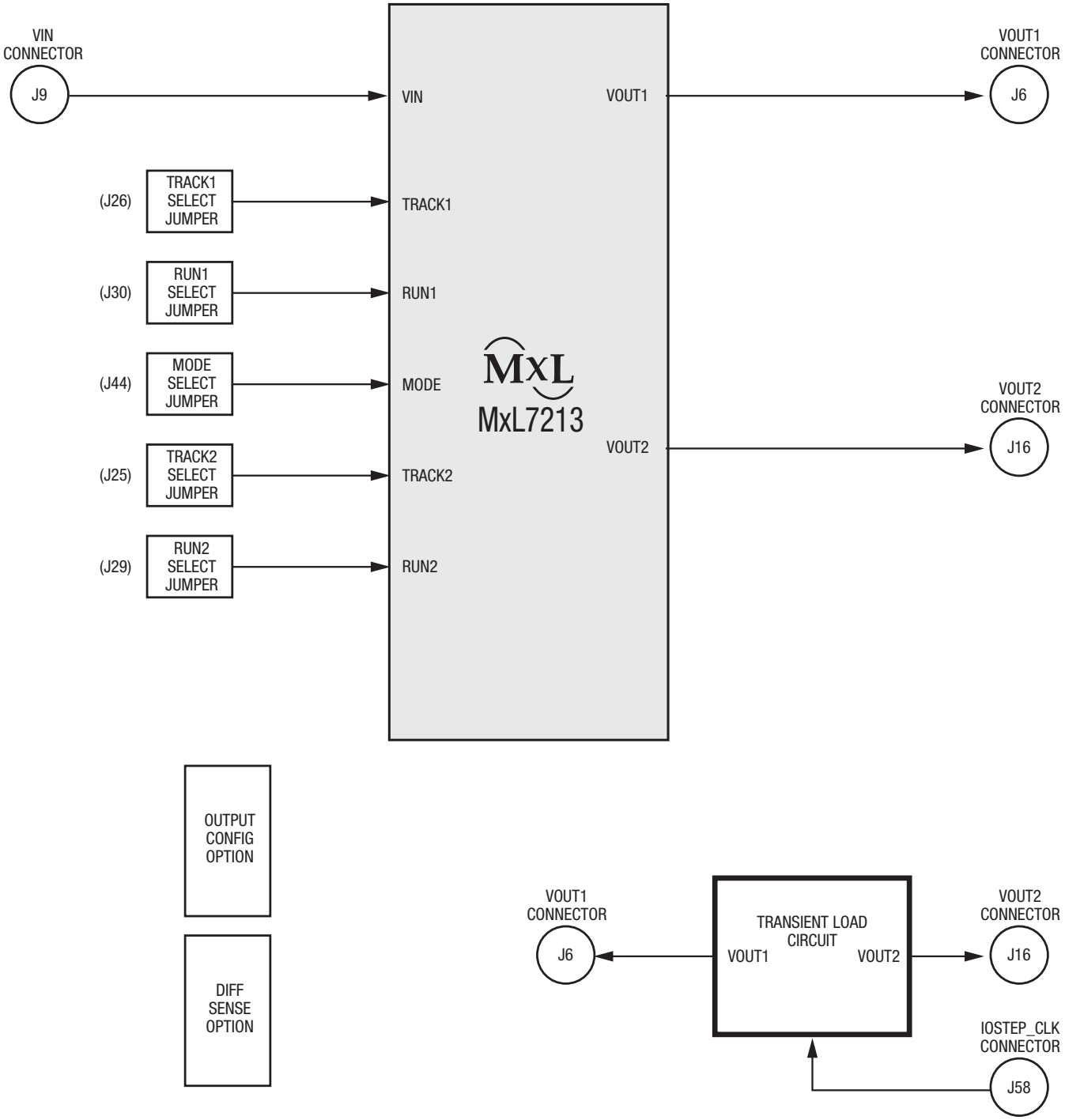


Figure 3: Block Diagram MxL7213 Two Channel EVB

Configuration and I/O Interfaces

MODE

The MODE (J44) jumper is provided for overall device configuration:

Force Continuous Mode, Pulse-Skipping Mode and External Synchronization are selectable.

RUN1, RUN2

A RUN jumper is provided for both channels (J30 for RUN1 and J29 for RUN2).

TRACK1 SEL, TRACK2 SEL

A TRACK jumper is provided for both channels.

VOUT, EXT and SOFTSTART are selectable.

Test points are allocated for probing of TRACK1 (J26) and TRACK2 (J25).

PHASMD

A CLKOUT (J45) jumper is provided for clock phase selection.

60, 90 or 120 degrees of phase offset is configurable.

EXTVCC

An EXTVCC test point (J2) is provided to monitor or inject EXTVCC.

TEMP

A TEMP test point (J3) is provided to monitor temperature.

PGOOD1, PGOOD2

A PGOOD test point is provided for both channels (J24 for PGOOD1 and J23 for PGOOD2[(1)]).

Both PGOOD signals are tied to INTVCC through 10kΩ resistors.

1. J23 and J24 are mislabeled on the board. J24 is PGOOD1 and J23 is PGOOD2.

SW1, SW2

A SW test point is provided for both switching signals (TP1 for SW1 and TP2 for SW2), and are located on the bottom (back) of the board.

Set-Up Options

Jumpers are factory installed per Table 2 to configure the EVB for operation. Jumper and testing options are described in the next sections. Refer to the product datasheet for additional information.

Table 2: Factory Settings

Jumper	Label	Factory Setting	Description
J44	MODE	Jumper 3-4	FCM
J30	RUN1	Jumper 1-2	On
J29	RUN2	Jumper 1-2	On
J26	TRACK1	Jumper 5-6	Soft-Start
J25	TRACK2	Jumper 5-6	Soft-Start
J45	PHASEMD	No Jumper	90°

Jumper J44 MODE

Table 3: J44 Options

Jumper Options	Description
Jumper 1-2	PSM - Pulse Skipping Mode.
Jumper 3-4	FCM - Force Continuous Mode.
Pin 6	Apply an external clock to pin 6 to put both channels into continuous mode, synchronized to the applied clock.

Jumpers J30 RUN1 and J29 RUN2

Table 4: J30, J29 Options

Jumper Options	Description
Jumper 1-2	On. RUN1/2 connected to VIN.
Jumper 2-3	Off. RUN1/2 connected to GND.

Jumper J26 TRACK1 SEL

Table 5: J26 Options

Jumper Options	Description
Jumper 1-2	V_{OUT2} master track mode.
Jumper 3-4	External master track mode.
Jumper 5-6	Soft start. Track1 connected to cap to GND.

Jumper J25 TRACK2 SEL

Table 6: J25 Options

Jumper Options	Description
Jumper 1-2	V_{OUT1} master track mode.
Jumper 3-4	External master track mode.
Jumper 5-6	Soft start. Track1 connected to cap to GND.

Jumper J45 PHASMD

Table 7: J45 Options

Jumper Options	Description
Jumper 1-2	120°
No Jumper	90°
Jumper 2-3	60°

Test Interfaces

Load Transient Circuit

A load transient circuit is provided to allow optional testing of load transients. The IOSTEP clock input is used to drive the transient signal. The load step generated by the FET (Q1) is very fast; the step slew rate is >40A/µs for a 6.5A transient load test case.

To measure load transient response for either channel, use the circuit shown in Figure 4. To test CH1, populate R56 and depopulate R57 and apply a small duty cycle pulse signal to IOSTEP CLK input (~ 1%). Adjust the amplitude of the IOSTEP CLK pulse to set the load current. Start at a pulse amplitude of 2V and increase while monitoring the IOSTEP (J59) voltage. The load current at IOSTEP (J59) is 10mV/A. For an example, a 6.5A load will occur when a 65mV pulse is observed at J59.

To test load transient response on CH2, depopulate R56 and populate R57 and repeat procedure.

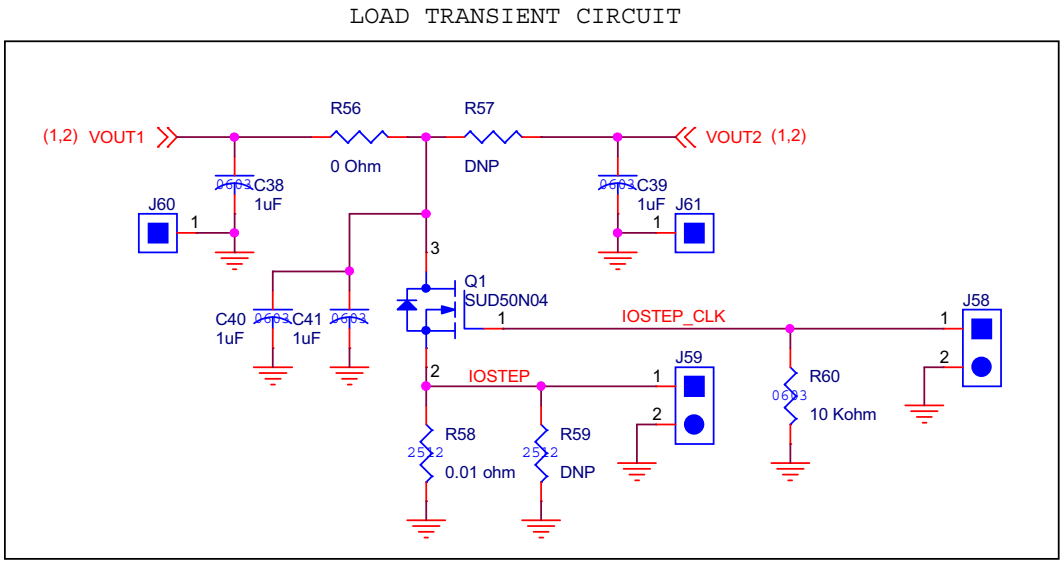


Figure 4: Load Transient Circuit

MxL7213 EVB Mode Selection

The MxL7213 EVB can be configured for 6 different modes of operation:

- Mode 1: Dual 13A with no remote sense amplifier
- Mode 2: Dual 13A with remote sense amplifier on V_{OUT1}
- Mode 3: Dual 13A with remote sense amplifier on V_{OUT2}
- Mode 4: Single 26A with no remote sense amplifier
- Mode 5: Single 26A with remote sense amplifier on V_{OUT1}
- Mode 6: Single 26A with remote sense amplifier on V_{OUT2}

The stuffing options to configure the EVB into each of the 6 modes are shown below with the block diagram for each mode on the next page.

Table 8: Board Stuffing for Operation Mode Selection

Pin Function	Component	Mode 1 Dual Rail Single Phase Diff Amp NC	Mode 2 Dual Rail Single Phase Diff Amp V_{OUT1}	Mode 3 Dual Rail Single Phase Diff Amp V_{OUT2}	Mode 4 Single Rail Dual Phase Diff Amp NC	Mode 5 Single Rail Dual Phase Diff Amp V_{OUT1}	Mode 6 Single Rail Dual Phase Diff Amp V_{OUT2}
Single Rail	R6	DNP	DNP	DNP	0Ω	0Ω	0Ω
	R50	DNP	DNP	DNP	0Ω	0Ω	0Ω
	R51	DNP	DNP	DNP	0Ω	0Ω	0Ω
VOUTS1	R4	0Ω	DNP	0Ω	0Ω	DNP	DNP
VOUTS2	R7	0Ω	0Ω	DNP	DNP	DNP	DNP
DIFFP (VOUT1+)	R34	DNP	0Ω	DNP	DNP	0Ω	DNP
DIFFP (VOUT2+)	R40	DNP	DNP	0Ω	DNP	DNP	0Ω
DIFFN (VOUT1-)	R54	DNP	0Ω	DNP	DNP	0Ω	DNP
DIFFN (VOUT2-)	R55	DNP	DNP	0Ω	DNP	DNP	0Ω
DIFFOUT (VOUTS1+)	R41	DNP	0Ω	DNP	DNP	0Ω	DNP
DIFFOUT (VOUTS2+)	R42	DNP	DNP	0Ω	DNP	DNP	0Ω
TRACK	R45	DNP	DNP	DNP	0Ω	0Ω	0Ω
TRACK1	J26 (5-6)	On	On	On	On	On	On
TRACK2	J25 (5-6)	On	On	On	Off	Off	Off
RUN	R43	DNP	DNP	DNP	0Ω	0Ω	0Ω
COMP	R44	DNP	DNP	DNP	0Ω	0Ω	0Ω
PGOOD	R47	DNP	DNP	DNP	0Ω	0Ω	0Ω
VFB	R46	DNP	DNP	DNP	0Ω	0Ω	0Ω

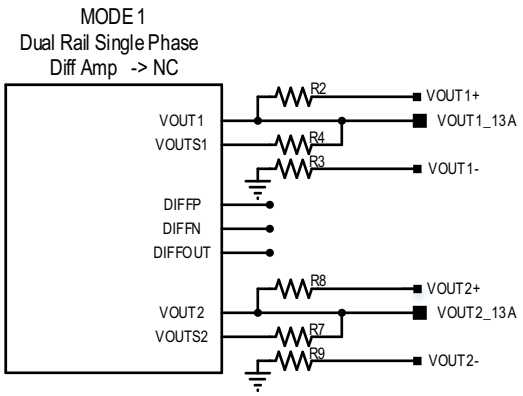


Figure 5: Mode 1 Block Diagram

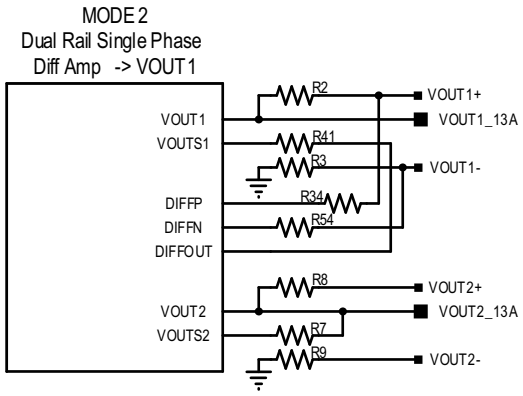


Figure 6: Mode 2 Block Diagram

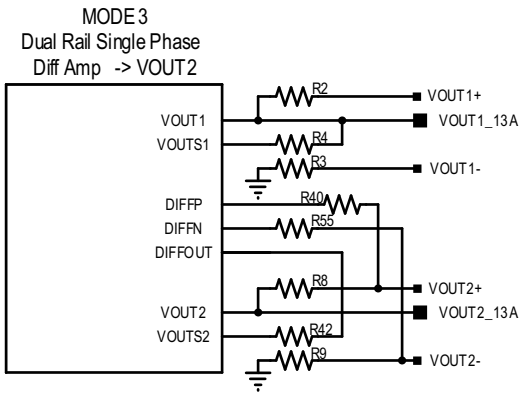


Figure 7: Mode 3 Block Diagram

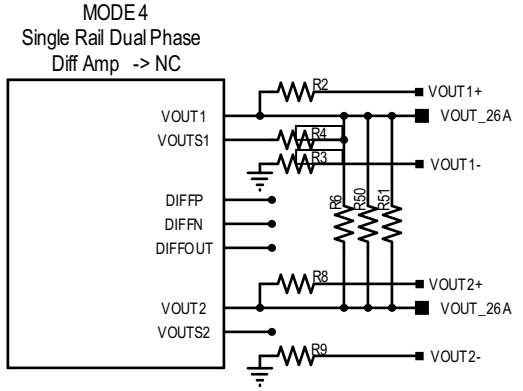


Figure 8: Mode 4 Block Diagram

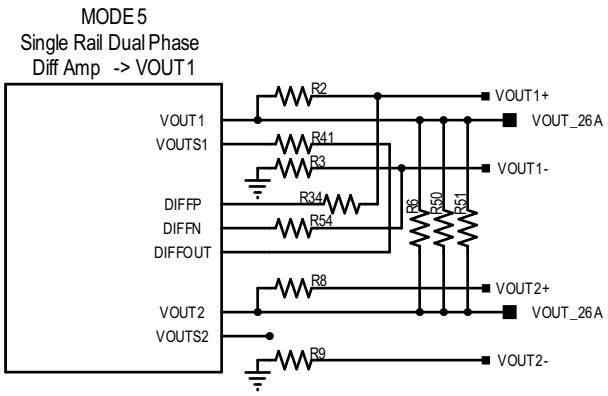


Figure 9: Mode 5 Block Diagram

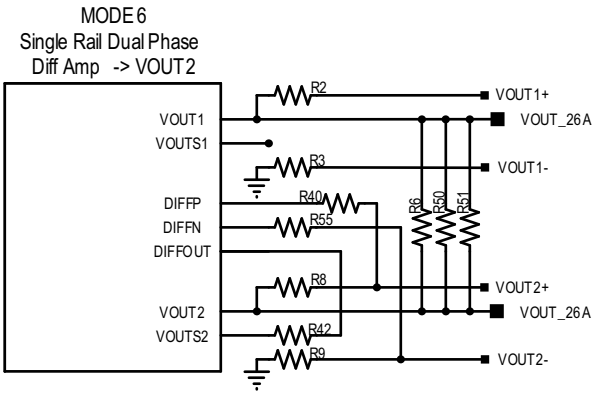


Figure 10: Mode 6 Block Diagram

Performance

Efficiency

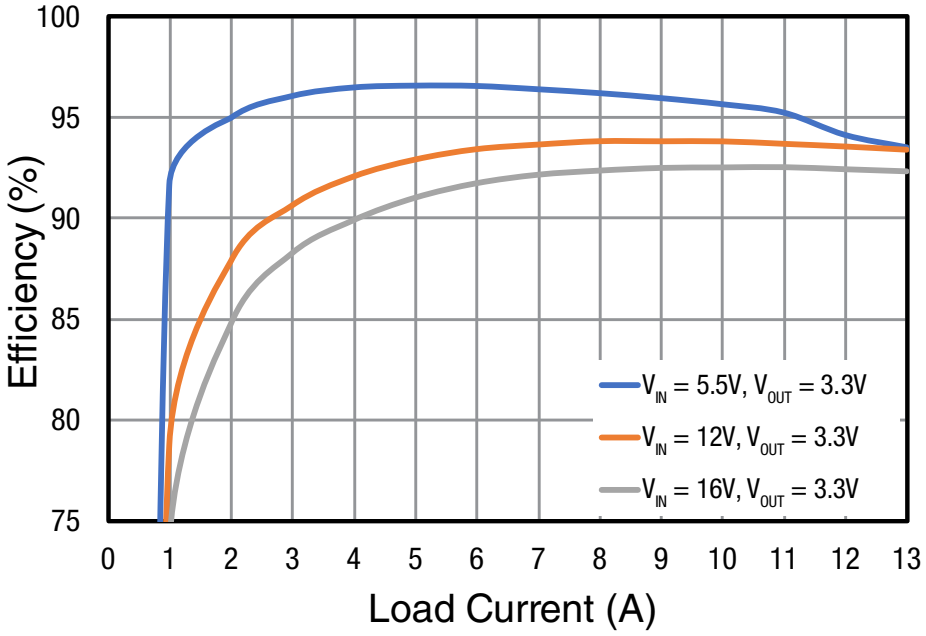


Figure 11: Channel 1 Measured Efficiency (V_{OUT} = 3.3V, f_{SW} = 750kHz, Ch 2 Disabled)

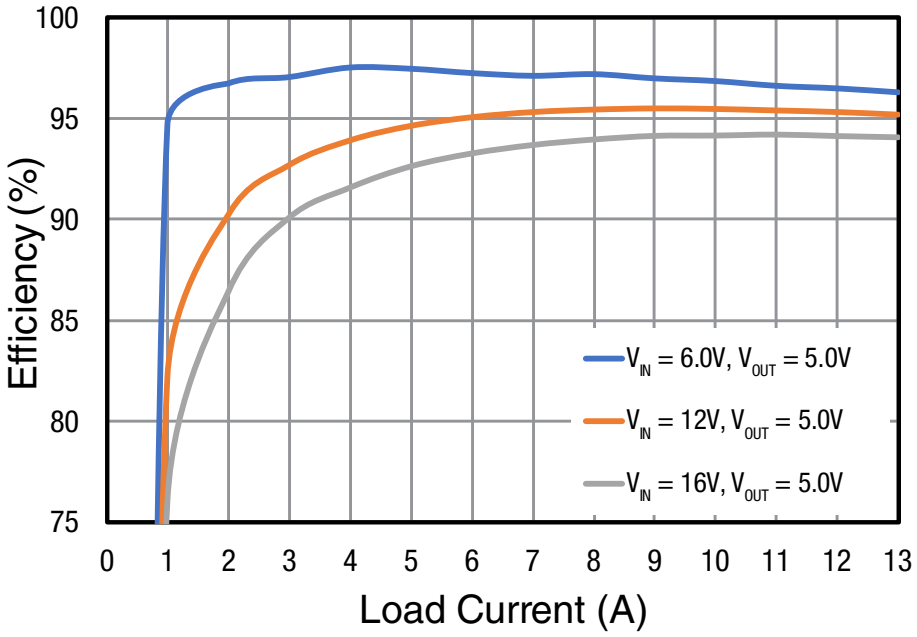


Figure 12: Channel 2 Measured Efficiency (V_{OUT} = 5.0V, f_{SW} = 750kHz, Ch 1 Disabled)

Load Transient Response

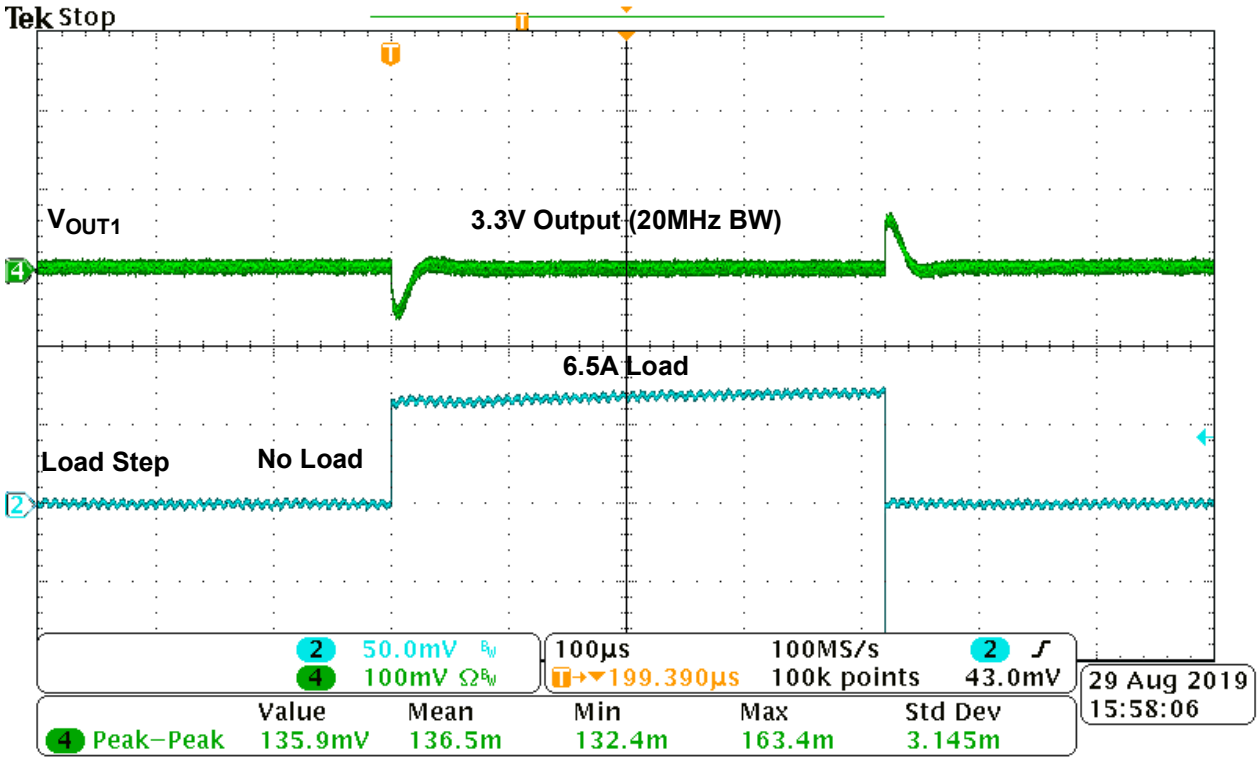


Figure 13: Channel 1 Load Transient Response (V_{OUT} = 3.3V, V_{IN} = 12V)

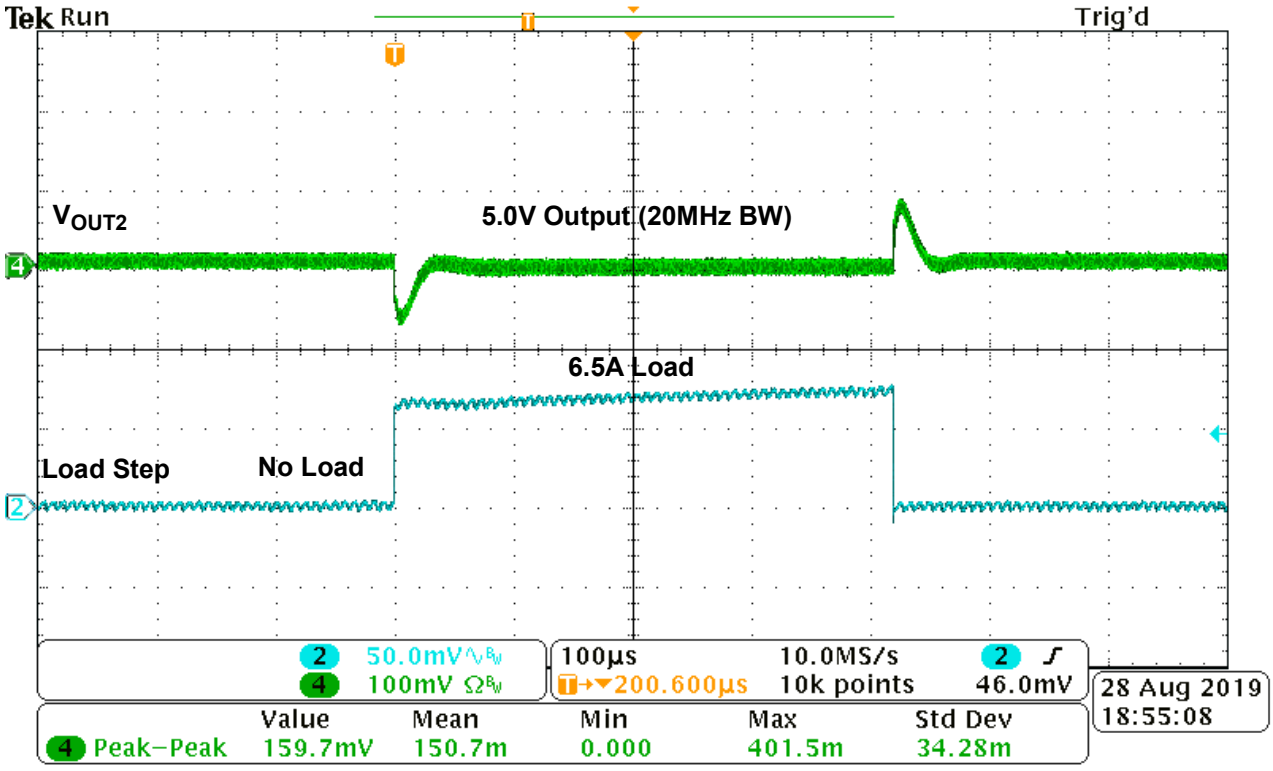
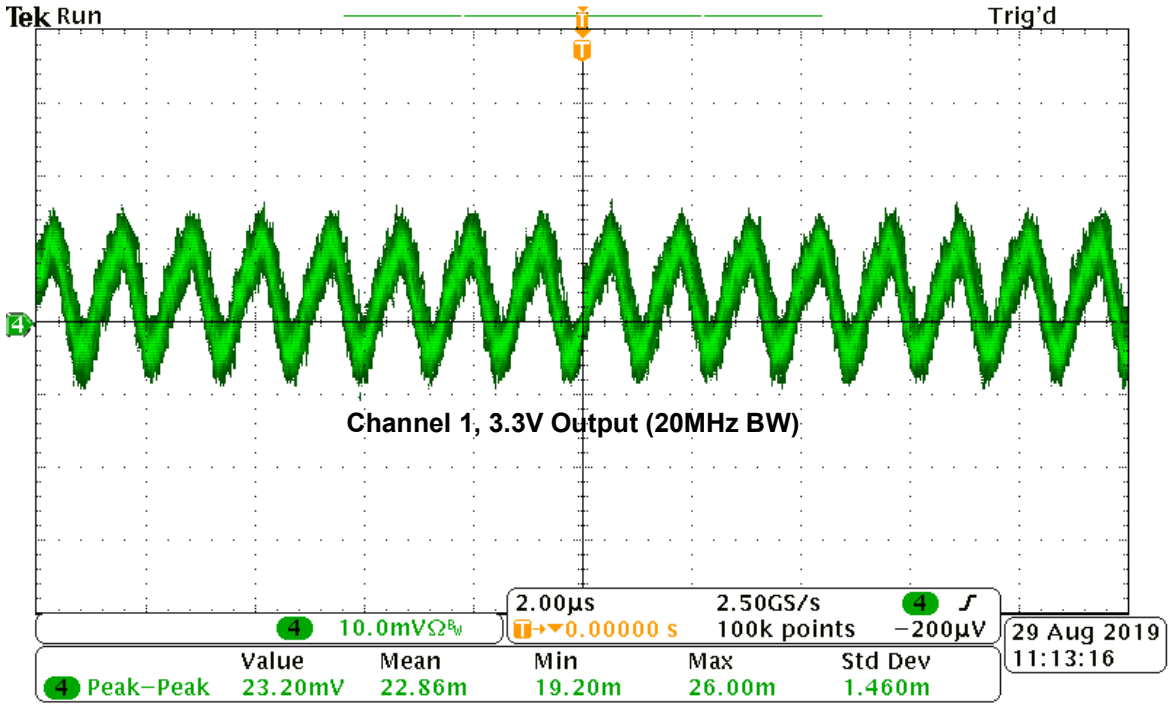


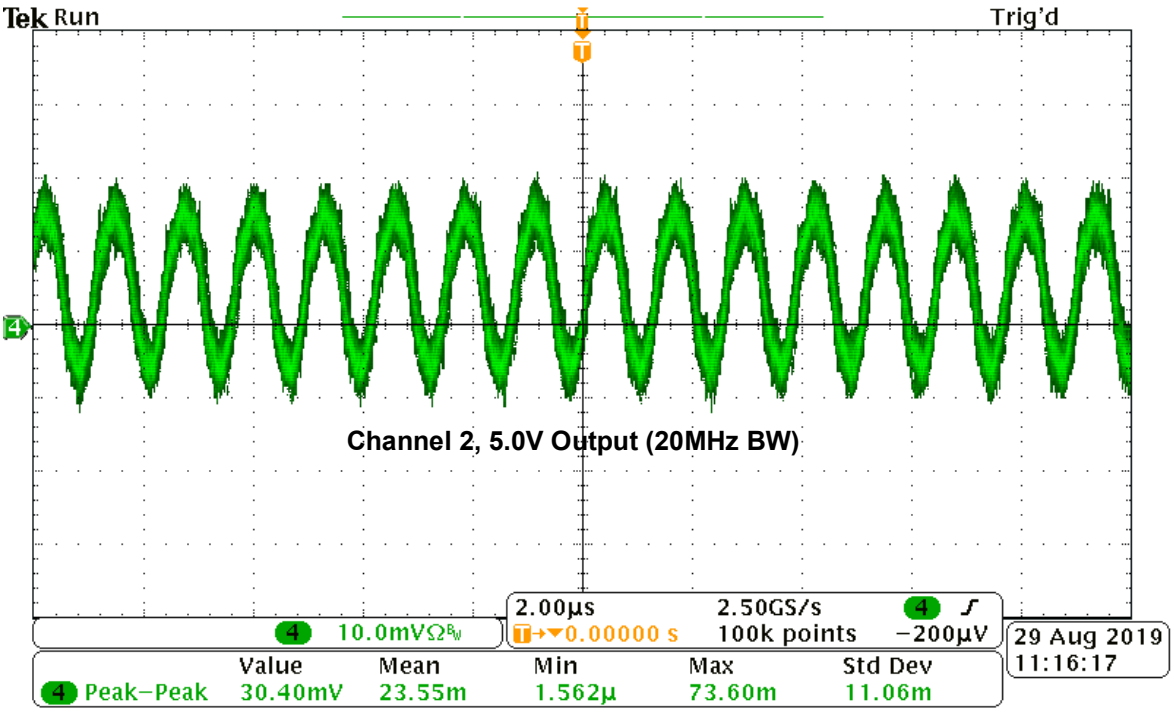
Figure 14: Channel 2 Load Transient Response (V_{OUT} = 5.0V, V_{IN} = 12V)

Output Ripple



2. Ripple waveform shown, measured at VOUT1 (J54). The ripple waveform characteristics ideally should be observed at the output capacitor closest to the MxL7213, C8.

Figure 15: Channel 1 Output Voltage Ripple (V_{IN} = 12V, V_{OUT} = 3.3V, Load = 13A)



3. Ripple waveform shown, measured at VOUT2 (J55). The ripple waveform characteristics ideally should be observed at the output capacitor closest to the MxL7213, C22.

Figure 16: Channel 2 Output Voltage Ripple (V_{IN} = 12V, V_{OUT} = 5.0V, Load = 13A)

MxL7213EVB Schematic

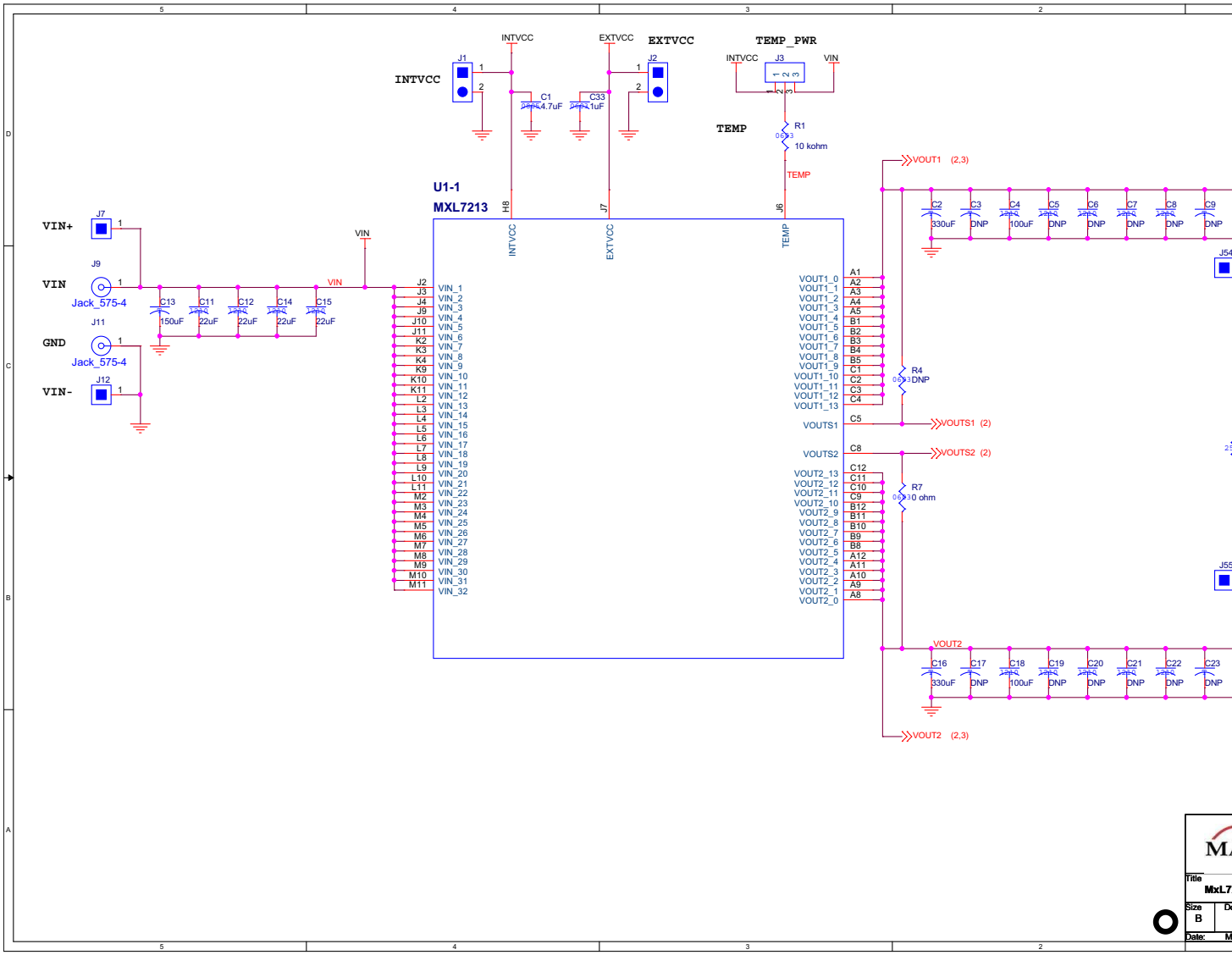


Figure 17: EVB Schematic

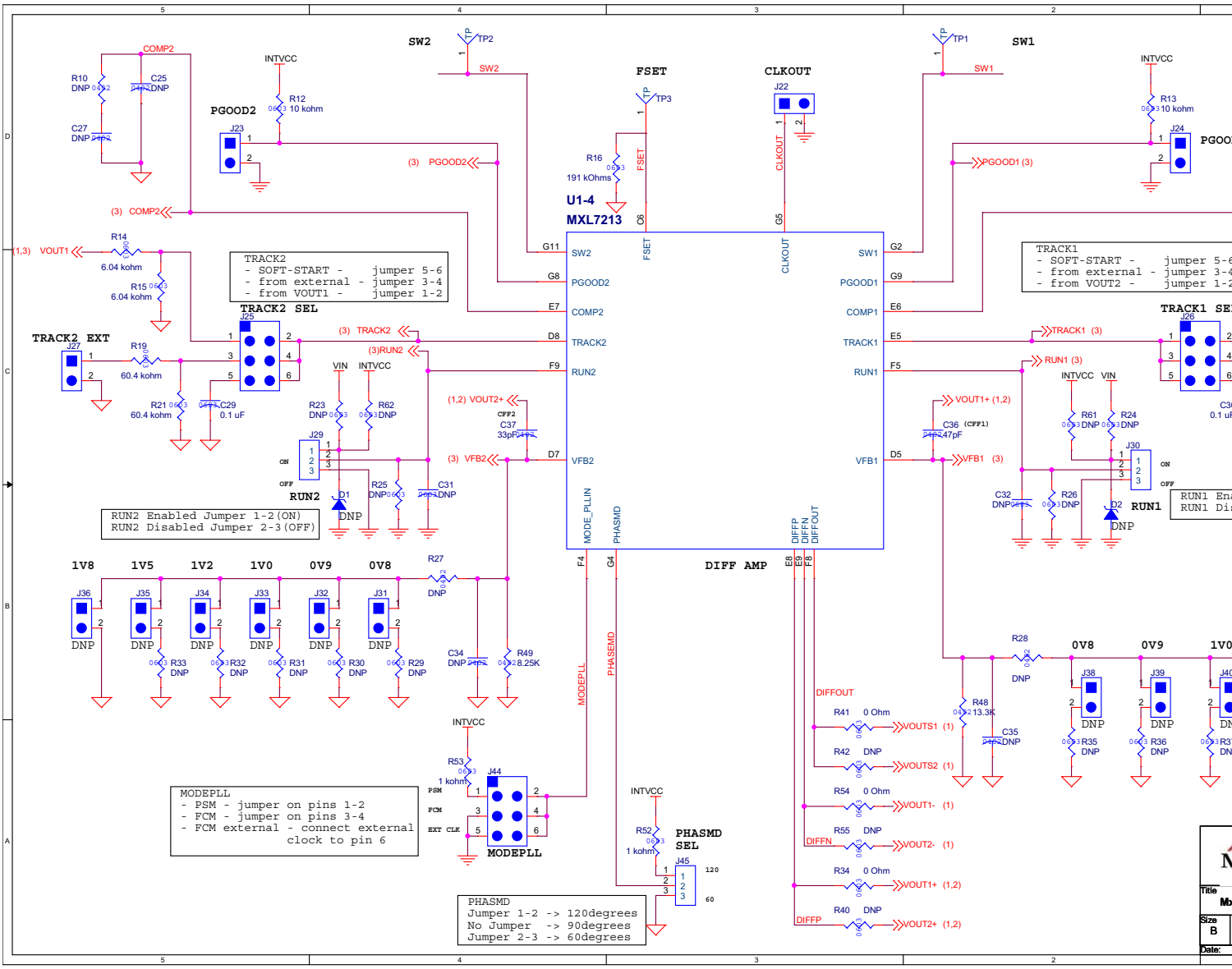


Figure 18: EVB Schematic, Continued

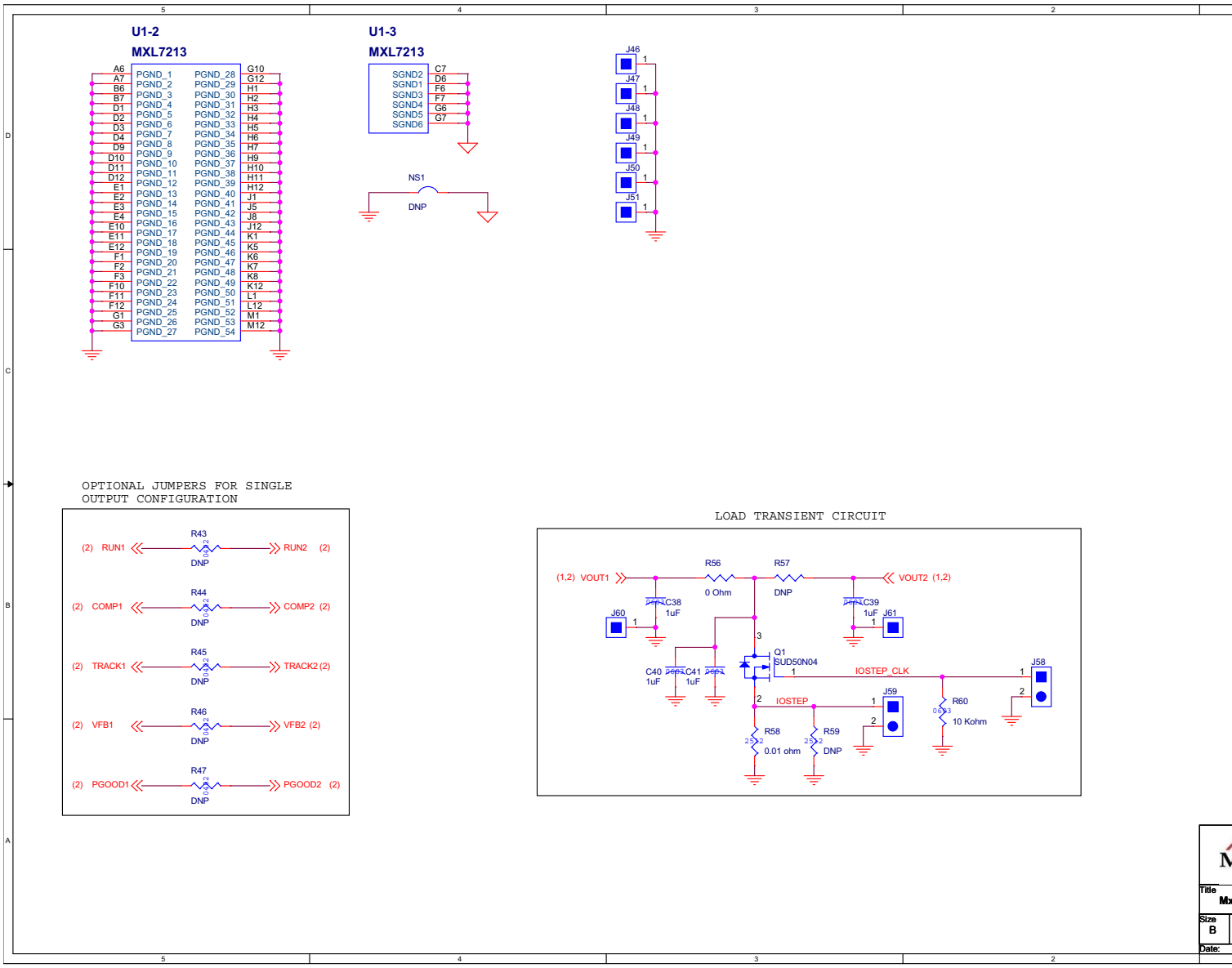


Figure 19: EVB Schematic, Continued

MxL7213EVB PCB Layers

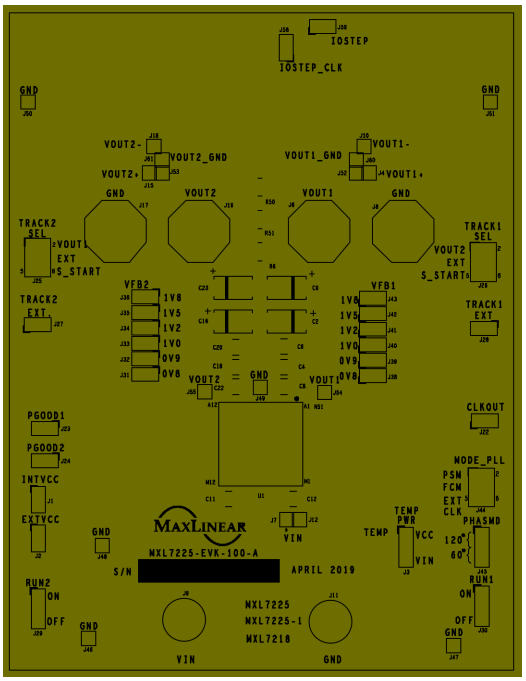


Figure 20: EVB PCB Silkscreen Top

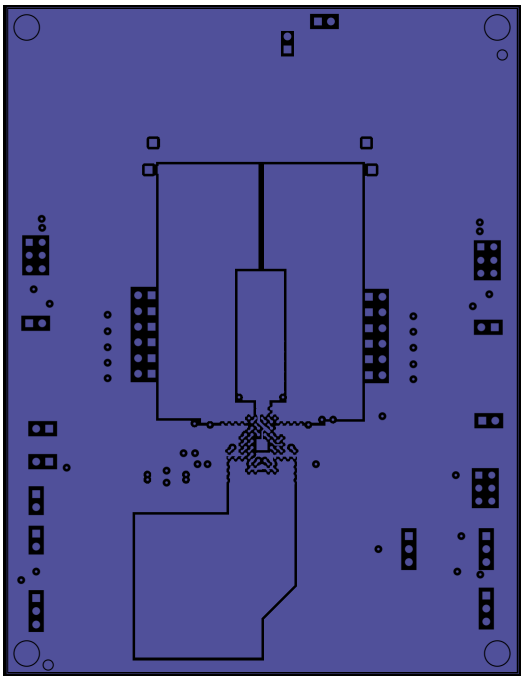


Figure 21: EVB PCB Layer 1

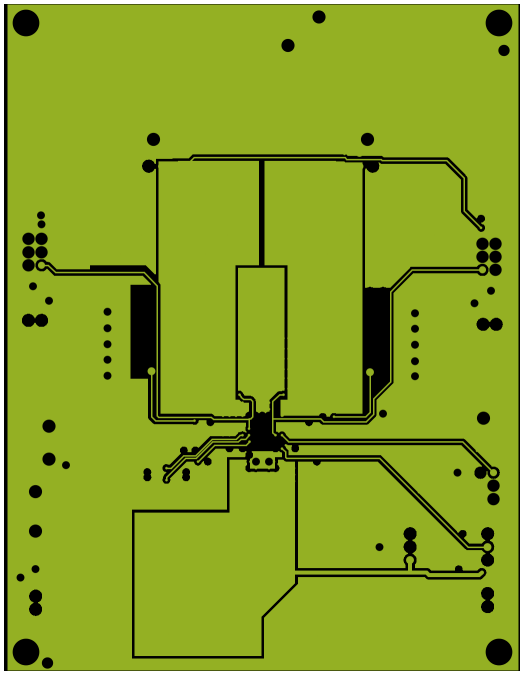


Figure 22: EVB PCB Layer 2

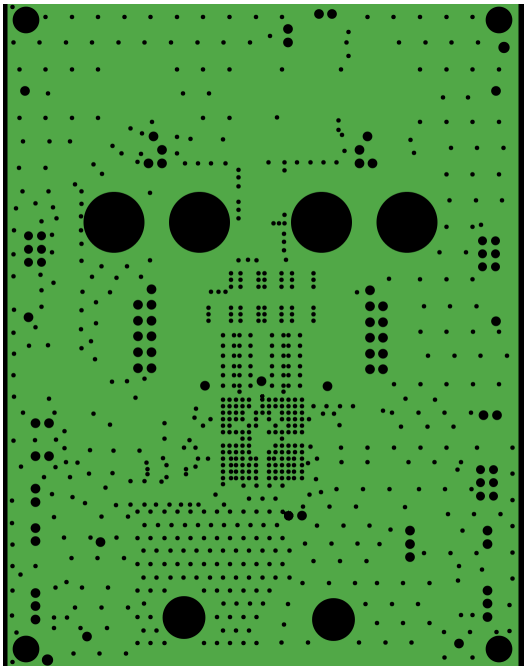


Figure 23: EVB PCB Layer 3

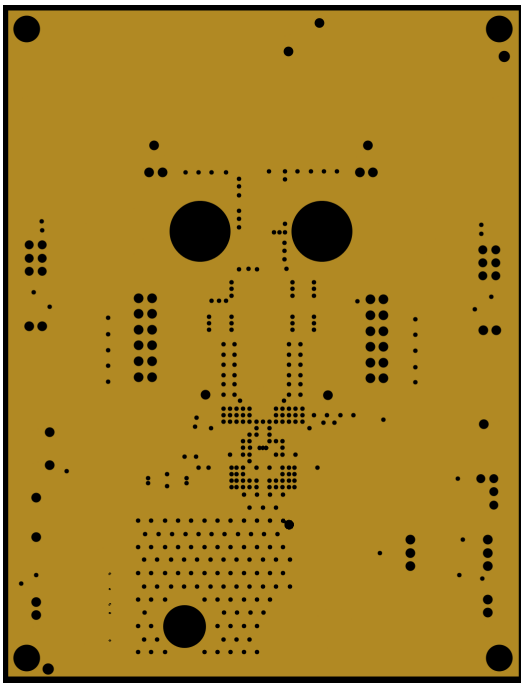


Figure 24: EVB PCB Layer 4

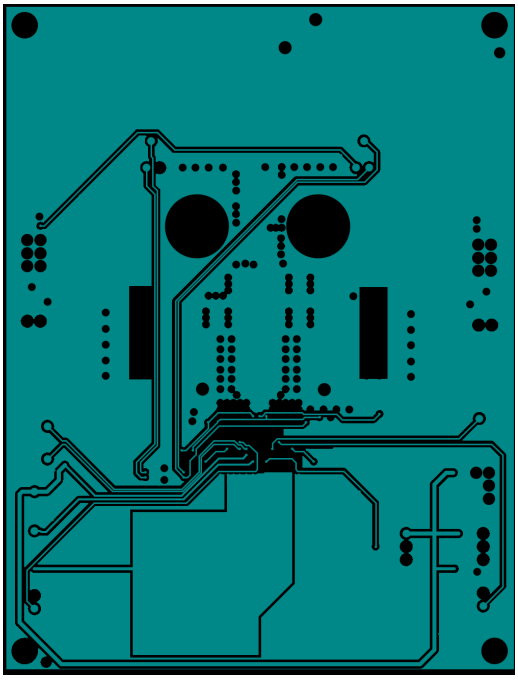


Figure 25: EVB PCB Layer 5

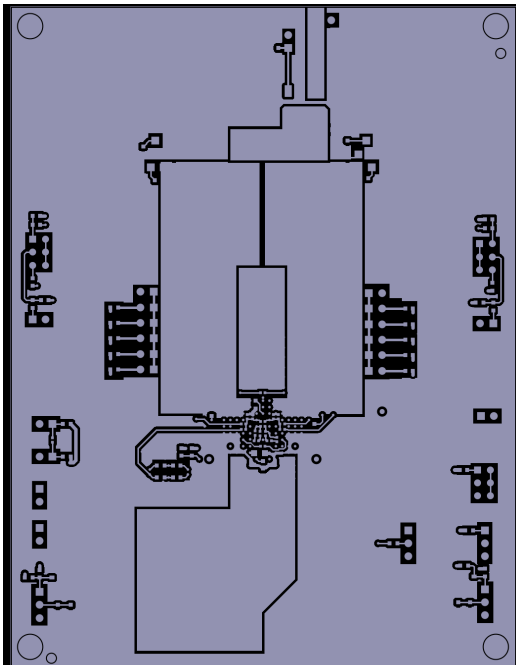


Figure 26: EVB PCB Layer 6

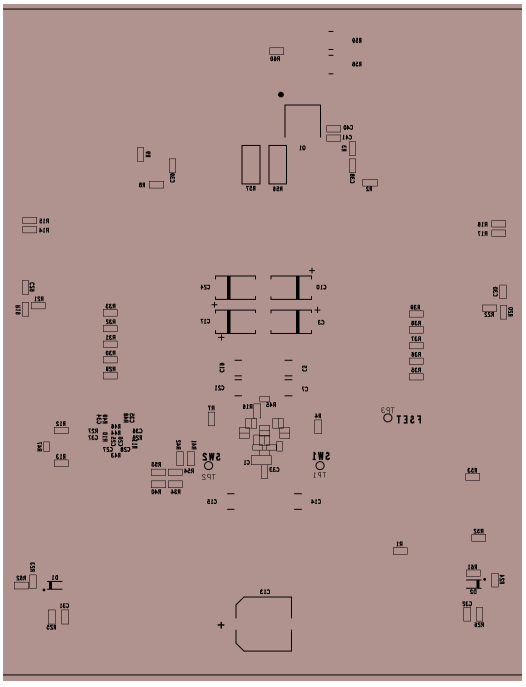


Figure 27: EVB PCB Silkscreen Bottom

MxL7213EVB Bill of Materials

Table 9: EVB Bill of Materials

Item	Qty	Reference Designator	Value	Tolerance	Description	Man Part
1	1	C1	4.7µF	10%	CAP CER 4.7UF 16V 10% X7R 0805	Wur 885
2	2	C2, C16	330µF	20%	CAP TANT POLY 330UF 6.3V 2917	Pan 6TP
3	2	C4, C18	100µF	10%	CAP CER 100UF 6.3V 20% X5R 1210	Wur 885
4	4	C11, C12, C14, C15	22µF	10%	CAP CER 22UF 10% 25V X5R 1210	Wur 885
5	1	C13	150µF	20%	CAP ALUM POLY 150UF 20% 25V SMD	Nich UCD
6	1	C26	DNP		CAP CER 22PF 50V COG/NPO	Yage CC0
7	1	C36	47pF		CAP CER 47PF 50V COG/NPO	KEM C04
8	1	C37	33pF		CAP CER 33PF 50V COG/NPO	Yage CC0
9	2	C29, C30	0.1µF	10%	CAP CER 0.1UF 10% 25V X7R 0603	Wur 885
10	5	C33, C38, C39, C40, C41	1µF	10%	CAP CER 1UF +/-10% 16V X7R 0603	Wur 885
11	9	J1, J2, J22, J23, J24, J27, J28, J58, J59	HEADER_1X2_2.54mm_M		HDR, 2.54mm Single Row/Male 1X2 GOLD	Wur 613
12	4	J3, J29, J30, J45	HEADER_1X3_2.54mm_M		HDR, 2.54mm Single Row/Male 1X3 GOLD	Wur 613
13	18	J4, J7, J10, J12, J15, J18, J46, J47, J48, J49, J50, J51, J52, J53, J54, J55, J60, J61	HEADER_1X1_2.54mm_M		HDR, Single Pin/Male 1X1 GOLD	Wur 613
14	4	J6, J8, J16, J17	KFH		Broaching Stud, KFH #10-32, Phosphor Bronze	Pen KFH

Table 9: EVB Bill of Materials (Continued)

Item	Qty	Reference Designator	Value	Tolerance	Description	Man Part
15	2	J9, J11			CONN. BANANA JACK	Keys 575-
16	3	J25, J26, J44	HEADER_2X3_0.1"		HDR, 0.1" Double Row/2x3	Wur 6130
17	1	Q1	SUD50N04		MOSFET N-CH 40V 14A TO-252	Vish SUD
18	4	R1, R12, R13, R60	10kΩ	1%	RES SMD10K OHM 1% 1/10W 0603	KOA ERJ
19	4	R2, R3, R8, R9	10Ω	1%	RES, Thick Film, 10 ohm, 1%, 1/10W, SMD, 0603	Vish CRC
20	6	R7, R34, R41, R54, R52, R53	0Ω		RES, Thick Film, 0 ohm, 1%, 1/10W, 50V, SMD, 0603	Yage RC0
21	1	R48	13.3kΩ	1%	RES SMD 13.3K OHM 1% 1/10W 0402	Pana ERJ
22	1	R49	8.25kΩ	1%	RES SMD 8.25K OHM 1% 1/10W 0402	Pana ERJ
23	2	R14, R15	6.04kΩ	1%	RES SMD 6.04K OHM 1% 1/10W 0603	Pana ERJ
24	1	R16	191kΩ	1%	RES SMD 191K OHM 1% 1/10W 0603	Yage RC0
25	4	R19, R20, R21, R22	60.4kΩ	1%	RES SMD 60.4K OHM 1% 1/10W 0603	Pana ERJ
26	1	R56	0Ω		Resistor 0 Ohm Jumper 1W, SMD	Vish CRC
27	1	R58	0.01Ω	1%	RES 0.01 OHM 2W 1% 2512 SMD	Roh PMF
28	1	U1	MxL7213		MXL IC MXL7213	Max MXL Max MXL

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