ENVISIONING • EMPOWERING • EXCELLING

MxL8321x

High Performance RS-485/422 Transceivers with Extended IEC ESD and EFT Protection

EVK User Manual

Revision History

Document No.	Release Date	Change Description
028UMR00	May 3, 2024	Initial release.

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Introduction

This document is used for the evaluation kits (EVKs) of the MxL83211, MxL83212, and MxL83214 (MxL8321x) devices. These EVKs provide a platform to evaluate the features and performance of the MxL8321x.

For more information about the MxL8321x devices, refer to the *MxL8321x Data Sheet* (274DS).

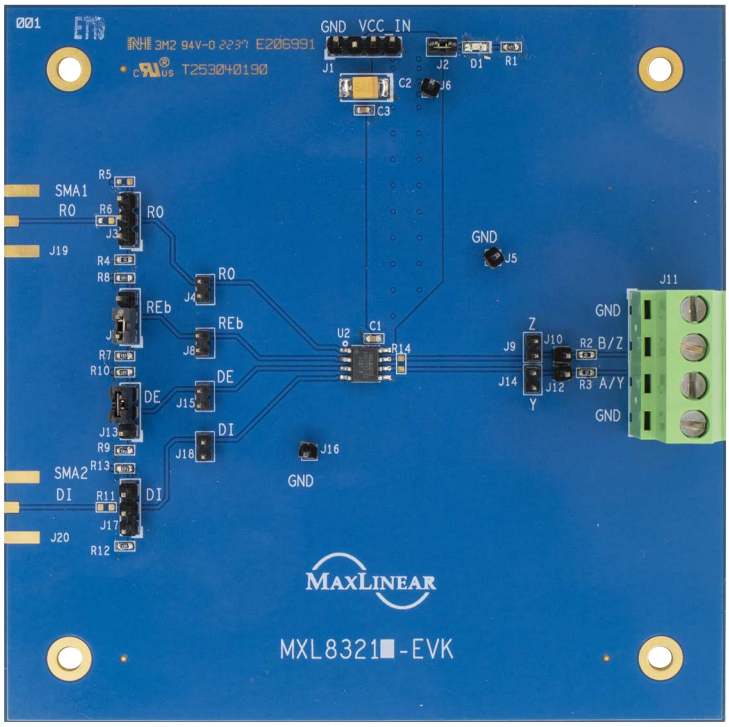


Figure 1: Top View of the MxL8321x EVK

Ordering Information

The following table lists the ordering part numbers for the evaluation kits.

Table 1: EVK Ordering Part Numbers

EVK Part Number	Description
MXL83211E-ADA-EVK-1	MxL83211 evaluation kit
MXL83212E-ADA-EVK-1	MxL83212 evaluation kit
MXL83214E-ADA-EVK-1	MxL83214 evaluation kit

Evaluation Kit Overview

The following figure shows the pin configuration and logic diagram of the MxL8321x device.

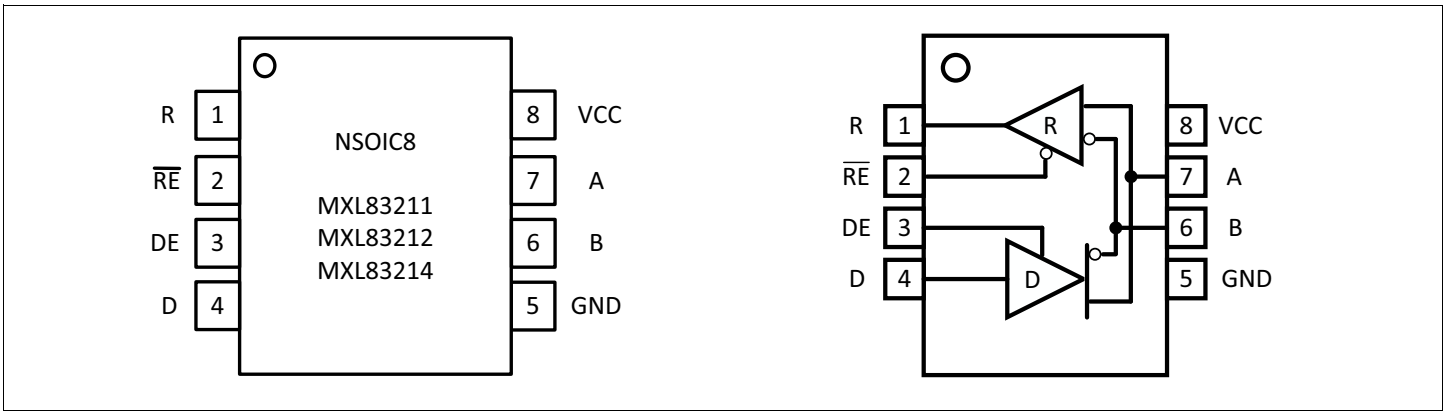


Figure 2: MxL8321x Half-Duplex Receiver

EVK Schematic

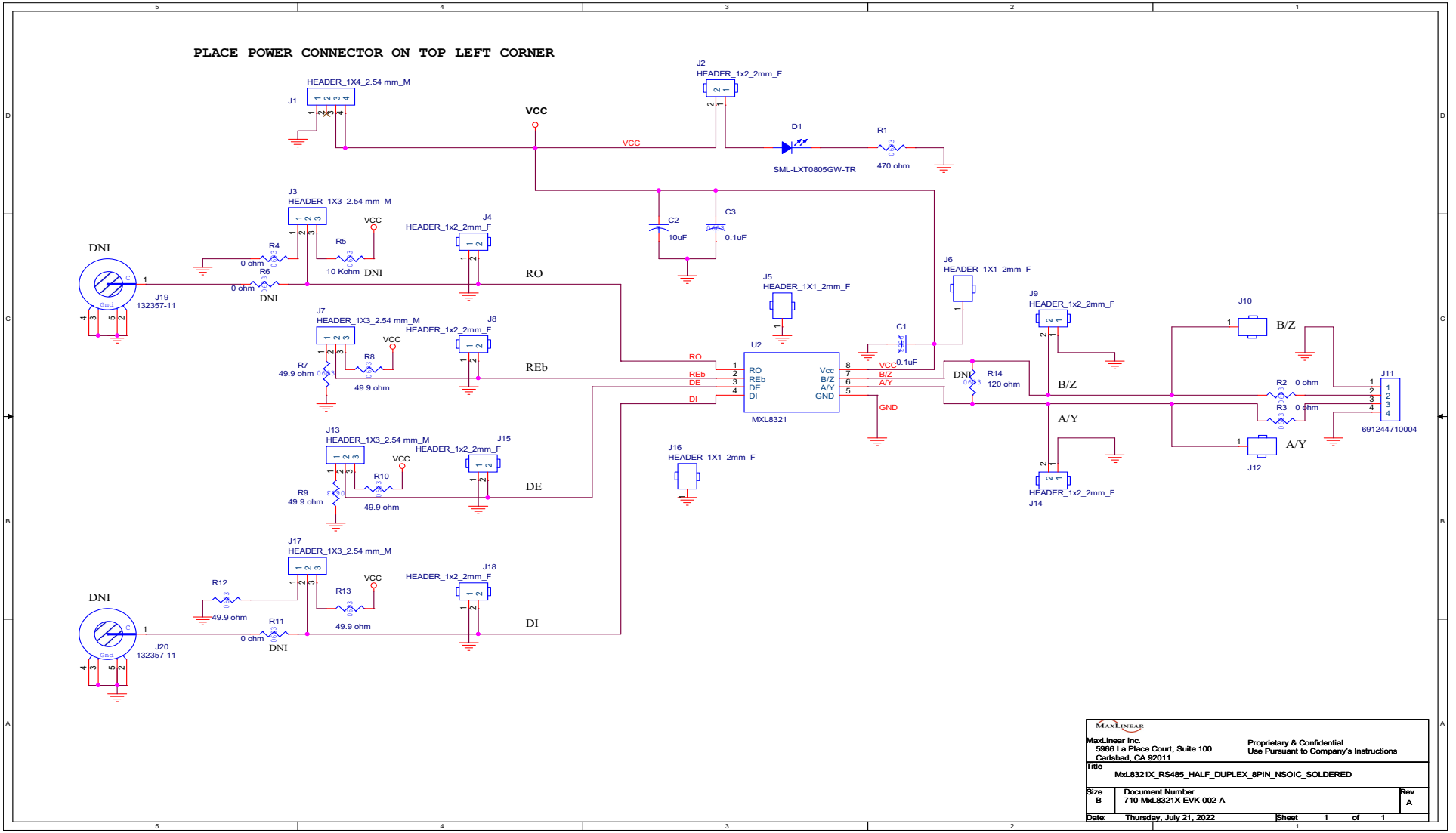


Figure 3: MxL8321x EVK Schematic

EVK PCB Layers (NSOIC8 Package)

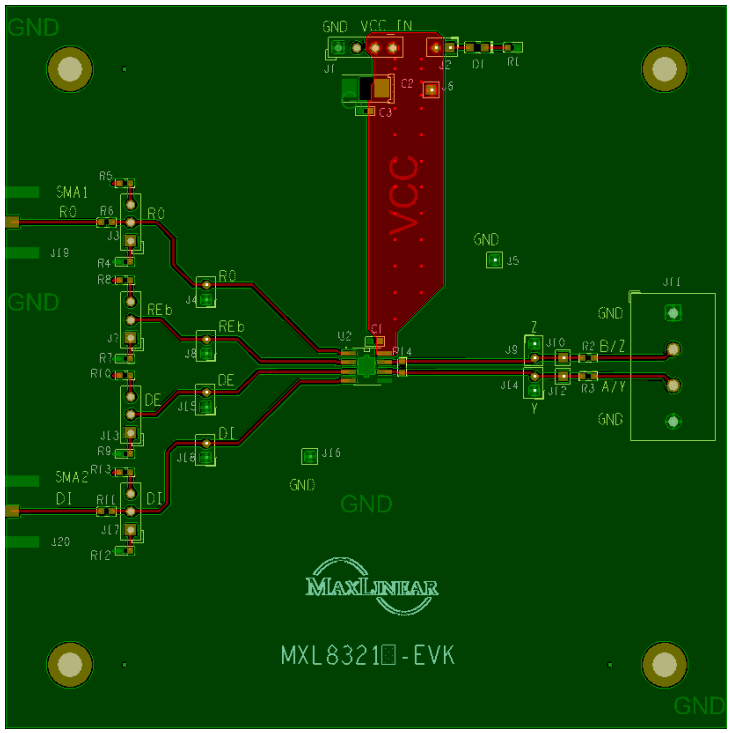


Figure 4: EVK PCB Layer 1—Top View

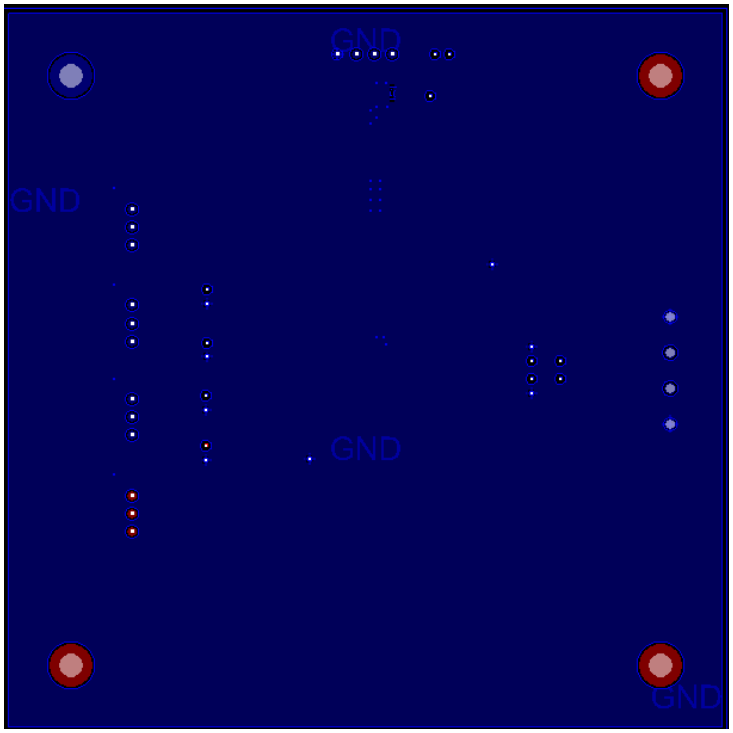


Figure 5: EVK PCB Layer 2—GND Plane

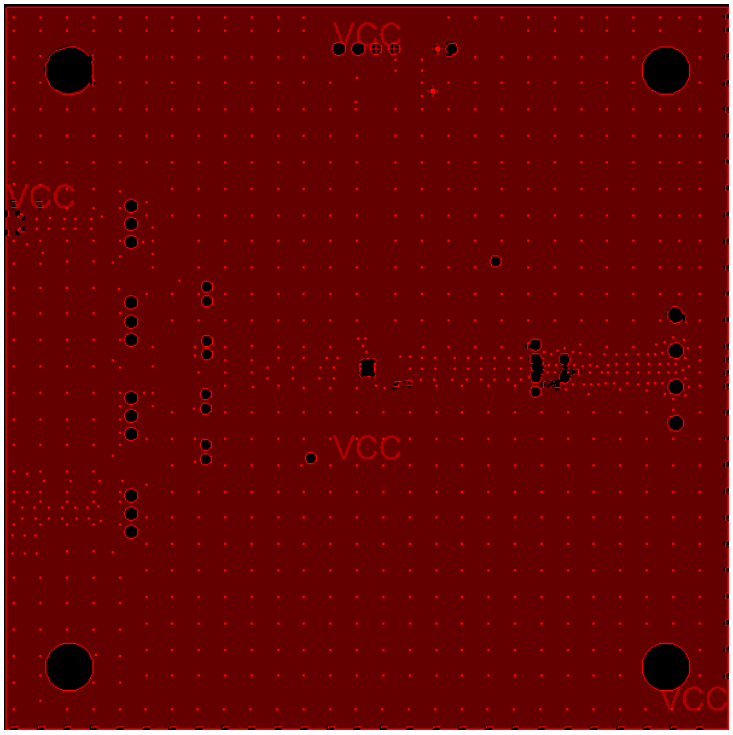


Figure 6: EVK PCB Layer 3—Power Plane

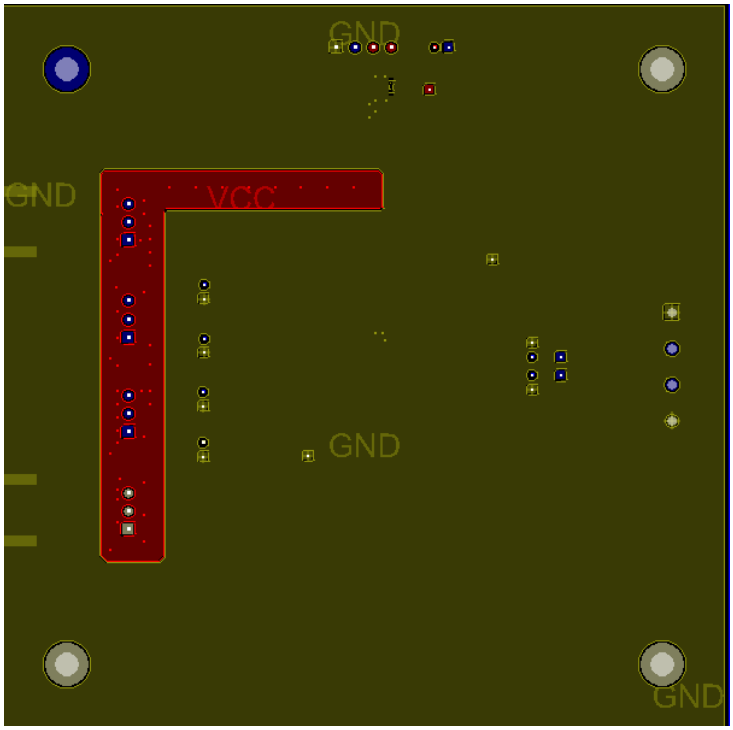


Figure 7: EVK PCB Layer 4—Bottom View

EVK Bill of Materials

Table 2: EVK Bill of Materials

Item	Qty	Reference Designator	Manufacturer	Manufacturer Part Number
1	2	C1, C3	KEMET	C0603C104K5RAC7081, 0.1UF 50V, 0603 X7R
2	1	C2	AVX	478-5235-1-ND, TANTALUM, 10µF, 16V, 500mOhm, 2312
3	1	D1	Lumex Opto	67-1553-1-ND LED GREEN DEFUSED SMD, 0805
4	1	J1	Wurth Eletronics	613 004 111 21 CONN. HEADER 1X4, 2.54mm, 4PIN
5	7	J2, J4, J8, J9, J14, J15, J18	Wurth Eletronics	620 002 111 21 CONN.HEADER, 1X2, 2mm, 2PIN
6	4	J3, J7, J13, J17	Wurth Eletronics	613 003 111 21 CONN. HEADER 1X3, 2.54mm, 3PIN
7	5	J5, J6, J10, J12, J16	Wurth Eletronics	613 001 111 21 CONN.HEADER, 1X1, 2.54mm, 1PIN
8	1	J11	Wurth Eletronics	691 244 710 004 TERMINAL BLOCK, HORIZONT 4POS
9	2	J19(SMA1), J20(SMA2)	Amphenol RF	132357-11 CONN. SMA RCPT, 50 Ohm NOT STUFF
10	1	R1	Panasonic	ERJ-3EKF4700V RES SMD, 470 Ohm, 1%, 1/10W, 0603
11	3	R2, R3, R4	Panasonic	ERJ-3GEY0R00V RERS JUMPER, 0 Ohm, SMD,1/10W, 0603
12	1	R5	Panasonic	ERJ-3EKF1002V RES SMD, 10K Ohm, 1%, 1/10W, 0603 NOT STUFF
13	6	R7, R8, R9, R10, R12, R13	Panasonic	ERJ-3EKF49R9V RES SMD, 49.9 Ohm, 1%, 1/10W, 0603
14	1	R14	Panasonic	ERJ-H3EF1200V RES SMD, 120 Ohm, 1%, 1/8W, 0603 NOT STUFF
15	2	R6, R11	Panasonic	ERJ-3GEY0R00V RERS JUMPER, 0 Ohm, SMD,1/10W, 0603 NOT STUFF
16	1	U2	MaxLinear	MXL83211/MXL83212/MXL83214

EVK Setup and Configurations

The following table lists the header pin descriptions.

Table 3: EVK Header Pin Description

J1	J1-Pin 1	J1-Pin 2	J1-Pin 3	J1-Pin 4
Name 	GND	NC	V_{CC}[1]	V_{CC}[1]

1. V_{CC} = 3.0V to 5.5V.

The following table lists the header pin factory settings and descriptions. For a complete view of the MxL8321x EVK, see Figure 1 on page 1.

Table 4: EVK Header Pin Description and Default Settings

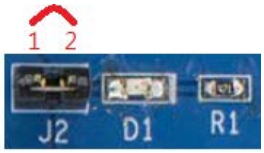
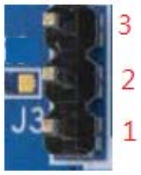
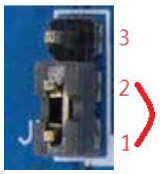
Header	Factory Setting	Description
J2 	Jumper 1-2	Enables power LED.
J3 	Header 3 pins	■ J3.1: GND. ■ J3.2: Receiver output (RO). ■ J3.3: V_{CC}.
J4 	Header 2 pins	■ J4.1: RO (test point). ■ J4.2: GND.
J7 	Jumper 1-2	Enables receiver, REb = GND.
J8 	Header 2 pins	■ J8.1: REb (test point). ■ J8.2: GND.

Table 4: EVK Header Pin Description and Default Settings (Continued)

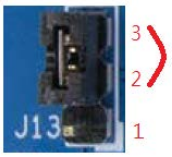
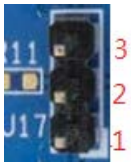
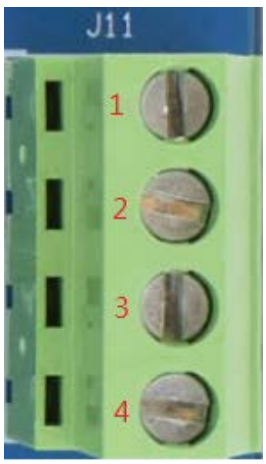
Header	Factory Setting	Description
J13 	Jumper 2-3	Enables driver, DE = V_{CC}.
J15 	Header 2 pins	■ J15.1: DE (test point). ■ J15.2: GND.
J17 	Header 3 pins	■ J17.1: GND. ■ J17.2: Driver input (DI). ■ J17.3: V_{CC}.
J18 	Header 2 pins	■ J18.1: DI (test point). ■ J18.2: GND.
J9 	Header 2 pins	■ J9.1: B inverting input (test point). ■ J9.2: GND.
J14 	Header 2 pins	■ J14.1: A non-inverting input (test point). ■ J14.2: GND.
J11 	4-pin terminal block	■ J11.1: GND. ■ J11.2: B inverting input. ■ J11.3: A non-inverting input. ■ J11.4: GND.

Table 4: EVK Header Pin Description and Default Settings (Continued)

Header	Factory Setting	Description
J10 	Header 1 pin	J10.1: B inverting input (test point).
J12 	Header 1 pin	J12.1: A non-inverting input (test point).
J6 	Header 1 pin	J6.1: GND.
J5 	Header 1 pin	J5.1: GND.
J16 	Header 1 pin	J16.1: GND.

Layout Recommendations

The following are recommended layout practices that are already applied in the EVK:

- Application of bypass capacitors of at least 100nF as close as possible to the V_{CC} terminal of the device.

  Note: If the supply source is generated from a linear power supply or regulator, MaxLinear recommends that you use additional 10µF (C2) and 100nF (C3) ceramic capacitors.

- Use of at least two vias for the V_{CC} and ground connections of the bypass capacitors to minimize effective via inductance.
- When possible, use of a V_{CC} and ground plane to provide low-inductance traces and signal path.

For more information and tips on layout, refer to the *RS-232 and RS-485 PCB Layout Application Note* (293AN).

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