ENVISIONING • EMPOWERING • EXCELLING

MxL83411
Quad Receiver
EVK User Manual

Revision History

Document No.	Release Date	Change Description
029UMR00	November 2, 2023	Initial release.

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Introduction

This document is used for the evaluation kits (EVKs) of the MxL83411 device. These EVKs provide a platform to evaluate the features and performance of the MxL83411.

EVK Setup and Pre-configuration

- The EVK is pre-configured for global enable with RE = V_{CC} and REb = GND. All four receiver outputs are enabled simultaneously in this configuration.
- Apply V_{CC} = 5.0V bench power supply to header J1 at pin 2 (J1.2) or pin3(J1.3).
- Apply GND connection to J1 at pin 1 (J1.1)
- J14 and J16 are GND probe points on the EVK.
- When the power V_{CC} is applied at header J1, the LED at location D1 is ON.
- Screw terminal block J5, J30, J26, and J18 are inputs to receiver channel 1, channel 2, channel 3, and channel 4 respectively.
- Apply differential signals at J5, J30, J26, and J18. Monitor receiver outputs at J7, J10, J23, and J20.
- Figure 4 on page 4 shows the schematic of the EVK.

For more information about the MxL83411 device, refer to the *MxL83411 Data Sheet* (281DS).

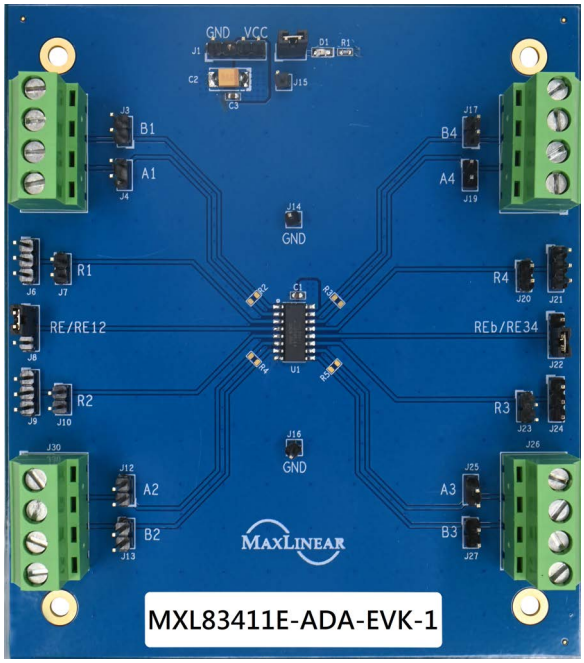


Figure 1: Top View of the MxL83411 (NSOIC16) EVK

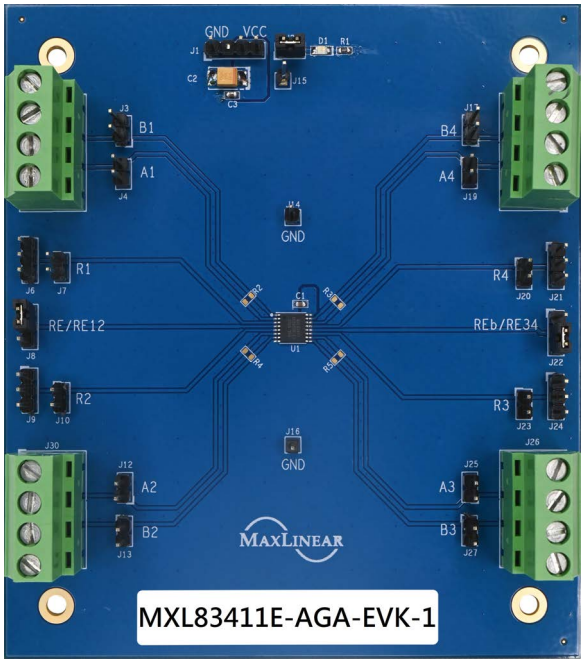


Figure 2: Top View of the MxL83411 (TSSOP16) EVK

Ordering Information

The following table lists the ordering part number for this evaluation kit.

Table 1: EVK Ordering Part Number

EVK Part Number	Description
MXL83411E-ADA-EVK-1	MxL83411 Evaluation Kit NSOIC16
MXL83411E-AGA-EVK-1	MxL83411 Evaluation Kit TSSOP16

Evaluation Kit Overview

The following figures show the pin configuration and logic diagram of the MxL83411 device.

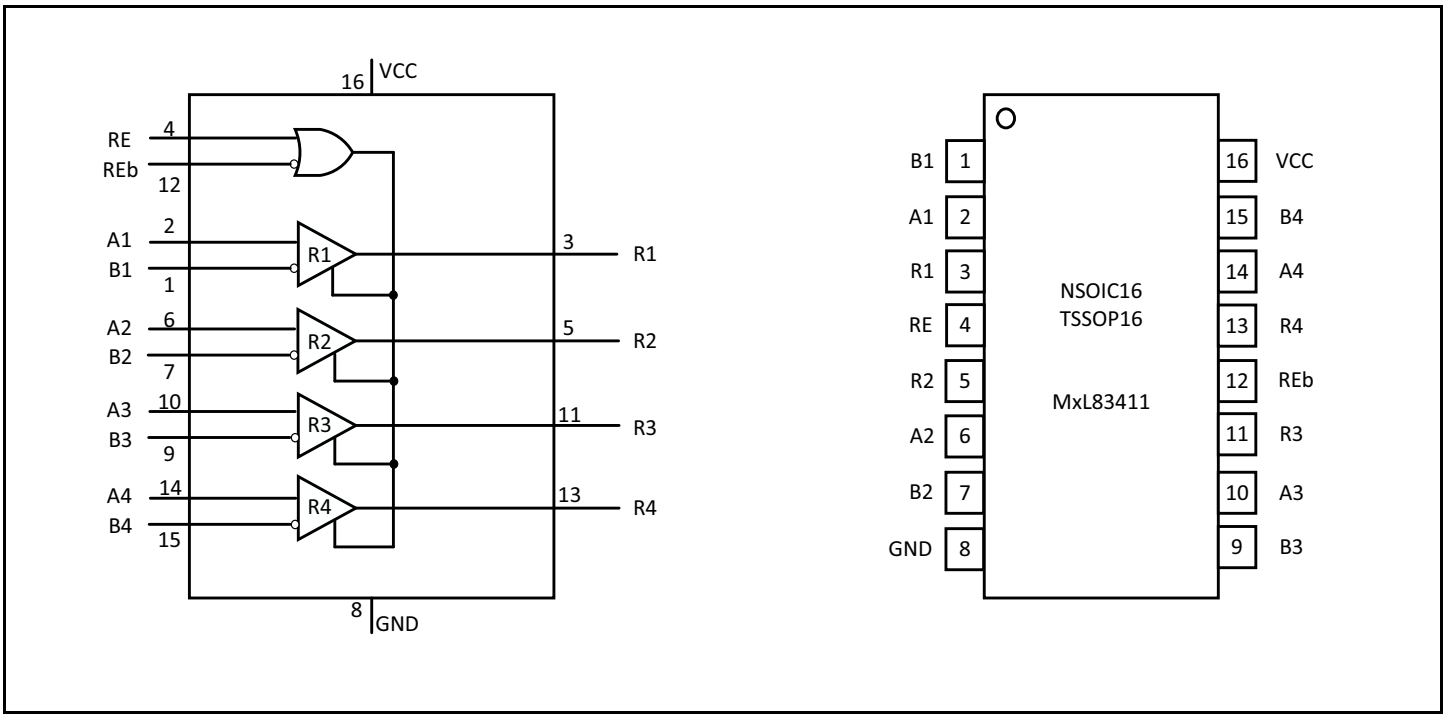


Figure 3: MxL83411 Quad Receiver

EVK Schematic

The following figure show the EVK schematic design of the MxL83411 device.

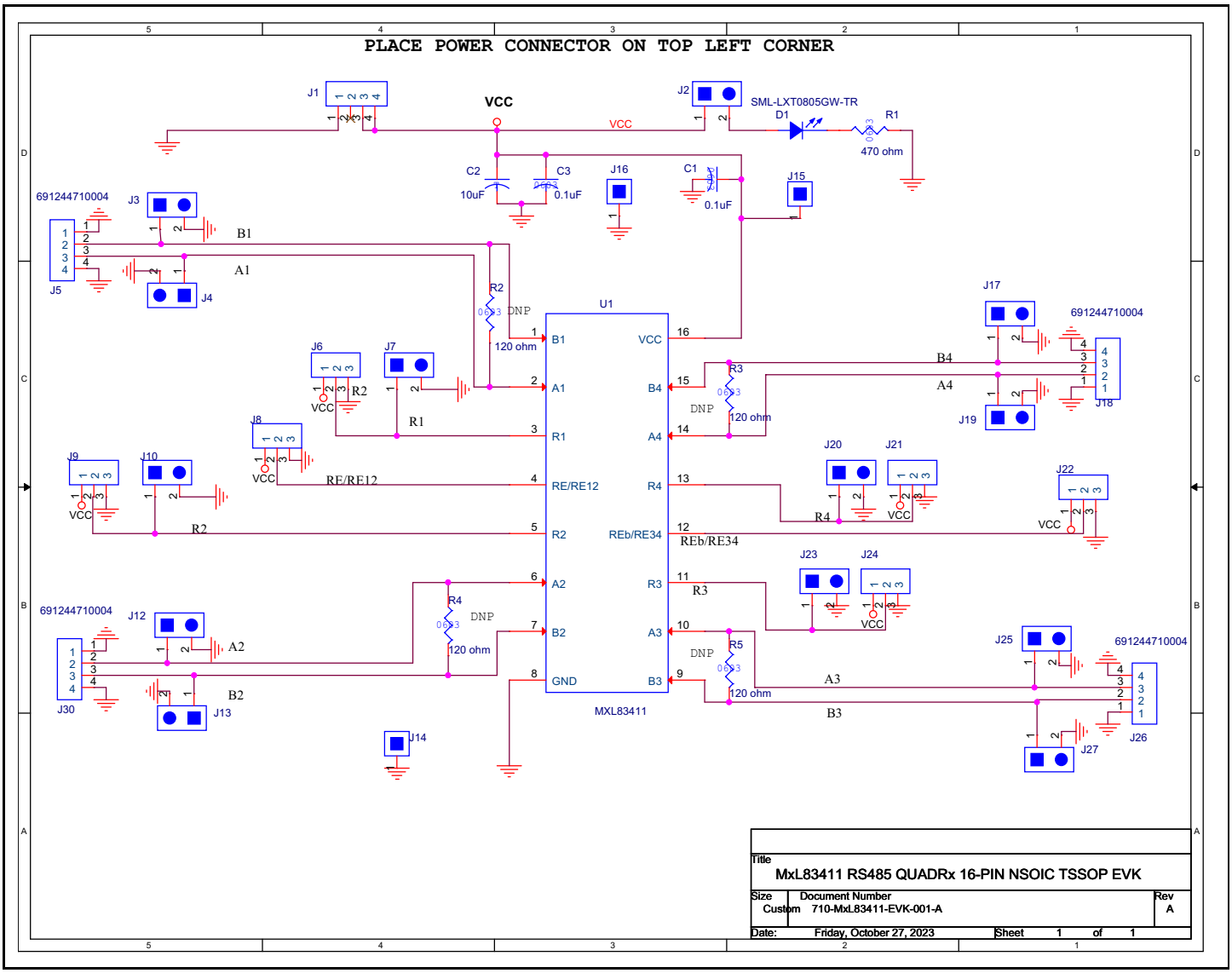


Figure 4: MxL83411 EVK Schematic

EVK PCB Layers (NSOIC16 Package)

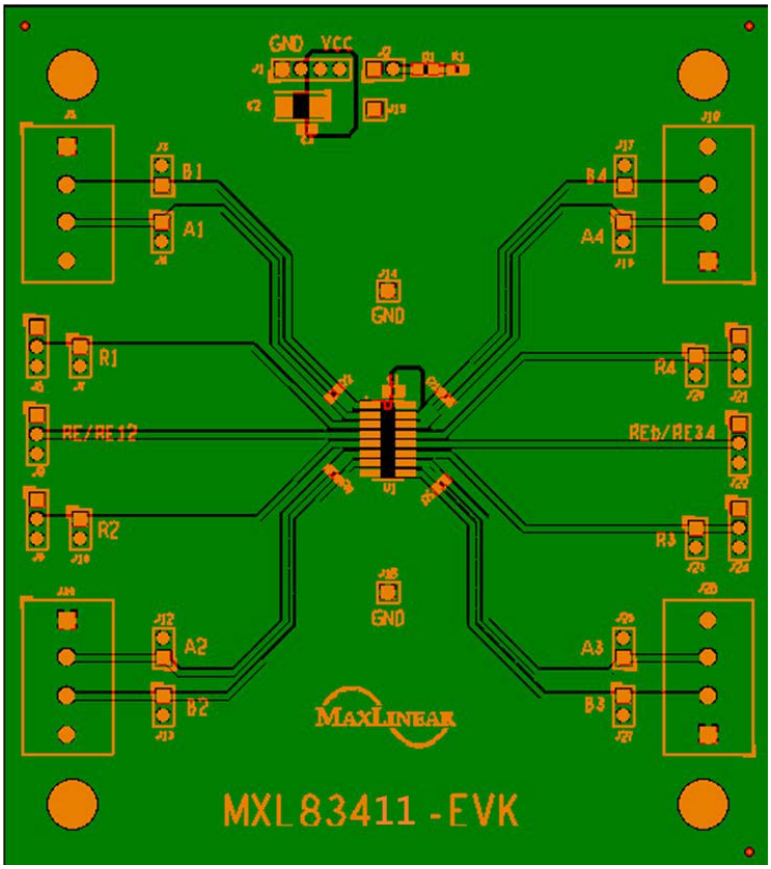


Figure 5: EVK PCB Layer 1—Top View (NSOIC16)

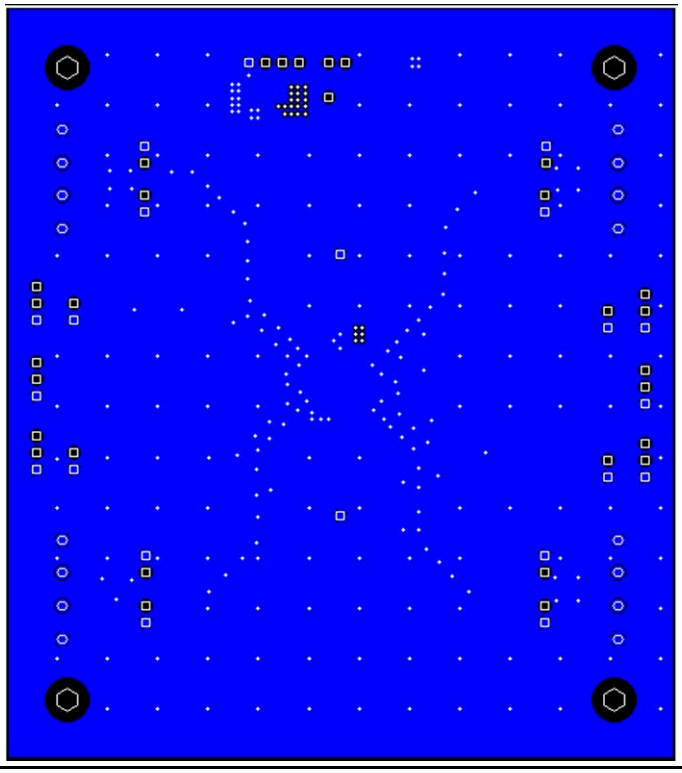


Figure 6: EVK PCB Layer 2—GND Plane (NSOIC16)

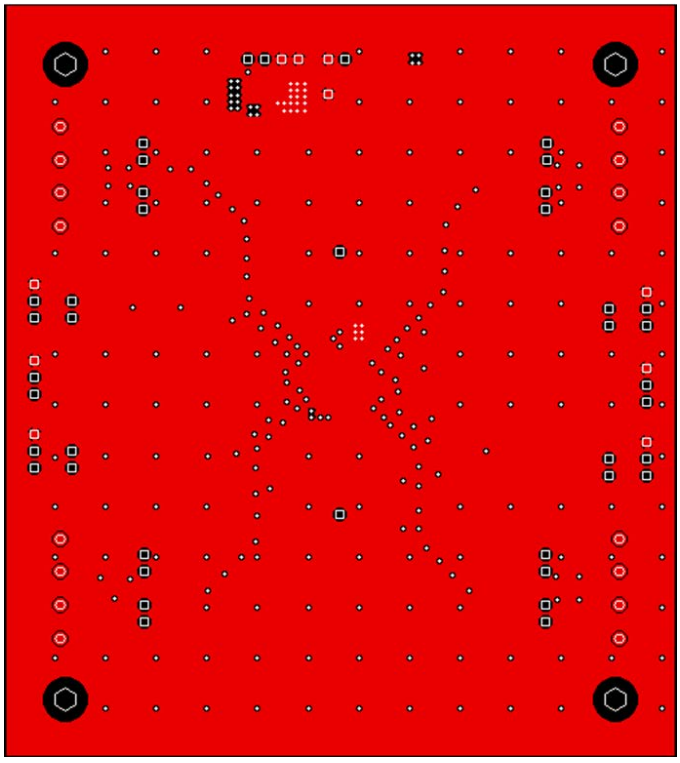


Figure 7: EVK PCB Layer 3—Power Plane (NSOIC16)

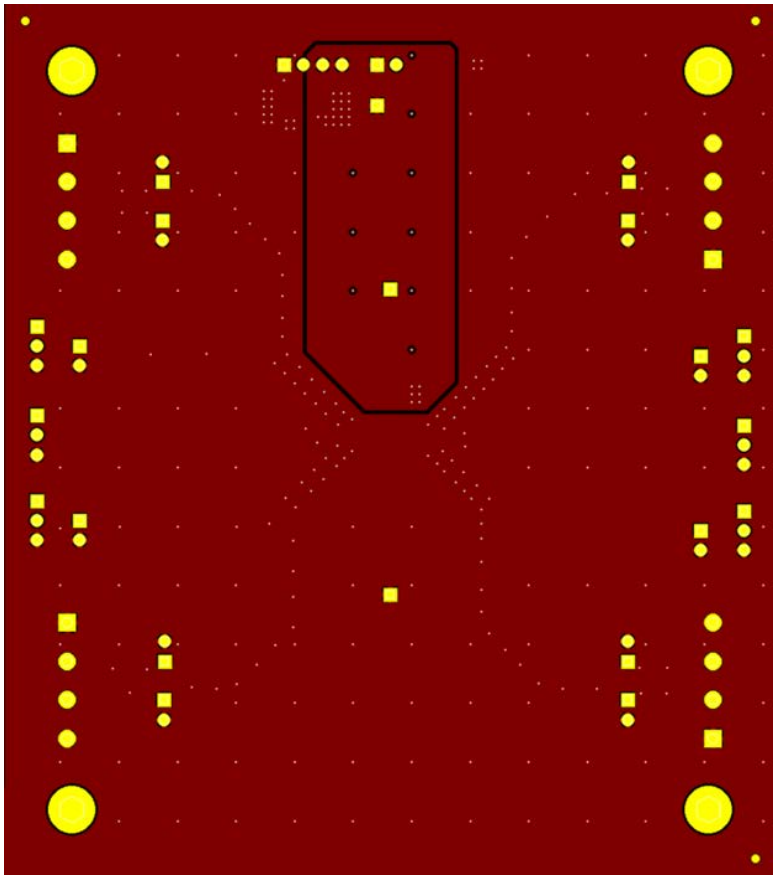


Figure 8: EVK PCB Layer 4—Bottom View (NSOIC16)

EVK PCB Layers (TSSOP16 Package)

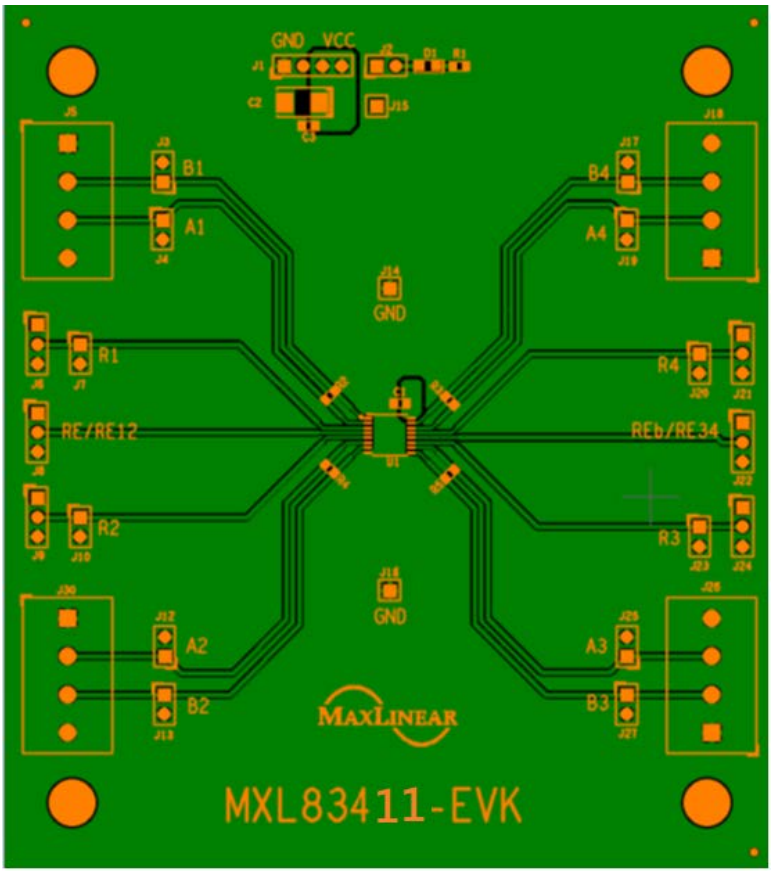


Figure 9: EVK PCB Layer 1—Top View (TSSOP16)

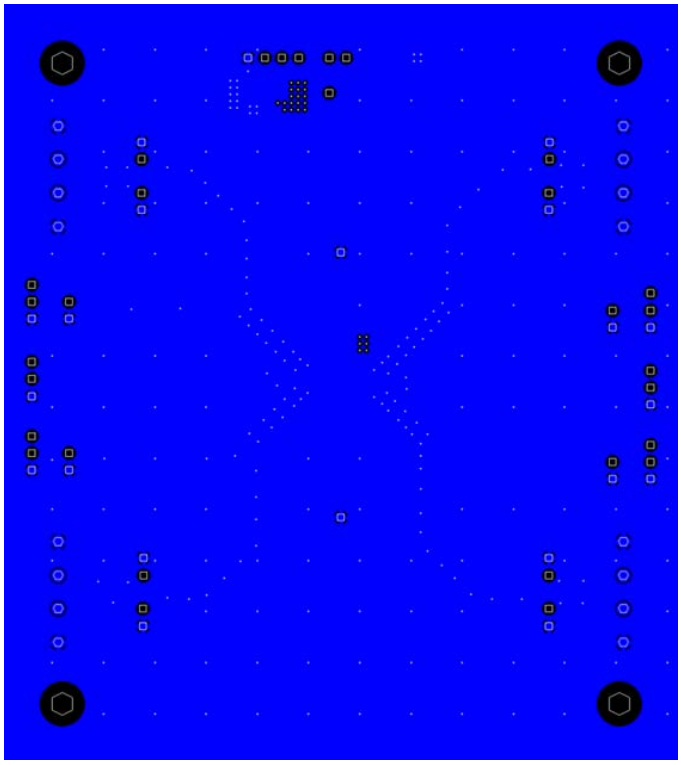


Figure 10: EVK PCB Layer 2—GND Plane (TSSOP16)

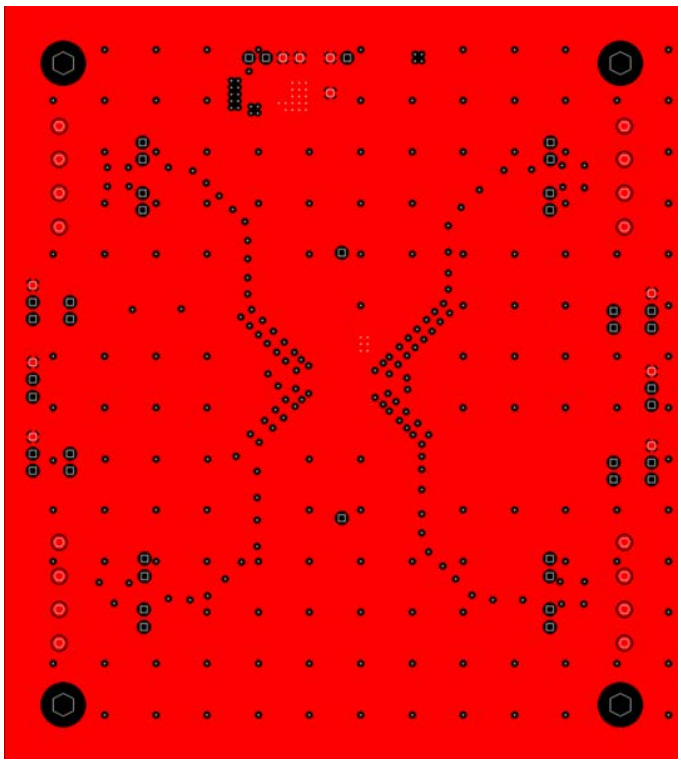


Figure 11: EVK PCB Layer 3—Power Plane (TSSOP16)

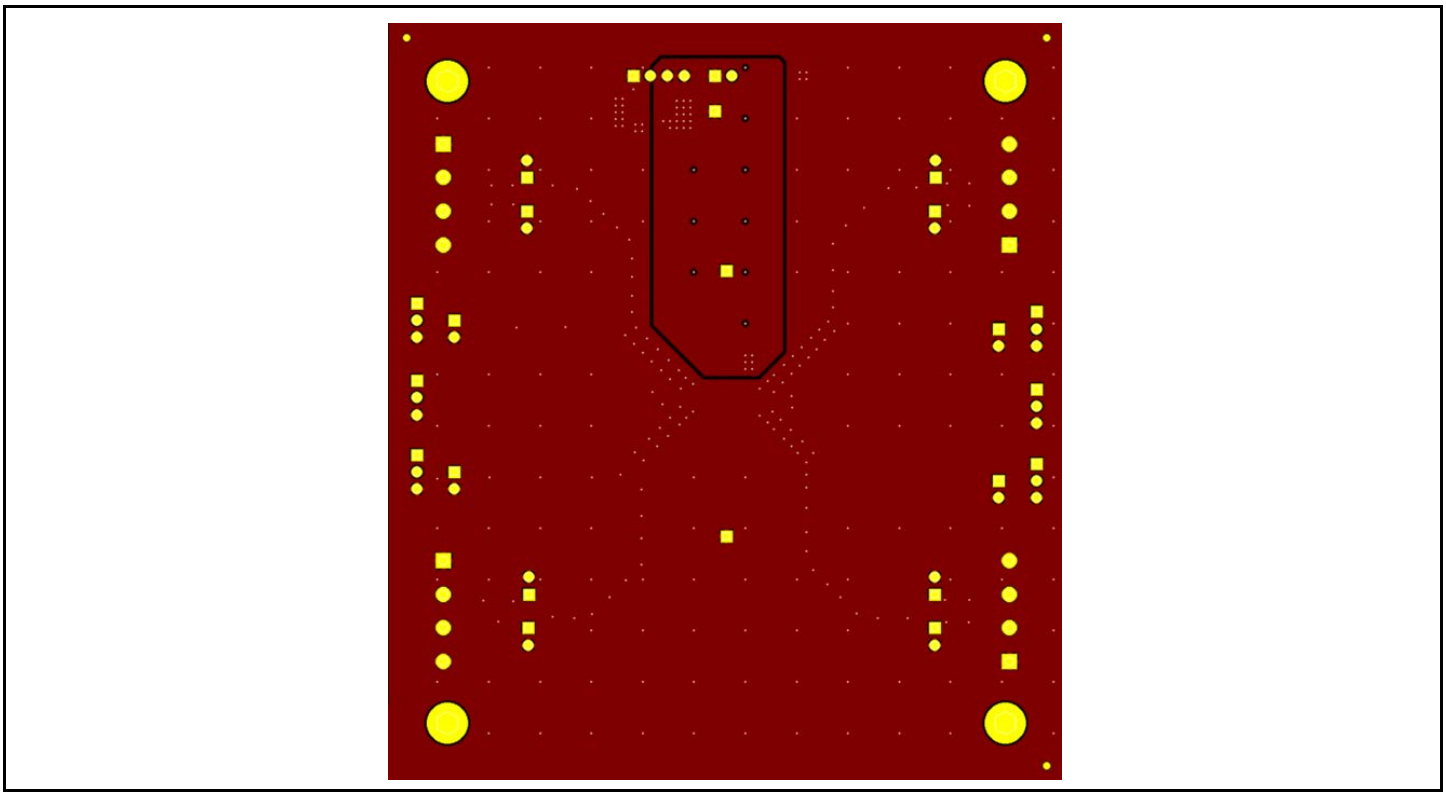


Figure 12: EVK PCB Layer 4—Bottom View (TSSOP16)

EVK Bill of Material (BOM)

Table 2: Bill of Materials for NSOIC16

Item	Quantity	Reference	Manufacturer	Part
1	2	C1, C3	Kemet	C0603C104K5RAC7081, 0.1UF 50V, 0603 X7R
2	1	C2	AVX	478-5235-1-ND, TANTALUM, 10µF, 16V, 500mΩ, 2312
3	1	D1	Lumex	67-1553-1-ND LED GREEN DEFUSED SMD, 0805
4	1	J1	Samtec	TSW-104-07-G-S CONN. HEADER 1×4, 2.54mm, 4PIN
5	13	J2, J3, J4, J7, J10, J12, J13, J17, J19, J20, J23, J25, J27	Samtec	TSW-102-07-G-S CONN.HEADER, 1×2, 2mm, 2PIN
6	4	J5, J18, J26, J30	Wurth Electronics	732 691 244 710 004 5.00 MM terminal block
7	6	J6, J8, J9, J21, J22, J24	Samtec	TSW-103-07-G-S CONN.HEADER, 1×3, 2mm, 1PIN
8	3	J14, J15, J16	Samtec	TSW-101-07-G-S CONN.HEADER, 1×1, 2mm, 1PIN
9	1	R1	Xicon	ERJ-3EKF4700V RES SMD, 470Ω, 1%, 1/10W, 0603
10	4	R2, R3, R4, R5. Termination resistors. Optional, not stuff by default.	Xicon	ERJ-3EKF1200V RES SMD, 120Ω, 1%, 1/10W, 0603
11	1	U1	MaxLinear	MXL83411E-ADA-R (NSOIC16)

Table 3: Bill of Materials for TSSOP16

Item	Quantity	Reference	Manufacturer	Part
1	2	C1, C3	Kemet	C0603C104K5RAC7081, 0.1UF 50V, 0603 X7R
2	1	C2	AVX	478-5235-1-ND, TANTALUM, 10µF, 16V, 500mΩ, 2312
3	1	D1	Lumex	67-1553-1-ND LED GREEN DEFUSED SMD, 0805
4	1	J1	Samtec	TSW-104-07-G-S CONN. HEADER 1×4, 2.54mm, 4PIN
5	13	J2, J3, J4, J7, J10, J12, J13, J17, J19, J20, J23, J25, J27	Samtec	TSW-102-07-G-S CONN.HEADER, 1×2, 2mm, 2PIN
6	4	J5, J18, J26, J30	Wurth Electronics	732 691 244 710 004 5.00 MM terminal block
7	6	J6, J8, J9, J21, J22, J24	Samtec	TSW-103-07-G-S CONN.HEADER, 1×3, 2mm, 1PIN
8	3	J14, J15, J16	Samtec	TSW-101-07-G-S CONN.HEADER, 1×1, 2mm, 1PIN
9	1	R1	Xicon	ERJ-3EKF4700V RES SMD, 470Ω, 1%, 1/10W, 0603
10	4	R2, R3, R4, R5. Termination resistors. Optional, not stuff by default.	Xicon	ERJ-3EKF1200V RES SMD, 120Ω, 1%, 1/10W, 0603
11	1	U1	MaxLinear	MXL83411E-AGA-R (TSSOP16)

Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should have a ceramic capacitor of at least 100nF located as close to the supply terminals (V_{CC}) as possible. If the supply source is generated from a linear power supply/regulator, MaxLinear recommends you to use additional 10µF (C2) and 100nF (C3) ceramic capacitors.

Table 4: EVK Header Pin Description

J1	J1-Pin 1	J1-Pin 2	J1-Pin 3	J1-Pin 4
Name 	GND	NC	V_{CC}	V_{CC}

Where V_{CC} = 3.0V to 5.5V

Table 5: EVK Header Pin Description and Default Settings

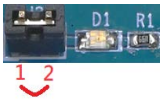
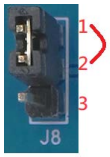
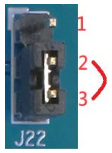
Header	Factory Setting	Description
J2 	Jumper 1-2	Enable power LED.
J8 	Jumper 1-2	Enable all receivers, RE = V_{CC}
J22 	Jumper 2-3	Enable all receivers, REb = GND.
R2, R3, R4, R5	Not stuff	Receiver termination resistor. Optional, not stuff by default.
J3 	Header 2 pins	■ J3.1: B1 inverting input (test point). ■ J3.2: GND.
J4 	Header 2 pins	■ J4.1: A1 non-inverting input (test point). ■ J4.2: GND.

Table 5: EVK Header Pin Description and Default Settings

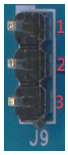
Header	Factory Setting	Description
J5 	4 Pins terminal block	■ J5.1: GND. ■ J5.2: B1 inverting input. ■ J5.3: A1 non-inverting input. ■ J5.4: GND.
J6 	Header 3pins	■ J6.1: V_{CC} ■ J6.2: R1 output. ■ J6.3: GND.
J7 	Header 2 pins	■ J7.1: R1 output (test point). ■ J7.2: GND.
J9 	Header 3pins	■ J9.1: V_{CC} ■ J9.2: R2 output. ■ J9.3: GND.
J10 	Header 2 pins	■ J10.1: R2 output (test point). ■ J10.2: GND.
J12 	Header 2 pins	■ J12.1: A2 non-inverting input (test point). ■ J12.2: GND.
J13 	Header 2 pins	■ J13.1: B2 inverting input (test point). ■ J13.2: GND.
J30 	4 Pins terminal block	■ J30.1: GND. ■ J30.2: A2 non-inverting input. ■ J30.3: B2 inverting input. ■ J30.4: GND.
J25 	Header 2 pins	■ J25.1: A3 non-inverting input (test point). ■ J25.2: GND.

Table 5: EVK Header Pin Description and Default Settings

Header	Factory Setting	Description
J27 	Header 2 pins	■ J27.1: B3 inverting input (test point). ■ J27.2: GND.
J26 	4 Pins terminal block	■ J26.1: GND. ■ J26.2: B3 inverting input. ■ J26.3: A3 non-inverting input. ■ J26.4: GND.
J23 	Header 2 pins	■ J23.1: R3 output (test point). ■ J23.2: GND.
J24 	Header 3pins	■ J24.1: V_{CC} ■ J24.2: R3 output. ■ J24.3: GND.
J20 	Header 2 pins	■ J20.1: R4 output (test point). ■ J20.2: GND.
J21 	Header 3 pins	■ J21.1: V_{CC} ■ J21.2: R4 output. ■ J21.3: GND
J19 	Header 2 pins	■ J17.1: B4 inverting input (test point). ■ J17.2: GND.
J19 	Header 2 pins	■ J19.1: A4 non-inverting input (test point). ■ J19.2: GND.

Table 5: EVK Header Pin Description and Default Settings

Header	Factory Setting	Description
J18 	4 Pins terminal block	■ J18.1: GND. ■ J18.2: A4 non-inverting input. ■ J18.3: B4 inverting input. ■ J18.4: GND.
J14 	Header 1 pins	J14.1: GND
J15 	Header 1 pins	J15.1: V_{CC}
J16 	Header 1 pins	J16.1: GND

The MxL83411 device offers a global enable configuration.

All four receiver outputs are enabled simultaneously when RE = V_{CC} or REb = GND.

When RE = GND and REb = V_{CC}, all four receiver outputs are in high impedance state

Layout Recommendations

- Apply bypass capacitors of at least 100nF as close as possible to the V_{CC} terminal of device.
- Use at least two vias for V_{CC} and ground connections of the bypass capacitors to minimize the effective via-inductance.
- When possible, use V_{CC} and the ground plane to provide low-inductance traces and signal path.

For additional layout tips, refer to the *RS-232 and RS-485 PCB Layout Application Note* (293AN).

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