

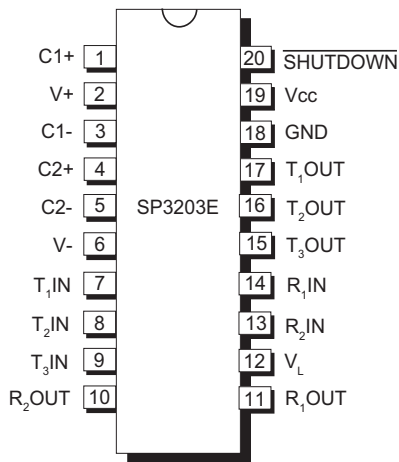


**SP3203E**

## 3V RS-232 Serial Transceiver with Logic Selector and 15kV ESD Protection

### FEATURES

- 3 Driver / 2 Receiver Architecture
- Logic selector function ( $V_L$ ) sets TTL input/output levels for mixed logic systems
- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- Interoperable with EIA/TIA-232 and adheres to EIA/TIA-562 down to a +2.7V power source
- Minimum 250Kbps data rate under load
- Regulated Charge Pump Yields Stable RS-232 Outputs Regardless of  $V_{CC}$  Variations
- ESD Specifications:
  - ±15KV Human Body Model
  - ±15KV IEC61000-4-2 Air Discharge
  - ±8KV IEC61000-4-2 Contact Discharge
- Applications
  - Palmtops
  - Cell phone Data Cables
  - PDA's



*Now Available in Lead Free Packaging*

### DESCRIPTION

The **SP3203E** provides a RS-232 transceiver solution for portable and hand-held applications such as palmtops, PDA's and cell phones. The **SP3203E** uses an internal high-efficiency, charge-pump power supply that requires only 0.1 $\mu$ F capacitors during 3.3V operation. This charge pump and **Exar's** driver architecture allow the **SP3203E** to deliver compliant RS-232 performance from a single power supply ranging from +3.0V to +5.5V.

The **SP3203E** is a 3-driver/2-receiver device, with a unique  $V_L$  pin to program the TTL input and output logic levels to allow inter operation in mixed-logic voltage systems such as PDA's and cell phones. Receiver outputs will not exceed  $V_L$  for  $V_{OH}$  and transmitter input logic levels are scaled by the magnitude of the  $V_L$  input.

## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V <sub>CC</sub> .....	-0.3V to +6.0V
V+ (NOTE 1).....	-0.3V to +7.0V
V- (NOTE 1).....	+0.3V to -7.0V
V+ +  V-  (NOTE 1).....	+13V
I <sub>CC</sub> (DC V <sub>CC</sub> or GND current).....	±100mA
<b>Input Voltages</b>	
TxIN, SHUTDOWN .....	-0.3V to V <sub>L</sub> +0.3V
RxIN.....	±25V

### Output Voltages

TxOUT.....	±13.2V
RxOUT, .....	-0.3V to (V <sub>L</sub> + 0.3V)

### Short-Circuit Duration

TxOUT.....	Continuous
Storage Temperature.....	-65°C to +150°C

### Power Dissipation per package

20-pin TSSOP (derate 7.0mW/°C above +70°C..560mW)

**NOTE 1:** V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

## ELECTRICAL CHARACTERISTICS

V<sub>CC</sub> = V<sub>L</sub> = +3.0V to +5.5V, C1 - C4 = 0.1μF, tested at +3.3V +/-10%, C1 = 0.047μF, C2 - C4 = 0.33μF, tested at +5.0V +/-10%, T<sub>AMB</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at V<sub>CC</sub> = V<sub>L</sub> = 3.3V, T<sub>A</sub> = +25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS	
<b>DC CHARACTERISTICS</b> (V <sub>CC</sub> = +3.3V or +5V, T <sub>A</sub> = +25°C)						
Supply Current		0.3	1	mA	SHUTDOWN = V <sub>CC</sub> , No Load	
Supply Current, Shutdown		1.0	10.0	μA	SHUTDOWN = GND	
<b>LOGIC INPUTS</b>						
Input Logic Threshold Low			0.8	V	TxIN, SHUTDOWN	V <sub>L</sub> = 3.3V or 5.0V
			0.6	V		V <sub>L</sub> = 2.5V
Input Logic Threshold High	2.4			V	TxIN, SHUTDOWN	V <sub>L</sub> = 5.0V
	2.0					V <sub>L</sub> = 3.3V
	1.4					V <sub>L</sub> = 2.5V
		0.9				V <sub>L</sub> = 1.8V
Transmitter Input Hysteresis		0.5		V		
Input Leakage Current		+/-0.01	+/-1.0	μA	TxIN, SHUTDOWN	
<b>RECEIVER OUTPUTS</b>						
Output Leakage Current		+/-0.05	+/-10	μA	RxOUT, receivers disabled	
Output Voltage LOW			0.4	V	I <sub>OUT</sub> = 1.6mA	
Output Voltage HIGH	V <sub>L</sub> - 0.6	V <sub>L</sub> - 0.1		V	I <sub>OUT</sub> = -1.0mA	

## ELECTRICAL CHARACTERISTICS

$V_{CC} = V_L = +3.0V$  to  $+5.5V$ ,  $C1 - C4 = 0.1\mu F$ , tested at  $+3.3V \pm 10\%$ ,  $C1 = 0.047\mu F$ ,  $C2 - C4 = 0.33\mu F$ , tested at  $+5.0V \pm 10\%$ ,  $T_{AMB} = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{CC} = V_L = 3.3V$ ,  $T_A = +25^\circ C$ .

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>RECEIVER INPUTS</b>					
Input Voltage Range	-25		+25	V	
Input Threshold Low	0.8	1.5		V	$T_A = +25^\circ C$ $V_L = 5.0V$
	0.6	1.2		V	
Input Threshold High		1.8	2.4	V	$T_A = +25^\circ C$ $V_L = 5.0V$
		1.5	2.4	V	
Input Hysteresis		0.5		V	
Input Resistance	3	5	7	k $\Omega$	
<b>TRANSMITTER OUTPUTS</b>					
Output Voltage Swing	+/-5.0	+/-5.4		V	All transmitter outputs loaded with $3k\Omega$ to GND, $T_{AMB} = +25^\circ C$
Output Resistance	300	10M		$\Omega$	$V_{CC} = V_+ = V_- = 0V$ , $V_{out} = +/-2V$
Output Short-Circuit Current			+/-60	mA	$V_{out} = 0V$
Output Leakage Current			+/-25	$\mu A$	$V_{CC} = 0V$ or $3.0V$ to $5.5V$ , $V_{out} = +/-12V$ , Driver disabled
<b>ESD PROTECTION</b>					
RxIN, TxOUT		+/-15		kV	Human Body Model
		+/-15		kV	IEC 61000-4-2 Air Gap Discharge
		+/-8		kV	IEC 61000-4-2 Contact Discharge

## TIMING CHARACTERISTICS

Unless otherwise noted, the following specifications apply for  $V_{CC} = +3.0V$  to  $+5.5V$  with  $T_{AMB} = T_{MIN}$  to  $T_{MAX}$ . Typical values apply at  $V_{CC} = +3.3V$  or  $+5.0V$  and  $T_{AMB} = 25^{\circ}C$ .

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Maximum Data Rate	250			kbps	$R_L = 3k\Omega$ , $C_L = 1000pF$ , one transmitter switching
Receiver Propagation Delay, $t_{PHL}$		0.15		$\mu s$	Receiver input to Receiver output, $C_L = 150pF$
Receiver Propagation Delay, $t_{PLH}$		0.15			
Receiver Output Enable Time		200		ns	Normal Operation
Receiver Output Disable Time		200		ns	Normal Operation
Time To Exit Shutdown		100		$\mu s$	$ V_{TXOUT}  > 3.7V$
Transmitter Skew $ t_{PHL} - t_{PLH} $		100		ns	(Note 2)
Receiver Skew $ t_{PHL} - t_{PLH} $		50		ns	
Transition-Region Slew Rate	6		30	$V/\mu s$	$C_L = 150pF$ to $1000pF$  $V_{CC} = 3.3V$ , $T_{AMB} = 25^{\circ}C$ , $R_L = 3K\Omega$ to $7K\Omega$ , measurements taken from $-3.0V$ to $+3.0V$ or $+3.0V$ to $-3.0V$
	4		30		

Note 2. Transmitter skew is measured at the transmitter zero crosspoint.

TYPICAL OPERATING CIRCUIT

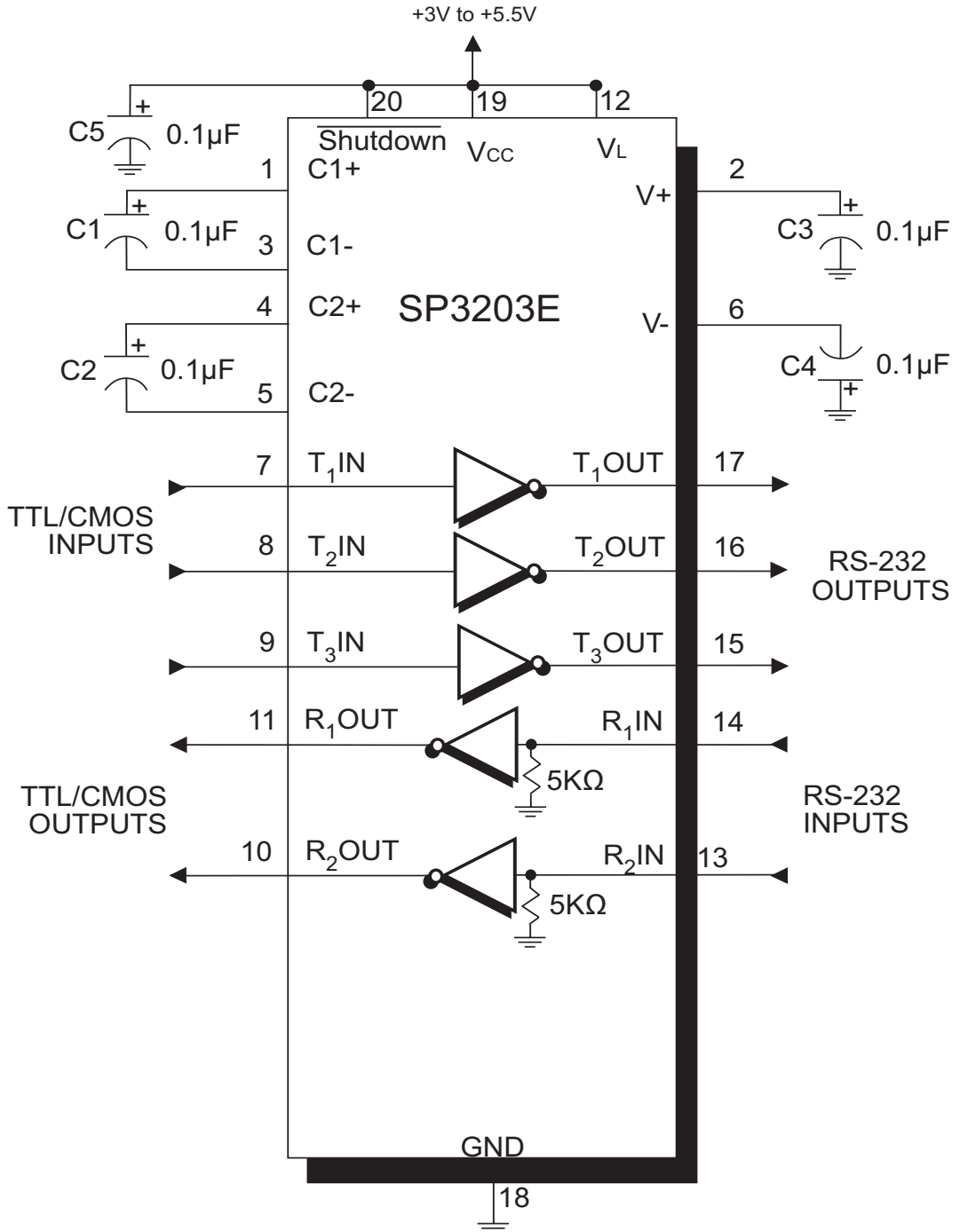


Figure 1. SP3203E Typical Operating Circuit

Name	Function	Pin #
C1+	Positive terminal of the voltage doubler charge-pump capacitor	1
V+	Regulated +5.5V output generated by charge pump	2
C1-	Negative terminal of the voltage doubler charge-pump capacitor	3
C2+	Positive terminal of the inverting charge-pump capacitor	4
C2-	Negative terminal of the inverting charge-pump capacitor	5
V-	Regulated -5.5V output generated by charge pump	6
T <sub>1</sub> IN	TTL/CMOS driver input	7
T <sub>2</sub> IN	TTL/CMOS driver input	8
T <sub>3</sub> IN	TTL/CMOS driver input	9
R <sub>2</sub> OUT	TTL/CMOS receiver output	10
R <sub>1</sub> OUT	TTL/CMOS receiver output	11
V <sub>L</sub>	Logic-Level Supply Voltage Selection	12
R <sub>2</sub> IN	RS-232 receiver input	13
R <sub>1</sub> IN	RS-232 receiver input	14
T <sub>3</sub> OUT	RS-232 Driver output	15
T <sub>2</sub> OUT	RS-232 Driver output	16
T <sub>1</sub> OUT	RS-232 Driver output	17
GND	Ground	18
Vcc	+3.0V to +5.5V supply voltage	19
<u>SHUTDOWN</u>	Apply logic LOW to shut down drivers and charge pump.	20

## DESCRIPTION

The **SP3203E** is a 3-driver/2-receiver device ideal for portable or handheld applications. The **SP3203E** transceivers meet the EIA/TIA-232 and ITU-TV.28/V.24 communication protocols and can be implemented in battery-powered, portable, or handheld applications such as notebook or palmtop computers, PDA's and cell phones. The **SP3203E** device features **Exar's** proprietary and patented (U.S.-- 5,306,954) on-board charge pump circuitry that generates  $\pm 5.5V$  RS-232 voltage levels from a single +3.0V to +5.5V power supply. The **SP3203E** can operate at a minimum data rate of 250kbps.

## THEORY OF OPERATION

The **SP3203E** is made up of four basic circuit blocks:

1. Drivers, 2. Receivers, 3. The Exar proprietary charge pump, and 4.  $V_L$  circuitry.

### Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to 5.0V EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is  $\pm 5.4V$  with no load and  $\pm 5V$  minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. These drivers comply with the EIA-TIA-232F and all previous RS-232 versions. The driver output stages are turned off (High Impedance) when the device is in shutdown mode.

The drivers can guarantee output data rates fully loaded with  $3k\Omega$  in parallel with  $1000pF$ , ensuring compatibility with PC-to-PC communication software.

The slew rate of the driver output is internally limited to a maximum of  $30V/\mu s$  in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from HIGH to LOW also meets the monotonicity requirements of the standard.

Figure 2 shows a loopback test circuit used to test the RS-232 Drivers. Figure 3 shows the test results with all drivers active at 120kbps with typical RS-232 loads in parallel with a  $1000pF$  capacitors. Figure 4 shows the test results where one driver was active at 250kbps and all three drivers loaded with an RS-232 receiver in parallel with a  $1000pF$  capacitor. The transmitter inputs do not have pull-up resistors. Connect unused inputs to ground or  $V_L$ .

### Receivers

The receivers convert  $\pm 5.0V$  EIA/TIA-232 levels to TTL or CMOS logic output levels. Receivers are disabled when in shutdown. The truth table logic of the SP3203E driver and receiver outputs can be found in Table 1.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of  $500mV$ . This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal  $5k\Omega$  pull-down resistor to ground will commit the output of the receiver to a HIGH state.

### Charge Pump

The charge pump is a patented design (U.S. 5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages of  $\pm 5.5V$  regardless of input voltage ( $V_{CC}$ ) over the +3.0V to +5.5V range. This is important to maintain compliant RS-232 levels regardless of power supply fluctuations.

Device: SP3203E			
SHUTDOWN	T <sub>x</sub> OUT	R <sub>x</sub> OUT	Charge Pump
0	High-Z	High-Z	Inactive
1	Active	Active	Active

Table 2. SHUTDOWN Truth Tables

(Note: When the device is shutdown, the SP3203E's charge pump is turned off and V<sup>+</sup> decays to V<sub>CC</sub>, V<sup>-</sup> is pulled to ground and the transmitter outputs are disabled as High Impedance.)

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pump is enabled. If the output voltages exceed a magnitude of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

### Phase 1

— V<sub>SS</sub> charge storage — During this phase of the clock cycle, the positive side of capacitors C<sub>1</sub> and C<sub>2</sub> are initially charged to V<sub>CC</sub>. C<sub>1</sub><sup>+</sup> is then switched to GND and the charge in C<sub>1</sub><sup>-</sup> is transferred to C<sub>2</sub><sup>-</sup>. Since C<sub>2</sub><sup>+</sup> is connected to V<sub>CC</sub>, the voltage potential across capacitor C<sub>2</sub> is now 2 times V<sub>CC</sub>.

### Phase 2

— V<sub>SS</sub> transfer — Phase two of the clock connects the negative terminal of C<sub>2</sub> to the V<sub>SS</sub> storage capacitor and the positive terminal of C<sub>2</sub> to GND. This transfers a negative generated voltage to C<sub>3</sub>. This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C<sub>3</sub>, the positive side of capacitor C<sub>1</sub> is switched to V<sub>CC</sub> and the negative side is connected to GND.

### Phase 3

— V<sub>DD</sub> charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C<sub>1</sub> produces -V<sub>CC</sub> in the negative terminal of C<sub>1</sub>, which is applied to the negative side of capacitor C<sub>2</sub>. Since C<sub>2</sub><sup>+</sup> is at V<sub>CC</sub>, the voltage potential across C<sub>2</sub> is 2 times V<sub>CC</sub>.

### Phase 4

— V<sub>DD</sub> transfer — The fourth phase of the clock connects the negative terminal of C<sub>2</sub> to GND, and transfers this positive generated voltage across C<sub>2</sub> to C<sub>4</sub>, the V<sub>DD</sub> storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C<sub>4</sub>, the positive side of capacitor C<sub>1</sub> is switched to V<sub>CC</sub> and the negative side is switched to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V<sup>+</sup> and V<sup>-</sup> are separately generated from V<sub>CC</sub>, in a no-load condition V<sup>+</sup> and V<sup>-</sup> will be symmetrical. Older charge pump approaches that generate V<sup>-</sup> from V<sup>+</sup> will show a decrease in the magnitude of V<sup>-</sup> compared to V<sup>+</sup> due to the inherent inefficiencies in the design.

### V<sub>L</sub> Supply Level

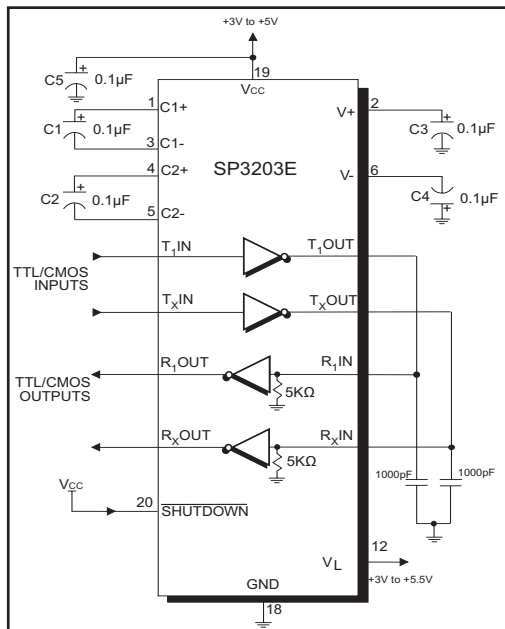


Figure 2. Loopback Test Circuit for RS-232 Driver High Data Transmission Rates



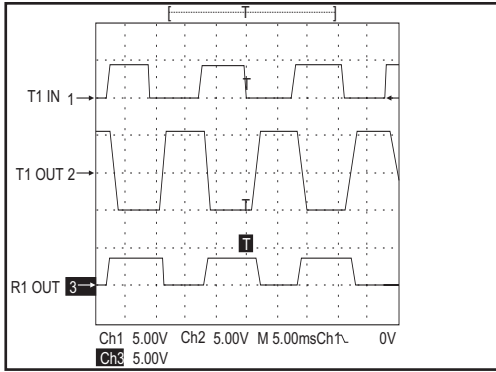


Figure 3. Loopback Test Circuit result at 120Kbps (All Drivers Fully Loaded)

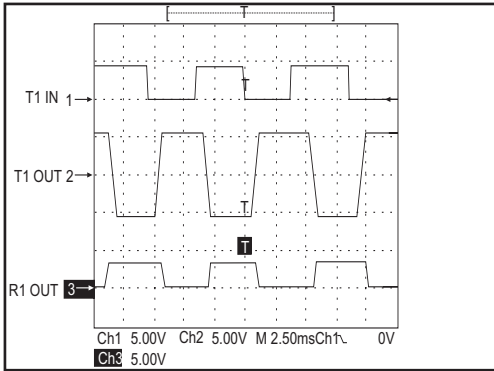


Figure 4. Loopback Test Circuit result at 250Kbps (All Drivers Fully Loaded)

Current RS-232 serial transceivers are designed with fixed 5V to 3.3V TTL input/output voltage levels. The  $V_L$  function in the SP3203E allows the end user to set the TTL input/output voltage levels independent of  $V_{cc}$ . By connecting  $V_L$  to the main logic bus of system, the TTL input/output limits and thresholds are reset to interface with the on board low voltage logic circuitry.

Capacitor Selection Table:

$V_{cc}$ (V)	C1 ( $\mu\text{F}$ )	C2 - C4 ( $\mu\text{F}$ )
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.22	1

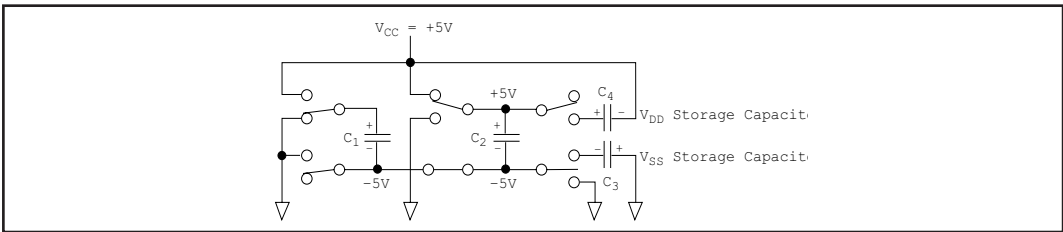


Figure 5. Charge Pump - Phase 1

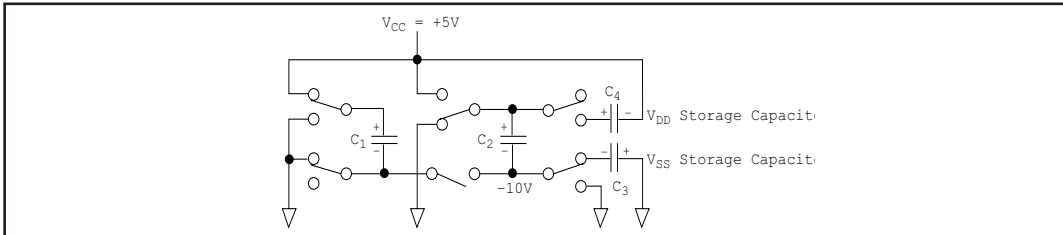


Figure 6. Charge Pump - Phase 2

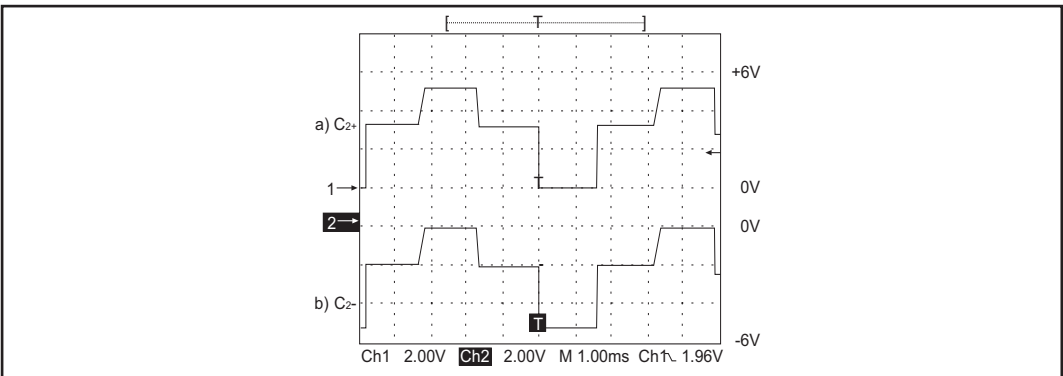


Figure 7. Charge Pump Waveforms

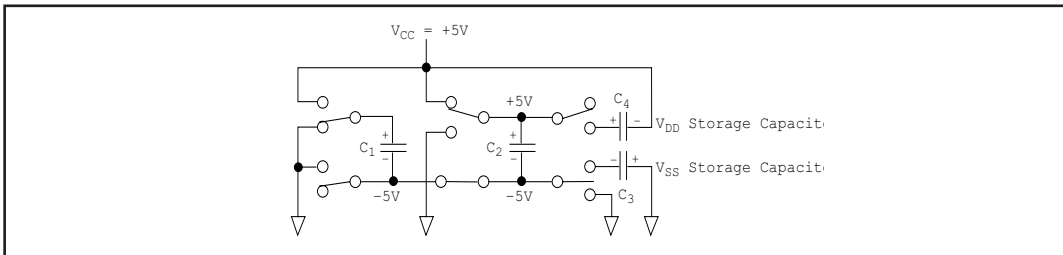


Figure 8. Charge Pump - Phase 3

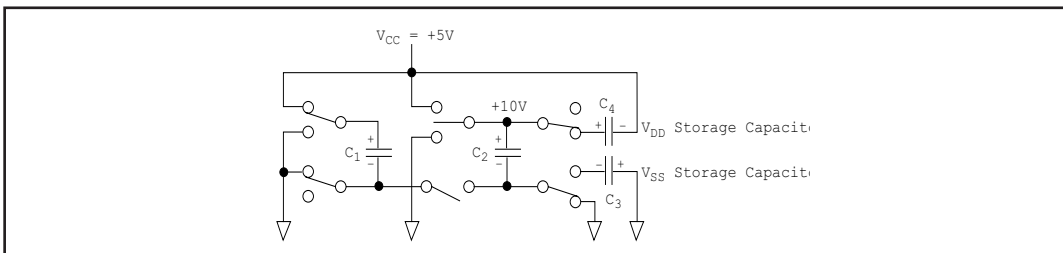


Figure 9. Charge Pump - Phase 4

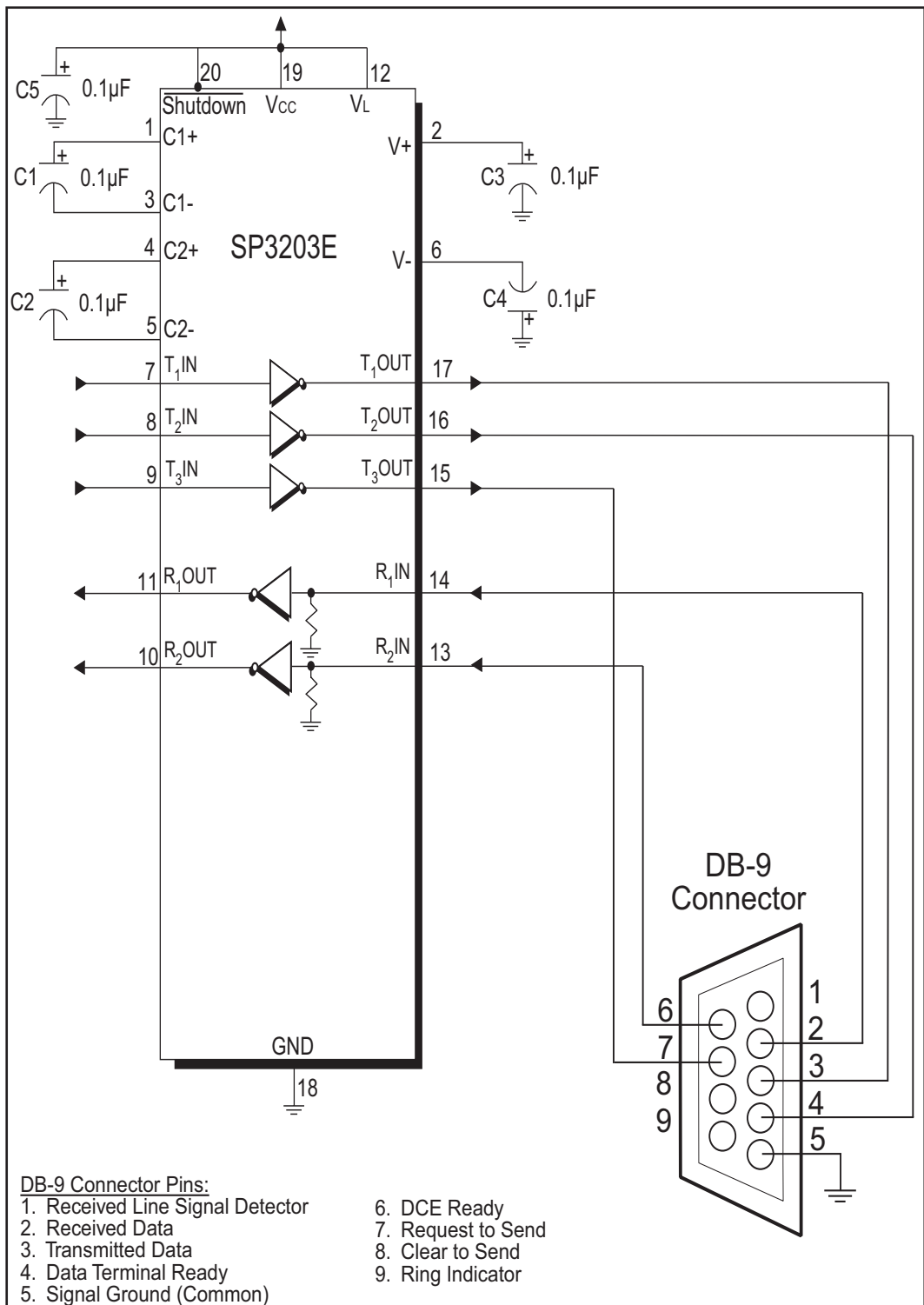


Figure 10. Circuit for the connectivity of the SP3203E with a DB-9 connector

## ESD TOLERANCE

The SP3203E incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least  $\pm 15\text{kV}$  without damage nor latch-up.

There are different methods of ESD testing applied:

- a) MIL-STD-883, Method 3015.7
- b) IEC61000-4-2 Air-Discharge
- c) IEC61000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 11. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the IC's tend to be handled frequently.

The IEC-61000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC61000-4-2 is that the system is required to withstand an amount of static electricity when ESD

is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC61000-4-2 is shown on Figure 12. There are two methods within IEC61000-4-2, the Air Discharge method and the Contact Discharge method. With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed. The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

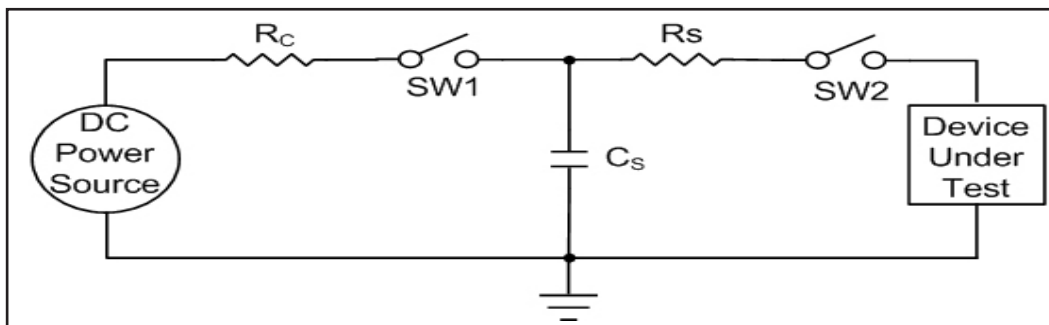


Figure 11. ESD Test Circuit for Human Body Model

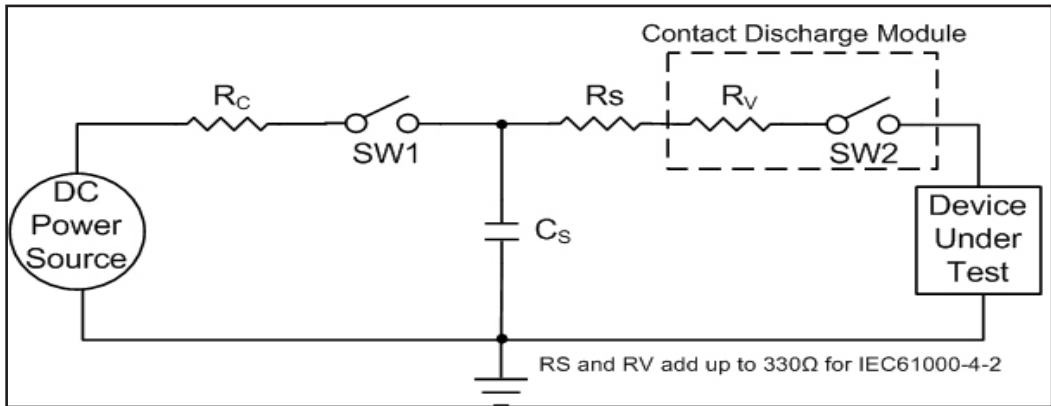


Figure 12. ESD Test Circuit for IEC61000-4-2

The circuit model in Figures 11 and 12 represent the typical ESD testing circuit used for all three methods. The  $C_s$  is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through  $R_s$ , the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor ( $R_s$ ) and the source capacitor ( $C_s$ ) are  $1.5k\Omega$  and  $100pF$ , respectively. For IEC-1000-4-2, the current limiting resistor ( $R_s$ ) and the source capacitor ( $C_s$ ) are  $330\Omega$  and  $150pF$ , respectively.

The higher  $C_s$  value and lower  $R_s$  value in the IEC61000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

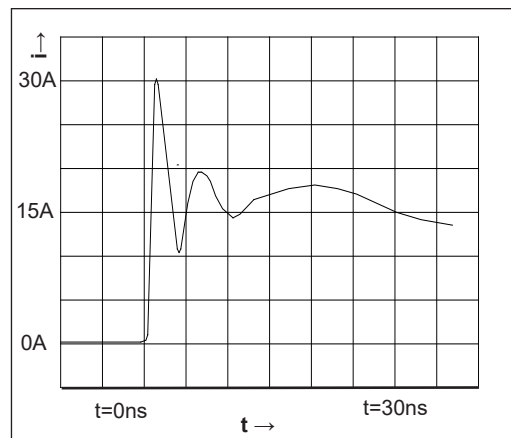
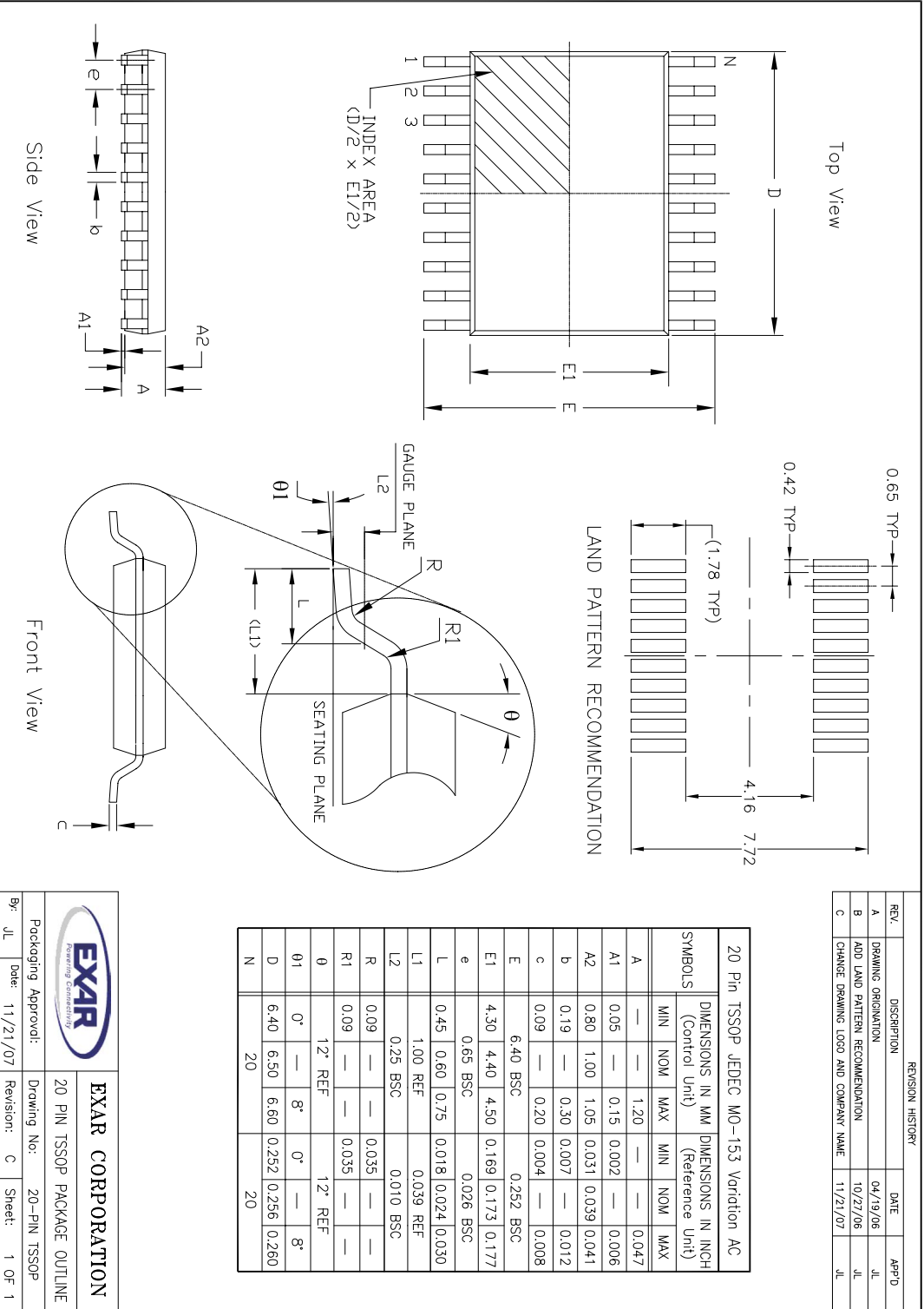


Figure 13. ESD Test Waveform for IEC61000-4-2

DEVICE PIN TESTED	HUMAN BODY MODEL	IEC61000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	$\pm 15kV$	$\pm 15kV$	$\pm 8kV$	4
Receiver Inputs	$\pm 15kV$	$\pm 15kV$	$\pm 8kV$	4

Table 4. Transceiver ESD Tolerance Levels



REVISION HISTORY			
REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIENTATION	04/19/06	JL
B	ADD LAND PATTERN RECOMMENDATION	10/27/06	JL
C	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL

20 Pin TSSOP JEDEC MO-153 Variation AC						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	1.20	—	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	—	0.30	0.007	—	0.012
c	0.09	—	0.20	0.004	—	0.008
E	6.40 BSC			0.252 BSC		
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
L2	0.25 BSC			0.010 BSC		
R	0.09	—	—	0.035	—	—
R1	0.09	—	—	0.035	—	—
θ	12° REF		12° REF		—	
θ1	0°	—	8°	0°	—	8°
D	6.40	6.50	6.60	0.252	0.256	0.260
N	20			20		

		<b>EXAR CORPORATION</b>			
				20 PIN TSSOP PACKAGE OUTLINE	
Packaging Approval:	By: JL	Date: 11/21/07	Drawing No: 20-PIN TSSOP	Revision: C	Sheet: 1 OF 1

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## ORDERING INFORMATION<sup>(1)</sup>

Part Number	Temperature Range	Package	Packaging Method	Lead-Free <sup>(2)</sup>
SP3203ECY-L/TR	0°C to +70°C	20-pin TSSOP	Tape and Reel	Yes
SP3203EEY-L/TR	-40°C to +85°C	20-pin TSSOP	Tape and Reel	Yes

### NOTES:

1. Refer to [www.maxlinear.com/SP3203E](http://www.maxlinear.com/SP3203E) for the most up-to-date Ordering Information.
2. Visit [www.maxlinear.com](http://www.maxlinear.com) for additional information on Environmental Rating.

## REVISION HISTORY

DATE	REVISION	DESCRIPTION
03-01-05	---	Legacy Sipex datasheet
Dec 2010	1.0.0	Convert to Exar datasheet format and remove EOL parts.
Mar 2020	1.0.1	Update to MaxLinear logo. Update Ordering Information.



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