SP6669

600mA 1.5MHz Synchronous Step Down Converter

February 2012 Rev. 2.1.0

GENERAL DESCRIPTION

The SP6669 is a synchronous current mode PWM step down (buck) converter capable of delivering up to 600mA of current. It features a pulse skip mode (PSM) for light load efficiency and a LDO mode for 100% duty cycle.

With a 2.5V to 5.5V input voltage range and a 1.5MHz switching frequency, the SP6669 allows the use of small surface mount inductors and capacitors ideal for battery powered portable applications. The internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode. Low output voltages are easily supported with the 0.6V feedback reference voltage. The SP6669 is available in an adjustable output voltage version, using an external resistor divider circuit, as well as fixed output voltage versions of 1.2V, 1.5V and 1.8V.

Built-in over temperature and output over voltage lock-out protections insure safe operations under abnormal operating conditions.

The SP6669 is offered in a RoHS compliant, "green"/halogen free 5-pin SOT23 package.

APPLICATIONS

- **Portable Equipments**
- **Battery Operated Equipments**
- **Audio-Video Equipments**
- **Networking & Telecom Equipments**

FEATURES

- **Guaranteed 600mA Output Current**
  - Input Voltage: 2.5V to 5.5V
- **1.5MHz PWM Current Mode Control**
  - 100% Duty Cycle LDO Mode Operations
  - Achieves 95% Efficiency
- **Fixed/Adjustable Output Voltage Range**
  - As Low as 0.6V with ±3% Accuracy
  - 1.2V, 1.5V, 1.8V Fixed Voltage Options
- **Excellent Line/Load Transient Response**
- **200µA Quiescent Current**
- **Over Temperature Protection**
- **RoHS Compliant "Green"/Halogen Free 5-Pin SOT23 Package**

TYPICAL APPLICATION DIAGRAM

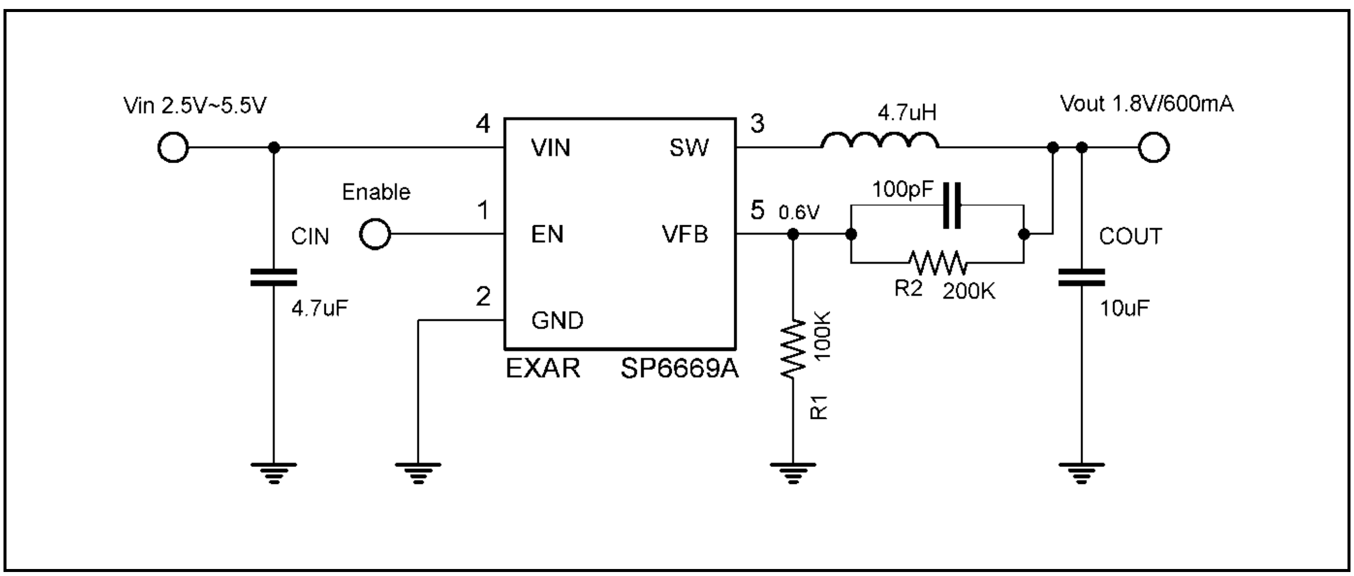

Fig. 1: SP6669 Application Diagram (Adj. version shown)

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ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Input Voltage V_{IN} ....-0.3V to 6.0V
Enable V_{FB} Voltage .... -0.3V to V_{IN}
SW Voltage..................................... -0.3V to (V_{IN}+0.3V)
PMOS Switch Source Current (DC)........................800mA
NMOS Switch Sink Current 800mA
Peak Switch Sink/Source Current 1.3A
Operating Junction Temperature[1] .... 125°C
Storage Temperature .... -65°C to 150°C
Lead Temperature (Soldering, 10 sec) ....240°C
ESD Rating (HBM - Human Body Model).................... 2kV
ESD Rating (MM - Machine Model) 200V

OPERATING RATINGS

Input Voltage Range V_{IN}...............................2.7V to 5.5V
Operating Temperature Range.................. -40°C to 85°C
Thermal Resistance θ_{JA} ....250°C/W
Thermal Resistance θ_{JC}...................................... 90°C/W

Note 1: T_J is a function of the ambient temperature T_A and power dissipation P_D (T_J= T_A + P_D x 250°C/W).

ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Operating Junction Temperature of T_J = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN} = 3.6V.

Parameter	Min.	Typ.	Max.	Units		Conditions
Feedback Current I_{VFB}			±30	nA		
Regulated Feedback Voltage V_{FB}	0.588	0.600	0.612	V		T_A=25°C
Reference Voltage Line Regulation ΔV_{FB}			0.4	%/V	•	V_{IN}=2.5V to 5.5V
Output Voltage Accuracy ΔV_{OUT}%	-3		+3	%	•	
Output Over-Voltage Lockout ΔV_{OVL}	20	50	80	mV		ΔV_{OVL} = V_{OVL} – V_{FB} (Adj.)
	2.5	7.8	13	%		ΔV_{OVL} = V_{OVL} – V_{OUT} (Fixed)
Output Voltage Line Regulation ΔV_{OUT}			0.4	%/V	•	V_{IN}=2.5V to 5.5V
Peak Inductor Current I_{PK}		1.0		A		V_{IN}=3V, V_{FB}=0.5V or V_{OUT}=90%, Duty cycle <35%
Output Voltage Load Regulation $V_{LOADREG}$		0.5		%		
Quiescent Current[2] I_Q		200	340	μA		V_{FB}=0.5V or V_{OUT}=90%
Shutdown Current I_{SHTDWN}		0.1	1	μA		V_{EN}=0V, V_{IN}=4.2V
Oscillator Frequency f_{OSC}	1.2	1.5	1.8	MHz	•	V_{FB}=0.6V or V_{OUT}=100%
		290		Hz	•	V_{FB}=0V or V_{OUT}=0V
RDS(ON) of PMOS R_{PFET}		0.45	0.55	Ω		I_{SW}=100mA
RDS(ON) of NMOS R_{NFET}		0.40	0.50	Ω		I_{SW}=100mA
SW Leakage I_{LSW}			±1	μA		V_{EN}=0V, V_{SW}=0V or 5V, V_{IN}=5V
Enable Threshold V_{EN}			1.2	V	•	
Shutdown Threshold V_{EN}	0.4			V	•	
EN Leakage Current I_{EN}			±1	μA	•	

Note 1: The Switch Current Limit is related to the Duty Cycle. Please refer to figure 15 for details.
Note 2: Dynamic quiescent current is higher due to the gate charge being delivered at the switching frequency.

BLOCK DIAGRAM

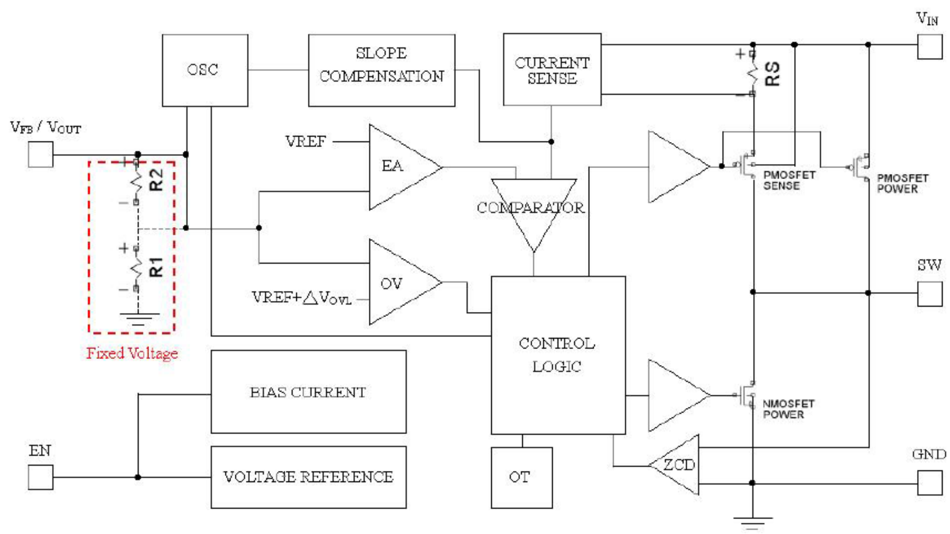


Fig. 2: SP6669 Block Diagram

PIN ASSIGNMENT

Fig. 3: SP6669 Pin Assignment

PIN DESCRIPTION

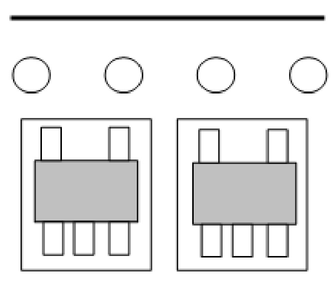
Name	Pin Number	Description
EN	1	Enable Pin. Do not leave the pin floating. V_{EN}<0.4V: Shutdown mode V_{EN}>1.2V: Device enabled
GND	2	Ground Signal
SW	3	Switching Node
VIN	4	Power Supply Pin. Must be decoupled to ground with a 4.7μF or greater ceramic capacitor.
VFB	5	Adjustable Version Feedback Input Pin. Connect VFB to the center point of the resistor divider.
VOUT	5	Fixed Output Voltage Version, Output Voltage Pin. An internal resistive divider divides the output voltage down for comparison to the internal reference voltage.

ORDERING INFORMATION

Part Number	Temperature Range	Marking	Package	Packing Quantity	Note 1	Note 2
SP6669AEK-L/TRR3	-40°C≤T_A≤+85°C	QBWW	SOT23-5	3K/Tape & Reel	Halogen Free	Adjustable output voltage
SP6669BEK-L/TRR3	-40°C≤T_A≤+85°C	RBWW	SOT23-5	3K/Tape & Reel	Halogen Free	1.2V fixed output voltage
SP6669CEK-L/TRR3	-40°C≤T_A≤+85°C	SBWW	SOT23-5	3K/Tape & Reel	Halogen Free	1.5V fixed output voltage
SP6669DEK-L/TRR3	-40°C≤T_A≤+85°C	TBWW	SOT23-5	3K/Tape & Reel	Halogen Free	1.8V fixed output voltage
SP6669EB	SP6669 Evaluation Board					

"YY" = Year – "WW" = Work Week – "X" = Lot Number; when applicable.

Note that the SP6669 series is packaged in Tape and Reel with a reverse part orientation as per the following diagram



TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at V_{IN} = 2.7V to 5.5V, T_J = T_A = 25°C, unless otherwise specified - Schematic and BOM from Application Information section of this datasheet.

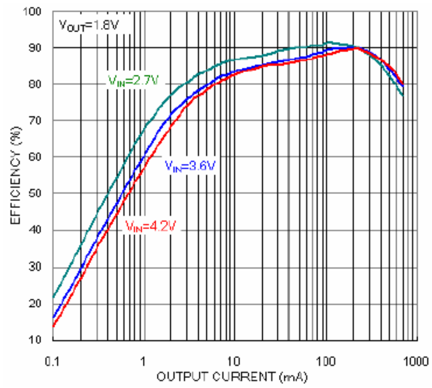


Fig. 4: Efficiency vs Output Current (mA)

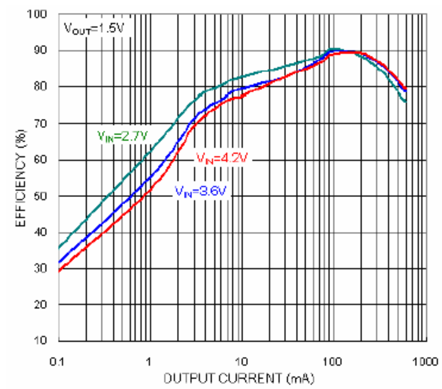


Fig. 5: Efficiency vs Output Current (mA)

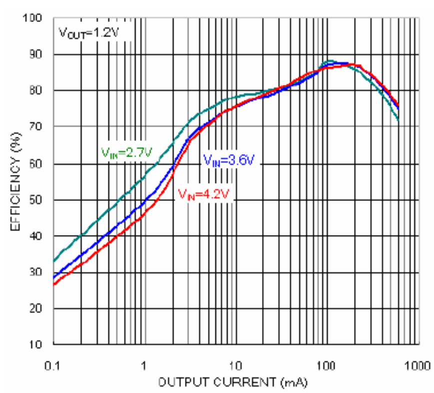


Fig. 6: Efficiency vs Output Current (mA)

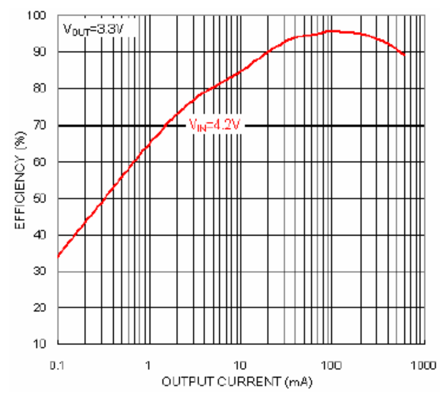


Fig. 7: Efficiency vs Output Current (mA)

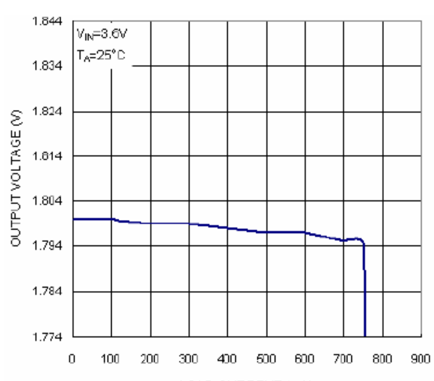


Fig. 8: Output Voltage vs Load Current

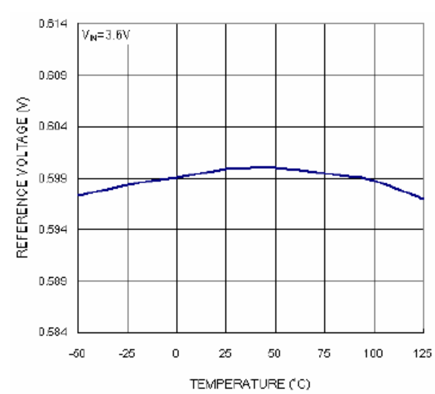


Fig. 9: Reference Voltage vs Temperature

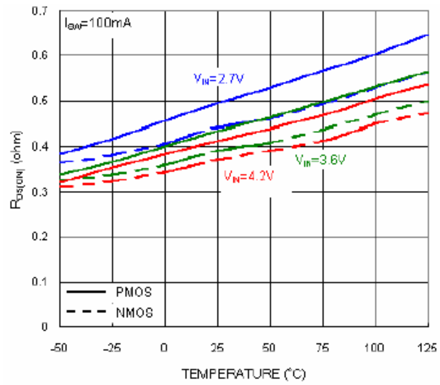


Fig. 10: $R_{DS(ON)}$ vs Temperature

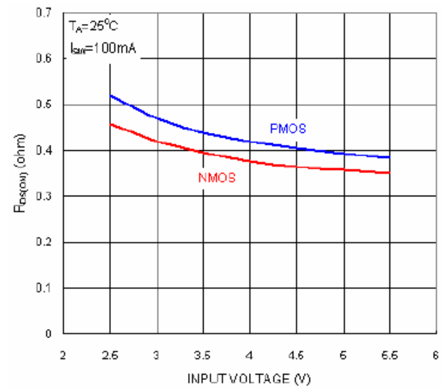


Fig. 11: $R_{DS(ON)}$ vs Input Voltage

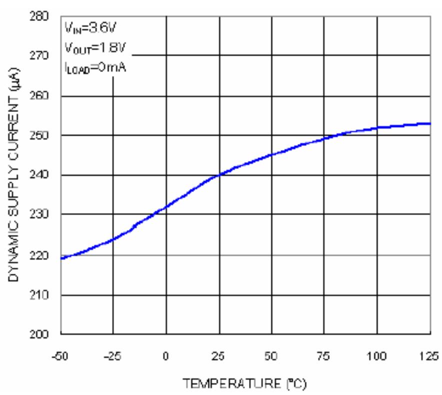


Fig. 12: Dynamic Supply Current vs Temperature

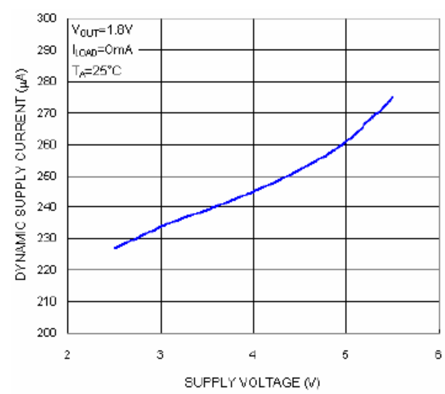


Fig. 13: Dynamic Supply Current vs Supply Voltage

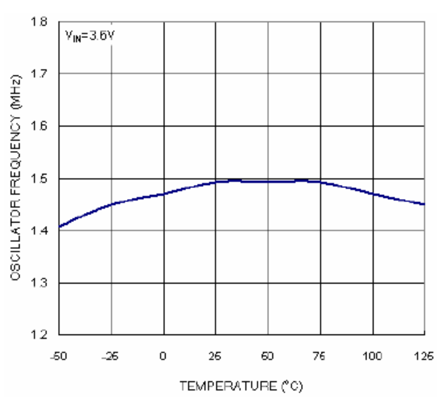


Fig. 14: Oscillator Frequency vs Temperature

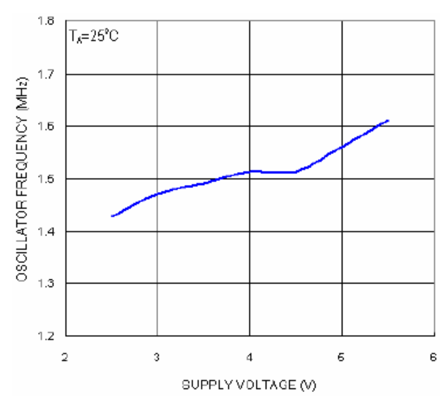


Fig. 15: Oscillator Frequency vs Supply Voltage

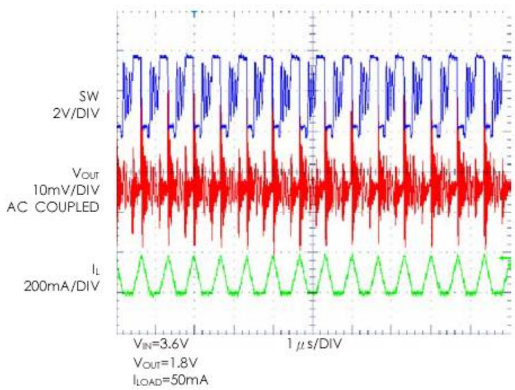


Fig. 16: Discontinuous Operation

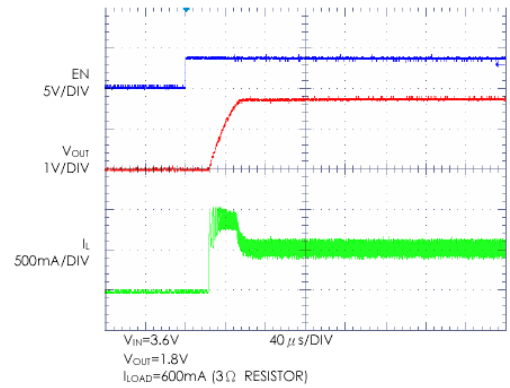


Fig. 17: Start-up from Shutdown

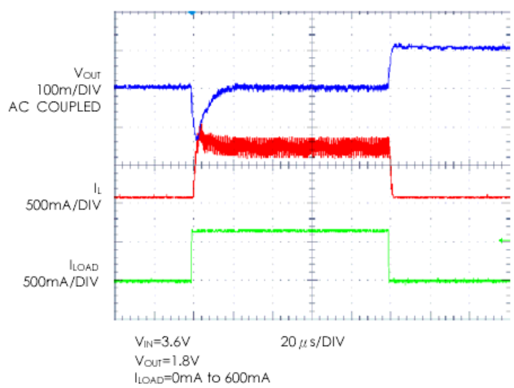


Fig. 18: Load Step

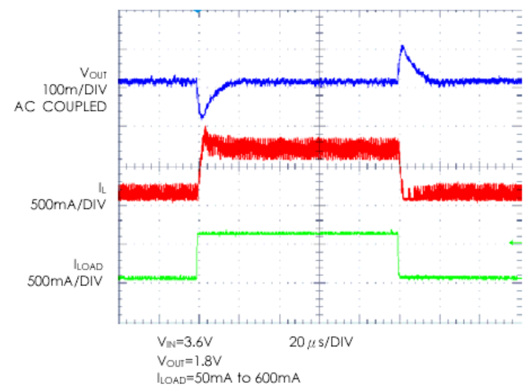


Fig. 19: Load Step

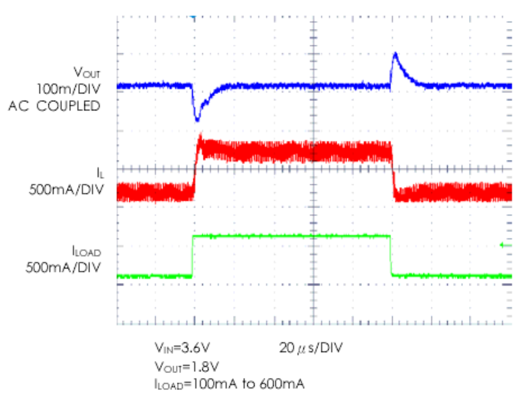


Fig. 20: Load Step

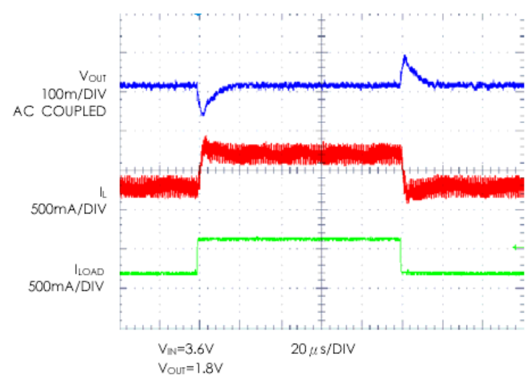


Fig. 21: Load Step

THEORY OF OPERATION

APPLICATIONS

The typical application circuit of the adjustable output voltage option and the fixed output voltage option are shown below.

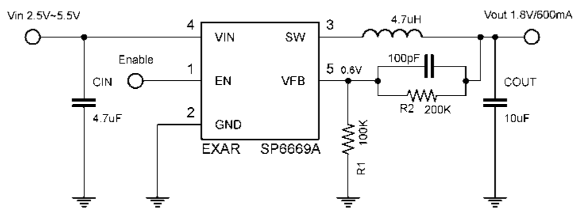


Fig. 22: Adjustable Output Voltage Version

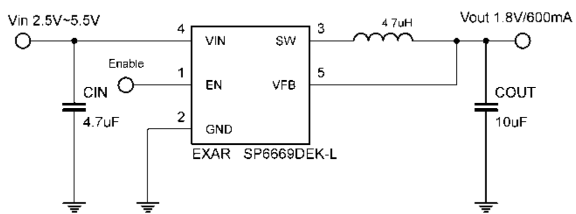


Fig. 23: Fixed Output Voltage Version

INDUCTOR SELECTION

Inductor ripple current and core saturation are two factors considered to select the inductor value.

Eq. 1: $$\Delta I_L = \frac{1}{f \cdot L} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Equation 1 shows the inductor ripple current as a function of the frequency, inductance, V_{IN} and V_{OUT}. It is recommended to set the ripple current between 30% to 40% of the maximum load current. A low ESR inductor is preferred.

C_{IN} AND C_{OUT} SELECTION

A low ESR input capacitor can prevent large voltage transients at V_{IN}. The RMS current rating of the input capacitor is required to be larger than I_{RMS} calculated by:

Eq. 2: $$I_{RMS} \cong I_{OMAX} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

The ESR rating of the capacitor is an important parameter to select C_{OUT}. The output ripple V_{OUT} is determined by:

Eq. 3: $$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8 \cdot f \cdot C_{OUT}} \right)$$

Higher values, lower cost ceramic capacitors are now available in smaller sizes. These capacitors have high ripple currents, high voltage ratings and low ESR that makes them ideal for switching regulator applications. As C_{OUT} does not affect the internal control loop stability, its value can be optimized to balance very low output ripple and circuit size. It is recommended to use an X5R or X7R rated capacitors which have the best temperature and voltage characteristics of all the ceramics for a given value and size.

OUTPUT VOLTAGE – ADJUSTABLE VERSION

The adjustable output voltage version is determined by:

Eq. 4: $$V_{OUT} = 0.6V \cdot \left(1 + \frac{R_2}{R_1}\right)$$

THERMAL CONSIDERATIONS

Although the SP6669 has an on board over temperature circuitry, the total power dissipation it can support is based on the package thermal capabilities. The formula to ensure safe operation is given in note 1.

PCB LAYOUT

The following PCB layout guidelines should be taken into account to ensure proper operation and performance of the SP6669:

1- The GND, SW and V_{IN} traces should be kept short, direct and wide.

2- V_{FB} pin must be connected directly to the feedback resistors. The resistor divider network must be connected in parallel to the C_{OUT} capacitor.

3- The input capacitor C_{IN} must be kept as close as possible to the V_{IN} pin.

4- The SW and VFB nodes should be kept as separate as possible to minize possible effects from the high frequency and voltage swings of the SW node.

5- The ground plates of C_{IN} and C_{OUT} should be kept as close as possible.

OUPTUT VOLTAGE RIPPLE FOR V_{IN} CLOSE TO V_{OUT}

When the input voltage V_{IN} is close to the output voltage V_{OUT}, the SP6669 transitions smoothly from the switching PWM converter mode into a LDO mode. The following diagram shows the output voltage ripple versus the input voltage for a 3.3V output setting and a 200mA current load.

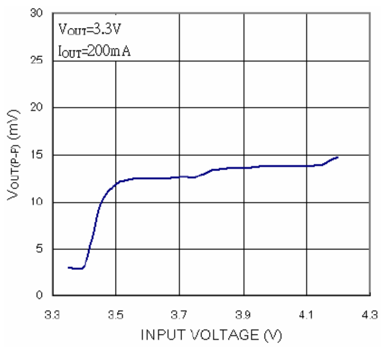


Fig. 24: VOUT Ripple Voltage for VIN decreasing close to V_{OUT}

DESIGN EXAMPLE

In a single Lithium-Ion battery powered application, the V_{IN} range is about 2.7V to 4.2V. The desired output voltage is 1.8V.

The inductor value needed can be calculated using the following equation

$$L = \frac{1}{f \cdot \Delta I_L} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Substituting V_{OUT}=1.8V, V_{IN}=4.2V, ΔI_L=180mA to 240mA (30% to 40%) and f=1.3MHz gives

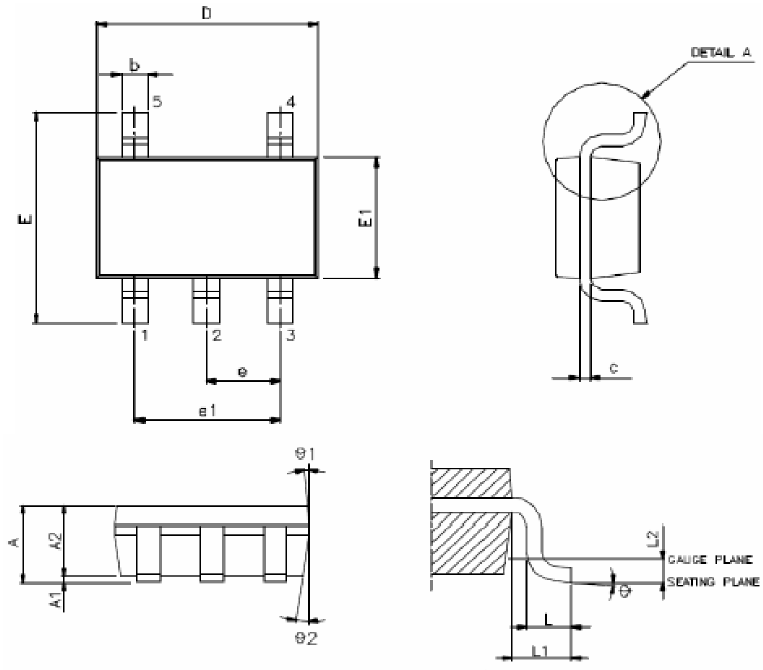
$$L = 2.86\mu H \ to \ 3.81\mu H$$

A 3.3μH inductor can be chosen with this application. An inductor of greater value with less equivalent series resistance would provide better efficiency. The CIN capacitor requires an RMS current rating of at least $I_{LOAD(MAX)}/2$ and low ESR. In most cases, a ceramic capacitor will satisfy this requirement.

PACKAGE SPECIFICATION

5-PIN SOT23

Unit: mm



Symbol	Min.	Nom.	Max
A	0.90	1.30	1.40
A1	0.00	0.075	0.15
A2	0.90	1.20	1.25
b	0.30	-	0.50
c	0.08	-	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 BSC		
Θ	0	5	10
Θ1	3	5	7
Θ2	6	8	10

Note: JEDEC Outline MO-178 AA

REVISION HISTORY

Revision	Date	Description
2.0.0	07/15/2011	Reformat of datasheet Updated package specification
2.1.0	02/07/2012	Updated Typical Application schematics and Design example

FOR FURTHER ASSISTANCE

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