XR77103

Universal PMIC
3-Output Programmable Buck Regulator

Description

The XR77103 features three high efficiency, wide input range, synchronous buck converters. Each converter is digitally programmable requiring minimal external components, thus providing the smallest size solution possible.

The converters can operate in 5V, 9V, and 12V systems and have integrated power switches. The output voltage of each converter can be adjusted by programming the values in the V_{OUT} setting registers through the I²C interface. The adjustable range is 0.8V to 6V with 50mV resolution. The output voltage also can be set externally using an external resistor divider. The output sequence among the outputs, soft-start time, and the peak inductor current limit are also set through I²C.

The switching frequency of the converters can either be set with I²C or can be synchronized to an external clock connected to SYNC pin if needed. The switching regulators are designed to operate from 440kHz to 2.3MHz. Each converter operates in phase or out-of-phase according to the value in the phase setting register. This can minimize the input filter requirements.

XR77103 features a supervisor circuit that monitors each converter output. The PGOOD pin is asserted once sequencing is done, all outputs are reported in regulation, and the reset timer expires. The polarity of the signal is active high.

XR77103 also features a light load pulse skipping mode (PSM). It is set through I²C. The PSM mode allows for a reduction on the input power supplied to the system when the host processor is in stand-by (low activity) mode.

FEATURES

- 4.5V to 14V wide input supply voltage range
- Built-In MOSFET and synchronous rectifier
- I²C programmable supplies
  - Output voltage (0.8V to 6V)
  - Power on sequence
  - Soft-start timing
  - Switching frequency (440kHz to 2.3MHz)
  - Individual current limit
  - Optional power saving mode at light loads
- Non volatile memory (NVM) with up to 10,000 times write operation
- High accuracy 0.8V reference (1%)
- Current-mode control with simple compensation circuit
- External synchronization
- Power good
- Protection
  - Thermal shutdown
  - Overvoltage transient protection
  - Overcurrent protection
- 32-pin 4mm x 4mm TQFN package

APPLICATIONS

- FPGA and DSP supplies
- Video processor supplies
- Applications processor power

Typical Application

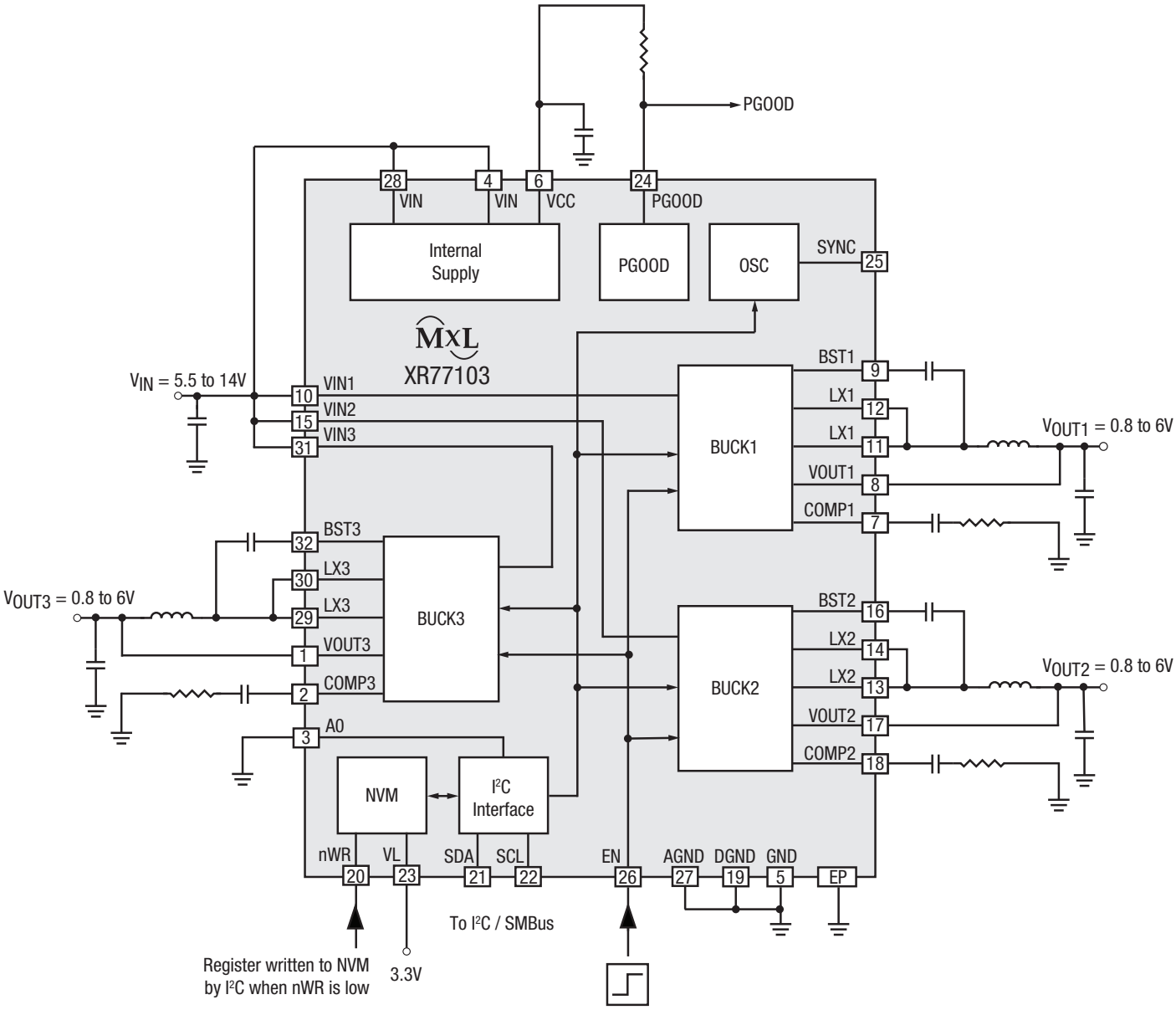


Figure 1. Typical Application

Absolute Maximum Ratings

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to any absolute maximum rating condition for extended periods may affect device reliability and lifetime.

V_{IN1}, V_{IN2}, V_{IN3}, LX1, LX2, LX3 ..... -0.3V to 18V

VL, EN, SCL, SDA, nWR, A0, V_{CC} ..... -0.3V to 7V

PGOOD, SYNC ..... -0.3V to 7V

BST# to LX# ..... -0.3V to 7V

AGND, DGND to GND ..... -0.3V to 0.3V

Storage temperature ..... -65°C to 150°C

Junction temperature ..... 150°C

Power dissipation ..... Internally Limited

Lead temperature (soldering, 10 seconds) ..... 260°C

CDM 700V

ESD rating (HBM – human body model) 2kV

Operating Conditions

V_{IN} ..... 4.5V to 14V

V_{CC} ..... 4.5V to 5.5V

LX# ..... -0.3V to 14V(1)

Junction temperature range (T_J) ..... -40°C to 125°C

XR77103 package power dissipation max at 25°C 3.4W

XR77103 thermal resistance θ_{JA} ..... 30°C/W

NOTE:

1. LX# pins' DC range is from -0.3V, transient -1V for less than 10ns.

Electrical Characteristics

T_A = 25°C, V_{IN} = 12V, EN = V_{CC}, f_{SW} = 1MHz, unless otherwise specified. Limits applying over the full operating temperature range are denoted by a •.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Power Supply Characteristics							
V_{IN}	Input voltage range		•	5.5		14	V
V_{IN}	Input voltage range	VCC tied to VIN for V_{IN} = 5V	•	4.5		5.5	V
V_{UVLO}	UVLO threshold	UV = 0, V_{IN} rising/falling			4.22/4.1		V
		UV = 1, V_{IN} rising/falling			7/6.88		
$UVLO_{DEGLITCH}$	UVLO deglitch	Rising/falling			110		µs
I_{VIN}	V_{IN} supply current	EN = GND			250		µA
I_{VINQ}		EN = high, no load, CCM			36		mA
I_{VINQ_LP}		EN = high, no load, PSM			2.6		mA
Internal Supply Voltage							
V_{CC}	Internal biasing supply	I_{LOAD} = 0mA	•	4.9	5	5.1	V
I_{VCC}	Internal biasing supply current	V_{IN} = 12V	•			10	mA
V_{UVLO}	UVLO threshold for V_{CC}	V_{CC} rising			3.8		V
		V_{CC} falling			3.6		V
$UVLO_{DEGLITCH}$	UVLO deglitch for V_{CC}	Falling edge			110		µs

Electrical Characteristics (Continued)

T_A = 25°C, V_{IN} = 12V, EN = V_{CC}, f_{SW} = 1MHz, unless otherwise specified. Limits applying over the full operating temperature range are denoted by a •.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Protections							
T_{SD}	Thermal shutdown temperature	Temperature rising, Non-latch off. T_{SD} release threshold, temperature = T_{SD}-HY_{TSD}			160		°C
HY_{TSD}	Thermal shutdown hysteresis				20		°C
$T_{SD\_DEGLITCH}$	Thermal shutdown deglitch				110		µs
V_{OVBUCK}	Threshold voltage for buck overvoltage	Output rising (HS FET will be forced off)			109		%
		Output falling (HS FET will be allowed to switch)			107		%
Buck Converter							
f_{SW}	Switching frequency	I²C control	•	0.44		2.3	MHz
V_{OUTx}	Output voltage range		•	0.8		6	V
	Output voltage resolution				0.05		V
	Adjustable soft-start period range		•	0.5		4	ms
I_{LIMx}	Peak inductor current limit range		•	2		4.5	A
I_{LIMx}	Peak inductor current limit accuracy	Peak inductor current limit set at 4A		-30		+30	%
R_{ON_HSx}	HS switch on-resistance	V_{IN} = 12V			200		mΩ
R_{ON_LS1}	LS switch on-resistance of Buck1	V_{IN} = 12V			60		mΩ
$R_{ON\_LS2/3}$	LS switch on-resistance of Buck2/3	V_{IN} = 12V			80		mΩ
I_O	Output current capability	Continuous loading			2[1]		A
D_{MAX}	Maximum duty cycle				95		%
$t_{ON\ MIN}$	Minimum on time				120		ns
	Line regulation ($\Delta V_{OX}/\Delta V_{INX}$)	V_{INX} = 5.5 to 14V, I_{OX} = 1A			0.5		$\%V_O$
	Load regulation ($\Delta V_{OX}/\Delta I_{OX}$)	I_O = 10 to 90%, I_O = MAX			0.5		$\%V_O/A$
	Output voltage accuracy	V_{IN} = 12V		-1	Normal	1	%
		5.5V ≤ V_{IN} ≤ 14V	•	-2	Normal	2	
$SYNC_{RANGE}$	Synchronization range		•	f_{SW} + 5%		2.31	MHz
$SYNC_{D\_MIN}$	Synchronization signal minimum duty cycle		•	40			%
$SYNC_{D\_MAX}$	Synchronization signal maximum duty cycle		•			60	%

NOTE:
1. Subject to thermal derating. Design must not exceed the package thermal rating.

Electrical Characteristics (Continued)

T_A = 25°C, V_{IN} = 12V, EN = V_{CC}, f_{SW} = 1MHz, unless otherwise specified. Limits applying over the full operating temperature range are denoted by a •.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Power Good Reset Generator							
V_{UVBUCK}	Threshold voltage for buck under voltage	Output falling, (disabled after t_{ON_HICCUP})			85		%
		Output rising, (PG will be asserted)			90		
$t_{PG\_DEGLITCH}$	Deglitch time	Rising and falling			11		ms
t_{ON_HICCUP}	Hiccup mode on time	$V_{UVBUCKX}$ asserted			12		ms
t_{OFF_HICCUP}	Hiccup mode off time	Once t_{OFF_HICCUP} elapses, all converters will start up again			15		ms
t_{RP}	Minimum reset period				1		s
	PGOOD output low	I_{SINK} = 1mA	•			0.4	V
Input Threshold (SDA, SCL, nWR, A0)							
V_{IH}	Input threshold high	V_{INPUT} rising, V_L = 3.3V	•	2.45			V
V_{IL}	Input threshold low	V_{INPUT} falling, V_L = 3.3V	•			0.95	V
	A0, nWR pull up resistor				100		kΩ
Input Threshold (SYNC, EN)							
V_{IH}	Input threshold high	V_{INPUT} rising	•	2.53			V
V_{IL}	Input threshold low	V_{INPUT} falling	•			1.36	V

Electrical Characteristics (Continued)

T_A = 25°C, V_{IN} = 12V, EN = V_{CC}, f_{SW} = 1MHz, unless otherwise specified. Limits applying over the full operating temperature range are denoted by a •.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
I²C Interface							
V_L	Supply voltage				3.3		V
V_{OL_I2C}	SDA logic output low voltage	At 3mA sink current	•			0.4	V
f_{SCL}	SCL clock frequency		•			400	kHz
t_{HIGH}	SCL clock high period		•	0.6			µs
t_{LOW}	SCL clock low period		•	1.3			µs
t_{SP}	I²C spike rejection filter pulse width		•	0		50	ns
$t_{SU;DAT}$	I²C data setup time		•	100			ns
$t_{HD;DAT}$	I²C data hold time		•	0		900	ns
t_R	SDA, SCL rise time	CB = total capacitance of bus line in pF	•		20 + 0.1 x C_B	300	ns
t_F	SDA, SCL fall time	CB = total capacitance of bus line in pF	•		20 + 0.1 x C_B	300	ns
t_{BUF}	I²C bus free time between stop and start		•	1.3			µs
$t_{SU;STA}$	I²C repeated start condition setup time		•	0.6			µs
$t_{HD;STA}$	I²C repeated start condition hold time		•	0.6			µs
$t_{SU;STO}$	I²C stop condition setup time		•	0.6			µs
$t_{VD;DAT}$	I²C data valid time		•			0.9	µs
$t_{VD;ACK}$	I²C data valid acknowledge time		•			0.9	µs
C_B	I²C bus capacitive load		•			400	pF
C_{SDA}	SDA input capacitance		•			10	pF
C_{SCL}	SCL input capacitance		•			10	pF

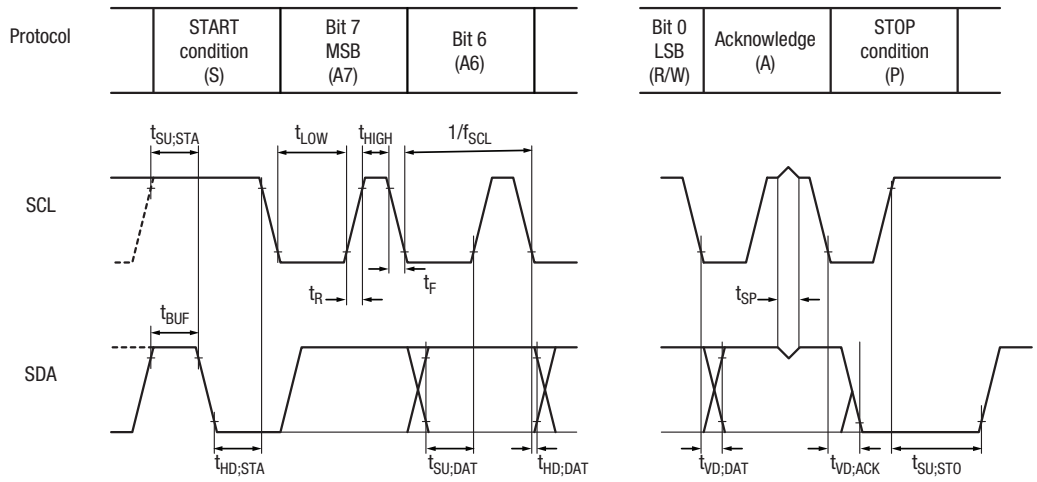
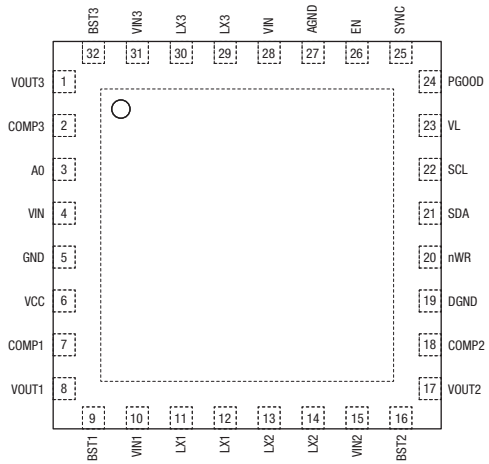


Figure 2. I²C Bus Timing Diagram

Pin Configuration



Pin Functions

Pin Number	Pin Name	Description
1	VOUT3	Buck 3 output sense pin.
2	COMP3	Compensation pin for Buck 3. Connect a series RC circuit to this pin for compensation.
3	A0	I²C address select pin. A0 is internally pulled HIGH through a 100kΩ pull up resistor.
4	VIN(1)	IC supply pin. Connect a capacitor as close as possible to this pin and AGND.
5	GND	Ground.
6	VCC	Internal supply. Connect a ceramic capacitor from this pin to AGND. Tie VCC to VIN for VIN = 5V.
7	COMP1	Compensation pin for Buck 1. Connect a series RC circuit to this pin for compensation.
8	VOUT1	Buck 1 output sense pin.
9	BST1	Bootstrap capacitor for Buck 1. Connect a bootstrap capacitor from this pin to LX1.
10	VIN1(1)	Input supply for Buck 1. Connect a capacitor as close as possible to this pin and PGND.
11	LX1	Switching node for Buck 1.
12	LX1	Switching node for Buck 1.
13	LX2	Switching node for Buck 2.
14	LX2	Switching node for Buck 2.
15	VIN2(1)	Input supply for Buck 2. Connect a capacitor as close as possible to this pin and PGND.
16	BST2	Bootstrap capacitor for Buck 2. Connect a bootstrap capacitor from this pin to LX2.
17	VOUT2	Buck 2 output sense pin.
18	COMP2	Compensation pin for Buck 2. Connect a series RC circuit to this pin for compensation.
19	DGND	Digital ground.
20	nWR	Write protection input for NVM. The data can be written to NVM when this pin is low. This pin is internally pulled high through a 100kΩ pull up resistance.

NOTE:
1. VIN, VIN1, VIN2, and VIN3 must be tied together.

Pin Functions (Continued)

Pin Number	Pin Name	Description
21	SDA	Data I/O pin for I²C serial interface.
22	SCL	Clock input pin for I²C serial interface.
23	VL	Supply pin for I²C interface. Supply 3.3V typically for I²C communication. This pin can be left floating if the I²C interface is not used.
24	PGOOD	Power good output. Open drain output asserted after all converters are sequenced and within regulation.
25	SYNC	External clock input pin. Connect to AGND when unused.
26	EN	Enable control input. Set EN high to enable converters.
27	AGND	Analog ground.
28	VIN(1)	IC supply pin. Connect a capacitor as close as possible to this pin and AGND.
29	LX3	Switching node for Buck 3.
30	LX3	Switching node for Buck 3.
31	VIN3(1)	Input supply for Buck 3. Connect a capacitor as close as possible to this pin and PGND.
32	BST3	Bootstrap capacitor for Buck 3. Connect a bootstrap capacitor from this pin to LX3.
-	e-PAD	Power ground (PGND).

NOTE:
1. VIN, VIN1, VIN2, and VIN3 must be tied together.

Typical Performance Characteristics

All data taken at T_A = 25°C unless otherwise specified.

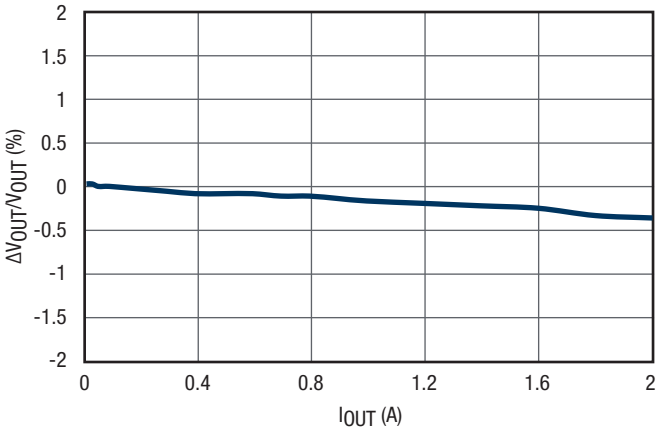


Figure 3. Load Regulation $12V_{IN}$, $3.3V_{OUT}$, f_{SW} = 1MHz

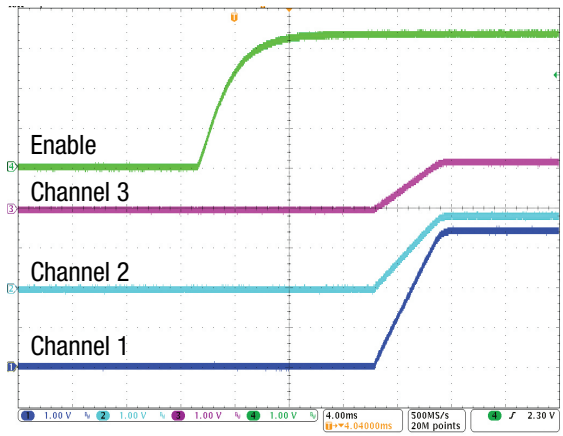


Figure 4. Power-up Sequence with Delay

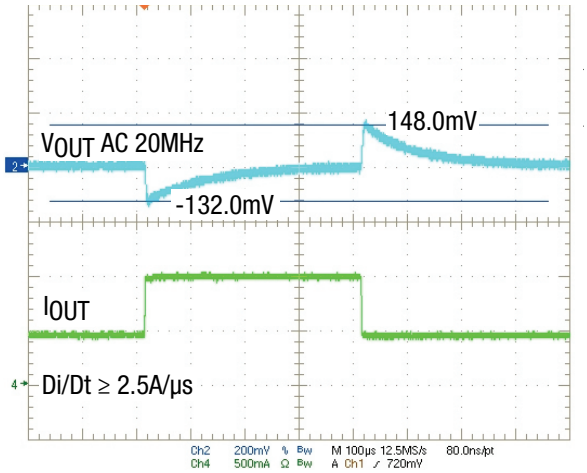


Figure 5. $12V_{IN}$, $3.3V_{OUT}$, f_{SW} = 440kHz Transient Response, 0.5A to 1.0A

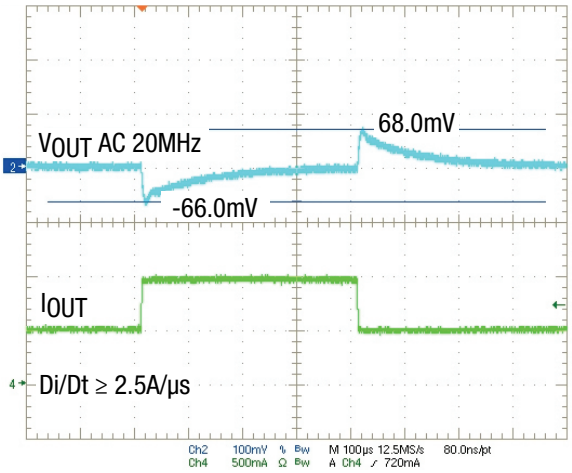


Figure 6. $5V_{IN}$, $1.8V_{OUT}$, f_{SW} = 440kHz Transient Response, 0.5A to 1.0A

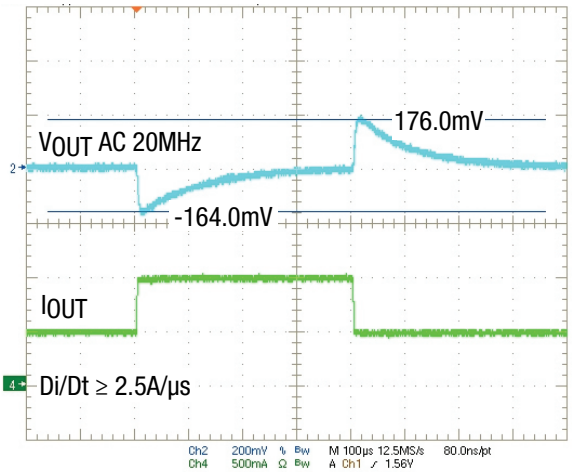


Figure 7. $12V_{IN}$, $5.0V_{OUT}$, f_{SW} = 1MHz Transient Response, 0.5A to 1.0A

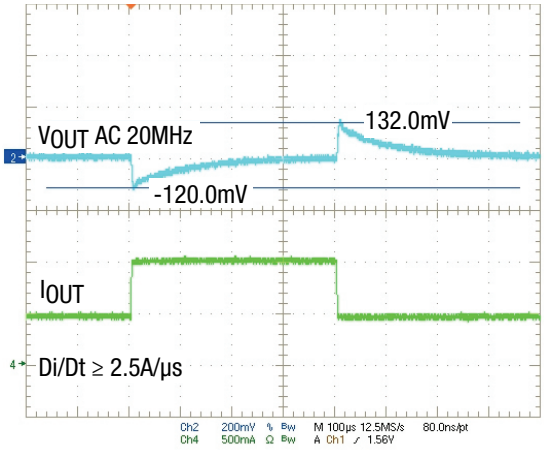


Figure 8. $5V_{IN}$, $3.3V_{OUT}$, f_{SW} = 1MHz Transient Response, 0.5A to 1.0A

Typical Performance Characteristics (Continued)

Efficiency

f_{SW} = 440kHz, T_A = 25°C, no airflow, only individual channel operating, inductor losses are included.

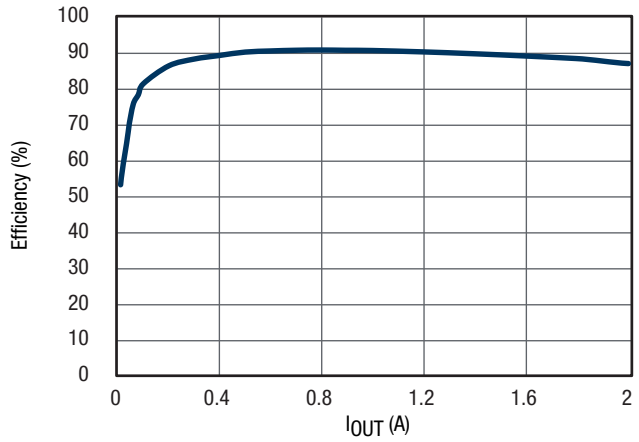


Figure 9. Efficiency Channel 1, $12V_{IN}$ $3.3V_{OUT}$

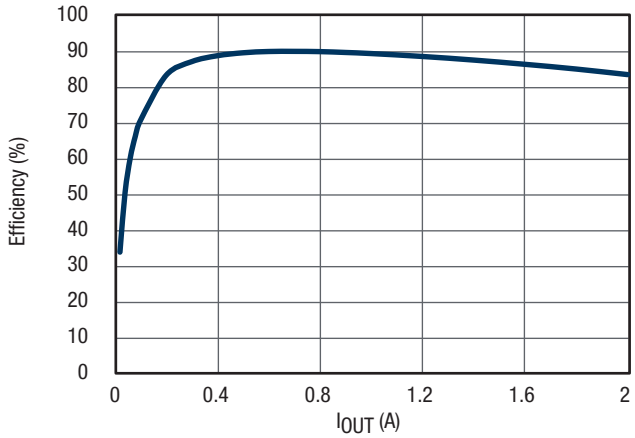


Figure 10. Efficiency Channel 1, $5V_{IN}$ $3.3V_{OUT}$

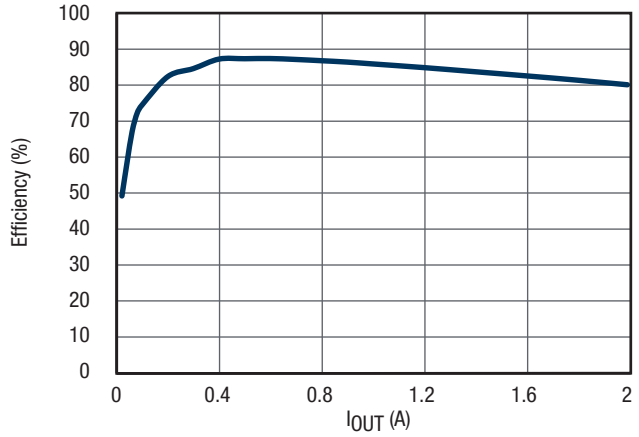


Figure 11. Efficiency Channel 2, $12V_{IN}$ $1.8V_{OUT}$

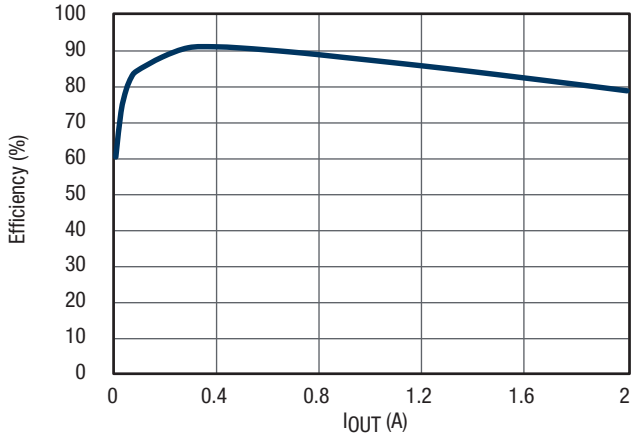


Figure 12. Efficiency Channel 2, $5V_{IN}$ $1.8V_{OUT}$

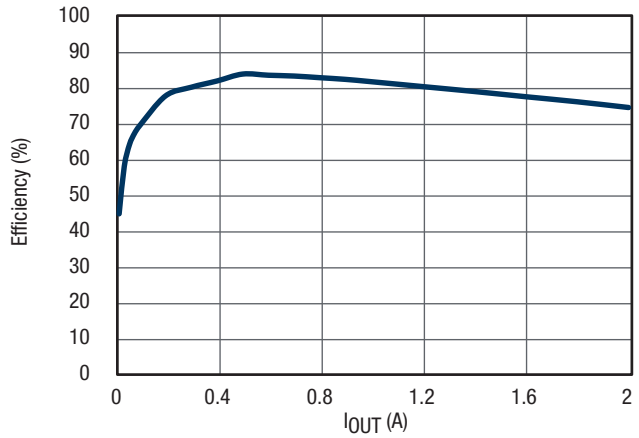


Figure 13. Efficiency Channel 3, $12V_{IN}$ $1.2V_{OUT}$

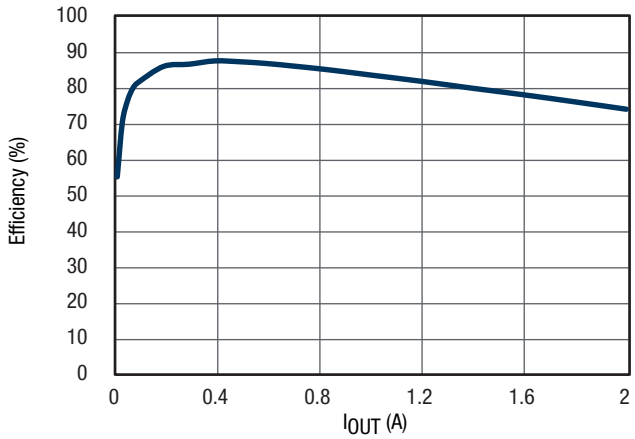


Figure 14. Efficiency Channel 3, $5V_{IN}$ $1.2V_{OUT}$

Typical Performance Characteristics (Continued)

Efficiency

f_{SW} = 1MHz, T_A = 25°C, no airflow, only individual channel operating, inductor losses are included.

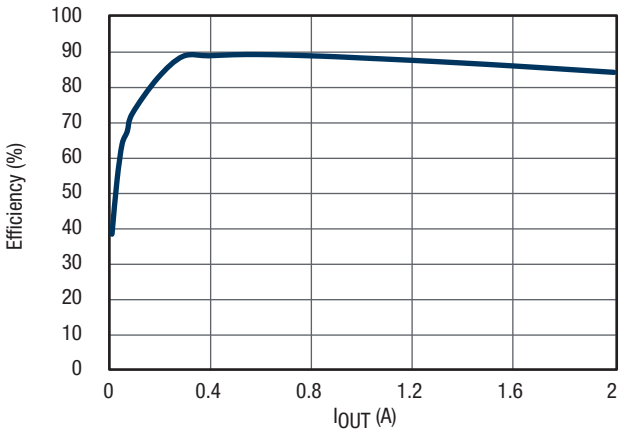


Figure 15. Efficiency Channel 1, $12V_{IN}$ $3.3V_{OUT}$

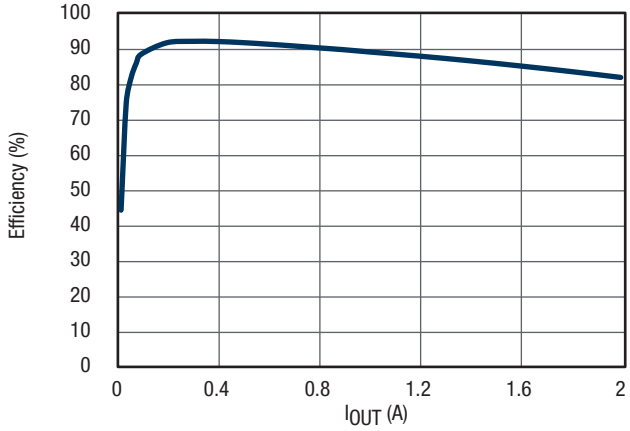


Figure 16. Efficiency Channel 1, $5V_{IN}$ $3.3V_{OUT}$

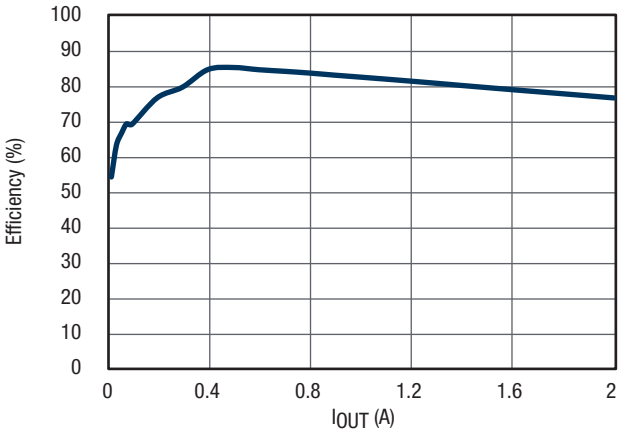


Figure 17. Efficiency Channel 2, $12V_{IN}$ $1.8V_{OUT}$

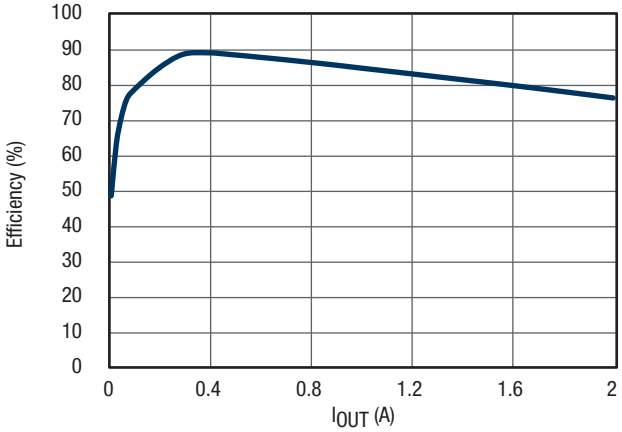


Figure 18. Efficiency Channel 2, $5V_{IN}$ $1.8V_{OUT}$

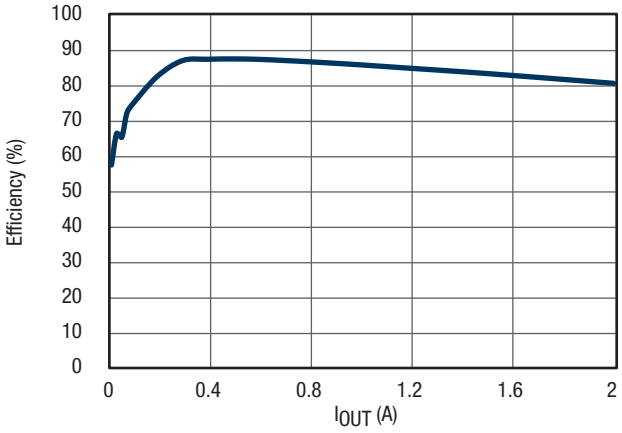


Figure 19. Efficiency Channel 3, $12V_{IN}$ $2.5V_{OUT}$

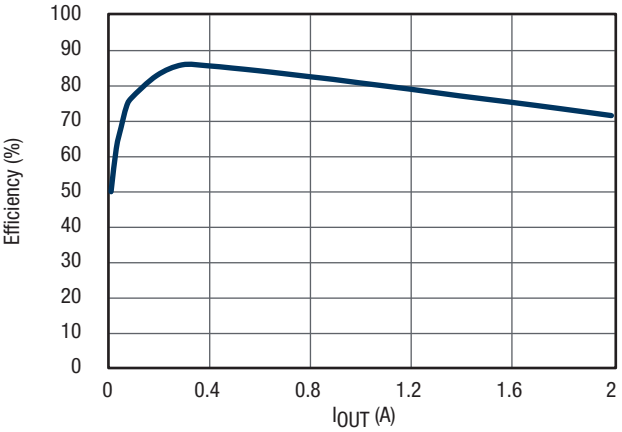


Figure 20. Efficiency Channel 3, $5V_{IN}$ $1.2V_{OUT}$

Typical Performance Characteristics (Continued)

Thermal Characteristics

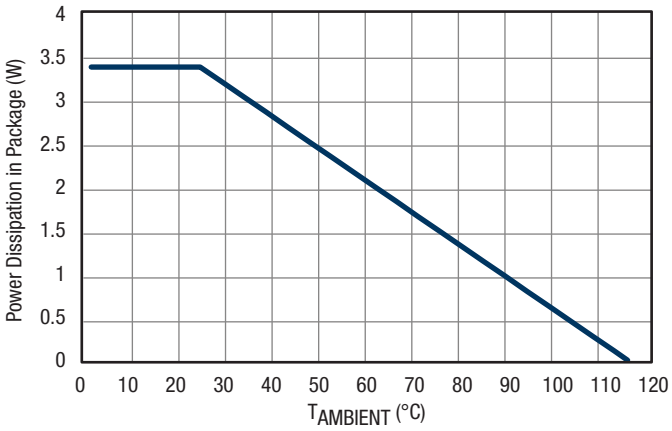


Figure 21. Package Thermal Derating

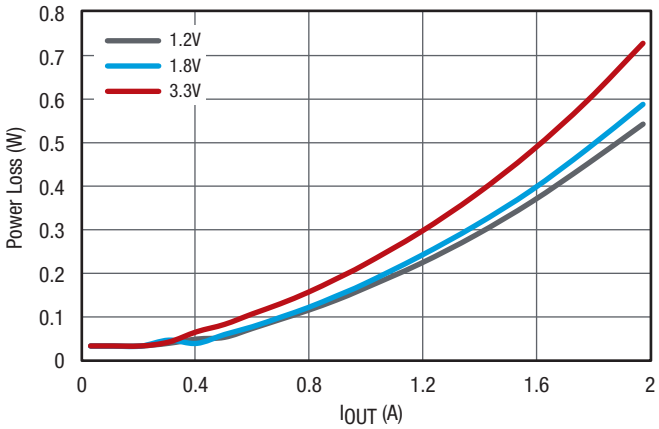


Figure 22. Channel 1 Power Loss at f_{SW} = 440kHz, V_{IN} = 12V, No Airflow

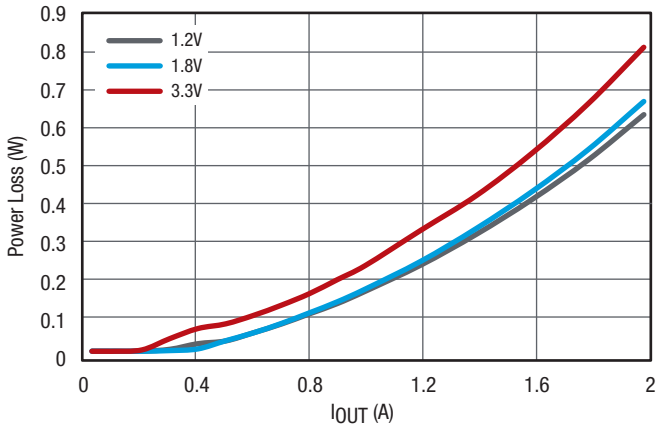


Figure 23. Channel 2 Power Loss at f_{SW} = 440kHz, V_{IN} = 12V, No Airflow

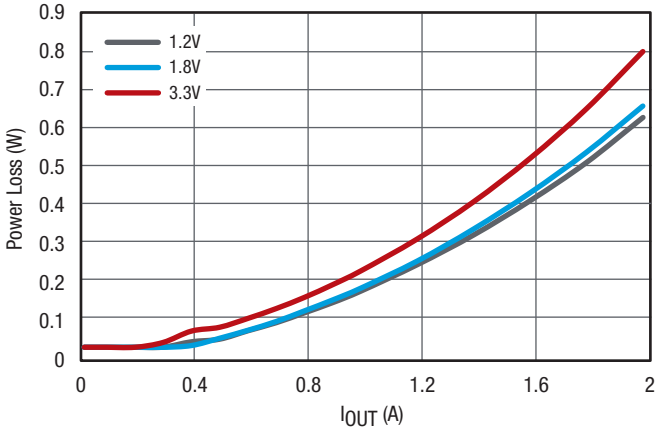


Figure 24. Channel 3 Power Loss at f_{SW} = 440kHz, V_{IN} = 12V, No Airflow

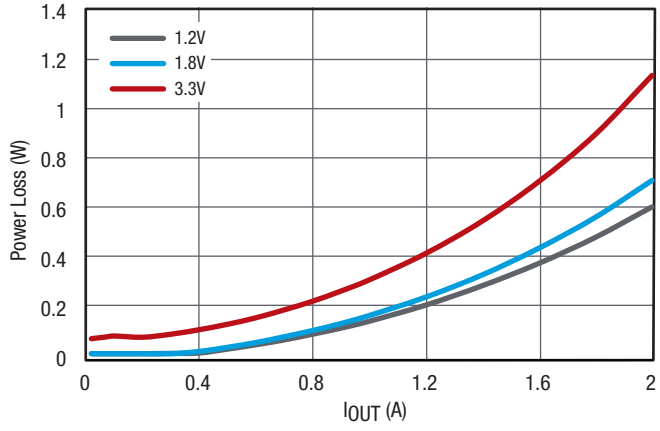


Figure 25. Channel 1 Power Loss at f_{SW} = 440kHz, V_{IN} = 5V, No Airflow

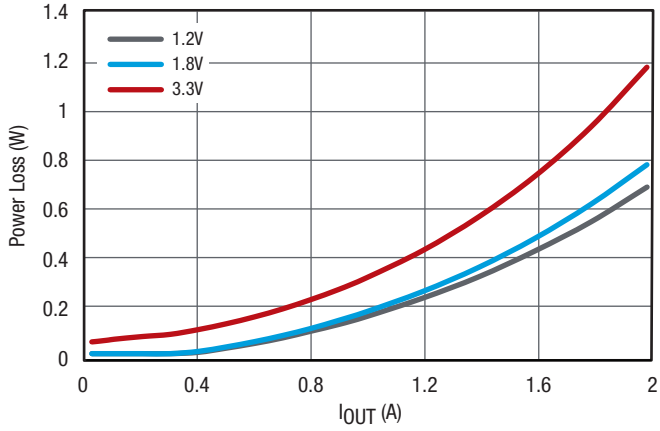


Figure 26. Channel 2 Power Loss at f_{SW} = 440kHz, V_{IN} = 5V, No Airflow

Typical Performance Characteristics (Continued)

Thermal Characteristics

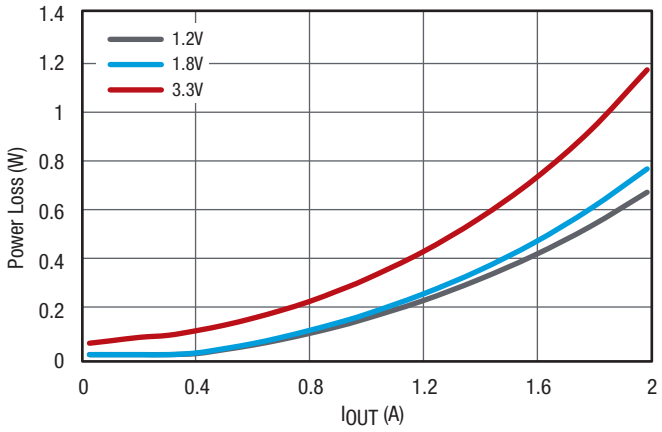


Figure 27. Channel 3 Power Loss at f_{SW} = 440kHz, V_{IN} = 5V, No Airflow

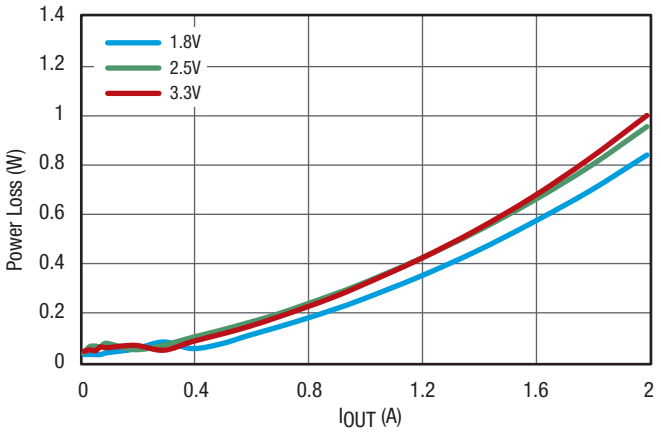


Figure 28. Channel 1 Power Loss at f_{SW} = 1MHz, V_{IN} = 12V, No Airflow

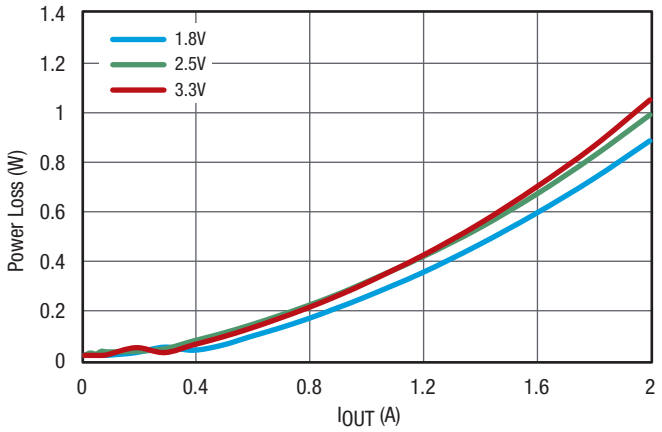


Figure 29. Channel 2 Power Loss at f_{SW} = 1MHz, V_{IN} = 12V, No Airflow

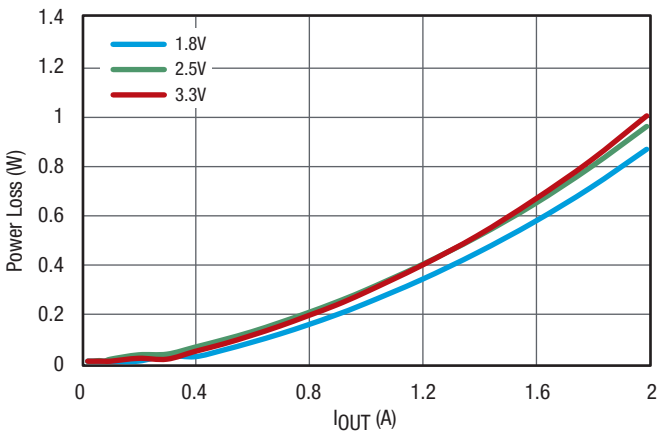


Figure 30. Channel 3 Power Loss at f_{SW} = 1MHz, V_{IN} = 12V, No Airflow

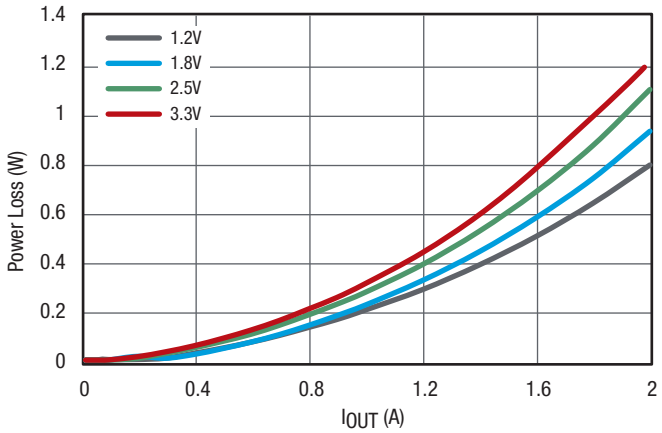


Figure 31. Channel 1 Power Loss at f_{SW} = 1MHz, V_{IN} = 5V, No Airflow

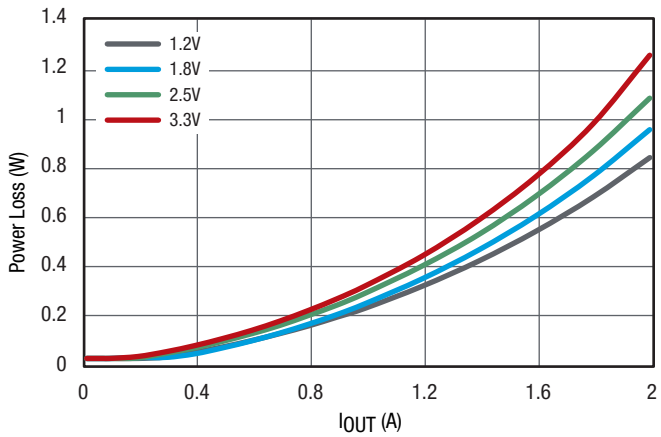


Figure 32. Channel 2 Power Loss at f_{SW} = 1MHz, V_{IN} = 5V, No Airflow

Typical Performance Characteristics (Continued)

Thermal Characteristics

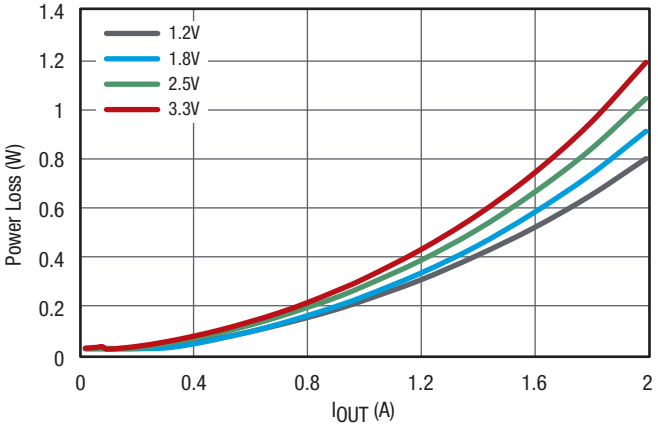


Figure 33. Channel 3 Power Loss at f_{SW} = 1MHz, V_{IN} = 5V, No Airflow

Functional Block Diagram

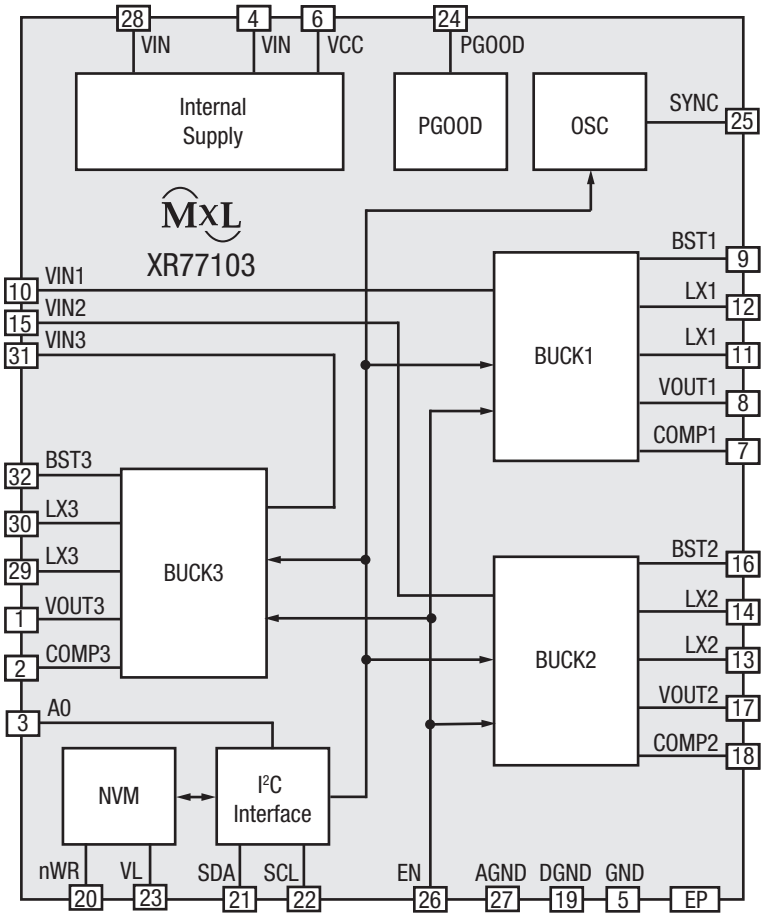


Figure 34. Functional Block Diagram

Applications Information

Operation

XR77103 is a power management IC with three step-down buck converters. Both high-side and low-side MOSFETs are integrated to provide fully synchronous conversion with higher efficiency. XR77103 can support a 4.5V to 14V input supply, high load current, and 440kHz to 2.3MHz clocking. The buck converters have an optional PSM mode which can improve power dissipation at light loads. Alternatively, the device implements a constant frequency mode. The wide switching frequency of 440kHz to 2.3MHz allows for efficiency and size optimization. The switching frequency is adjustable by writing data through I²C. The SYNC pin also provides means to synchronize the power converter to an external clock signal. Input ripple is reduced by operation 180 degrees out-of-phase among converters. All three buck converters have peak current mode control which simplifies external frequency compensation. Each buck converter has an individual peak inductor current limit which is set through I²C. The adjustable current limit enables high efficiency design with smaller and less expensive inductors. The device has a power good comparator monitoring the output voltages. Each converter has its own soft-start independently controlled through I²C.

Continuous Conduction Mode (CCM)

This is a natural mode of a synchronous buck converter. Advantage of the CCM mode is that the switching frequency is always constant and allows for better EMI control in the system. The downside of CCM mode is that at light loads system efficiency will become lower.

Pulse Skipping Mode (PSM)

In order to improve efficiency at light load, the device implements two functions. Both functions are enabled simultaneously. One function is a Zero Current Detect comparator (ZCD) which detects zero current in the inductor and turns off the synchronous MOSFET, preventing negative inductor current. This ensures that the device enters DCM mode as the load decreases. In this mode, the device still operates at a constant frequency. The second function is an internal skip comparator. This comparator detects low levels of output current. If low level is detected, the device will start to skip pulses. This is done to improve light load efficiency by effectively reducing switching frequency.

Minimum On-Time $t_{ON\ (min)}$ Considerations

The XR77103 can regulate with pulse widths as low as 95ns. However, to ensure sufficent control range, the design must use 120ns as the minimum on-time as stated in the electrical table. Failure to meet this condition when CCM is selected can result in overcharging of the output to the point that the OVP will shut down the output.

When operating in default PSM mode, failure to meet $t_{ON(MIN)}$ can result in overcharging of the output and V_{OUT} not meeting specification.

Output Voltage Setting

Output voltage of each converter can be programmed by I²C interface. It can be set from 0.8V to 6V with 6-bit resolution. The registers 00h to 02h are allocated to setting each output of the converters. Alternatively, output voltages can be set externally using external resistor dividers. Setting EXTx (bit 7) of the registers 00h to 02h allows external resistor divider for feedback. Output voltage is determined by the following equation.

$$V_{0X} = 0.8V \times \left(1 + \frac{R1}{R2}\right)$$

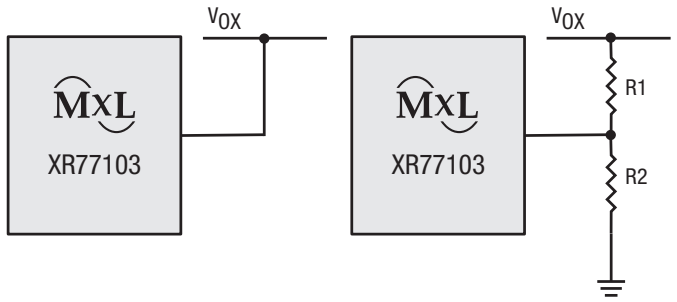


Figure 35. Output Voltage Setting

This feature can make the device applicable to an AVS (automatic voltage scaling) system. Output voltage can be adjusted automatically by external DC voltage. Figure 36 shows the application circuit of the supply for the AVS system.

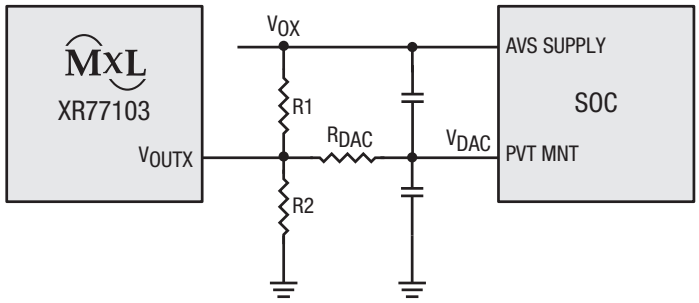


Figure 36. AVS Control

Applications Information (Continued)

Frequency Compensation

In order to properly frequency compensate the device, the following component selection is recommended. The table below is for 2A loads.

V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R_{COMP} (kΩ)	C_{COMP} (nF)
440kHz Switching Frequency					
12/5.0	1.0	2.2	47 x 2	20	2.2
12/5.0	1.2	2.2	47 x 2	20	2.2
12/5.0	1.5	3.3	22 x 3	20	4.7
12/5.0	1.8	3.3	22 x 2	20	4.7
12/5.0	2.5	4.7	22 x 2	20	4.7
12/5.0	3.3	4.7	22 x 1	20	4.7
12	5.0	6.8	22 x 1	20	4.7
1MHz Switching Frequency					
5.0	1.0	1.5	22 x 3	20	2.2
5.0	1.2	1.5	22 x 3	20	2.2
5.0	1.5	1.5	22 x 2	20	4.7
12/5.0	1.8	1.5	22 x 2	20	4.7
12/5.0	2.5	3.3	22 x 1	20	4.7
12/5.0	3.3	3.3	22 x 1	20	4.7
12	5.0	3.3	22 x 1	20	4.7

Switching Frequency Setting

Switching frequency can be set from 440kHz to 2.31MHz with a 140kHz step. Lower 5 bits of the register 09h are allocated to setting the switching frequency.

Current Limit Setting

Peak inductor current limit level of each converter can be set individually from 2A to 4.5A with a 0.5A step. The lower 3 bits of the registers 06h, 07h, and 08h are allocated to setting the peak inductor current limit of Buck 1, Buck 2, and Buck 3, respectively.

Soft-start Time Setting

Soft-start time of each converter can be set individually (see Figure 36). The lower 3 bits of the registers 03h, 04h, and 05h are allocated to setting the soft-start time of Buck 1, Buck 2, and Buck 3, respectively.

The soft-start times are relative to switching frequency. They scale with switching frequency.

At switching frequency set at 1MHz, the available soft-start range is from 0.5ms to 4ms with a 0.5ms step. If soft-start is set at less than 1.5ms when PSM is selected, V_{OUT} may overshoot initially by 3%.

At switching frequency set at 440kHz, the available soft-start range is from 1ms to 8ms with a 1ms step. If soft-start is set at less than 3ms when PSM is selected, V_{OUT} may overshoot initially by 3%.

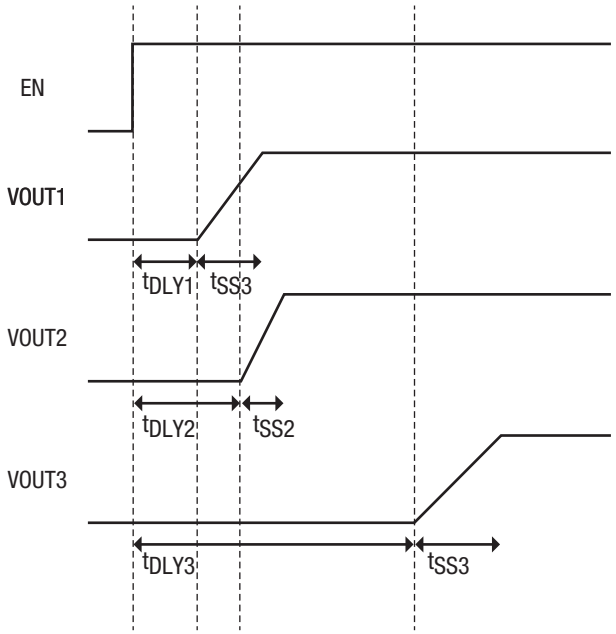


Figure 37. Programmable Soft-start Time and Delay Time of each Converter

Delayed Start-Up

All outputs start up once the EN pin is high and select bits of each converter are set. If a delayed start-up is required on any of the buck converters, set delay time of each converter. The bits [6:4] of the registers 03h, 04h, and 05h are allocated to setting delay time of Buck 1, Buck 2, and Buck 3, respectively.

The soft-start delay times are relative to switching frequency. They scale with switching frequency.

At switching frequency set at 1MHz, the available soft-start delay time range is from 0ms to 35ms with a 5ms step.

At switching frequency set at 440kHz, the available soft-start delay time range is from 0ms to 70ms with a 10ms step.

Applications Information (Continued)

Synchronization

The status of the SYNC pin will be ignored during start-up and the XR77103's control will only synchronize to an external signal after the PGOOD signal is asserted. When synchronization is applied, the PWM oscillator frequency must be lower than the sync pulse frequency to allow the external signal to trump the oscillator pulse reliably. When synchronization is not applied, the SYNC pin should be connected to AGND.

Although the device can lock to an external clock running up to 2.31MHz, doing this will alter the start-up times, start-up delays, and PGOOD delays, and there will be higher losses than what is shown in Figures 22-33.

Out-of-Phase Operation

All converters operate in phase, or one converter operates 180 degrees out-of-phase with the other two converters (see Figure 38). The phase shift among the converter is programmable. The bits 6, 5 of the register 09h are allocated for this feature. This enables the system, having less input ripple, to lower component cost, save board space and reduce EMI.

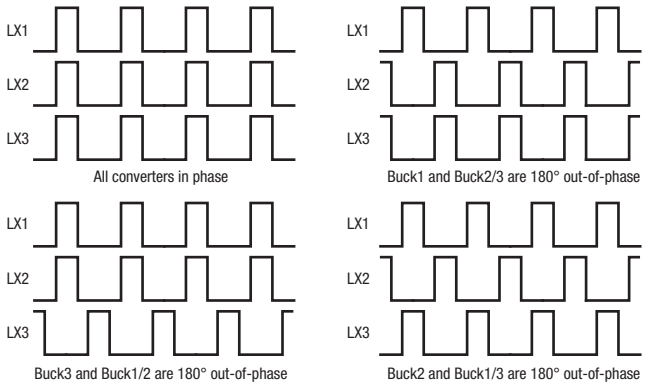


Figure 38. Out-of-Phase Operation

Two Buck Regulators in Parallel Operation (Current Sharing)

The XR77103 can be used in parallel operation to increase output current capacity. Figure 39 shows one of possible configurations. To enable this, a user needs to:

Hardware Configuration

a) Connect both V_{OUTx} together.

b) Connect both C_{OMPx} together.

Software Configuration

a) Set 180 out-of-phase operation between buck regulators (register 09h).

b) Program both V_{OUTx} to the same output.

Then, two out of three bucks will run in parallel and load current is shared in average.

The ideal case is to use Buck 2 and Buck 3 in parallel operation since they are both identical in design.

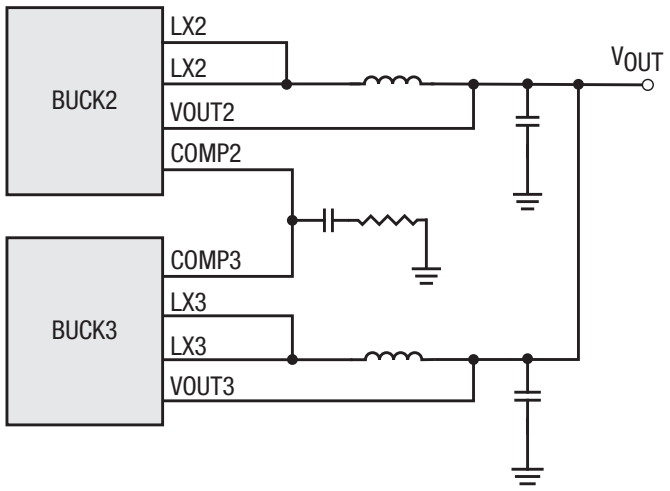


Figure 39. Parallel Operation

Applications Information (Continued)

Power Good

The PGOOD pin is an open drain output. The PGOOD pin is pulled low when any buck converter is pulled below 85% of the nominal output voltage. The PGOOD is pulled up when selected buck converters' outputs are more than 90% of their nominal output voltage and the PGOOD reset timer expires. The polarity of the PGOOD is active high. The PGOOD reset time is determined by following equation. Figure 40 shows the relationship between switching frequency and the PGOOD reset time. For example, when the switching frequency is 1MHz, the PGOOD reset time is 1s.

$$t_{RP} = \frac{1}{f_{SW}} \times 10^6$$

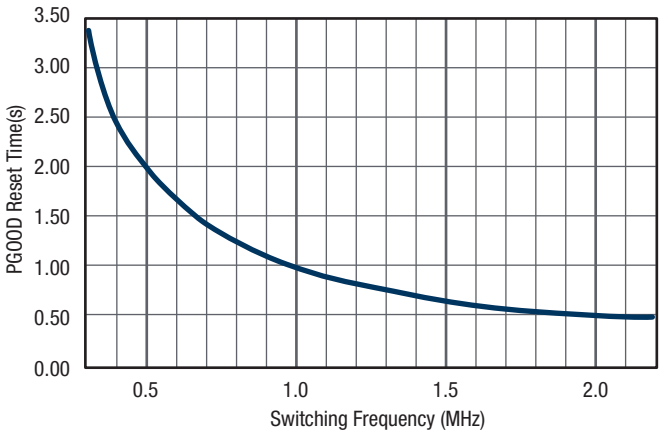


Figure 40. PGOOD Reset Time vs. f_{SW}

Selectable UVLO Threshold

The threshold for UVLO is selectable (7V/4.2V). When input voltage is higher, 9V and 12V for example, both settings can be used. However, when the input voltage is 5V, the UVLO setting must be 4.2V.

Supply Voltage for Data Programming and Writing to NVM

V_L is the supply voltage for I²C interface and is required for all I²C transactions. The V_L pin can be left floating if the I²C interface is not used.

To write data to NVM, V_{IN} must be 8V or higher.

The state of the nWR pin determines where the data gets written to. If the nWR pin is pulled low to ground, the data is written to the NVM. The I²C write transaction can start immediately after the nWR pin has been pulled low. A 100ms delay shall be added in between consecutive I²C writes to the NVM. After each byte is written to the NVM location, the data gets automatically transferred to the run time equivalent register. If the nWR pin is pulled high or left floating, the data gets written to run time registers.

When V_{IN} is below 8V, writing to NVM is not possible, and the nWR pin must be pulled high or left floating to assure reliable writing to run time registers.

V_L	V_{IN}	EN	nWR	I²C Write Behavior
3.3V	≥8V	LOW	LOW	Write to NVM, values loaded to run-time registers
3.3V	≥8V	HIGH	LOW	Not supported
3.3V	≤8V	X	LOW	Write has no effect
3.3V	4.5V to 14V	LOW	HIGH	Write to run-time registers with offsets > 02h
3.3V	4.5V to 14V	HIGH	HIGH	Not supported
3.3V	4.5V to 14V	X	HIGH	Write to run-time registers with offsets ≤ 02h

In addition, the nWR pin state determines where data gets read from in case a read I²C command is transmitted on the bus. When initiating a read transaction while the nWR pin is pulled high or left floating, the data is read from the run time registers. Reading run time registers can be done at any time.

On the other hand, if the nWR pin is pulled low at the time when a read transaction is sent, the data is read from NVM. It is recommended not to permanently pull the nWR pin low. In designs where the nWR pin is pulled low permanently, the host shall not initiate read transactions while channels are enabled. Failing to do so will cause regulation interruption. Reading in this scenario shall be done while EN is low and the channels are shut down.

V_L	V_{IN}	EN	nWR	I²C Read Behavior
3.3V	4.5V to 14V	LOW	LOW	Read from NVM (when all channels are disabled)
3.3V	4.5V to 14V	HIGH	LOW	Not supported
3.3V	4.5V to 14V	X	HIGH	Read from run-time registers

At power-on, the run-time registers are loaded with their default values from the NVM. This process takes approximately 200µs. No I²C operation should be performed during this time.

Applications Information (Continued)

Thermal Design

Proper thermal design is critical in controlling device temperatures and in achieving robust designs. There are a number of factors that affect the thermal performance. One key factor is the temperature rise of the devices in the package, which is a function of the thermal resistances of the devices inside the package and the power being dissipated.

The thermal resistance of the XR77103 (30°C/W) is specified in the Operating Conditions section of this datasheet. The θ_{JA} thermal resistance specification is based on the XR77103 evaluation board operating without forced airflow. Since the actual board design in the final application will be different, the thermal resistances in the final design may be different from those specified.

The package thermal derating and power loss curves are shown in Figures 21 through 33. These correspond to input voltages of 12V and 5V, and 440kHz and 1MHz switching frequencies.

Layout Guidelines

Proper PCB layout is crucial in order to obtain a good thermal and electrical performance.

For thermal considerations it is essential to use a number of thermal vias to connect the central thermal pad to the ground layer(s).

In order to achieve good electrical and noise performance following steps are recommended:

- Place the output inductor close to the LX pins and minimize the area of the connection. Doing this on the same layer is advisable.
- Central thermal pad, PGND, shall be connected as many layers as possible for good thermal performance. The input capacitors connected between VIN1, VIN2, VIN3 and PGND represent an AC current loop which should be minimized. PGND should connect to the system ground with vias placed at the output filtering capacitors.
- The AC current loop created by the output inductors, output filtering capacitors, and the regulator pins should also be minimized. However this loop is less critical than the input capacitors.
- GND, AGND, DGND can all be connected at the device and be connected to system ground at the output capacitor.
- Compensation networks shall be placed close to the pins and referenced to AGND.
- The VCC bypass capacitor shall be placed close to the pin and connected to AGND.

I²C Bus Interface

The XR77103 features an I²C compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the IC and the master device at clock rates up to 400kHz. The I²C interface follows all standard I²C protocols. Some information is provided below. For additional information, refer to the I²C-bus specifications.

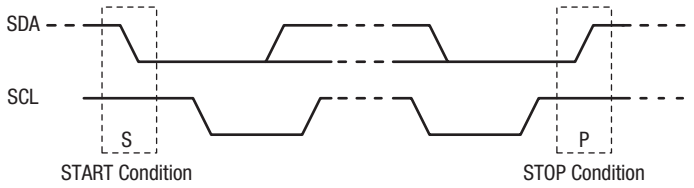


Figure 41. I²C Start and Stop Conditions

Start Condition

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 41.

Slave Address Cycle

After the start condition, the first byte sent by the master is the 7-bit address and the read / write direction bit R/W on the SDA line. If the address matches the XR77103's internal fixed I²C slave address, the XR77103 will respond with an acknowledgement by pulling the SDA line low for one clock cycle while SCL is high.

Data Cycle

After the master detects this acknowledgement, the next byte transmitted by the master is the sub-address. This 8-bit sub-address contains the address of the register to access. The XR77103 Register Map is on page 20.

Applications Information (Continued)

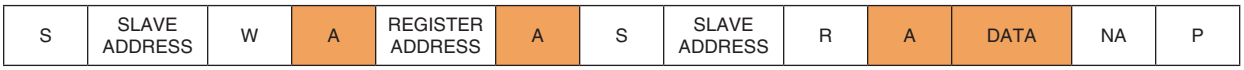
Stop Condition

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high, as shown in Figure 41.

Figures 42 and 43 illustrate a write and a read cycle. For complete details, see the I²C-bus specifications.

NOTES:
White Block = host to XR77103, Orange Block = XR77103 to host.

Figure 42. Master Writes to Slave



NOTES:
White Block = host to XR77103, Orange Block = XR77103 to host.

Figure 43. Master Reads from Slave

Slave Address

The slave address is one byte of data which is used as the unique identifier. The first 7 bits of the slave address are hard-coded and the least significant bit (LSB) of the slave address byte is the read / write (R/W) bit which is used to determine whether a command is a write command or a read command. The slave address is the first byte of information sent to the device after the START condition. Table below shows the possible slave addresses for the XR77103.

Device	Address (A0 = Low)	Address (A0 = High)
XR77103	0x74	0x75

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	0	1	0	A0	R/$\overline{W}$

Register Map

Register Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Factory Default NVM Value
00h	V_{BUCK1}	EXT1	V_{BUCK1} [6:0] V_{BUCK2} [6:0] V_{BUCK3} [6:0]							00h
01h	V_{BUCK2}	EXT2								
02h	V_{BUCK3}	EXT3								
03h	Soft-start and Delay 1	-	DLY1 [2:0]			-	SST1 [2:0]			15h
04h	Soft-start and Delay 2	-	DLY2 [2:0]			-	SST2 [2:0]			
05h	Soft-start and Delay 3	-	DLY3 [2:0]			-	SST3 [2:0]			
06h	Current Limit 1	-	-	-	-	-	LIM1 [2:0]			05h
07h	Current Limit 2	-	-	-	-	-	LIM2 [2:0]			
08h	Current Limit 3	-	-	-	-	-	LIM3 [2:0]			
09h	Switching Frequency and Phase	-	PHS [1:0]	-	FRQ [4:0]	-	-	-	-	40h
0Ah	PWR	-	UV	-	-	PSM	Buck3	Buck2	Buck1	7Fh

Applications Information (Continued)

V_{BUCK1} Register (00h)

The V_{BUCK1} register has 7 bits of data for setting the output of Buck 1 and 1 bit of data for use of external feedback voltage through a resistor divider. The Buck 1 programmable voltage range is from 0.8V to 6V with 0.05V resolution. When EXT1 is set to 1, the output voltage is adjusted by the external resistor divider from the output to ground with the center tap connected to the V_{OUT1} pin regardless of the value of the output voltage setting register. The factory default NVM value is 00h (0.8V).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXT1	D6	D5	D4	D3	D2	D1	D0

Hex	V_{OUT} (V)
00	0.8
01	0.85
02	0.9
03	0.95
04	1
05	1.05
06	1.1
07	1.15
08	1.2
09	1.25
0A	1.3
0B	1.35
0C	1.4
0D	1.45
0E	1.5
10	1.6
11	1.65
12	1.7
13	1.75
14	1.8
15	1.85
16	1.9
17	1.95
18	2
19	2.05

Hex	V_{OUT} (V)
1A	2.1
1B	2.15
1C	2.2
1D	2.25
1E	2.3
20	2.4
21	2.45
22	2.5
23	2.55
24	2.6
25	2.65
26	2.7
27	2.75
28	2.8
29	2.85
2A	2.9
2B	2.95
2C	3
2D	3.05
2E	3.1
30	3.2
31	3.25
32	3.3
33	3.35
34	3.4

Hex	V_{OUT} (V)
35	3.45
36	3.5
37	3.55
38	3.6
39	3.65
3A	3.7
3B	3.75
3C	3.8
3D	3.85
3E	3.9
40	4
41	4.05
42	4.1
43	4.15
44	4.2
45	4.25
46	4.3
47	4.35
48	4.4
49	4.45
4A	4.5
4B	4.55
4C	4.6
4D	4.65
4E	4.7

Hex	V_{OUT} (V)
50	4.8
51	4.85
52	4.9
53	4.95
54	5
55	5.05
56	5.1
57	5.15
58	5.2
59	5.25
5A	5.3
5B	5.35
5C	5.4
5D	5.45
5E	5.5
60	5.6
61	5.65
62	5.7
63	5.75
64	5.8
65	5.85
66	5.9
67	5.95
68	6

Applications Information (Continued)

V_{BUCK2} Register (01h)

The V_{BUCK2} register has 7 bits of data for setting the output of Buck 2 and 1 bit of data for use of external feedback voltage through a resistor divider. The Buck 2 programmable voltage range is from 0.8V to 6V with 0.05V resolution. When EXT2 is set to 1, the output voltage is adjusted by the external resistor divider from the output to ground with the center tap connected to the V_{OUT2} pin regardless of the value of the output voltage setting register. The factory default NVM value is 00h (0.8V).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXT2	D6	D5	D4	D3	D2	D1	D0

V_{BUCK3} Register (02h)

The V_{BUCK3} register has 7 bits of data for setting the output of Buck 3 and 1 bit of data for use of external feedback voltage through a resistor divider. The Buck 3 programmable voltage range is from 0.8V to 6V with 0.05V resolution. When EXT3 is set to 1, the output voltage is adjusted by the external resistor divider from the output to ground with the center tap connected to the V_{OUT3} pin regardless of the value of the output voltage setting register. The factory default NVM value is 00h (0.8V).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXT3	D6	D5	D4	D3	D2	D1	D0

SST1 and DLY1 Register (03h)

The soft-start time 1 and delay time 1 register has 6 effective bits. Three bits are for setting the soft-start time of Buck 1 and three bits are for setting the delay time from EN to Buck 1 start-up. The factory default soft-start and delay times are 6ms and 10ms, respectively, at 440kHz switching frequency. Both soft-start and delay times are relative to the switching frequency. They will be two times smaller at 1MHz switching frequency.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	D6	D5	D4	X	D2	D1	D0

D2	D1	D0	t_{SS} (ms) at f_{SW} = 440kHz	t_{SS} (ms) at f_{SW} = 1MHz
0	0	0	1	0.5
0	0	1	2	1
0	1	0	3	1.5
0	1	1	4	2
1	0	0	5	2.5
1	0	1	6	3
1	1	0	7	3.5
1	1	1	8	4

D6	D5	D4	t_{DLY} (ms) at f_{SW} = 440kHz	t_{DLY} (ms) at f_{SW} = 1MHz
0	0	0	0	0
0	0	1	10	5
0	1	0	20	10
0	1	1	30	15
1	0	0	40	20
1	0	1	50	25
1	1	0	60	30
1	1	1	70	35

Applications Information (Continued)

SST2 and DLY2 Register (04h)

The soft-start time 2 and delay time 2 register has 6 effective bits. Three bits are for setting the soft-start time of Buck 2 and three bits are for setting the delay time from EN to Buck 2 start-up. The factory default soft-start and delay times are 6ms and 10ms, respectively, at 440kHz switching frequency. Both soft-start and delay times are relative to the switching frequency. They will be two times smaller at 1MHz switching frequency.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	D6	D5	D4	X	D2	D1	D0

SST3 and DLY3 Register (05h)

The soft-start time 3 and delay time 3 register has 6 effective bits. Three bits are for setting the soft-start time of Buck 3 and three bits are for the setting delay time from EN to Buck 3 start-up. The factory default soft-start and delay times are 6ms and 10ms respectively at 440kHz switching frequency. Both soft-start and delay times are relative to the switching frequency. They will be two times smaller at 1MHz switching frequency.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	D6	D5	D4	X	D2	D1	D0

Current Limit 1 Register (06h)

The current limit 1 register has 3 effective bits. The factory default value is 4A (05h).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	D2	D1	D0

D2	D1	D0	I_{LIM1}(A)
0	0	1	2
0	1	0	2.5
0	1	1	3
1	0	0	3.5
1	0	1	4
1	1	0	4.5

Current Limit 2 Register (07h)

The current limit 2 register has 3 effective bits. The factory default value is 4A (05h).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	D2	D1	D0

Current Limit 3 Register (08h)

The current limit 3 register has 3 effective bits. The factory default value is 4A (05h).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	D2	D1	D0

Applications Information (Continued)

Switching Frequency and Phase Register (09h)

The switching frequency and phase register has 7 effective bits. The 5 least significant bits are setting the switching frequency. The factory default value is 440kHz (00000b).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	D6	D5	D4	D3	D2	D1	D0

D [4:0] Hex	f_{SW} [MHz]
00	0.44
01	0.58
02	0.72
03	0.86
04	1.00
05	1.14
06	1.28

D [4:0] Hex	f_{SW} [MHz]
07	1.42
08	1.56
09	1.70
0A	1.84
0B	1.98
0C	2.12

Bits 5 and 6 are for setting the phase shift among the buck converters. The factory default value is channel 3 180° out-of-phase in respect to the channels 1 and 2 (10b).

D6	D5	Phase Shift
0	0	All converters operate in phase
0	1	Buck1 and Buck2/3 operate 180° out-of-phase
1	0	Buck1/2 and Buck3 operate 180° out-of-phase
1	1	Buck1/3 and Buck2 operate 180° out-of-phase

PWR Register (0Ah)

PWR register has 5 effective bits. Bits 0-2 select which channels will be enabled at the transition of the ENABLE pin from low to high. The state of bit 3 determines whether the buck converters operate in Pulse Skipping Mode or not. Setting this bit to 1 allows Pulse Skipping Mode operation to minimize power losses at light load levels. Bit 6 determines threshold voltage for V_{IN} UVLO. The factory default of this register is 7Fh.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	UV	X	X	PSM	BUCK 3	BUCK 2	BUCK 1

		0	1
D0	BUCK 1	Not Used	Select
D1	BUCK 2	Not Used	Select
D2	BUCK 3	Not Used	Select
D3	PSM	Disable	Enable
D6	UV	4.2V	7V

Applications Information (Continued)

Typical Applications

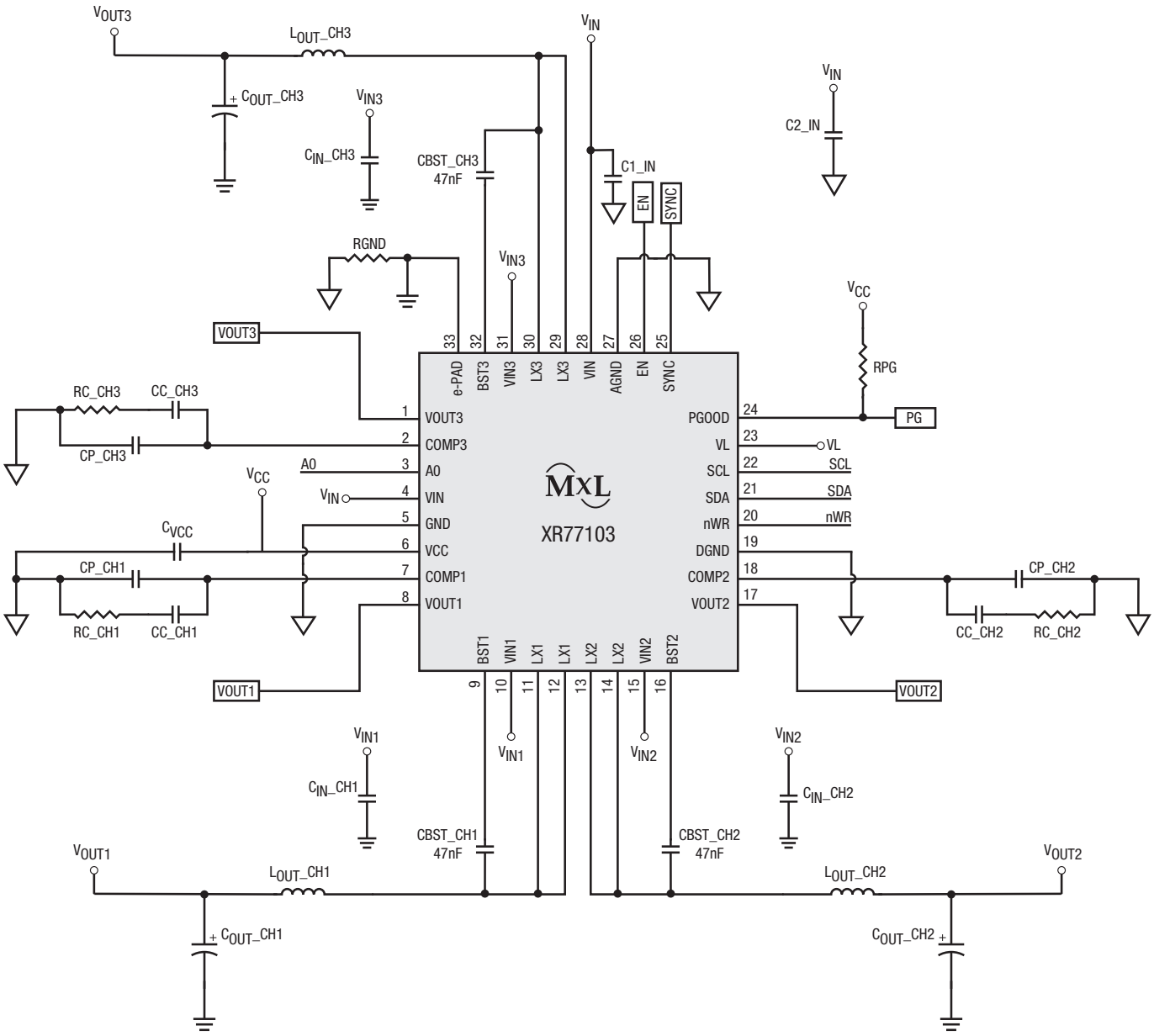
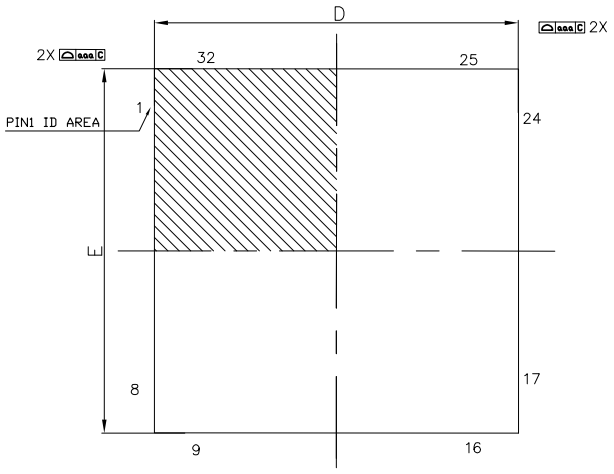
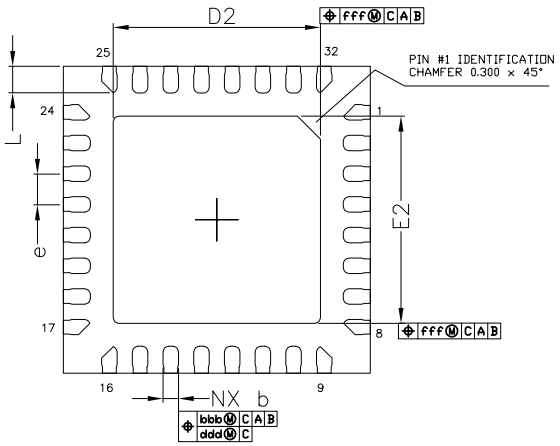


Figure 44. Typical Applications Schematic

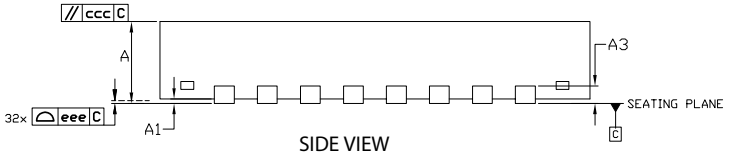
Mechanical Dimensions



TOP VIEW



BOTTOM VIEW



SIDE VIEW

DIM / SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203Ref	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
L	0.30	0.35	0.40
K	0.20	–	–
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
N		32	

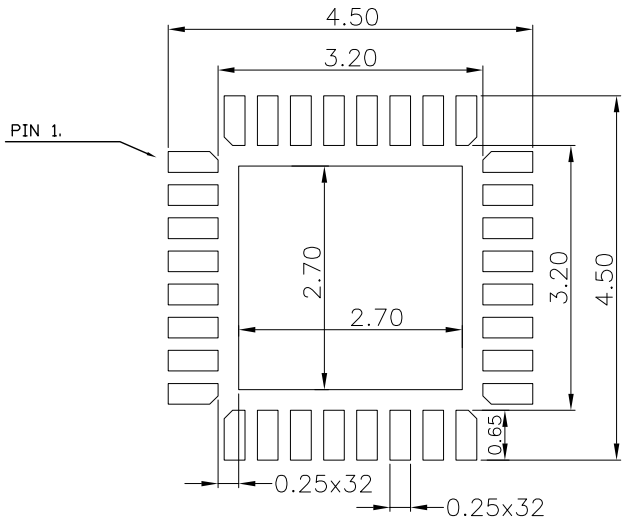
TERMINAL DETAILS

- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-220.

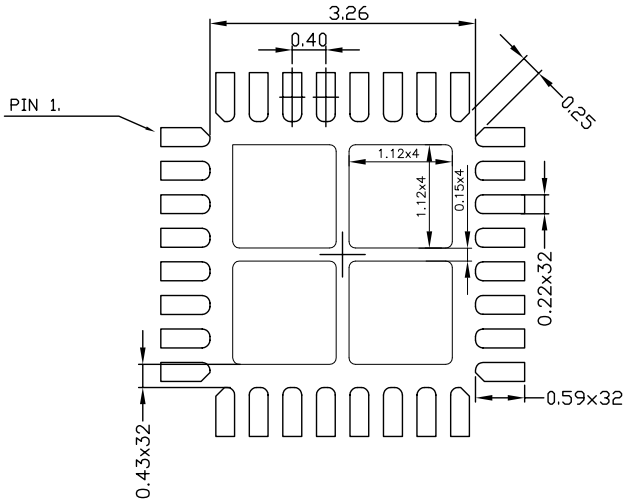
Drawing No.: POD-00000079

Revision: C

Recommended Land Pattern and Stencil



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

Drawing No.: POD-00000079

Revision: C

Order Information[1]

Part Number	Operating Temperature Range	Lead-Free	Package	Packaging Method
XR77103ELBTR	-40°C ≤ T_J ≤ 125°C	Yes[2]	32-pin, 4mm x 4mm TQFN package	Tape and Reel
XR77103EVB-DEMO-1	XR77103 evaluation board			
XR77103EVB-DEMO-1-KIT	XR77103 evaluation board with interface board and software			

NOTE:
1. Refer to www.maxlinear.com/XR77103 for most up-to-date Ordering Information.
2. Visit www.maxlinear.com for additional information on Environmental Rating.

Revision History

Revision	Date	Description
1A	March 2016	Initial Release
1B	May 2016	Clarified Pin Descriptions. Added description for Continuous Conduction Mode and Pulse Skipping Mode. Added I²C Bus Timing waveform and updated I²C symbols and functional description. Added details for NVM programming and behavior. Added factory default NVM value to Register Map table. Updated Application Circuit. Updated layout guidelines.
1C	November 2017	Added MaxLinear logo. Updated format and ordering information format. Changed Packaging Description section name to Mechanical Dimensions and Recommended Land Pattern and Stencil. Corrected typo on Mechanical Dimensions, dimension A.
1D	January 2019	Updated I_{LIMx} current range and accuracy, output voltage accuracy, Frequency Compensation Table and Soft-start Time Setting Section. Added Minimum On-Time section, updated Switching Frequency and Phase Register (09h) section. Updated input thresholds. Updated register 06h, bits 0-2. Updated Ordering Information.
1E	April 2019	PGOOD output specification change from pull-down resistance to voltage level. Updated switching frequency, peak inductor current limit range and accuracy, Current Limit 1 Register (06h) and default value of Current Limit Registers (06h - 08h) and Switching Frequency and Phase Register (09h).
1F	September 2019	Updated Typical Application Diagram to clarify I²C operation.

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