

## GENERAL DESCRIPTION

The [XRP6141](#) is a synchronous step-down controller for point-of load supplies up to 35A. A wide 4.5V to 22V input voltage range allows for single supply operation from industry standard 5V, 12V, and 19.6V rails.

With a proprietary emulated current mode Constant On-Time (COT) control scheme, the XRP6141 provides extremely fast line and load transient response using ceramic output capacitors. It requires no loop compensation, hence simplifying circuit implementation and reducing overall component count. The control loop also provides exceptional line regulation and maintains constant operating frequency. A selectable power saving mode allows the user to operate in discontinuous mode (DCM) at light current loads, thereby significantly increasing the converter efficiency.

A host of protection features, including over-current, over-temperature, short-circuit, and UVLO, help achieve safe operation under abnormal operating conditions.

The XRP6141 is available in a RoHS compliant, green / halogen free space-saving 16-pin 3x3mm QFN package.

## APPLICATIONS

- **Networking and communications**
- **Fast transient Point-of-Loads**
- **Industrial and medical equipment**
- **Embedded high power FPGA**

## FEATURES

- **35A capable step down controller**
  - Wide input voltage range
    - 5V to 22V single supply
    - 4.5V to 5.5V low  $V_{IN}$
  - Integrated high current 2A/3A drivers
  - 0.6V to 18V adjustable output voltage
- **Proprietary Constant On-Time control**
  - No loop compensation required
  - Ceramic output capacitor stable operation
  - Programmable 200ns - 2 $\mu$ s
  - Constant 200kHz - 800kHz frequency
  - Selectable CCM or CCM / DCM operation
- **Programmable hiccup current limit with thermal compensation**
- **Precision enable and Power-Good flag**
- **Programmable soft-start**
- **Integrated bootstrap diode**
- **16-pin QFN package**

## TYPICAL APPLICATION DIAGRAM

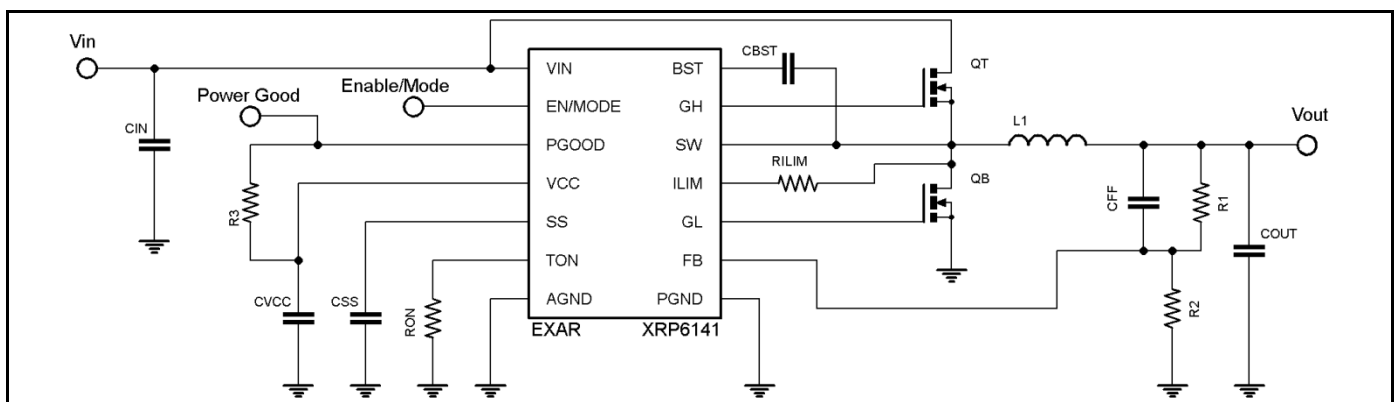


Fig. 1: XRP6141 Application Diagram

## 35A Synchronous Step Down COT Controller

### ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

$V_{IN}$ .....	-0.3V to 28V
$V_{CC}$ .....	-0.3V to 6.0V
BST .....	-0.3V to 34V <sup>2</sup>
BST-SW .....	-0.3V to 6V
SW, ILIM .....	-5V to 28V <sup>1,2</sup>
GH.....	-0.3V to BST+0.3V
GH-SW.....	-0.3V to 6V
ALL other pins.....	-0.3V to $V_{CC}+0.3V$
Storage temperature .....	-65°C to 150°C
Junction temperature.....	150°C
Power dissipation .....	Internally Limited
Lead temperature (Soldering, 10 sec) .....	300°C
ESD rating (HBM - Human Body Model).....	2kV

### OPERATING RATINGS

$V_{IN}$ .....	-0.3V to 22V
$V_{CC}$ .....	-0.3V to 5.5V
SW, ILIM .....	-1V to 26V <sup>1</sup>
PGOOD, VCC, TON, SS, EN, GL, FB .....	-0.3V to 5.5V
Switching frequency .....	200kHz - 800kHz <sup>3</sup>
Junction temperature range .....	-40°C to 125°C

Note 1: SW pin's minimum DC range is -1V, transient is -5V for less than 50ns

Note 2: No external voltage applied

Note 3: Recommended

### ELECTRICAL SPECIFICATIONS

Specifications are for the operating junction temperature of  $T_J = 25^\circ\text{C}$  only; limits applying over the full operating junction temperature range are denoted by a "•". Minimum and maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$ , and are provided for reference purposes only. Unless otherwise indicated,  $V_{IN} = 12V$ , BST = VCC, SW = GND = PGND = 0V, CGH = CGL = 3.3nF.

Parameter	Min.	Typ.	Max.	Units	Conditions
<b>Power Supply Characteristics</b>					
$V_{IN}$ , input voltage range	5	12	22	V	• VCC regulating • VCC tied to $V_{IN}$
	4.5	5.0	5.5		
$I_{VIN}$ , $V_{IN}$ supply current		0.7	2	mA	• Not switching, $V_{IN} = 12V$ , VFB = 0.7V
$I_{VCC}$ , VCC quiescent current		0.7	2	mA	• Not switching, $V_{CC} = V_{IN} = 5V$ , VFB = 0.7V
$I_{VIN}$ , $V_{IN}$ supply current		11		mA	f = 300kHz, RON = 108.8k, VFB = 0.58V
$I_{OFF}$ , shutdown current		0.1		µA	Enable = 0V, $V_{IN} = 12V$
<b>Enable and Under-Voltage Lock-Out UVLO</b>					
$V_{IH\_EN}$ , EN pin rising threshold	1.8	1.9	2.0	V	•
$V_{EN\_HYS}$ , EN pin hysteresis		50		mV	
$V_{IH\_EN}$ , EN pin rising threshold for DCM/CCM operation	2.9	3.0	3.1	V	•
$V_{EN\_HYS}$ , EN pin hysteresis		100		mV	
VCC UVLO start threshold, rising edge	4.00	4.25	4.50	V	•
VCC UVLO hysteresis		200		mV	
<b>Reference Voltage</b>					
$V_{REF}$ , reference voltage	0.597	0.600	0.603	V	$V_{IN} = 5V-22V \rightarrow$ VCC regulating
	0.596		0.604	V	$V_{IN} = 4.5V-5.5V \rightarrow$ tie VCC to $V_{IN}$
	0.594	0.600	0.606	V	• $V_{IN} = 5V-22V \rightarrow$ VCC regulating, $V_{IN} = 4.5V-5.5V \rightarrow$ tie VCC to $V_{IN}$
DC line regulation		±0.1		%	CCM operation, closed loop, applies to any $C_{OUT}$
DC load regulation		±0.25		%	CCM operation, closed loop, applies to any $C_{OUT}$

**35A Synchronous Step Down COT Controller**

Parameter	Min.	Typ.	Max.	Units	Conditions
<b>Programmable Constant On-Time</b>					
On-time 1	1855	2182	2509	ns	• RON = 141.2kΩ, VIN = 22V
f corresponding to on-time 1	217	250	294	kHz	VIN = 22V, VOUT = 12V
Minimum programmable on-time		109		ns	RON = 7.059kΩ, VIN = 22V
On-time 2	170	200	230	ns	• RON = 7.059kΩ, VIN = 12V
f corresponding to on-time 2	1618	1375	1196	kHz	VOUT = 3.3V
f corresponding to on-time 2	490	417	362	kHz	VOUT = 1.0V
On-time 3	391	460	529	ns	• RON = 16.235kΩ, VIN = 12V
Minimum off-time		250	350	ns	•
<b>Diode Emulation Mode</b>					
Zero crossing threshold	-4	-1		mV	DC value measured during test
<b>Soft-Start</b>					
SS charge current	-14	-10	-6	μA	•
SS discharge current	1			mA	• Fault present
<b>VCC Linear Regulator</b> (VCC should be tied to VIN, for 4.5V ≤ VIN ≤ 5.5V)					
VCC output voltage	4.8	5.0	5.2	V	• VIN = 6V to 22V, Iload = 0 to 30mA
	4.51	4.7			• VIN = 5V, Iload = 0 to 20mA
Dropout voltage		200	490	mV	• IVCC = 30mA
<b>Power Good Output</b>					
Power Good threshold	-10	-7.5	-5	%	
Power Good hysteresis		2	4	%	
Power Good sink current	1			mA	
<b>Protection: OCP, OTP, Short-circuit</b>					
Hiccup timeout		110		ms	
ILIM pin source current	45	50	55	μA	
ILIM current temperature coefficient		0.4		%/°C	
OCP comparator offset	-8	0	+8	mV	•
Current limit blanking		100		ns	GL rising > 1V
Thermal shutdown threshold <sup>1</sup>		150		°C	Rising temperature
Thermal hysteresis <sup>1</sup>		15		°C	
VSCTH feedback pin short-circuit threshold	50	60	70	%	• Percent of VREF, short circuit is active after PGOOD is up
<b>Output Gate drivers</b>					
GH pull-down resistance		1.35	2.0	Ω	IGH = 200mA
GH pull-up resistance		1.8	2.8	Ω	IGH = 200mA
GL pull-down resistance		1.35	1.9	Ω	IGL = 200mA
GL pull-up resistance		1.7	2.7	Ω	IGL = 200mA
GH and GL pull-down resistance		50	---	kΩ	
GH and GL rise time		35	50	ns	10% to 90%
GH and GL fall time		30	40	ns	90% to 10%
GL to GH non-overlap time	20	30	60	ns	Measured GL falling edge = 1V to GH rising edge = 1V, BST = VCC, SW = 0V
GH to GL non-overlap time	15	20	40	ns	Measured GH falling edge = 1V to GL rising edge = 1V

Note 1: Guaranteed by design

**BLOCK DIAGRAM**

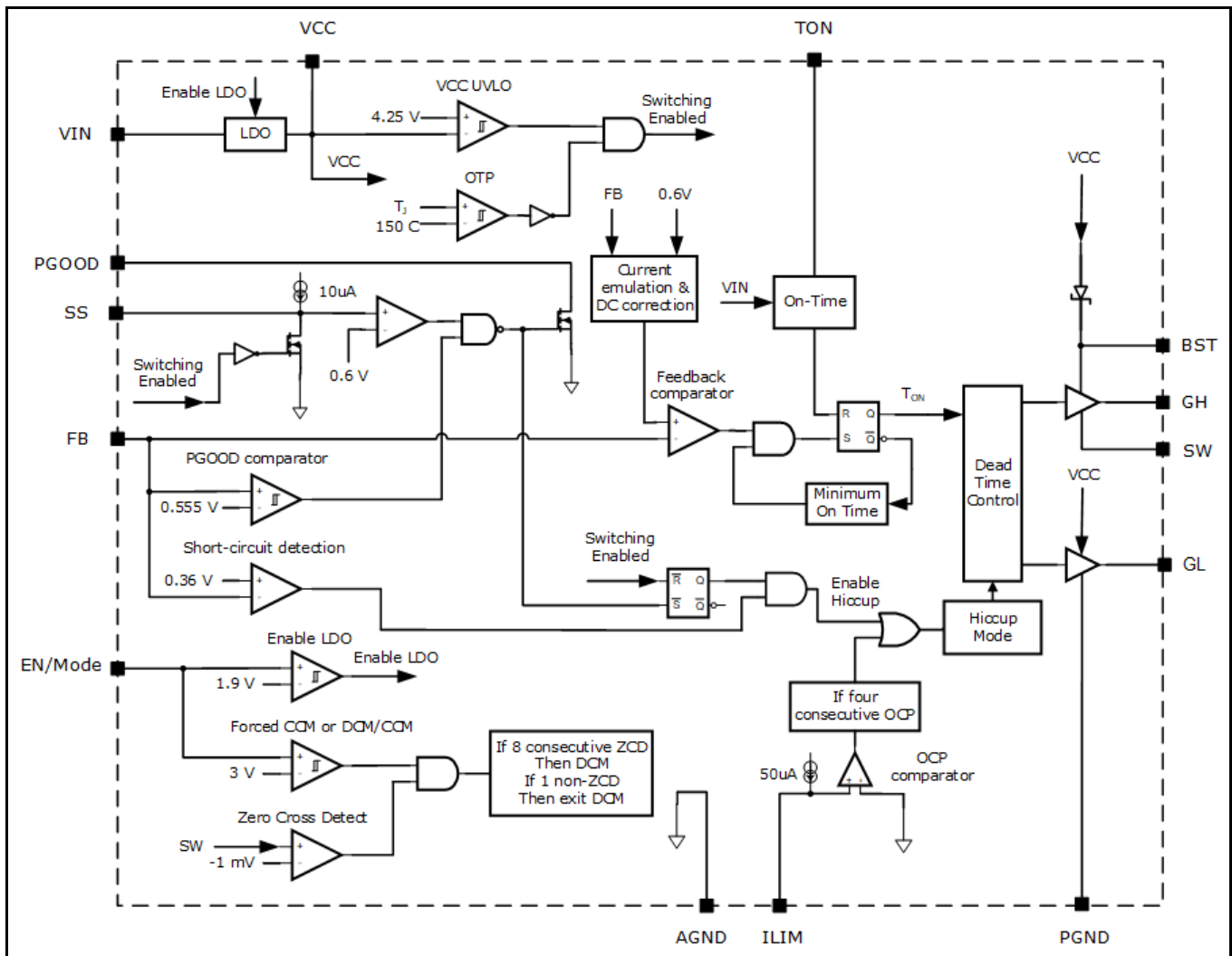


Fig. 2: XRP6141 Block Diagram

**PIN ASSIGNMENT**

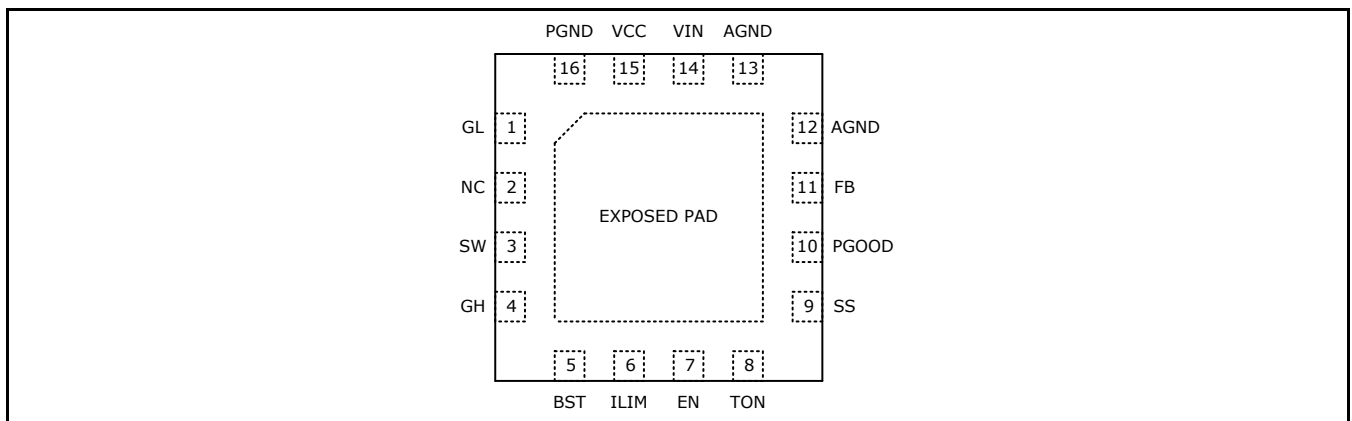


Fig. 3: XRP6141 Pin Assignment

**35A Synchronous Step Down COT Controller**
**PIN DESCRIPTION**

Name	Pin Number	Description
GL	1	Driver output for Low-side N-channel synchronous MOSFET.
NC	2	Internally not connected. Leave this pin floating.
SW	3	Lower supply rail for high-side gate driver GH. Connect this pin to the junction between the two external N-channel MOSFETs.
GH	4	Driver output for high-side N-channel switching MOSFET.
BST	5	High-side driver supply pin. Connect a 0.1 $\mu$ F bootstrap capacitor between BST and SW.
ILIM	6	Over-current protection programming. Connect with a resistor to the drain of the low-side MOSFET.
EN/MODE	7	Precision enable pin. Pulling this pin above 1.9V will turn the IC on and it will operate in Forced CCM. If the voltage is raised above 3.0V, then the IC will operate in DCM or CCM, depending on load.
TON	8	Constant on-time programming pin. Connect with a resistor to AGND.
SS	9	Soft-start pin. Connect an external capacitor between SS and AGND to program the soft-start rate based on the 10 $\mu$ A internal source current.
PGOOD	10	Power-good output. This open-drain output is pulled low when V <sub>OUT</sub> is outside the regulation.
FB	11	Feedback input to feedback comparator. Connect with a set of resistors to V <sub>OUT</sub> and GND in order to program V <sub>OUT</sub> .
AGND	12, 13	Analog ground. Control circuitry of the IC is referenced to this pin.
VIN	14	IC supply input. Provides power to internal LDO.
VCC	15	The output of LDO. For operation using a 5V rail, VCC should be shorted to VIN.
PGND	16	Low side driver ground.
Exposed Pad		Thermal pad for heat dissipation. Connect to AGND with a short trace.

**ORDERING INFORMATION<sup>(1)</sup>**

Part Number	Operating Temperature Range	Package	Packing Method	Lead-Free
XRP6141ELTR-F	-40°C ≤ T <sub>J</sub> ≤ +125°C	3x3mm QFN16	Tape & Reel	Yes <sup>(2)</sup>
XRP6141EVB	XRP6141 Evaluation Board			

**NOTES:**

1. Refer to [www.maxlinear.com/XRP6141](http://www.maxlinear.com/XRP6141) for most up-to-date Ordering Information
2. Visit [www.maxlinear.com](http://www.maxlinear.com) for additional information on Environmental Rating.

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### TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at  $V_{IN} = 12V$ ,  $V_{OUT} = 1.2V$ ,  $f = 300kHz$ ,  $T_A = 25^\circ C$ , unless otherwise specified - schematic and BOM from Application Information section of this datasheet.

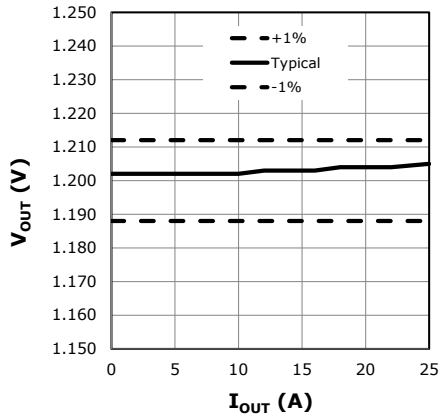


Fig. 4: Load Regulation,  $V_{IN} = 12V$

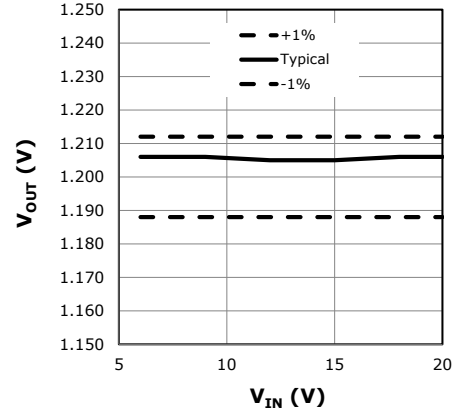


Fig. 5: Line Regulation,  $I_{OUT} = 25A$

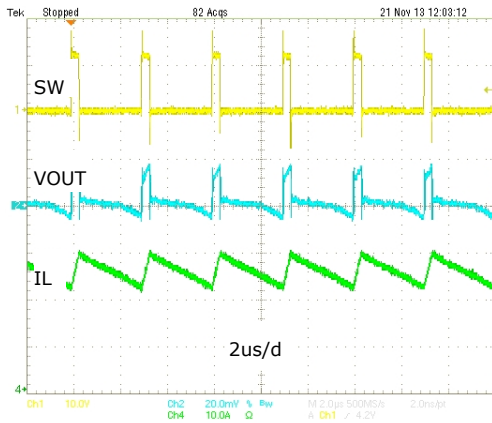


Fig. 6:  $V_{OUT}$  Ripple is 22mV at 25A, 12VIN, 1.2VOUT

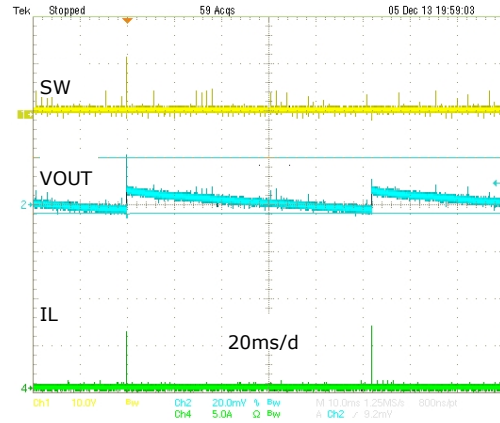


Fig. 7:  $V_{OUT}$  Ripple is 22mV at 0A, DCM, 12VIN, 1.2VOUT

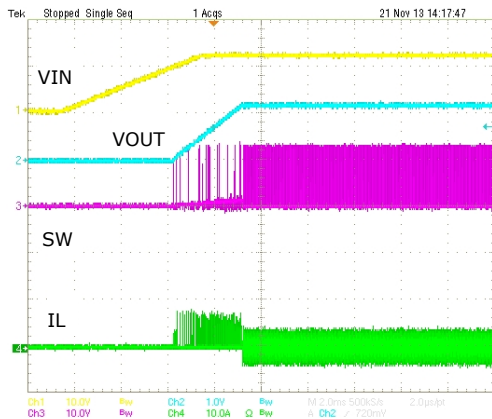


Fig. 8: Powerup, Forced CCM,  $I_{OUT} = 0A$

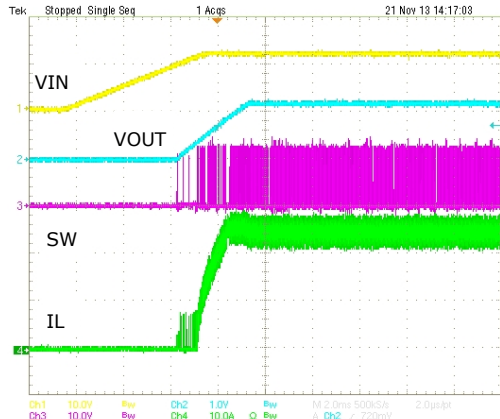


Fig. 9: Powerup, Forced CCM,  $I_{OUT} = 25A$

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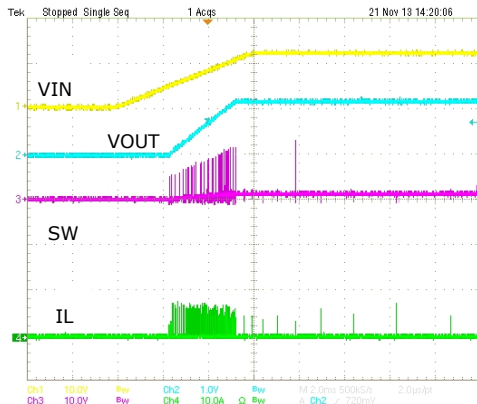


Fig. 10: Powerup, DCM / CCM,  $I_{OUT} = 0A$

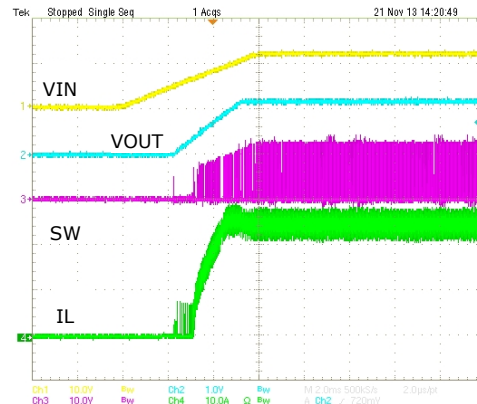


Fig. 11: Powerup, DCM / CCM,  $I_{OUT} = 25A$

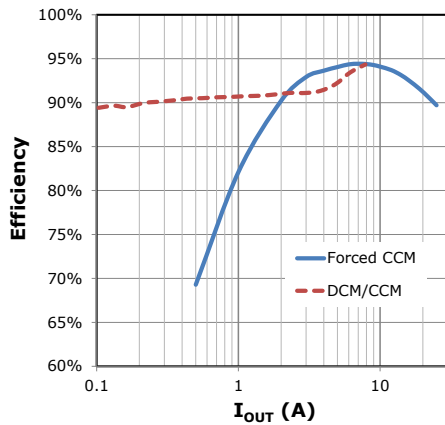


Fig. 12: Efficiency,  $5V_{IN}$ ,  $1.8V_{OUT}$ ,  $0.47\mu H$ ,  $300kHz$

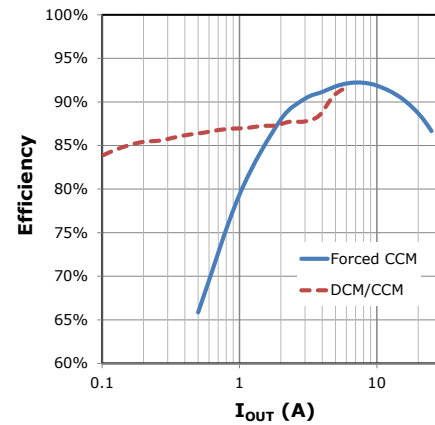


Fig. 13: Efficiency,  $5V_{IN}$ ,  $1.2V_{OUT}$ ,  $0.47\mu H$ ,  $300kHz$

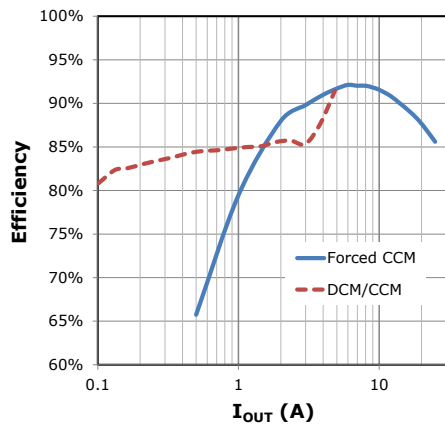


Fig. 14: Efficiency,  $5V_{IN}$ ,  $1.0V_{OUT}$ ,  $0.47\mu H$ ,  $300kHz$

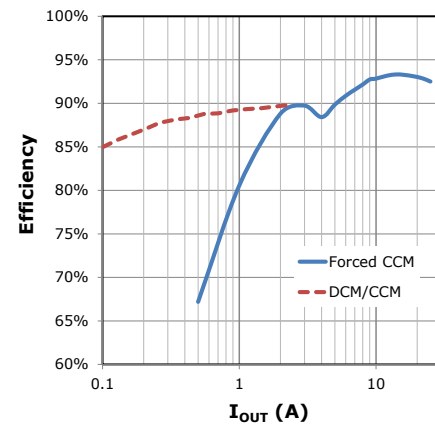


Fig. 15: Efficiency,  $12V_{IN}$ ,  $3.3V_{OUT}$ ,  $1\mu H$ ,  $300kHz$

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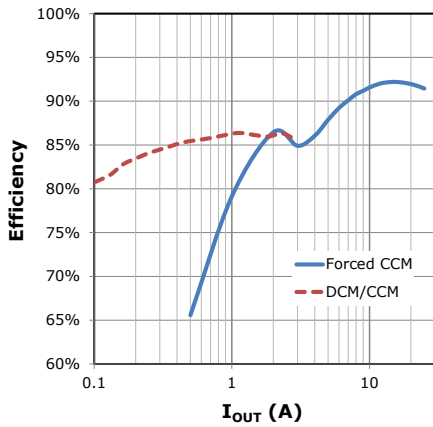


Fig. 16: Efficiency, 12V<sub>IN</sub>, 2.5V<sub>OUT</sub>, 1µH, 300kHz

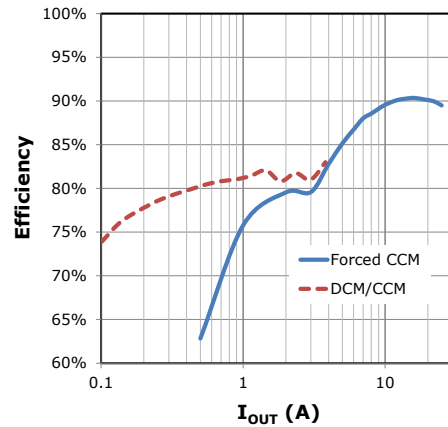


Fig. 17: Efficiency, 12V<sub>IN</sub>, 1.8V<sub>OUT</sub>, 1µH, 300kHz

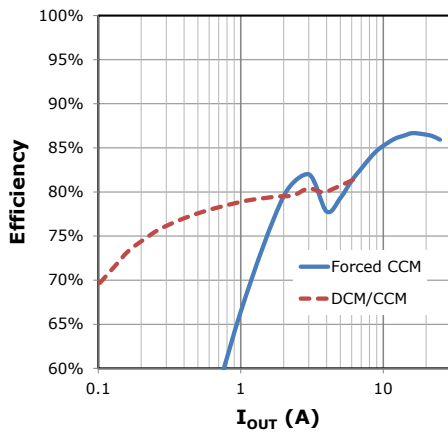


Fig. 18: Efficiency, 12V<sub>IN</sub>, 1.2V<sub>OUT</sub>, 0.47µH, 300kHz

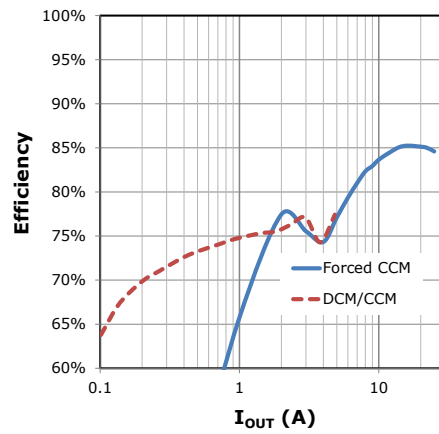


Fig. 19: Efficiency, 12V<sub>IN</sub>, 1.0V<sub>OUT</sub>, 0.47µH, 300kHz

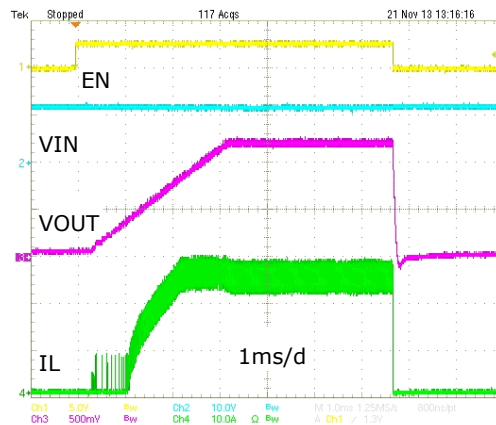


Fig. 20: Enable Turn On / Turn Off, 12V<sub>IN</sub>, 1.2V<sub>OUT</sub>, 25A



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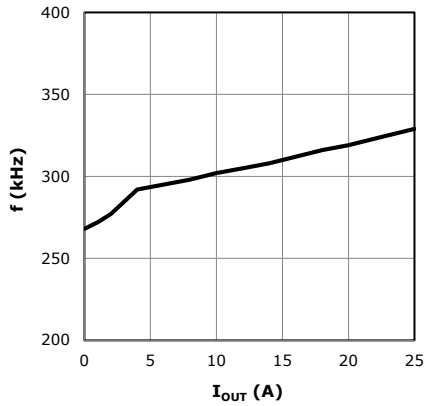


Fig. 22: Frequency versus I<sub>OUT</sub>, Forced CCM

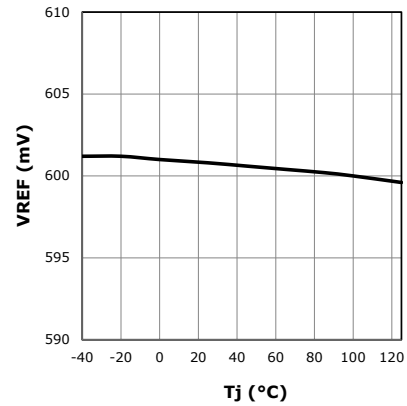


Fig. 23: VREF versus Temperature

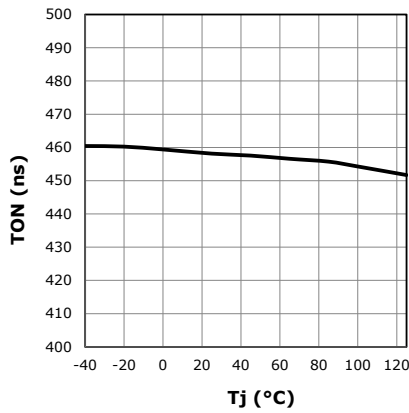


Fig. 24: On-Time versus Temperature

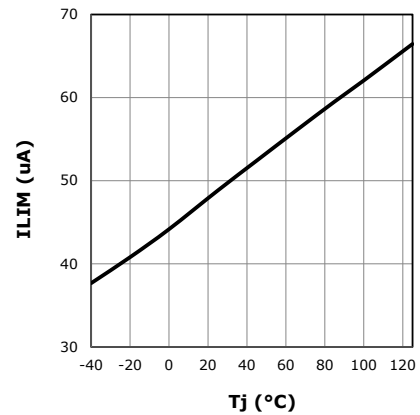


Fig. 25: ILIM versus Temperature

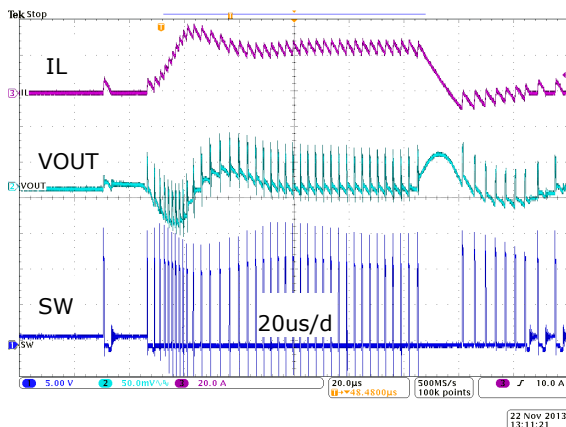


Fig. 26: Load Step, DCM/CCM, 0A-25A-0A

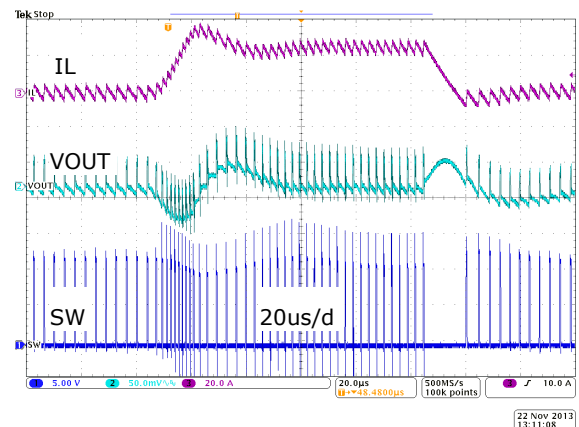


Fig. 27: Load Step, Forced CCM, 0A-25A-0A

### DETAILED OPERATION

XRP6141 is a synchronous step-down, proprietary emulated, current-mode Constant On-Time (COT) controller. The on-time, which is programmed via RON, is inversely proportional to VIN and maintains a nearly constant frequency. The emulated current-mode control allows the use of ceramic output capacitors.

Each switching cycle begins with the GH signal turning the high-side (switching) FET for a pre-programmed time. At the end of the on-time, the high-side FET is turned off and the low-side (synchronous) FET is turned on for a preset minimum time (250ns nominal). This parameter is termed Minimum Off-Time. After the Minimum Off-Time, the voltage at the feedback pin FB is compared to an internal voltage ramp at the feedback comparator. When VFB drops below the ramp voltage, the high-side FET is turned on and the cycle repeats. This voltage ramp constitutes an emulated current ramp and makes possible the use of ceramic capacitors, in addition to other capacitor types, for output filtering.

### ENABLE/MODE INPUT (EN/MODE)

The EN/MODE pin accepts a tri-level signal that is used to control turn on and off. It also selects between two modes of operation: 'Forced CCM' and 'DCM / CCM'. If EN is pulled below 1.9V, the controller shuts down. A voltage between 1.9V and 3.0V selects the Forced CCM Mode, which will run the converter in continuous conduction at all times. A voltage higher than 3.0V selects the DCM / CCM Mode, which will run the converter in discontinuous conduction at light loads.

#### Selecting the Forced CCM Mode

In order to set the controller to operate in Forced CCM, a voltage between 1.9V and 3.0V must be applied to the EN/MODE pin. This can be achieved with an external control signal that meets the above voltage requirement. Where an external control is not available, the EN/MODE can be derived from VIN. If VIN is well regulated, use a resistor divider and set the voltage to 2.5V. If VIN varies over a wide range, the circuit shown in Figure 28 can be used to generate the required voltage. Note that at VIN of 5.5V to 22V, the nominal Zener voltage is 4.0V to 5.0V respectively. Therefore, for VIN in the range of 5.5V to 22V, the circuit shown in Figure 28 will generate voltage at the EN/MODE pin required for Forced CCM.

#### Selecting the DCM/CCM Mode

In order to set the controller operation to DCM / CCM, a voltage between 3.1V and 5.5V must be applied to the EN/MODE pin. If an external control signal is available, it can be directly connected to the EN/MODE pin. In applications where an external control signal is not available, the EN/MODE input can be derived from VIN. If VIN is well regulated, use a resistor divider and set the voltage to 4V. If VIN varies over a wide range, the circuit shown in Figure 29 can be used to generate the required voltage.

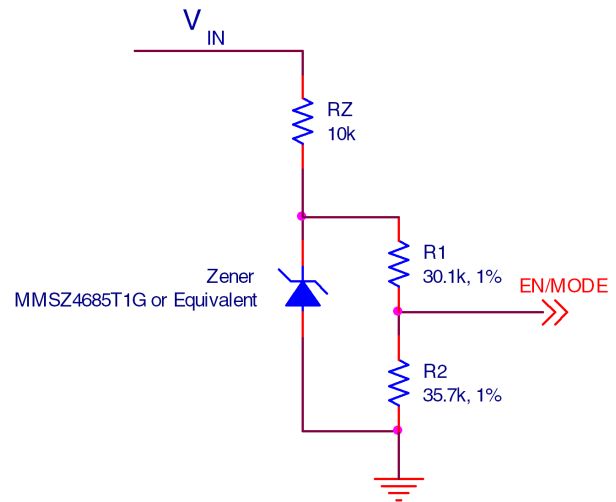


Figure 28. Selecting Forced CCM by Deriving EN/MODE from VIN

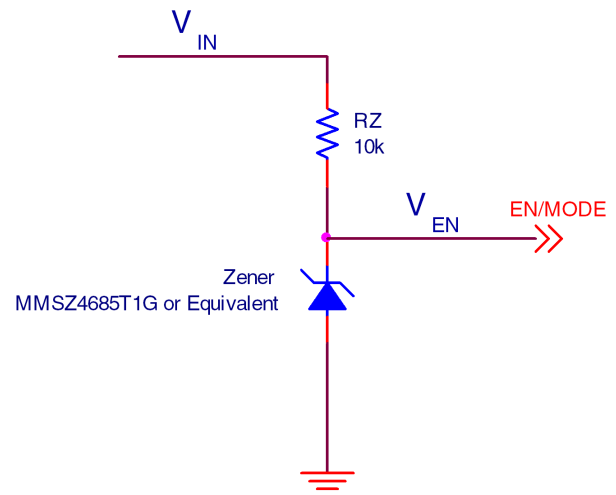


Figure 29. Selecting DCM / CCM by Deriving EN/MODE from VIN

### PROGRAMMING THE ON-TIME

The on-time TON is programmed via resistor RON according to following equation:

$$T_{ON} = \frac{(3.4E - 10) \times R_{ON}}{V_{IN}}$$

The required TON for a given application is calculated from:

$$T_{ON} = \frac{V_{OUT}}{V_{IN} \times f}$$

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Note that switching frequency  $f$  will increase somewhat, as a function of increasing load current and increasing losses (see Figure 22).

### OVER-CURRENT PROTECTION (OCP)

If load current exceeds the programmed over-current  $I_{OCP}$  for four consecutive switching cycles, then the IC enters hiccup mode of operation. In hiccup, the MOSFET gates are turned off for 110ms (hiccup timeout). Following the hiccup timeout, a soft-start is attempted. If OCP persists, hiccup timeout will repeat. The IC will remain in hiccup mode until load current is reduced below the programmed  $I_{OCP}$ . In order to program over-current protection, use the following equation:

$$RLIM = \frac{(I_{OCP} \times RDS) + 8mV}{ILIM}$$

Where:

$RLIM$  is resistor value for programming  $I_{OCP}$

$I_{OCP}$  is the over-current value to be programmed

$RDS$  is the MOSFET rated on resistance

8mV is the OCP comparator offset

$ILIM$  is the internal current that generates the necessary OCP comparator threshold (use 45 $\mu$ A)

Note that  $ILIM$  has a positive temperature coefficient of 0.4%/°C. This is meant to roughly match and compensate for positive temperature coefficient of the synchronous FET. In order for this feature to be effective, the temperature rise of the IC should approximately match the temperature rise of the FET.

### SHORT-CIRCUIT PROTECTION (SCP)

If the output voltage drops below 60% of its programmed value, the IC will enter hiccup mode. Hiccup will persist until the short-circuit is removed. The SCP circuit becomes active after PGOOD asserts high.

### OVER-TEMPERATURE PROTECTION (OTP)

OTP triggers at a nominal die temperature of 150°C. The gate of switching FET and synchronous FET are turned off. When die temperature cools down to 135°C, soft-start is initiated and operation resumes.

### PROGRAMMING THE OUTPUT VOLTAGE

Use an external voltage divider as shown in Figure 1 to program the output voltage  $V_{OUT}$ .

$$R1 = R2 \times \left( \frac{V_{OUT}}{0.6} - 1 \right)$$

The  $R2$  recommended range is 2k $\Omega$  to 10k $\Omega$ .

### PROGRAMMING THE SOFT-START

Place a capacitor  $CSS$  between the SS and GND pins to program the soft-start. In order to program a soft-start time of TSS, calculate the required capacitance  $CSS$  from the following equation:

$$CSS = TSS \times \frac{10\mu A}{0.6V}$$

### FEED-FORWARD CAPACITOR ( $C_{FF}$ )

A feed-forward capacitor ( $C_{FF}$ ) may be necessary depending on the Equivalent Series Resistance (ESR) of  $C_{OUT}$ . If only ceramic output capacitors are used, then a  $C_{FF}$  is necessary. Calculate  $C_{FF}$  from:

$$CFF = \frac{1}{2 \times \pi \times R1 \times 7 \times f_{LC}}$$

where:

$R1$  is the resistor that  $C_{FF}$  is placed in parallel with

$f_{LC}$  is the frequency of the output filter double pole

$f_{LC}$  must be less than 15kHz when using ceramic  $C_{OUT}$ . If necessary, increase  $C_{OUT}$  and/or  $L$  in order to meet this constraint.

When using capacitors with higher ESR such as the Panasonic TPE series, a  $C_{FF}$  is not required provided the following conditions are met:

1. The frequency of the output LC double pole  $f_{LC}$  should be less than 10kHz.
2. The frequency of ESR zero  $f_{ZERO,ESR}$  should be at least five times larger than  $f_{LC}$ .

Note that if  $f_{ZERO,ESR}$  is less than 5 x  $f_{LC}$ , then it is recommended to set the  $f_{LC}$  at less than 2kHz.  $C_{FF}$  is still not required.

### FEED-FORWARD RESISTOR ( $R_{FF}$ )

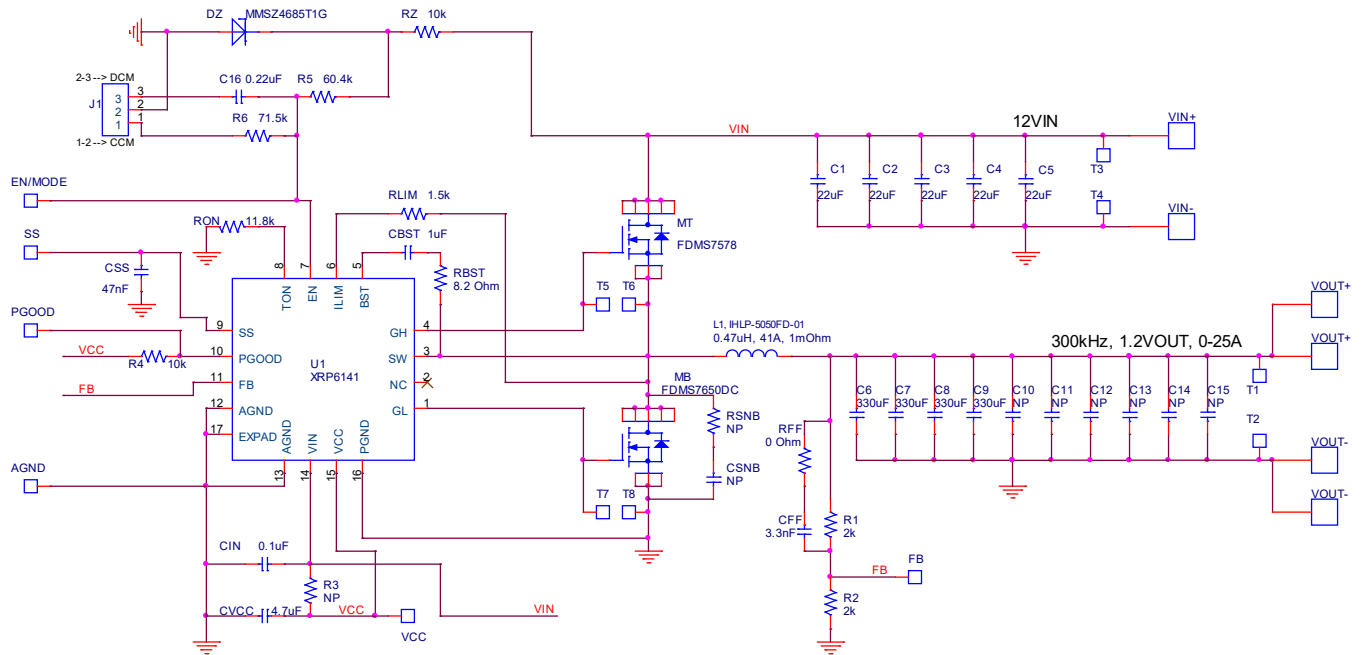
Poor PCB layout and/or extremely fast switching FETs can cause switching noise at the output and may couple to the FB pin via  $C_{FF}$ . Excessive noise at FB will cause poor load regulation. To solve this problem, place a resistor  $R_{FF}$  in series with  $C_{FF}$ . A  $R_{FF}$  value up to 2% of  $R1$  is acceptable.

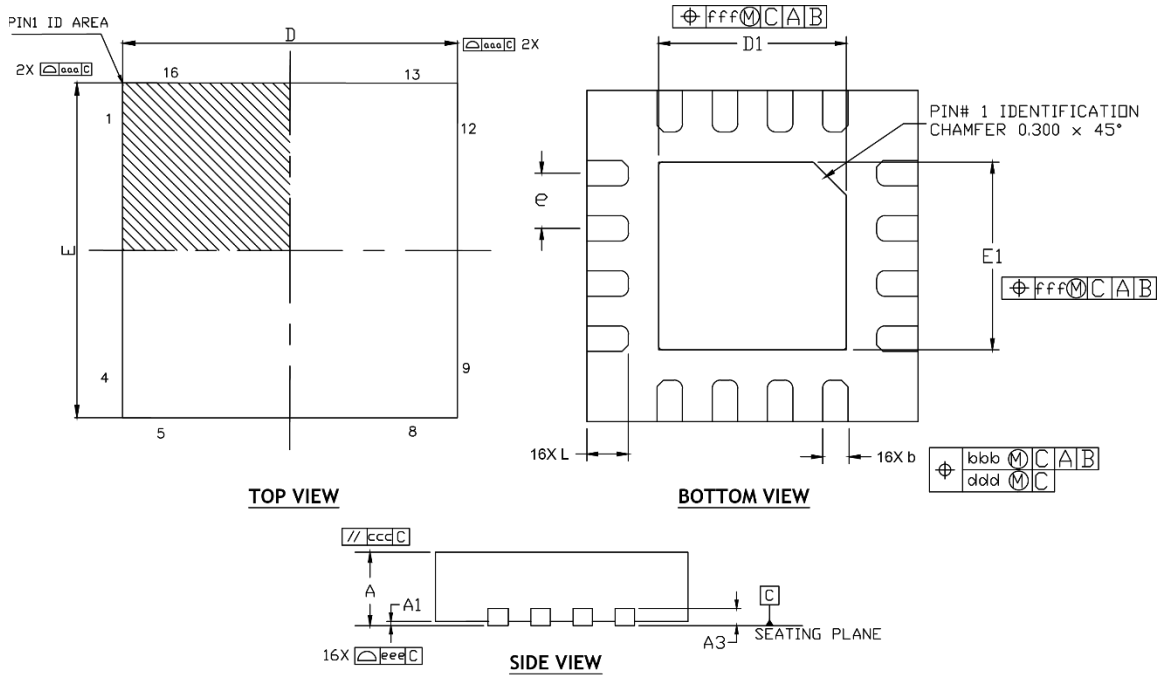
### MAXIMUM ALLOWABLE VOLTAGE RIPPLE AT FB PIN

Note that the steady-state voltage ripple at feedback pin ( $V_{FB,RIPPLE}$ ) must not exceed 50mV in order for the controller to function correctly. If  $V_{FB,RIPPLE}$  is larger than 50mV, then  $C_{OUT}$  should be increased as necessary in order to keep the  $V_{FB,RIPPLE}$  below 50mV.

**35A Synchronous Step Down COT Controller**

Applications Circuit



**35A Synchronous Step Down COT Controller**
**MECHANICAL DIMENSIONS**
**16 PIN 3X3 QFN**


DIMENSION TABLE			
SYMBOL	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	0.20Ref		
b	0.18	0.25	0.30
D	3.00 BSC		
E	3.00 BSC		
e	0.50 BSC		
D1	1.50	1.65	1.80
E1	1.50	1.65	1.80
L	0.20	0.30	0.40
K	0.20	-	-
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
N		16	

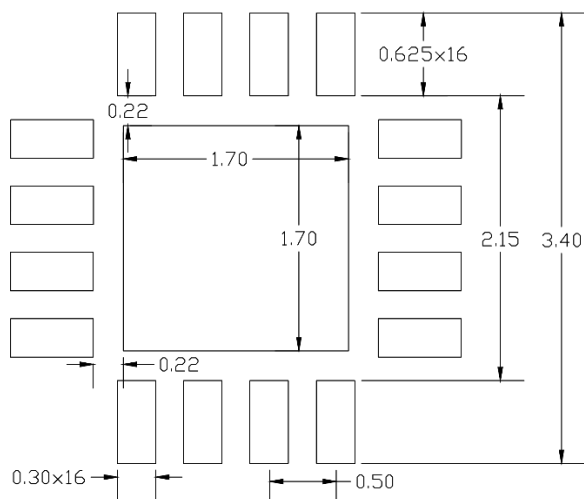
**TERMINAL DETAILS**

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-220.

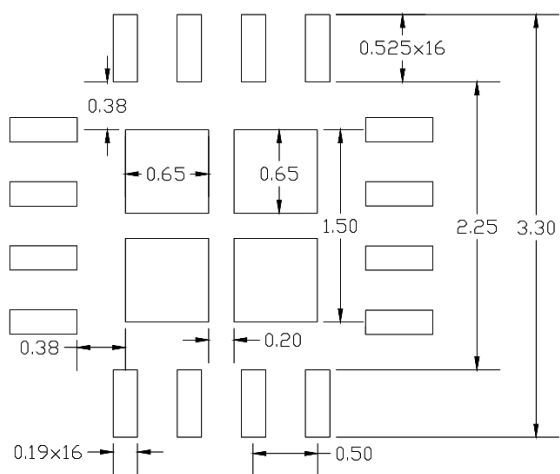
Drawing No.: POD- 00000138

Revision: A

**RECOMMENDED LAND PATTERN AND STENCIL**



**TYPICAL RECOMMENDED LAND PATTERN**



**TYPICAL RECOMMENDED STENCIL**

Drawing No.: POD- 00000138

Revision: A

**REVISION HISTORY**

Revision	Date	Description
1.0.0	12/16/2013	Initial release
1.0.1	12/20/2013	Specification improvement
2.0.0	7/31/2005	Modified Functional Block Diagram, Application Circuit, Feed-Forward Capacitor; added "Selecting the Forced CCM Mode", "Selecting the DCM/CCM Mode", "Feed-Forward Resistor", "Maximum Allowable Voltage Ripple at FB Pin" sections.
2.0.1	11/23/2015	Change VCC Linear Regulator Dropout Voltage from 200mV min and 300mV typ to 200mV typ.
2.0.2	5/24/2018	Update to MaxLinear logo. Update format and Ordering Information table. Added Revision History.
2.0.3	10/17/2019	Correct block diagram by changing the input gate to the Hiccup Mode block from an AND gate to an OR gate. Update ordering information.

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