MXD8512A

0.5~4.0GHz SPST Antenna Tuning Switch

General Description

The MXD8512A is a CMOS silicon-on-insulator (SOI), single-pole, single-throw (SPST) switch. The high linearity and ruggedness performance and extremely low insertion loss makes the device an ideal choice for GSM/WCDMA/LTE handset antenna tuning application.

The MXD8512A SPST switch is provided in a compact 0.7mm x 1.1mm x 0.377mm 6-lead QFN package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

Applications

- GSM/WCDMA/LTE band and mode switching
- Antenna tuning switch

Features

- Broadband frequency range: 0.1 to 4.0 GHz
- Low insertion 0.18dB @ 2.7 GHz
- High P0.1dB of 43.5dBm
- High Peak Vrf of 50V
- Very Low Ron of 1.2 Ohm
- Very Low Coff of 130fF
- Positive low voltage control: VC = 1.0 to 3.0 V, VDD = 1.7 to 3.3 V, Small, QFN (6-pin, 0.7mm x 1.1mm x 0.377mm) package , MSL1

Functional Block Diagram and Pin Function

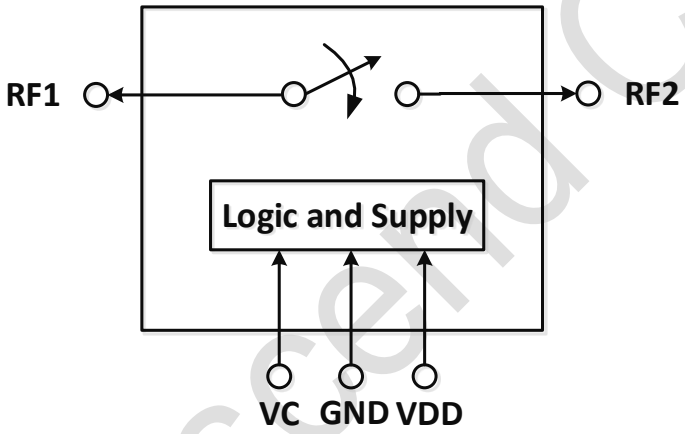


Figure 1.Functional Block Diagram

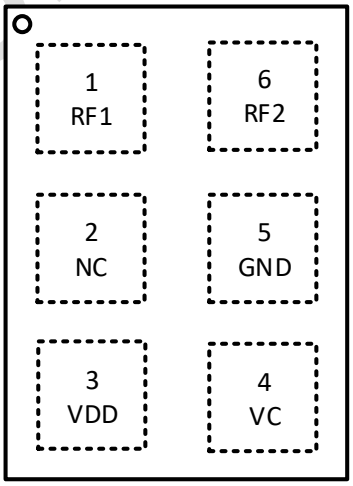


Figure 2.Pin-out (Top View)

Application Circuit

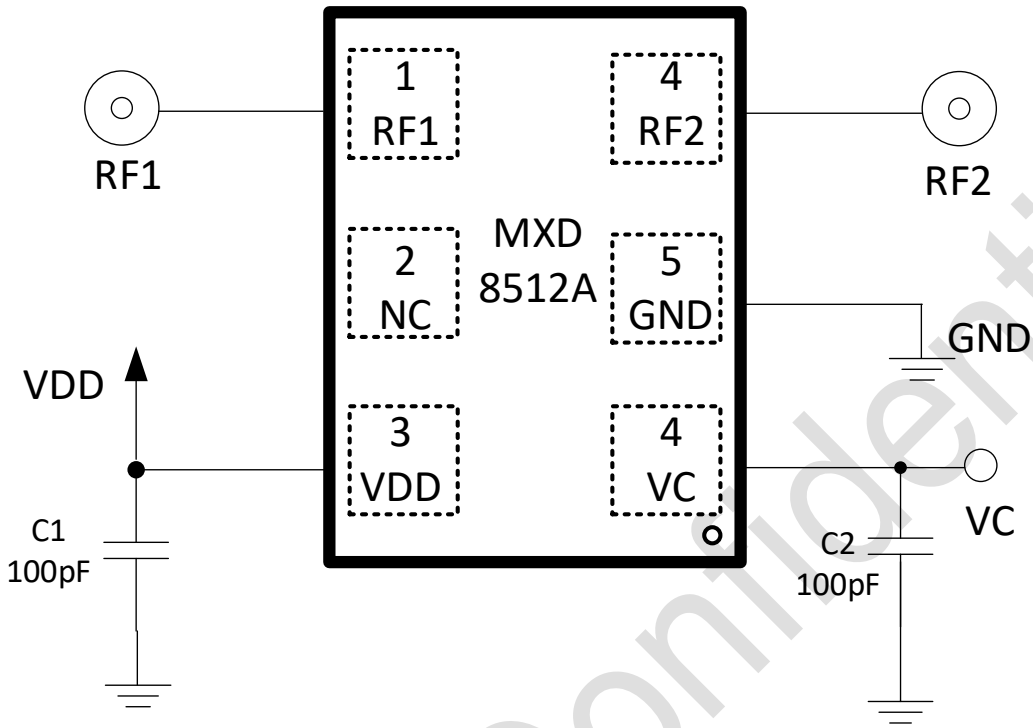


Figure 3. MXD8512A Application Circuit

Table 1. Pin Description

Pin No.	Name	Description	Pin No.	Name	Description
1	RF1	RF port 1	5	GND	Ground
2	NC	No connect	6	RF2	RF port 2
3	VDD	DC power supply			
4	VC	DC control voltage			

Truth Table

Table 2.

Active Path	VC
RF1 to RF2 OFF	0
RF1 to RF2 ON	1

Note: "1" = 1.0 V to 3.00 V. "0" = –0 V to +0.3 V.

Recommended Operation Range

Table 3.

Parameters	Symbol	Min	Typ	Max	Units
Operation Frequency	f1	0.5	-	4.0	GHz
Power supply	V_{DD}	1.7	2.8	3.3	V
Switch Control Voltage High	V_{CTL_H}	1.0	1.8	3.0	V
Switch Control Voltage Low	V_{CTL_L}	0	0	0.3	V

Specifications

Table 4.Electrical Specifications

Parameter	Symbol	Specification			Units	Test Condition
		Min.	Typical	Max.		
DC Specifications						
Control voltage: Low High	 V_{CTL_L} V_{CTL_H}	 0 1.0	 0 1.8	 0.3 3.0	 V V	
Supply voltage	V_{DD}	1.7	2.8	3.3	V	
Supply current	I_{DD}		100	150	μA	V_{DD} = 2.8 V
Control current	I_{CTL}		1	5	μA	V_{CTL}= 1.8 V
RF Specifications						
Insertion loss	IL		0.10 0.12 0.18 0.25	0.12 0.18 0.25 0.3	dB dB dB dB	0.5 to 1.0 GHz 1.0 to 2.2 GHz 2.2 to 3.0 GHz 3.0 to 4.0 GHz
Isolation	ISO	25 20 15 14	28 22 18 17		dB dB dB dB	0.5 to 1.0 GHz 1.0 to 2.2 GHz 2.2 to 3.0 GHz 3.0 to 4.0 GHz
Return loss	$\|S_{11}\|$		22		dB	0.5 to 4.0 GHz
On Resistance (RF1/2 to ANT)	Ron		1.2	1.4	Ω	Switch on Path
OFF Capacitance (RF1/2 to ANT)	Coff		130	140	fF	Switch off Path
Input 0.1 dB compression point	$P_{0.1dB}$		+43.5		dBm	0.5 to 4.0 GHz, ANT to RF1 and RF2
Maximum RF operating voltage	V_{max}		50		V	f0 = 500 to 4000 MHz, 25% duty cycle
LTE TX harmonic (RF1/2 to ANT)	2f0		-110	-95	dBm	f0 = 500 to 4000 MHz, PIN = +26 dBm
	3f0		-105	-85	dBm	
GSM LB harmonic (RF1/2 to ANT)	2f0		-60	-50	dBm	f0 = 824 to 915 MHz, PIN = +35 dBm
	3f0		-60	-50	dBm	
GSM HB harmonic (RF1/2 to ANT)	2f0		-60	-50	dBm	f0 = 1710 to 2690 MHz, PIN = +33 dBm
	3f0		-60	-50	dBm	
Second order intermodulation	IMD2		-115	-105	dBm	CW Carrier on RF Port, +20 dBm CW Interferer on ANT port, -15 dBm
Third order intermodulation	IMD3		-115	-105	dBm	CW Carrier on RF Port, +20 dBm CW Interferer on ANT port, -15 dBm
Switching on time			5	10	μs	50% VCTL to 90% RF
Switching off time			5	10	μs	50% VCTL to 10% RF
Startup time			15	30	μs	Power off state to any RF switch state

Table 5. IMD2 Test Conditions

Band	In-band freq	CW Carrier		CW Interferer	
	MHz	MHz	dBm	MHz	dBm
1 Low	2140	1950	+20	190	-15
1 High	2140	1950	+20	4090	-15
5 Low	881.5	836.5	+20	45	-15
5 High	881.5	836.5	+20	1718	-15

Table 6. IMD3 Test Conditions

Band	In-band freq	CW Carrier		CW Interferer	
	MHz	MHz	dBm	MHz	dBm
1	2140	1950	+20	1760	-15
5	881.5	836.5	+20	791.5	-15

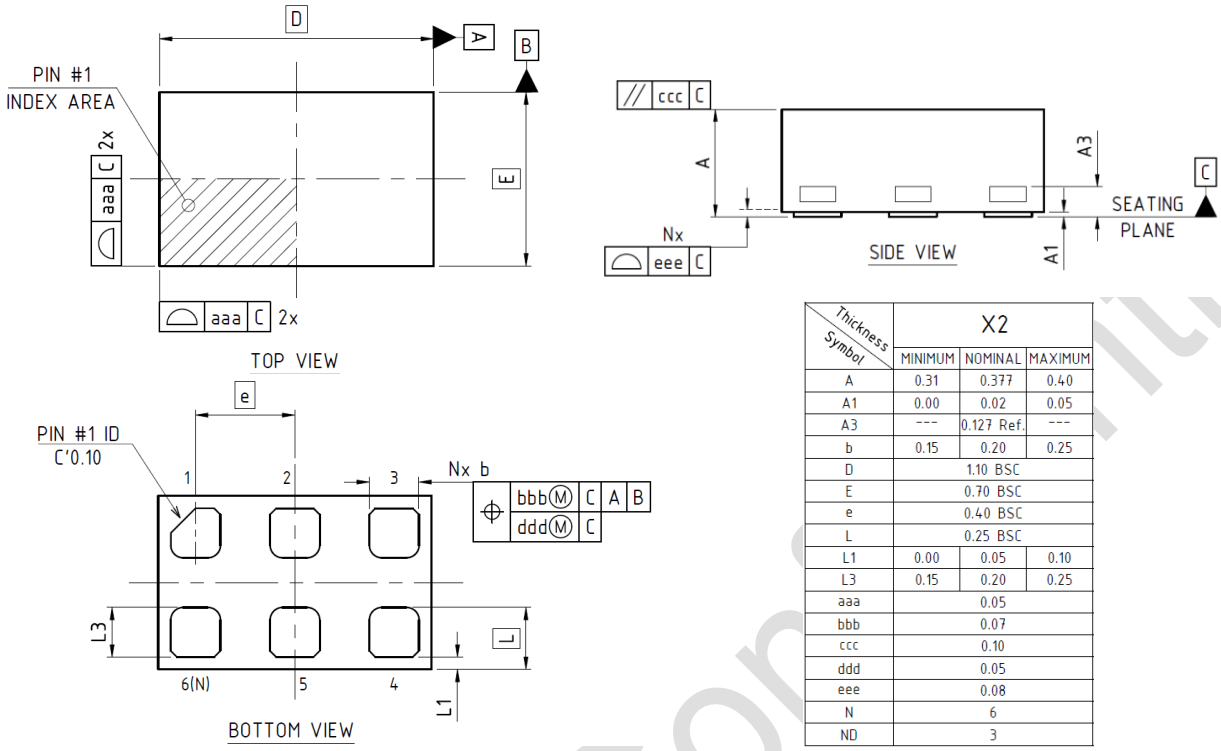
Absolute Maximum Ratings

Table 7. Maximum ratings

Parameters	Symbol	Minimum	Maximum	Units
Supply voltage	V_{DD}		+3.6	V
Digital control voltage	V_{CTL}	0	+3.3	V
RF input power CW (50 Ohm)	P_{IN}		+40	dBm
Operating temperature	T_{OP}	-35	+90	℃
Storage temperature	T_{STG}	-55	+150	℃
Electrostatic Discharge Human body model (HBM), Class 1C	ESD_HBM		1000	V
Machine Model (MM), Class A	ESD_MM		100	
Charged device model (CDM), Class III	ESD_CDM		500	

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

Package Outline Dimension



Thickness / Symbol	X2		
	MINIMUM	NOMINAL	MAXIMUM
A	0.31	0.377	0.40
A1	0.00	0.02	0.05
A3	---	0.127 Ref.	---
b	0.15	0.20	0.25
D		1.10 BSC	
E		0.70 BSC	
e		0.40 BSC	
L		0.25 BSC	
L1	0.00	0.05	0.10
L3	0.15	0.20	0.25
aaa		0.05	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
N		6	
ND		3	

Figure 4. Package outline dimension

Reflow Chart

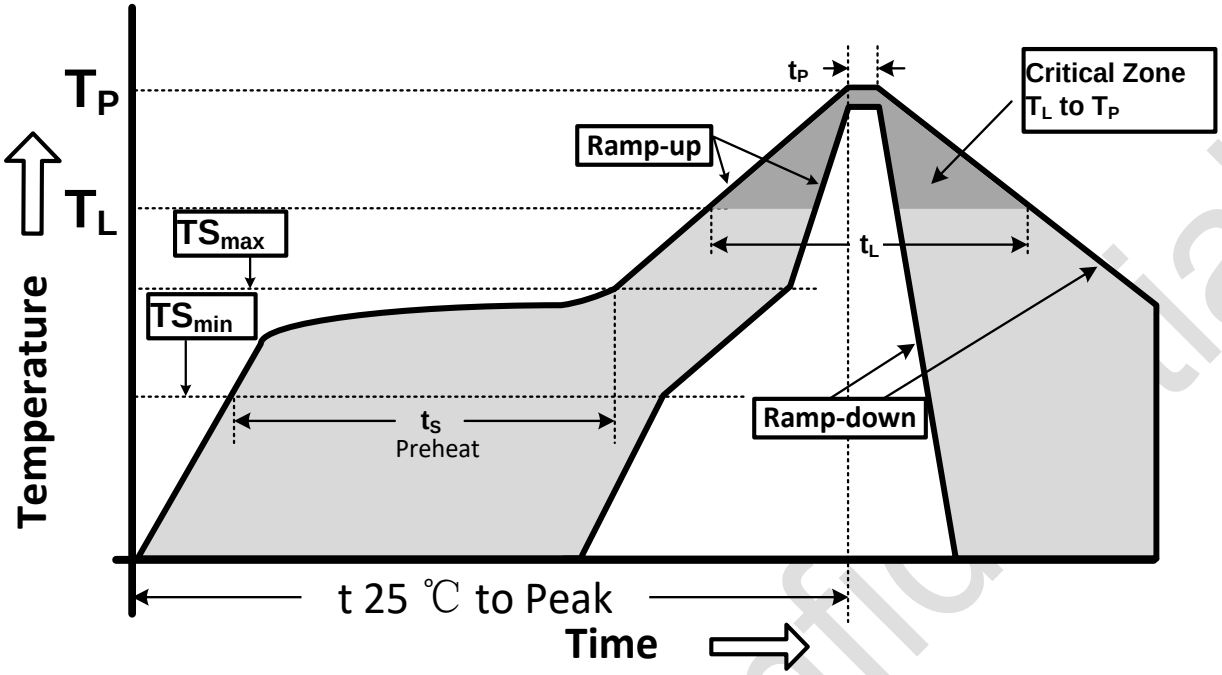


Figure 7. Recommended Lead-Free Reflow Profile

Table 8.

Profile Parameter	Lead-Free Assembly, Convection, IR/Convection
Ramp-up rate（TS_{max} to T_p）	3℃/second max.
Preheat temperature（TS_{min} to TS_{max}）	150℃ to 200℃
Preheat time（t_s）	60 - 180 seconds
Time above TL , 217℃（t_L）	60 - 150 seconds
Peak temperature（T_p）	260℃
Time within 5℃ of peak temperature(t_p)	20 - 40 seconds
Ramp-down rate	6℃/second max.
Time 25℃ to peak temperature	8 minutes max.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electric charge. Proper ESD protection techniques should be used when handling these devices.

RoHS Compliant

This product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE), and are considered RoHS compliant.

1.2.1

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