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## MXD8530

## SP3T Switch for 0.1~3G Application

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## General Description

The MXD8530 is a Single Pole, Triple-Throw (SP3T) antenna switch. The high linearity performance and low insertion loss achieved by the MXD8530 make it an ideal choice for main/diversity switching commonly used in LTEbased handsets, data cards, and tablets that use antenna diversity solutions. The symmetric port designs provide flexibility in signal routing for both receive diversity and higher power WCDMA/FDD, and WLANs transmit/receive applications.
Switching is controlled by two CMOS/TTLcompatible control voltage inputs (V1 and V2). Depending on the logic voltage level applied to the control pins, the ANT pin is connected to one of five switched RF outputs (RF1 to RF2) using a low insertion loss path, while the paths between the ANT pin and the other RF pins are in a high isolation state. No external blocking capacitors are
required on the RF paths unless VDC is externally applied.
The MXD8530 is manufactured in a compact, 12pin $2.0 \times 2.0 \mathrm{~mm}$, Quad Flat No-Lead (QFN) package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

## Applications

- WCDMA band and mode switching
- Antenna switch for multimode systems
- $802.11 \mathrm{~b} / \mathrm{g} / \mathrm{n}$ WLANs


## Features

- Broadband frequency range: 0.1 to 3.0 GHz
- Low insertion loss: 0.45 dB typical @ 2.5 GHz
- High isolation: >30 dB @ 2.5 GHz
- No external DC blocking capacitors requires
- Small QFN (12-pin, $2.0 \times 2.0 \mathrm{~mm}$ ) package


## Functional Block Diagram and Pin Function



Figure 1. Functional Block Diagram


Figure 2. Pin Diagram

## Application Circuit



Figure 3. MXD8530 Evaluation Board Schematic

Table 1. Pin Description

| Pin No. | Name | Description | Pin No. | Name | Description |
| :--- | :--- | :--- | :--- | :--- | :--- |
| 1 | RF1 | RF I/O path 1 | 7 | GND | Ground |
| 2 | GND | Ground | 8 | GND | Ground |
| 3 | RF3 | RF I/O path 3 | 9 | RF2 | RF I/O path 2 |
| 4 | V1 | DC control voltage 1 | 10 | GND | Ground |
| 5 | V2 | DC control voltage 2 | 11 | RFC | RF common port |
| 6 | VDD | DC supply | 12 | GND | Ground |

Note: Bottom ground paddles must be connected to ground.

Table 2. Truth Table

| Control pins |  | Switched RF Outputs |  |  |
| :---: | :---: | :---: | :---: | :---: |
| V1 | V2 | RF1 | RF2 |  |
| 0 | 0 |  | Shutdown |  |
| 0 | 1 | Insertion Loss | Isolation |  |
| 1 | 0 | Isolation | Insertion Loss | Isolation |
| 1 | 1 | Isolation | Isolation | Isolation |
| Note: $1 "=1.0 \mathrm{~V}$ to $3.30 \mathrm{~V} . " 0 "=0 \mathrm{~V}$ to +0.3 V. | Insertion Loss |  |  |  |

## Recommended Operation Range

Table 3.

| Parameters | Symbol | Min | Typ | Max | Units |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Operation Frequency | f1 | 0.1 | - | 3.0 | GHz |
| Power supply | VDD | 2.0 | 2.8 | 3.0 | V |
| Switch Control Voltage (H) | $\mathrm{V}_{\mathrm{H}}$ | 1.0 | 1.8 | 3.0 | V |
| Switch Control Voltage (L) | $\mathrm{V}_{\mathrm{L}}$ | 0 | 0 | 0.3 | V |

## Specifications

Table 4. Electrical Specifications

| Parameter | Symbol | Specification |  |  | Units | Test Condition (Note 2) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Typical | Max. |  |  |
| DC Specifications |  |  |  |  |  |  |
| Supply voltage | VDD | 2.0 | 2.8 | 3.0 | V |  |
| Supply current | IDD |  | 83 |  | $\mu \mathrm{A}$ |  |
| Control current | ICTL |  | 2 |  | $\mu \mathrm{A}$ | $\mathrm{VCTL}=1.8 \mathrm{~V}$ |
| Shutdown mode supply current | IOFF |  | 5 |  | $\mu \mathrm{A}$ | $\mathrm{V} 1 / 2 / 3=1.8 \mathrm{~V}, \mathrm{VDD}=3 \mathrm{~V}$ |
| Turn-on switching time | Ton |  | 2 |  | $\mu \mathrm{S}$ | $50 \%$ of final control voltage to $90 \%$ of final RF power, switching between RF1/2/3 |
| RF Specifications |  |  |  |  |  |  |
| Insertion loss (RFC pin to RF1/2/3 pins) | IL |  | $\begin{aligned} & 0.35 \\ & 0.40 \\ & 0.45 \end{aligned}$ | $\begin{aligned} & 0.40 \\ & 0.50 \\ & 0.55 \end{aligned}$ | dB <br> dB <br> dB | $\begin{aligned} & 0.8 \text { to } 1.0 \mathrm{GHz} \\ & 1.0 \text { to } 2.2 \mathrm{GHz} \\ & 2.2 \text { to } 3.0 \mathrm{GHz} \end{aligned}$ |
| Isolation (RFC pin to RF1/2/3 pins) | ISO | $\begin{aligned} & 38 \\ & 29 \\ & 26 \end{aligned}$ | $\begin{aligned} & 45 \\ & 36 \\ & 33 \end{aligned}$ |  | dB <br> dB <br> dB | $\begin{aligned} & 0.8 \text { to } 1.0 \mathrm{GHz} \\ & 1.0 \text { to } 2.2 \mathrm{GHz} \\ & 2.2 \text { to } 3.0 \mathrm{GHz} \end{aligned}$ |
| Input return loss (RFC pin to RF1/2/3 pins) | RL |  | -20 |  | dB | 0.8 to 3.0 GHz |
| Second harmonics (RFC pin to RF1/2/3 pins) | 2 fo |  | +85 |  | dBc | $\begin{aligned} & \mathrm{PIN}=+20 \mathrm{dBm}, \\ & 0.1 \text { to } 3.0 \mathrm{GHz} \end{aligned}$ |
| Third harmonics (RFC pin to RF1/2/3 pins) | 3 fo |  | +85 |  | dBc | $\begin{aligned} & \mathrm{PIN}=+20 \mathrm{dBm}, \\ & 0.1 \text { to } 3.0 \mathrm{GHz} \end{aligned}$ |
| 0.1 dB Compression Point <br> (ANT pin to RF1/2/3 pins) | $\mathrm{P}_{0.1 \mathrm{~dB}}$ |  | +36 |  | dBm | 0.1 GHz to 3 GHz |
| 3rd Order Input Intercept <br> Point | IIP3 | +65 | +70 |  | dBm | $\begin{aligned} & @ 3.0 \mathrm{GHz}, \\ & \mathrm{PIN}=+20 \mathrm{dBm}, \\ & \Delta \mathrm{f}=1 \mathrm{MHz} \end{aligned}$ |

## Absolute Maximum Ratings

Table 5. Maximum ratings

| Parameters | Symbol | Minimum | Maximum | Units |
| :--- | :---: | :---: | :---: | :---: |
| Supply voltage | $\mathrm{V}_{\mathrm{DD}}$ | +2.5 | +3.0 | V |
| Control voltage (V1 and V2) | $\mathrm{V}_{\mathrm{CTL}}$ | -0.5 | +3.0 | V |
| RF input power (RF1 to RF3) | $\mathrm{P}_{\mathrm{IN}}$ |  | +36 | dBm |
| Operating temperature | $\mathrm{T}_{\mathrm{OP}}$ | -40 | +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature | $\mathrm{T}_{\mathrm{STG}}$ | -55 | +150 | ${ }^{\circ} \mathrm{C}$ |
| Human Body Mode | HBM |  | 1000 | V |
| Machine Mode | MM |  | 100 | V |
| Charged Device Mode | CDM |  | 500 | V |

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device

## Package Outline Dimension



TOP VIEW



BOTTOM VIEW

| DESCRIPTION |  | SYMBOL | MILLIMETER |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | NOM | MAX |
| TOTAL THICKNESS |  |  | A | 0.50 | 0.55 | 0.60 |
| STAND OFF |  | A1 | 0.00 | --- | 0.05 |
| MOLD THICKNESS |  | A2 | 0.35 | 0.40 | 0.45 |
| L/F THICKNESS |  | A3 | 0.147 | 0.152 | 0.157 |
| LEAD WIDTH |  | b | 0.15 | 0.20 | 0.25 |
| BODY SIZE | X | D | 1.95 | 2.00 | 2.05 |
|  | Y | E | 1.95 | 2.00 | 2.05 |
| EAD PITCH |  | e | 0.50 BSC |  |  |
| EP SIZE | $X$ | $J$ | 0.71 | 0.76 | 0.81 |
|  | $Y$ | K | 0.71 | 0.76 | 0.81 |
| LEAD LENGTH |  | L | 0.24 | 0.29 | 0.34 |
| PACKAGE EDGE TOLERANCE |  | aoo | 0.05 |  |  |
| MOLD FLATNESS |  | bbb | 0.05 |  |  |
| COPLANARITY |  | ccc | 0.05 |  |  |
| EAD OFFSET |  | ddd | 0.1 |  |  |
| EXPOSED PAD OFFSET |  | eee | 0.1 |  |  |

Figure 4. package outline dimension

## Reflow Chart



Figure 5. Recommended Lead-Free Reflow Profile
Table 6.

| Profile Parameter | Lead-Free Assembly, Convection, IR/Convection |
| :--- | :--- |
| Ramp-up rate $\left(\mathrm{TS}_{\text {max }}\right.$ to $\left.\mathrm{T}_{\mathrm{p}}\right)$ | $3^{\circ} \mathrm{C} /$ second max. |
| Preheat temperature $\left(\mathrm{TS}_{\text {min }}\right.$ to $\left.\mathrm{TS}_{\text {max }}\right)$ | $150^{\circ} \mathrm{C}$ to $200^{\circ} \mathrm{C}$ |
| Preheat time $\left(\mathrm{t}_{\mathrm{s}}\right)$ | $60-180$ seconds |
| Time above $\mathrm{TL}, 217^{\circ} \mathrm{C}\left(\mathrm{t}_{\mathrm{L}}\right)$ | $60-150$ seconds |
| Peak temperature $\left(\mathrm{T}_{\mathrm{p}}\right)$ | $260^{\circ} \mathrm{C}$ |
| Time within $5^{\circ} \mathrm{C}$ of peak temperature $\left(\mathrm{t}_{\mathrm{p}}\right)$ | $20-40$ seconds |
| Ramp-down rate | $6^{\circ} \mathrm{C} /$ second max. |
| Time $25^{\circ} \mathrm{C}$ to peak temperature | 8 minutes max. |

## ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electric charge. Proper ESD protection techniques should be used when handling these devices.

## RoHS Compliant

This product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE), and are considered RoHS compliant.

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