



MXD8650

DP4T Switch for 3G/4G and Diversity Application

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General Description

MXD8650 is a general purpose DP4T for 3G/4G and diversity application.

The device is processed in advanced CMOS silicon-on-insulator (SOI) technology featuring low insertion loss, high isolation, high linearity and high ESD protection level. The excellent performance makes it ideal to be applied in application for 3G/4G multi-mode WCDMA, UMTS, and LTE.

The MXD8650 is packaged in small, ultra-thin, 10 pins, 0.4mm pitch (1.1 x 1.5 x 0.45 mm) package.

Features

- Advanced SOI Process
- Frequency Range : 0.1 ~ 3.0 GHz
- Low Control Voltage : 1.6 ~ 3.3 V
- Low Insertion Loss : 0.4 dB at 2.7 GHz
- High Isolation : 20 dB at 3.0 GHz
- RoHS / Halogen Free Compliant
- Moisture Sensitivity Level : MSL-1

Applications

- Cellular Handset Applications
- Cellular Modems and USB devices
- 3G/4G WCDMA and LTE Applications

Functional Block Diagram and Pin Function

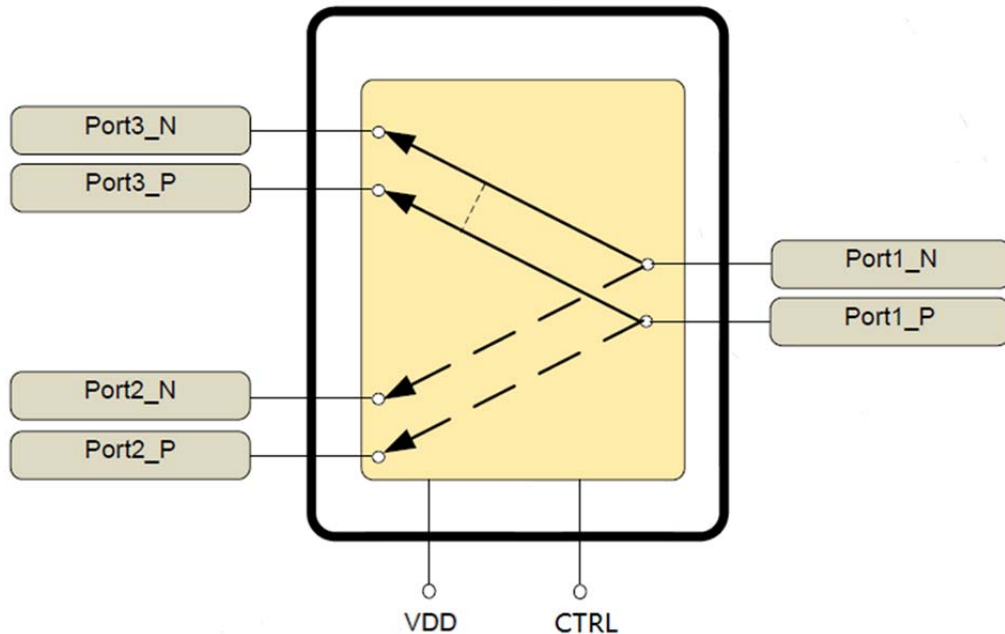


Figure 1. Functional Block Diagram

Application Circuit

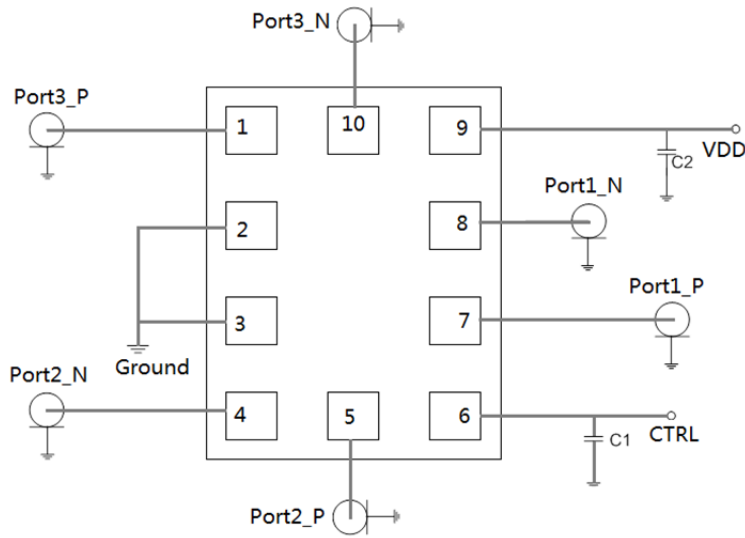


Figure 2. MXD8650 Pin Diagram

Note:
 1. Recommend:
 a) C1 =33pF
 b) C2=1uF

Table 1. Pin Description

Pin No.	Name	Pin No.	Name
1	Port3_P	6	CTRL
2	GND	7	Port1_P
3	GND	8	Port1_N
4	Port2_N	9	VDD
5	Port2_P	10	Port3_N

Truth Table

Table 2.

Insertion Loss Path	CTRL
Port1-Port2	0
Port1-Port3	1

Note: "0" = 0 ~ 0.4 V, "1" = 1.6 ~ 3.3 V

Recommended Operation Range

Table 3. Recommended Operation Range

Parameters	Symbol	Min	Typ	Max	Units
Operation Frequency	f1	0.1	-	3.0	GHz
Power supply	V _{DD}	2.0	2.8	3.3	V
Switch Control Voltage (H)	V _H	1.6	2.8	3.3	V
Switch Control Voltage (L)	V _L	0	0	0.4	V

Specifications
Table 4. Electrical Specifications

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
UMTS-Low Band					Nominal conditions unless otherwise stated. VDD = 2.8 V, VHIGH/VLOW = 1.8 V/0 V, Temp = 25°C, 50 Ω
Frequency Range	824		960	MHz	
Insertion Loss					
Port2_N to Port1_N		0.25		dB	824MHz to 960MHz
Port2_P to Port1_P		0.25		dB	
Port3_N to Port1_N		0.25		dB	
Port3_P to Port1_P		0.25		dB	
Isolation					
Port2_N - Port1_N	25			dB	824MHz to 960MHz; Port3 to Port1 active
Port2_N - Port1_N	25			dB	
Port2_P - Port1_N	25			dB	
Port2_N - Port1_P	25			dB	
Port2_P - Port1_P	25			dB	
Port2_N - Port3_N	25			dB	
Port2_P - Port3_N	25			dB	
Port2_N - Port3_P	25			dB	
Port2_P - Port3_P	25			dB	
Port3_N - Port1_N	25			dB	824MHz to 960MHz; Port2 to Port1 active
Port3_P - Port1_N	25			dB	
Port3_N - Port1_P	25			dB	
Port3_P - Port1_P	25			dB	
Port3_N - Port2_N	25			dB	
Port3_P - Port2_N	25			dB	
Port3_N - Port2_P	25			dB	
Port3_P - Port2_P	25			dB	
Balanced Isolation					
Port3_N/P - Port1_N/P	40	42		dB	TX = 450MHz to 960MHz, Port2 to Port1 path active, Port2_N/P terminated in 50 Ω
Port2_N/P - Port1_N/P	40	44		dB	TX = 450MHz to 960MHz, Port3 to Port1 path active, Port3_N/P terminated in 50 Ω
Harmonics					
Ports 2 or 3 to Port 1 (2fo)		90	85	dBc	TX = 824 to 960MHz, CW, Pin = 20dBm, 50 ohm
Ports 2 or 3 to Port 1 (3fo)		90	85	dBc	
Ports 2 or 3 to Port 1 (4fo to 12.75GHz)		85	83	dBc	
Phase Balance					
	-1	0	+1	Deg.	Between active paths; Test frequency 960MHz
Amplitude Balance					
	-1	0	+1	dB	Between active paths; Test frequency 960MHz
VSWR					
Port2 or Port3			1.5	:1	824MHz to 960MHz
Port1			1.5	:1	



MXD8650 DP4T Switch For 3G/4G and Diversity Application

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
UMTS-High Band					Nominal conditions unless otherwise stated. VDD = 2.8 V, VHIGH/VLOW = 1.8 V/0 V, Temp = 25°C, 50 Ω
Frequency Range	1710		2690	MHz	
Insertion Loss					
Port2_N to Port1_N		0.4		dB	1710MHz to 2690MHz
Port2_P to Port1_P		0.4			
Port3_N to Port1_N		0.4			
Port3_P to Port1_P		0.4			
Isolation					
Port2_N - Port1_N	20			dB	1710MHz to 2690MHz; Port3 to Port1 active
Port2_N - Port1_N	20			dB	
Port2_P - Port1_N	20			dB	
Port2_N - Port1_P	20			dB	
Port2_P - Port1_P	20			dB	
Port2_N - Port3_N	20			dB	
Port2_P - Port3_N	20			dB	
Port2_N - Port3_P	20			dB	
Port2_P - Port3_P	20			dB	
Port3_N - Port1_N	20			dB	
Port3_P - Port1_N	20			dB	
Port3_N - Port1_P	20			dB	
Port3_P - Port1_P	20			dB	
Port3_N - Port2_N	20			dB	
Port3_P - Port2_N	20			dB	
Port3_N - Port2_P	20			dB	
Port3_P - Port2_P	20			dB	
Balanced Isolation					
Port3_N/P - Port1_N/P	33	34		dB	TX = 2170MHz to 2690MHz, Port2 to Port1 path active, Port2_N/P terminated in 50 Ω
Port2_N/P - Port1_N/P	35	36		dB	TX = 2170MHz to 2690MHz z, Port3 to Port1 path active, Port3_N/P terminated in 50 Ω
Port3_N/P - Port1_N/P	34	35		dB	TX = 1710MHz to 2170MHz z, Port2 to Port1 path active, Port2_N/P terminated in 50 Ω
Port2_N/P - Port1_N/P	37	38		dB	TX = 1710MHz to 170MHz z, Port3 to Port1 path active, Port3_N/P terminated in 50 Ω
Ports 2 or 3 to Port 1 (2fo)		90	85	dBc	TX = 1710MHz to 2570MHz, CW, Pin = 20dBm, 50 ohm
Ports 2 or 3 to Port 1 (3fo)		90	85	dBc	
Ports 2 or 3 to Port 1 (4fo to 12.75GHz)		85	83	dBc	
Phase Balance					
	-1	0	+1	Deg.	Between active paths; Test frequency 2GHz
Amplitude Balance					
	-1	0	+1	dB	Between active paths; Test frequency 2GHz
VSWR					
Port2 or Port3			1.5	:1	1710MHz to 2690MHz
Port1			1.5	:1	



MXD8650 DP4T Switch For 3G/4G and Diversity Application

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
LTE-Low Band					Nominal conditions unless otherwise stated. VDD = 2.8 V, VHIGH/VLOW = 1.8 V/0 V, Temp = 25°C, 50 Ω
Frequency Range	698		792	MHz	
Insertion Loss					
Port2_N to Port1_N		0.3		dB	698MHz to 792MHz
Port2_P to Port1_P		0.3		dB	
Port3_N to Port1_N		0.3		dB	
Port3_P to Port1_P		0.3		dB	
Isolation					
Port2_N - Port1_N	25			dB	698MHz to 792MHz; Port3 to Port1 active
Port2_N - Port1_N	25			dB	
Port2_P - Port1_N	25			dB	
Port2_N - Port1_P	25			dB	
Port2_P - Port1_P	25			dB	
Port2_N - Port3_N	25			dB	
Port2_P - Port3_N	25			dB	
Port2_N - Port3_P	25			dB	
Port2_P - Port3_P	25			dB	
Port3_N - Port1_N	25			dB	
Port3_P - Port1_N	25			dB	
Port3_N - Port1_P	25			dB	
Port3_P - Port1_P	25			dB	
Port3_N - Port2_N	25			dB	
Port3_P - Port2_N	25			dB	
Port3_N - Port2_P	25			dB	
Port3_P - Port2_P	25			dB	
Balanced Isolation					
Port3_N/P - Port1_N/P	40	42		dB	TX = 450MHz to 960MHz, Port2 to Port1 path active, Port2_N/P terminated in 50 Ω
Port2_N/P - Port1_N/P	40	44		dB	TX = 450MHz to 960MHz, Port3 to Port1 path active, Port3_N/P terminated in 50 Ω
Phase Balance					
	-1	0	+1	Deg.	Between active paths; Test frequency 792MHz
Amplitude Balance					
	-1	0	+1	dB	Between active paths; Test frequency 792MHz
VSWR					
Port2 or Port3			1.5	:1	698MHz to 792MHz
Port1			1.5	:1	



MXD8650 DP4T Switch For 3G/4G and Diversity Application

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
LTE-High Band					Nominal conditions unless otherwise stated. VDD = 2.8 V, VHIGH/VLOW = 1.8 V/0 V, Temp = 25°C, 50 Ω
Frequency Range	2300		2690	MHz	
Insertion Loss					
Port2_N to Port1_N		0.4		dB	2300MHz to 2690MHz
Port2_P to Port1_P		0.4		dB	
Port3_N to Port1_N		0.4		dB	
Port3_P to Port1_P		0.4		dB	
Isolation					
Port2_N - Port1_N	20			dB	2300MHz to 2690MHz; Port3 to Port1 active
Port2_N - Port1_N	20			dB	
Port2_P - Port1_N	20			dB	
Port2_N - Port1_P	20			dB	
Port2_P - Port1_P	20			dB	
Port2_N - Port3_N	20			dB	
Port2_P - Port3_N	20			dB	
Port2_N - Port3_P	20			dB	
Port2_P - Port3_P	20			dB	2300MHz to 2690MHz z; Port2 to Port1 active
Port3_N - Port1_N	20			dB	
Port3_P - Port1_N	20			dB	
Port3_N - Port1_P	20			dB	
Port3_P - Port1_P	20			dB	
Port3_N - Port2_N	20			dB	
Port3_P - Port2_N	20			dB	
Port3_N - Port2_P	20			dB	
Port3_P - Port2_P	20			dB	
Balanced Isolation					
Port3_N/P - Port1_N/P	33	34		dB	TX = 2170MHz to 2690MHz, Port2 to Port1 path active, Port2_N/P terminated in 50 Ω
Port2_N/P - Port1_N/P	35	36		dB	TX = 2170MHz to 2690MHz z, Port3 to Port1 path active, Port3_N/P terminated in 50 Ω
Port3_N/P - Port1_N/P	34	35		dB	TX = 1710MHz to 2170MHz z, Port2 to Port1 path active, Port2_N/P terminated in 50 Ω
Port2_N/P - Port1_N/P	37	38		dB	TX = 1710MHz to 170MHz z, Port3 to Port1 path active, Port3_N/P terminated in 50 Ω
Phase Balance					
	-1	0	+1	Deg.	Between active paths; Test frequency 2690MHz
Amplitude Balance					
	-1	0	+1	dB	Between active paths; Test frequency 2690MHz
VSWR					
Port2 or Port3			1.5	:1	2300MHz to 2690MHz
Port1			1.5	:1	

Absolute Maximum Ratings

Table 5. Maximum ratings

Parameters	Range	Units
Power supply (VDD)	2.0 ~ 3.3	V
Control voltage (V1)	1.6 ~ 3.3	V
Maximum Input Power	+30	dBm
Operation Temperature Range	-40~85	°C
Junction Temperature	150	°C
Storage temperature Range	-65~160	°C
Soldering Temperature (reflow)	260	°C
Human Body Mode ESD	-1200~+1200	V
Machine Mode ESD	-100~+100	V
Charge Device Mode ESD	-500~+500	V

Package Outline Dimension

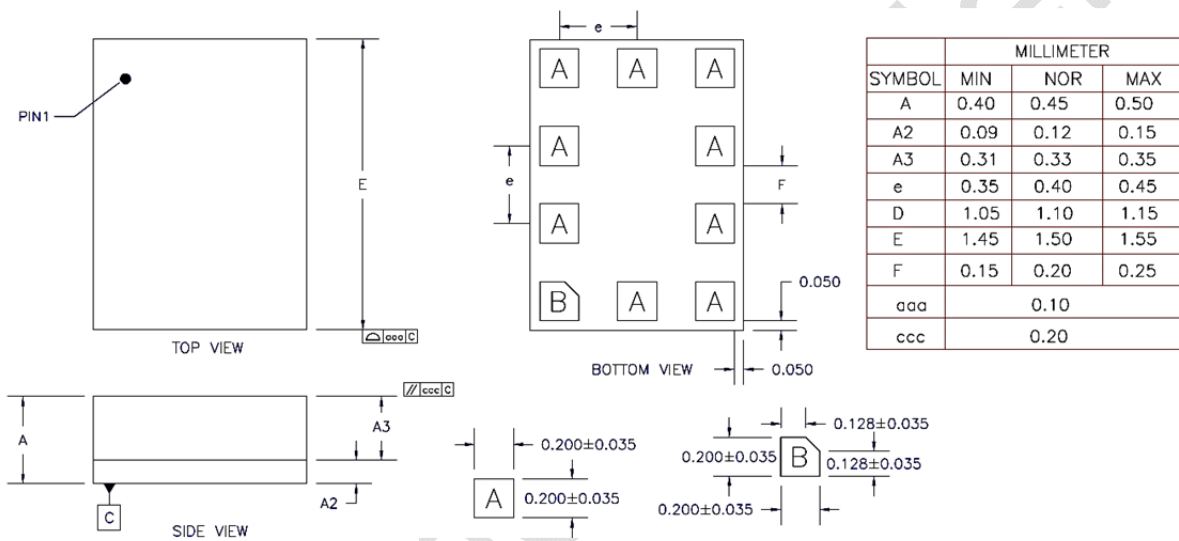


Figure 3. package outline dimension

Reflow Chart

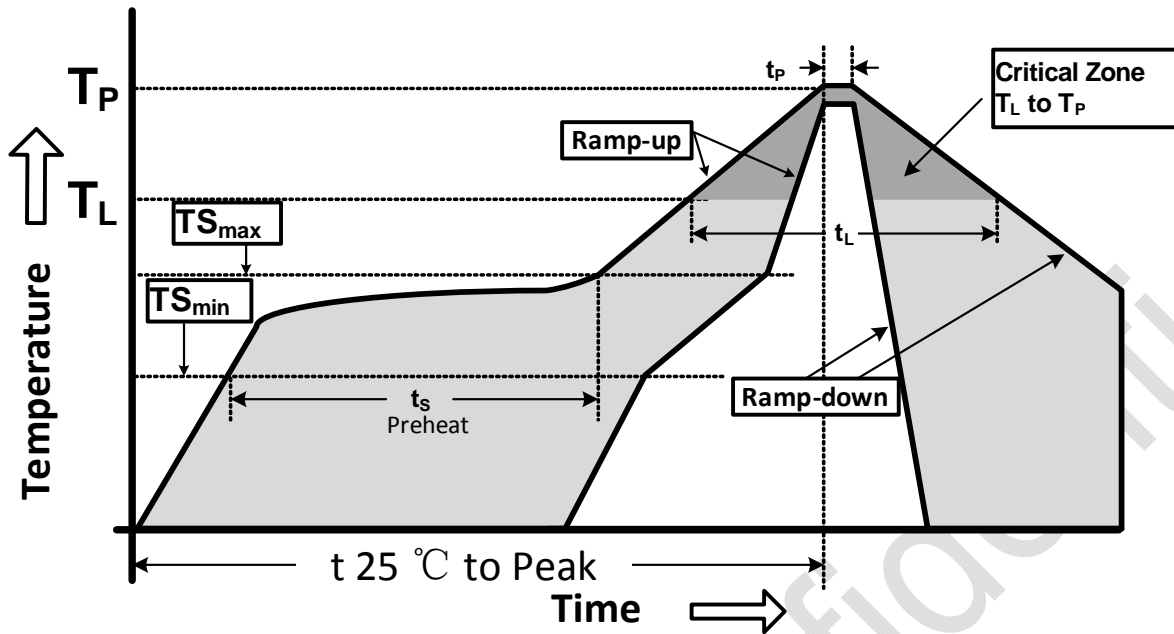


Figure 4. Recommended Lead-Free Reflow Profile

Table 6. Reflow condition

Profile Parameter	Lead-Free Assembly, Convection, IR/Convection
Ramp-up rate (TS _{max} to T _p)	3°C/second max.
Preheat temperature (TS _{min} to TS _{max})	150°C to 200°C
Preheat time (t _s)	60 - 180 seconds
Time above TL, 217°C (t _L)	60 - 150 seconds
Peak temperature (T _p)	260°C
Time within 5°C of peak temperature(t _p)	20 - 40 seconds
Ramp-down rate	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electric charge. Proper ESD protection techniques should be used when handling these devices.

RoHS Compliant

This product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE), and are considered RoHS compliant.

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