



## **MXD86C0S**

SP12T Switch with MIPI for LTE Diversity

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### General Description

The MXD86C0S is a low loss, high isolation SP12T switch for antenna diversity receiving.

The MXD86C0S is compatible with MIPI control, which is a key requirement for many cellular transceivers. This part is packaged in a compact 2.5mm x 2.5mm, 20-pin, QFN package which allows for a small solution size with no need for external DC blocking capacitors (when no external DC is applied to the device ports).

### Features

- Excellent insertion loss
  - 0.70 dB Insertion Loss at 2.7GHz
- P0.1dB @ 27dBm
- Multi-Band operation 700MHz to 3000MHz
- RFFE serial control interface
- Compact 2.5mm x 2.5mm in QFN-20 package , MSL3
- No DC blocking capacitors required (unless external DC is applied to the RF ports)

### Applications

- 2G/3G/4G antenna diversity
- Cellular modems and USB Devices

### Functional Block Diagram and Pin Function

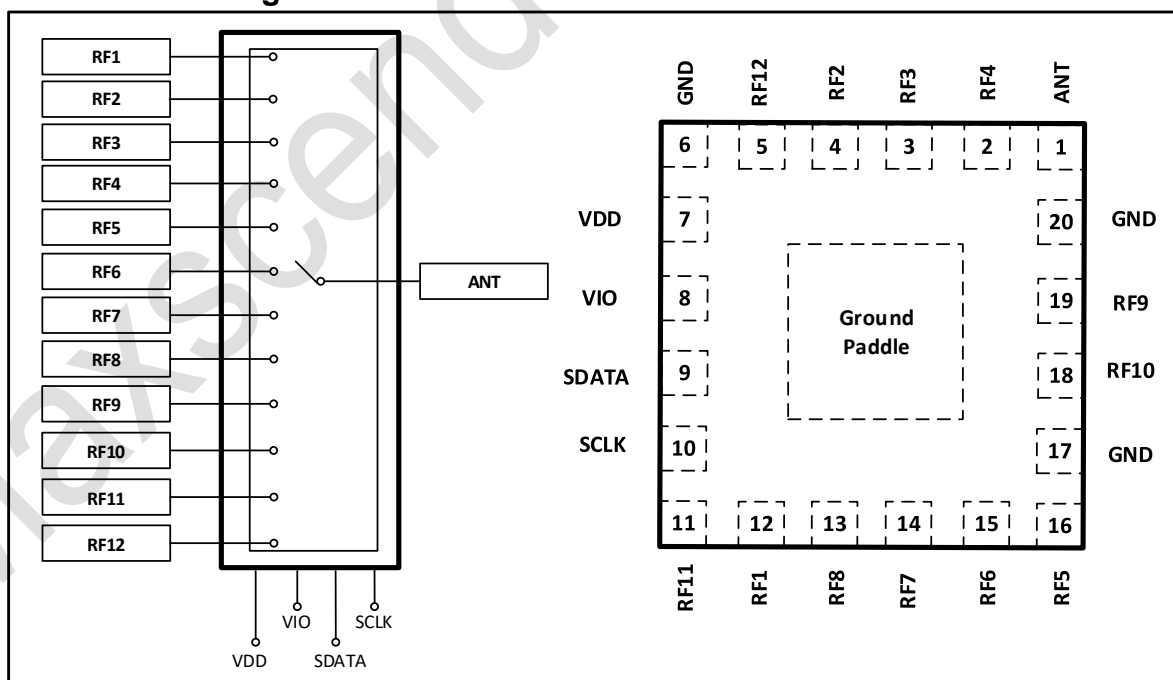


Figure 1 Functional Block Diagram and Pinout (Top View)

Application Circuit

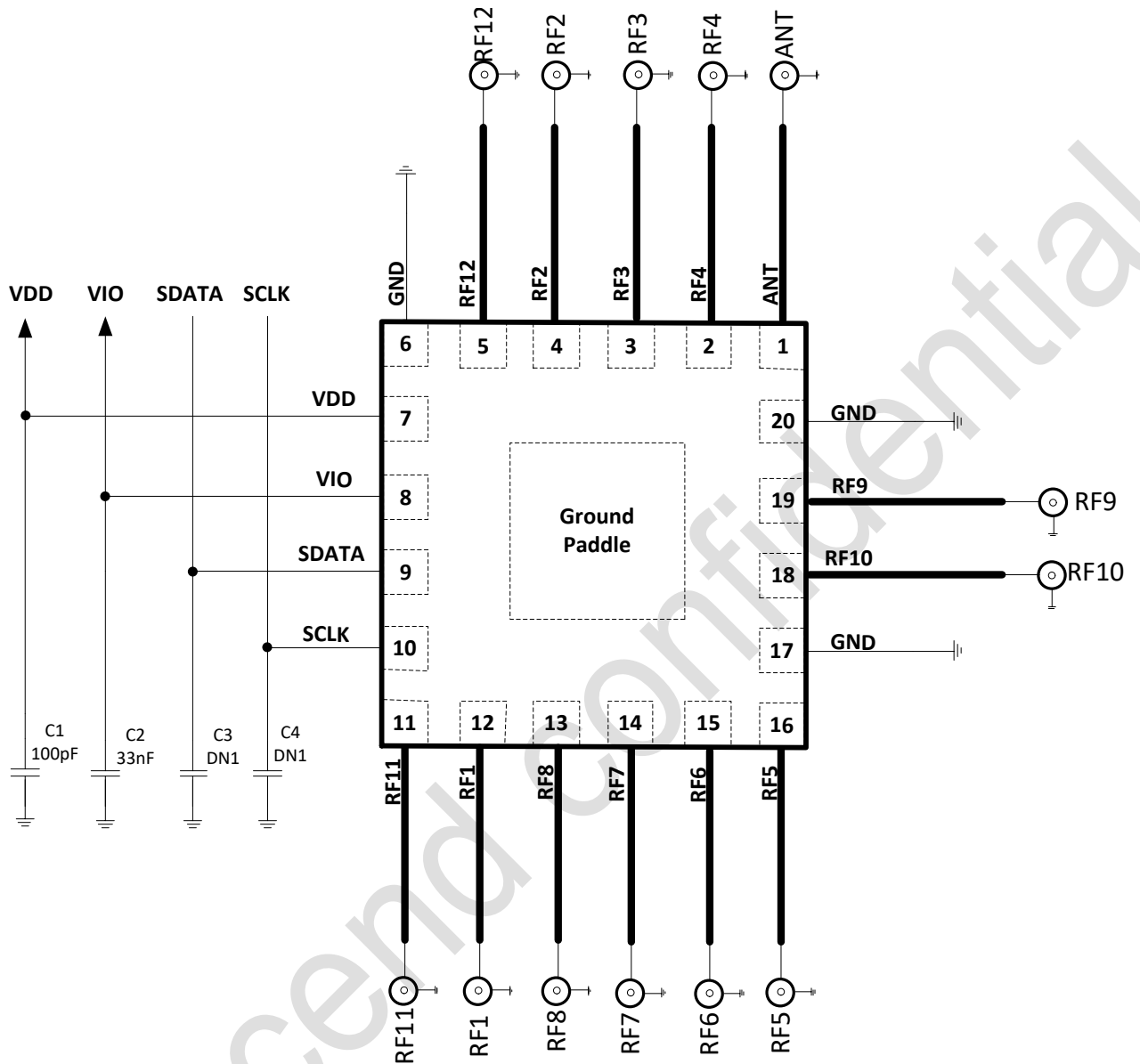


Figure 2 Evaluation Board Schematic

Table 1. Pin Description

| Pin No.       | Name  | Description             | Pin No. | Name | Description |
|---------------|-------|-------------------------|---------|------|-------------|
| 1             | ANT   | Antenna port            | 11      | RF11 | RF port11   |
| 2             | RF4   | RF port4                | 12      | RF1  | RF port1    |
| 3             | RF3   | RF port3                | 13      | RF8  | RF port8    |
| 4             | RF2   | RF port2                | 14      | RF7  | RF port7    |
| 5             | RF12  | RF port12               | 15      | RF6  | RF port6    |
| 6             | GND   | Ground                  | 16      | RF5  | RF port5    |
| 7             | VDD   | Power supply            | 17      | GND  | Ground      |
| 8             | VIO   | Supply voltage for MIPI | 18      | RF10 | RF port10   |
| 9             | SDATA | MIPI data input/output  | 19      | RF9  | RF port9    |
| 10            | SCLK  | MIPI clock              | 20      | GND  | Ground      |
| Ground Paddle | GND   | Ground                  |         |      |             |

**Note:** Bottom ground paddles must be connected to ground.

**Truth Table**
**Table 2.**

| State | Mode    | Register_0 |    |    |    |    |    |    |    |
|-------|---------|------------|----|----|----|----|----|----|----|
|       |         | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1     | ISO     | x          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| 2     | RF1 on  | x          | 0  | 0  | 0  | 0  | 1  | 0  | 1  |
| 3     | RF2 on  | x          | 0  | 0  | 0  | 1  | 0  | 0  | 1  |
| 4     | RF3 on  | x          | 0  | 0  | 0  | 1  | 0  | 1  | 1  |
| 5     | RF4 on  | x          | 0  | 0  | 0  | 1  | 0  | 1  | 0  |
| 6     | RF5 on  | x          | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| 7     | RF6 on  | x          | 0  | 0  | 0  | 0  | 1  | 0  | 0  |
| 8     | RF7 on  | x          | 0  | 0  | 0  | 0  | 0  | 1  | 1  |
| 9     | RF8 on  | x          | 0  | 0  | 0  | 1  | 1  | 0  | 0  |
| 10    | RF9 on  | x          | 0  | 0  | 0  | 0  | 0  | 1  | 0  |
| 11    | RF10 on | x          | 0  | 0  | 0  | 1  | 0  | 0  | 0  |
| 12    | RF11 on | x          | 0  | 0  | 0  | 0  | 1  | 1  | 0  |
| 13    | RF12 on | x          | 0  | 0  | 0  | 0  | 1  | 1  | 1  |

**Recommended Operation Range**
**Table 3. Recommended Operation Condition**

| Parameters                | Symbol          | Min                 | Typ | Max  | Units |
|---------------------------|-----------------|---------------------|-----|------|-------|
| Operation Frequency       | f1              | 0.7                 | -   | 3.0  | GHz   |
| Power supply              | V <sub>DD</sub> | 2.5                 | 2.8 | 3.0  | V     |
| Power supply for MIPI     | V <sub>IO</sub> | 1.65                | 1.8 | 1.95 | V     |
| MIPI Control Voltage High | V <sub>H</sub>  | 0.8*V <sub>IO</sub> | 1.8 | 1.95 | V     |
| MIPI Control Voltage Low  | V <sub>L</sub>  | 0                   | 0   | 0.3  | V     |

**Specifications**
**Table 4. Electrical Specifications**

| Parameter  | Symbol             | Test Condition     | Min                  | Typical         | Max  | Units |
|--|--------------------|--------------------|----------------------|-----------------|------|-------|
| <b>DC Specifications</b>   |                    |                    |                      |                 |      |       |
| Supply voltage   | V <sub>DD</sub>    |                    | 2.5                  | 2.8             | 3.0  | V     |
| Supply current   | I <sub>DD</sub>    |                    |                      | 30              | 50   | uA    |
| V <sub>IO</sub> supply voltage   | V <sub>IO</sub>    |                    | 1.65                 | 1.8             | 1.95 | V     |
| V <sub>IO</sub> Supply current   | I <sub>IO</sub>    |                    |                      | 4               | 10   | uA    |
| SDATA, SCLK control voltage: High<br>Low                                   | V <sub>CTL_H</sub> |                    | 0.8* V <sub>IO</sub> | V <sub>IO</sub> | 1.95 | V     |
|  | V <sub>CTL_L</sub> |                    | 0                    | 0               | 0.3  | V     |
| Switching Speed, one RF to another   |                    | 10% to 90% RF      |                      | 1               | 2    | uS    |
| <b>RF Specifications</b>   |                    |                    |                      |                 |      |       |
| Insertion loss (ANT pin to<br>RF1/2/3/4/5/6/7/8/9/10/11/12 pins)           | IL                 | 0.1 to 1.0 GHz     |                      | 0.50            |      | dB    |
|  |                    | 1.0 to 2.0 GHz     |                      | 0.60            |      | dB    |
|  |                    | 2.0 to 2.7 GHz     |                      | 0.70            |      | dB    |
| Isolation (ANT pin to<br>RF1/2/3/4/5/6/7/8/9/10/11/12 pins)                | Iso                | 0.1 to 1.0 GHz     | 35                   | 38              |      | dB    |
|  |                    | 1.0 to 2.0 GHz     | 25                   | 30              |      | dB    |
|  |                    | 2.0 to 2.7 GHz     | 18                   | 22              |      | dB    |
| Input return loss (ANT pin to<br>RF1/2/3/4/5/6/7/8/9/10/11/12 pins)        | RL                 | 0.1 to 1.0 GHz     | 20                   | 25              |      | dB    |
|  |                    | 1.0 to 2.0 GHz     | 15                   | 20              |      | dB    |
|  |                    | 2.0 to 2.7 GHz     | 12                   | 15              |      | dB    |
| 0.1 dB Compression Point (ANT pin to<br>RF1/2/3/4/5/6/7/8/9/10/11/12 pins) | P0.1dB             | 0.7 GHz to 3.0 GHz |                      | +27             |      | dBm   |

### MIPI Read and Write Timing

MIPI supports the following Command Sequences:

- Register Write
- Register\_0 Write
- Register Read

Figures 3 and 4 provide the timing diagrams for register write commands and read commands, respectively. Figure 5 shows the Register 0 Write Command Sequence. Refer to the MIPI Alliance Specification for RF Front-End Control Interface (RFFE), v1.10 (26 July 2011) for additional information on MIPI USID programming sequences and MIPI bus specifications.

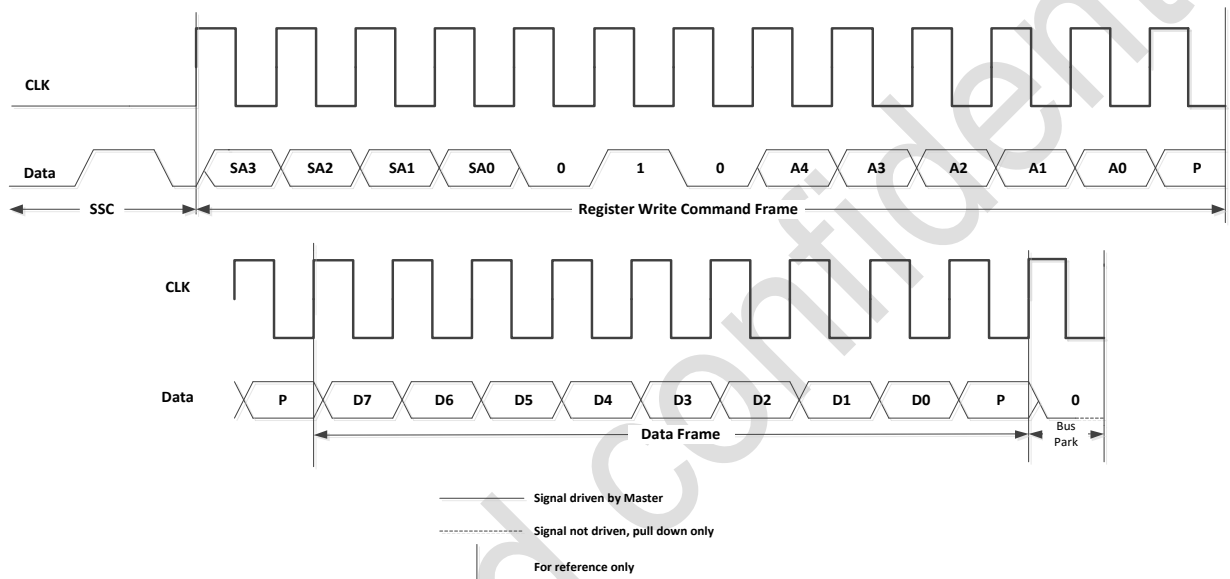


Figure 3 Register Write Command Sequence

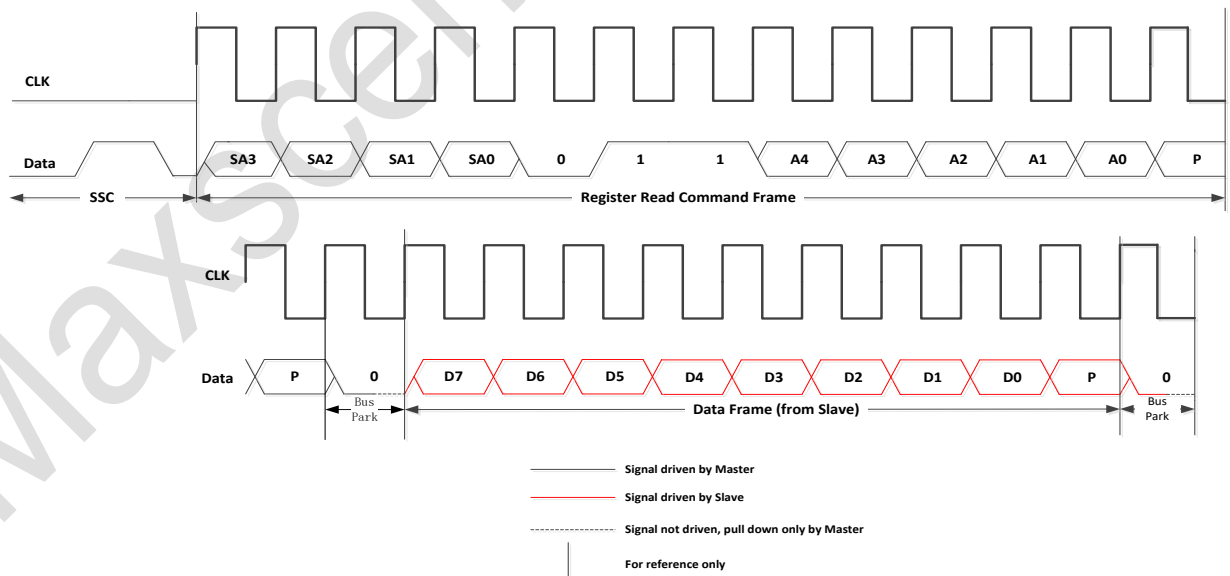
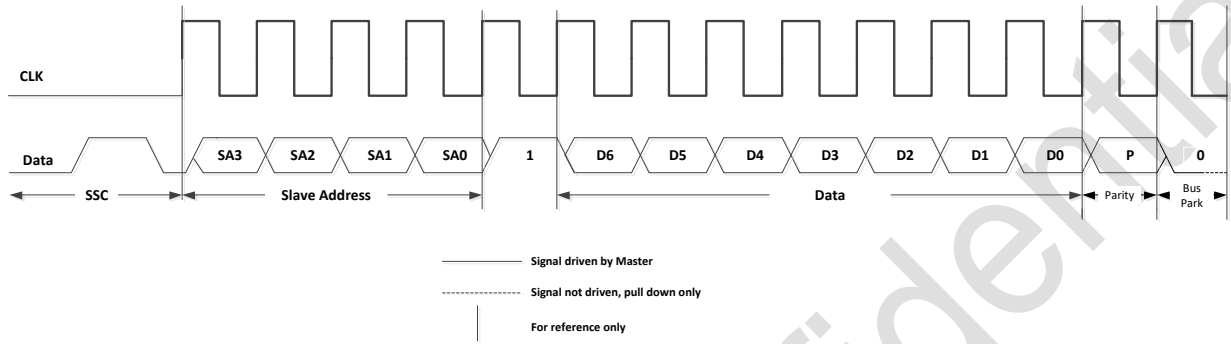


Figure 4 Register Read Command Sequence

In the timing figures, SA[3:0] is slave address. A[4:0] is register address. D[7:0] is data. “P” is odd parity bit.

**Register 0 Write Command Sequence**

Figure shows the Register 0 Write Command Sequence. The Command Sequence starts with an SSC, followed by the Register 0 Write Command Frame containing the Slave address, a logic one, and a seven bit word to be written to Register 0. The Command Sequence ends with a Bus Park Cycle.



**Figure 5 Register 0 Write Command Sequence**

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**Register definition**
**Table 5. Register definition table**

| Register Address | Register Name   | Data Bits | R/W | Function             | Description   | Default | BROADC AST_ID support | Trigger support |
|------------------|-----------------|-----------|-----|----------------------|---|---------|-----------------------|-----------------|
| 0x00             | REGISTER_0      | 7:0       | R/W | RF Control           | Register_0 truth Table: Table 2   | 0x00    | No                    | Yes             |
| 0x001B           | GROUP_SID       | 7:4       | R   | RESERVED             |   | 0x0     | No                    | No              |
|                  |                 | 3:0       | R/W | GSID                 | Group Slave ID  | 0x0     | No                    | No              |
| 0x001C           | PM_TRIG         | 7:6       | R/W | PWR_MODE             | 00: Normal Operation (ACTIVE)<br>01: Reset all registers to default settings (STARTUP)<br>10: Low power (LOW POWER)<br>11: Reserved<br>Note: Write PWR_MODE=2'h1 will reset all register, and puts the device into STARTUP state. | 0b10    | Yes                   | No              |
|                  |                 | 5         | R/W | Trigger_Mask_2       | If this bit is set, trigger 2 is disabled   | 0       | No                    | No              |
|                  |                 | 4         | R/W | Trigger_Mask_1       | If this bit is set, trigger 1 is disabled   | 0       | No                    | No              |
|                  |                 | 3         | R/W | Trigger_Mask_0       | If this bit is set, trigger 0 is disabled.<br>Note: When all triggers are disabled, writing to a register that is associated with trigger 0, 1, or 2, causes the data to go directly to the destination register.                 | 0       | No                    | No              |
|                  |                 | 2         | W   | Trigger_2            | A write of a one to this bit loads trigger 2's registers  | 0       | Yes                   | No              |
|                  |                 | 1         | W   | Trigger_1            | A write of a one to this bit loads trigger 1's registers  | 0       | Yes                   | No              |
|                  |                 | 0         | W   | Trigger_0            | A write of a one to this bit loads trigger 0's registers<br>Note: Trigger processed immediately then cleared. Trigger 0, 1, and 2 will always read as 0.  | 0       | Yes                   | No              |
| 0x001D           | PRODUCT_ID      | 7:0       | R   | PRODUCT_ID           | Product Number  | 0x5d    | No                    | No              |
| 0x001E           | MANUFACTURER_ID | 7:0       | R   | MANUFACTURER_ID[7:0] | Lower eight bits of MIPI registered Manufacturer ID   | 0x81    | No                    | No              |
| 0x001F           | MAN_USID        | 7:6       | R   | RESERVED             |   | 0b00    | No                    | No              |
|                  |                 | 5:4       | R   | MANUFACTURER_ID[9:8] | Upper two bits of MIPI registered Manufacturer ID   | 0b11    | No                    | No              |
|                  |                 | 3:0       | R/W | USID                 | USID of the device.   | 0xb     | No                    | No              |

**Absolute Maximum Ratings**
**Table 6. Maximum ratings**

| Parameters   | Symbol           | Minimum | Maximum | Units |
|--|------------------|---------|---------|-------|
| Supply voltage   | V <sub>DD</sub>  | +2.0    | +3.3    | V     |
| Supply voltage for MIPI                                  | V <sub>IO</sub>  | +1.0    | +2.0    | V     |
| MIPI Control voltage (SDATA, SCLK)                       | V <sub>CTL</sub> | 0       | +2.0    | V     |
| RF input power (RF1 to RF12)                             | P <sub>IN</sub>  |         | +28     | dBm   |
| Operating temperature                                    | T <sub>OP</sub>  | -35     | +90     | °C    |
| Storage temperature                                      | T <sub>STG</sub> | -40     | +125    | °C    |
| Electrostatic Discharge Human body model (HBM), Class 1C | ESD_HBM          |         | 1000    | V     |
| Machine Model (MM), Class A                              | ESD_MM           |         | 100     |       |
| Charged device model (CDM), Class III                    | ESD_CDM          |         | 500     |       |

**Note:** Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device

**Power ON and OFF sequence**

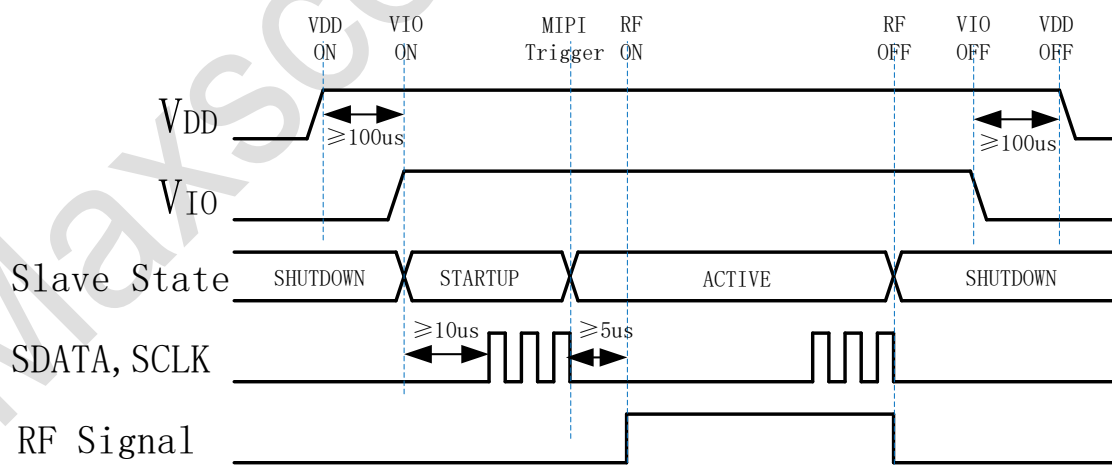
Here is the recommendation about power-on/off sequence in order to avoid damaging the device.

**Power ON**

- 1) Apply voltage supply - V<sub>DD</sub>
- 2) Apply logic supply - V<sub>IO</sub>
- 3) Wait 10μs or greater and then apply MIPI bus signals – SCLK and SDATA
- 4) Wait 5μs or greater after MIPI bus goes idle and then apply the RF Signal

**Power OFF**

- 1) Remove the RF Signal
- 2) Remove MIPI bus – SCLK and SDATA
- 3) Remove logic supply - V<sub>IO</sub>
- 4) Remove voltage supply - V<sub>DD</sub>



**Note:** V<sub>IO</sub> can be applied to the device before V<sub>DD</sub> or removed after V<sub>DD</sub>.

It is important to wait 10μs after V<sub>IO</sub> & V<sub>DD</sub> are applied before sending SDATA to ensure correction data transmission.

The minimum time between a power up and power down sequence (and vice versa) is ≥ 100μs.



Package Outline Dimension

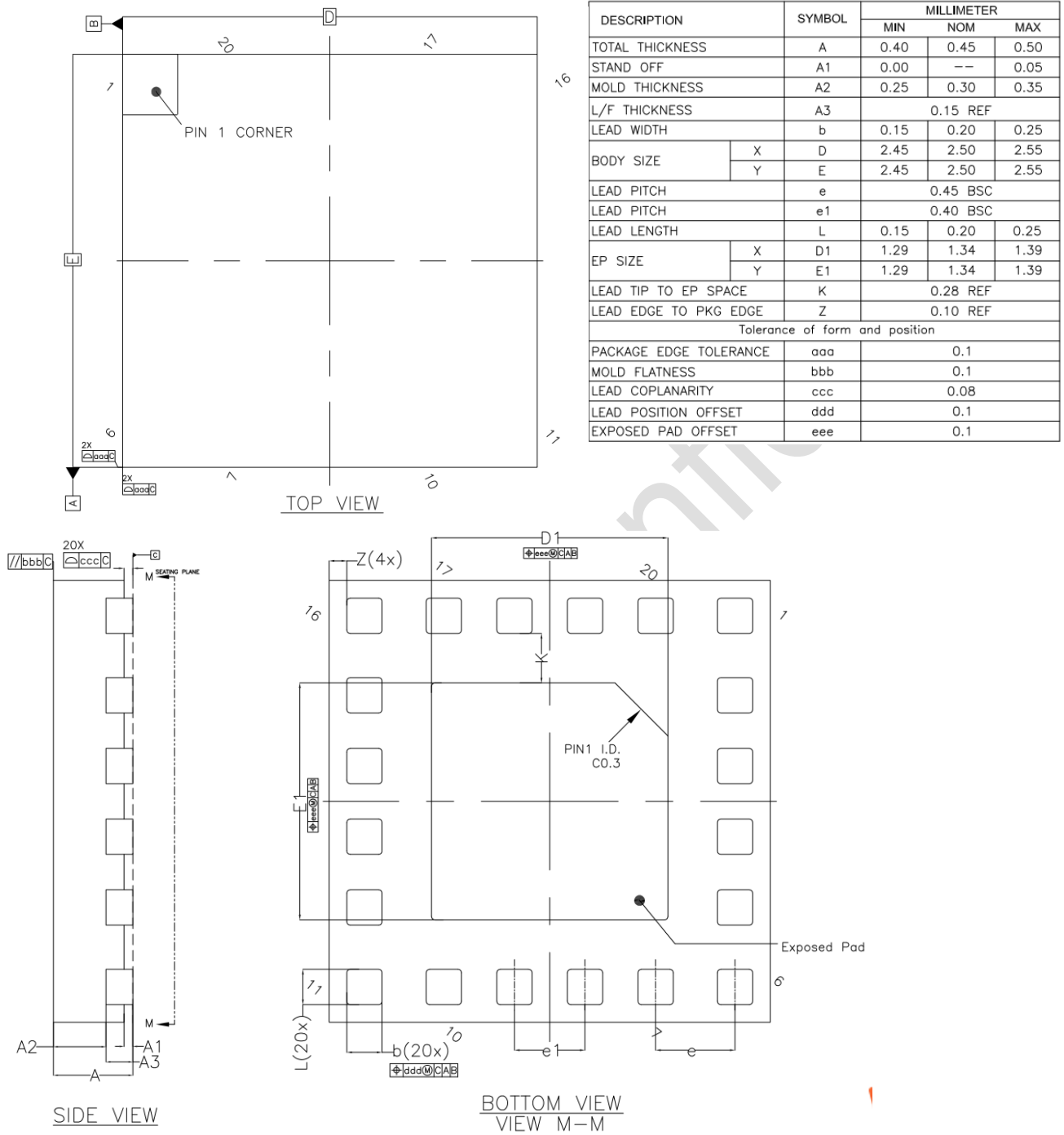


Figure 6 package outline dimension

**Marking Specification**

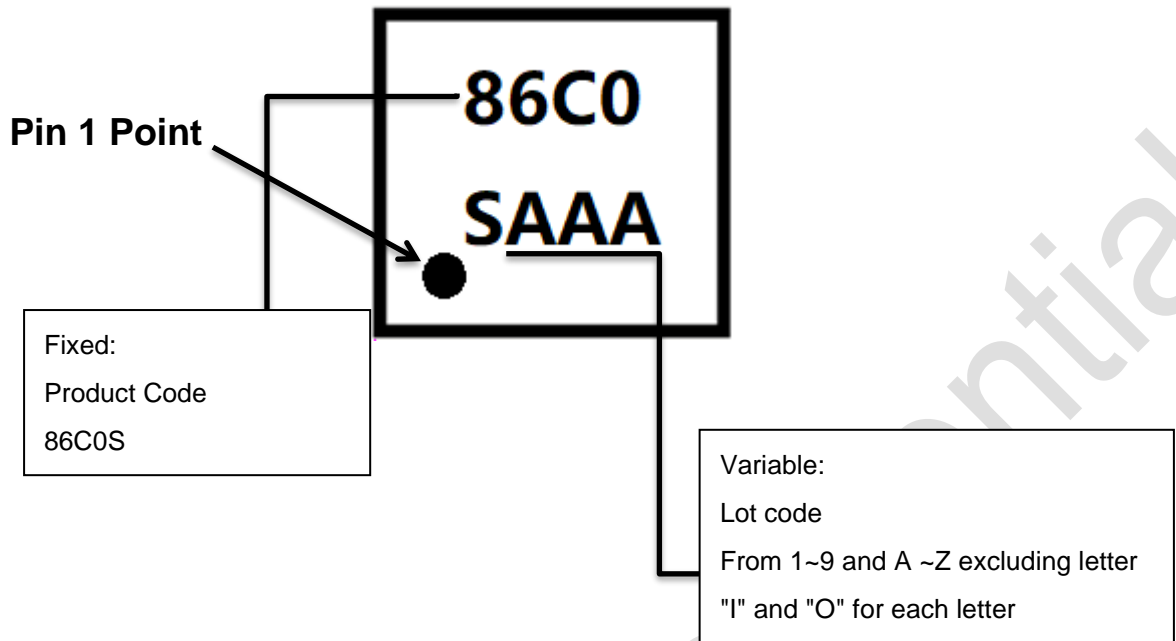
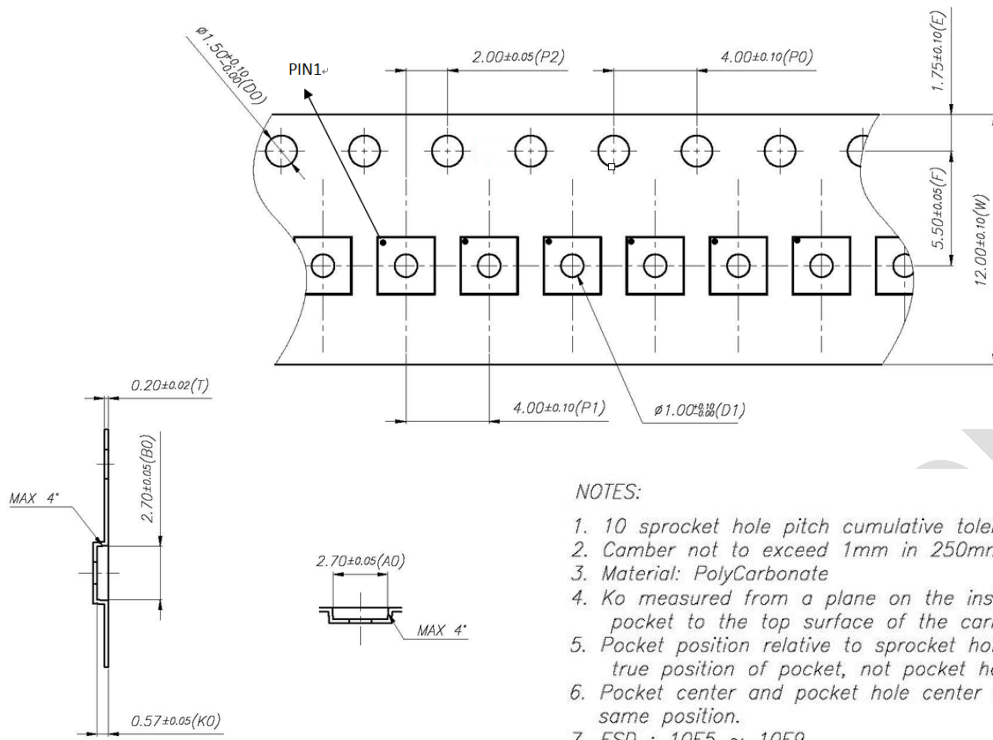


Figure 7 Marking specification (Top View)

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Tape and Reel Dimensions



NOTES:

1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$
2. Camber not to exceed 1mm in 250mm
3. Material: PolyCarbonate
4.  $K_0$  measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
5. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
6. Pocket center and pocket hole center must be same position.
7. ESD : 10E5 ~ 10E9

Figure 8 Tape and reel dimensions

## Reflow Chart

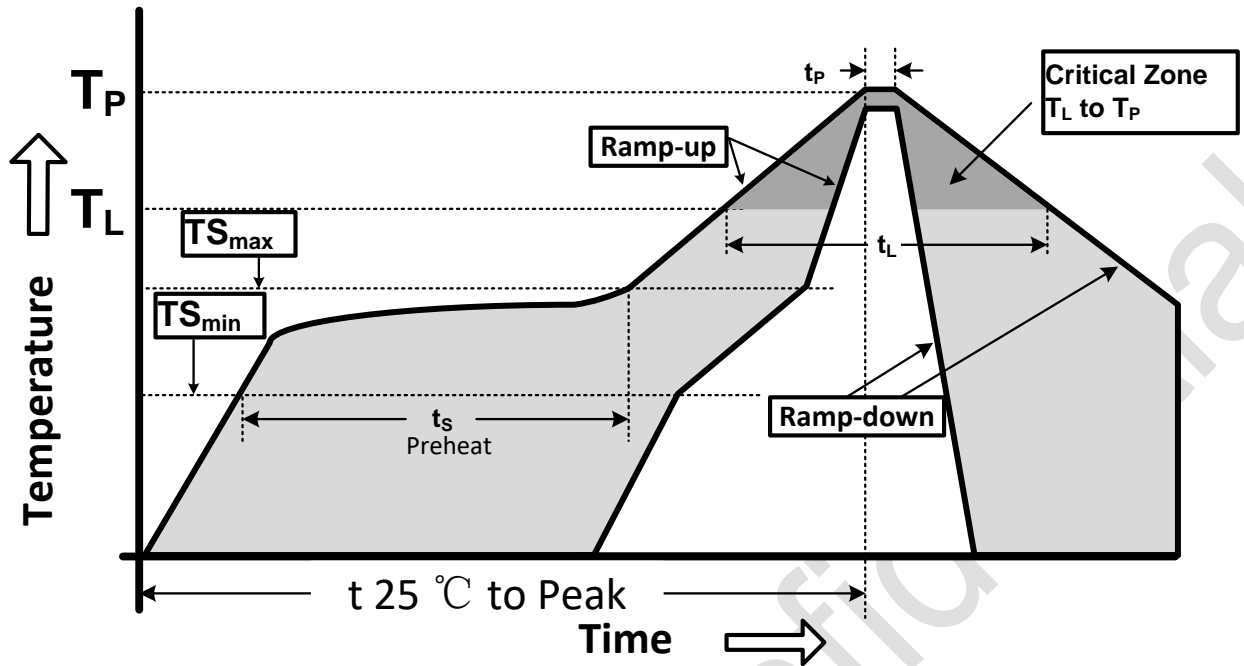


Figure 9 Recommended Lead-Free Reflow Profile

Table 7. Reflow condition

| Profile Parameter                                      | Lead-Free Assembly, Convection, IR/Convection |
|--|---|
| Ramp-up rate ( $T_{S_{max}}$ to $T_P$ )                | 3°C/second max.                               |
| Preheat temperature ( $T_{S_{min}}$ to $T_{S_{max}}$ ) | 150°C to 200°C                                |
| Preheat time ( $t_s$ )                                 | 60 - 180 seconds                              |
| Time above $T_L$ , 217°C ( $t_L$ )                     | 60 - 150 seconds                              |
| Peak temperature ( $T_P$ )                             | 260°C   |
| Time within 5°C of peak temperature( $t_p$ )           | 20 - 40 seconds                               |
| Ramp-down rate   | 6°C/second max.                               |
| Time 25°C to peak temperature                          | 8 minutes max.                                |

### ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electric charge. Proper ESD protection techniques should be used when handling these devices.

### RoHS Compliant

This product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE), and are considered RoHS compliant.

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