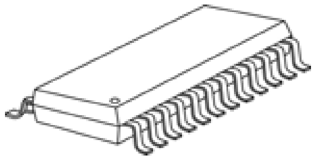
16-Channel Constant Current LED Sink Driver with Low Knee Voltage

Features

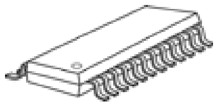
- 16 constant-current output channels
- Constant output current invariant to load voltage change:
  Constant output current range:
  3-45mA@V_{DD}=5V;
  3-30mA@V_{DD}=3.3V
- Excellent output current accuracy:
  -between channels: ±1.5% (typ.) and ±3% (max.)
  -between ICs: ±3% (typ.) and ±6% (max.)
- Low Knee Voltage:
  I_{OUT}=20mA@V_{DS}=0.2V; V_{DD}=3.3V
  I_{OUT}=20mA@V_{DS}=0.2V; V_{DD}=5.0V
- Output current adjusted through an external resistor
- Fast response of output current, $\overline{OE}$ (min.): 70ns with good uniformity between output channels
- Staggered delay of output
- 25MHz clock frequency
- Schmitt trigger input
- 3.3V/ 5V supply voltage
- "Pb-free & Green" Package

Small Outline Package



GF: SOP24L-300-1.00

Shrink SOP



GP: SSOP24L-150-0.64

Product Description

MBI5035 is a 16-channel constant current LED driver with V_{DS}=0.2V @ I_{OUT}=20mA, which is excellent compared to the conventional design. MBI5035 is especially designed for low power consumption LED display applications. The low knee voltage (LKV) design makes MBI5035 work at a constant output current with low V_{DS} and still guarantee PrecisionDrive™ feature. With PrecisionDrive™, MBI5035 is designed for LED displays which require to operate at low current and match the luminous intensity of each channel. MBI5035 contains a serial buffer and data latches converting serial input data into parallel output format. At MBI5035 output stage, sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs within a large range of V_F variations.

MBI5035 provides users with great flexibility and device performance in their low power system design for LED display applications. It accepts an input voltage range from 3.3V to 5.0V and maintains constant current up from 3mA to 45mA determined by an external resistor, R_{ext}, which gives users flexibility in controlling the light intensity of LEDs. MBI5035 guarantees to endure maximum 17V at the output port. The high clock frequency, 25 MHz, also satisfies the system requirements of high volume data transmission.

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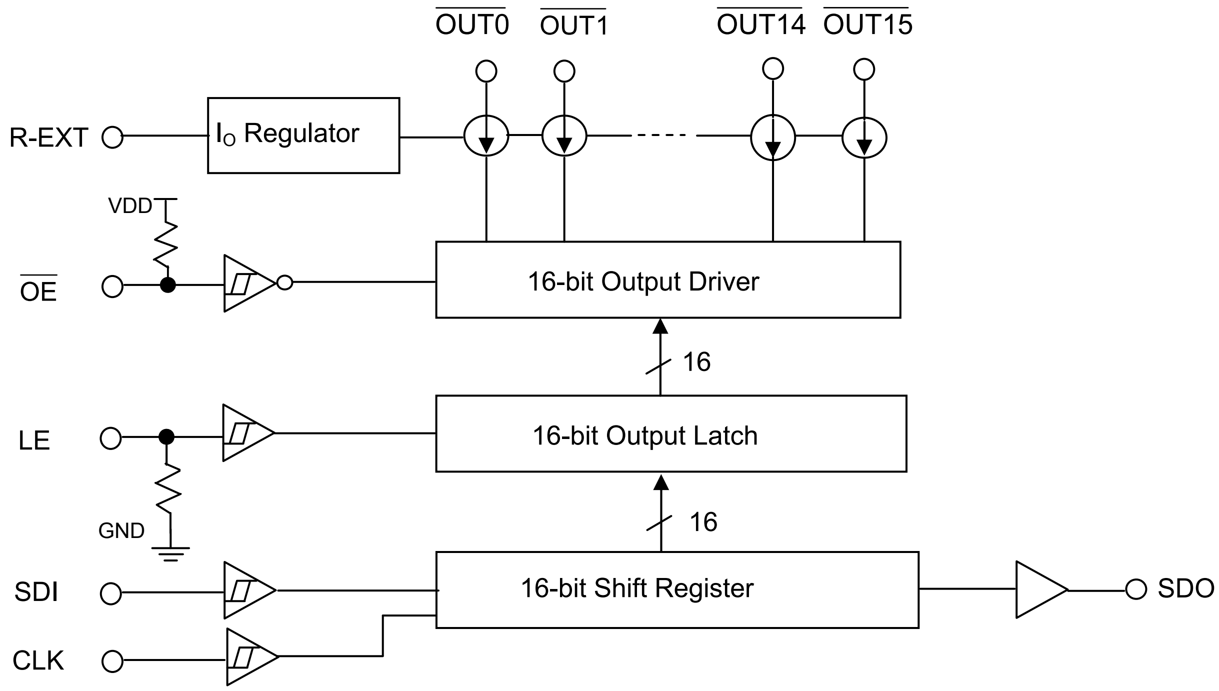
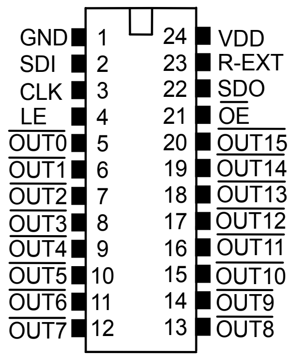
Block Diagram



Terminal Description

Pin No.	Pin Name	Function
1	GND	Ground terminal for control logic and current sink
2	SDI	Serial-data input to the shift register
3	CLK	Clock input terminal for data shift on rising edge
4	LE	Data strobe input terminal Serial data is transferred to the output latch when LE is high. The data will be latched when LE goes low.
5~20	$\overline{\text{OUT0}}$ ~ $\overline{\text{OUT15}}$	Constant current output terminals
21	$\overline{\text{OE}}$	Output enable terminal When $\overline{\text{OE}}$ is (active) low, the output drivers are enabled; when $\overline{\text{OE}}$ is high, all output drivers are turned OFF (blanked).
22	SDO	Serial-data output to the following SDI of next driver IC. SDO signal changes on rising edge of CLK.
23	R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
24	VDD	3.3V/5V supply voltage terminal

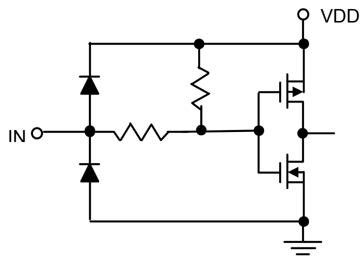
Pin Configuration



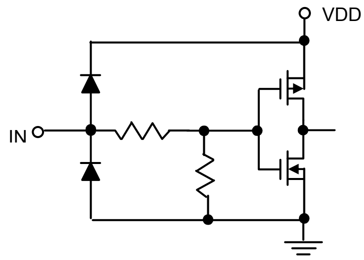
MBI5035 GF\GP

Equivalent Circuits of Inputs and Outputs

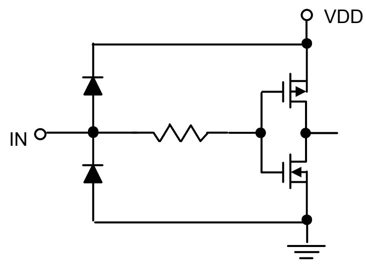
$\overline{OE}$ terminal



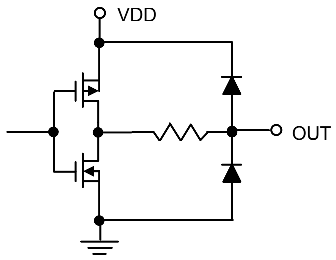
LE terminal



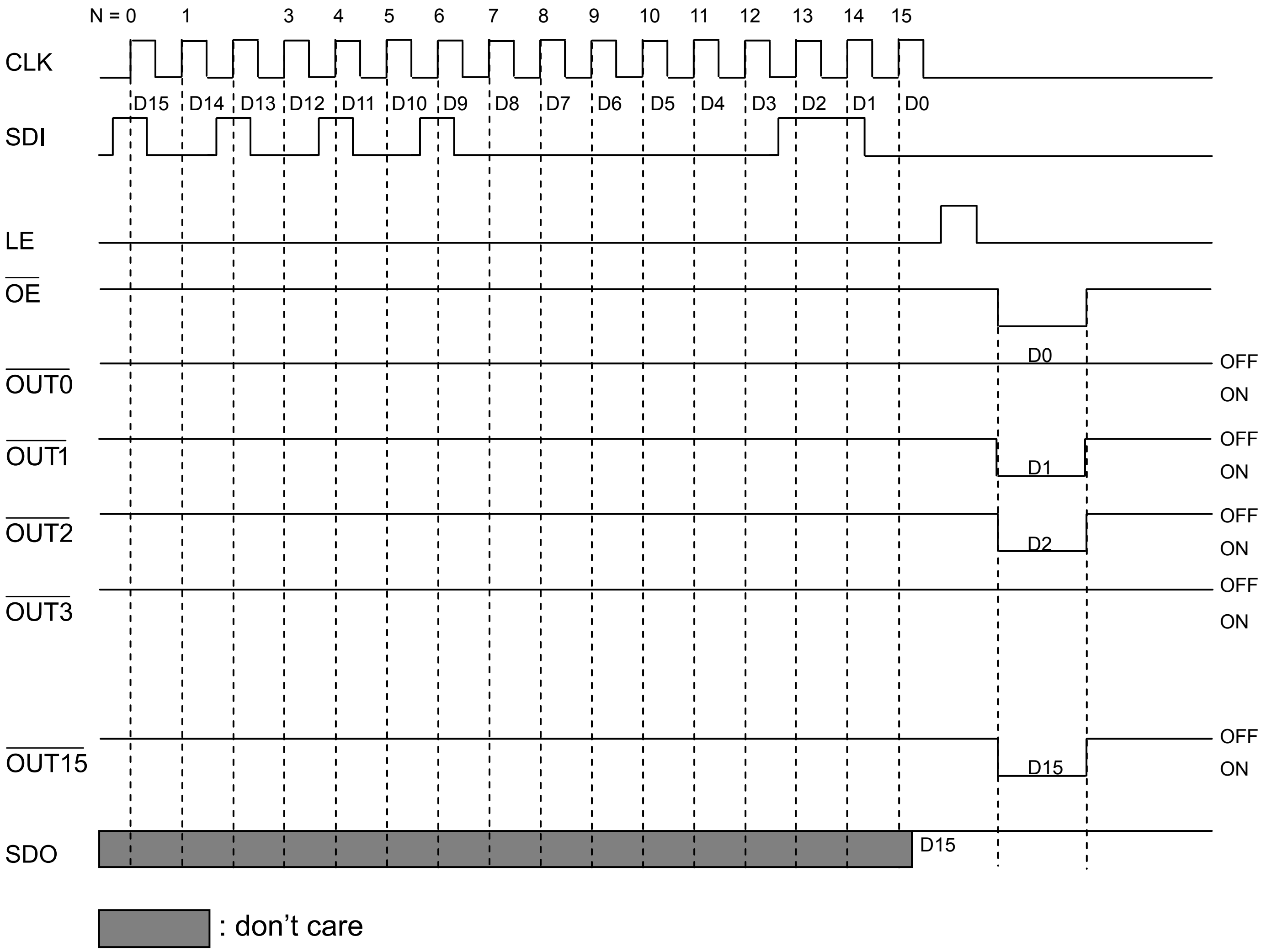
CLK, SDI terminal



SDO terminal



Timing Diagram



Truth Table

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}$ … $\overline{OUT7}$ … $\overline{OUT15}$	SDO
↑	H	L	D_n	$\overline{D_n}$ ….. $\overline{D_{n-7}}$ …. $\overline{D_{n-15}}$	D_{n-15}
↑	L	L	D_{n+1}	No Change	D_{n-14}
↑	H	L	D_{n+2}	$\overline{D_{n+2}}$ …. $\overline{D_{n-5}}$ …. $\overline{D_{n-13}}$	D_{n-13}
↓	X	L	D_{n+3}	$\overline{D_{n+2}}$ …. $\overline{D_{n-5}}$ …. $\overline{D_{n-13}}$	D_{n-13}
↓	X	H	D_{n+4}	Off	D_{n-13}

Maximum Ratings

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~7.0	V
Input Voltage		V_{IN}	-0.4~V_{DD}+0.4	V
Output Current		I_{OUT}	+50	mA
Sustaining Voltage at OUT Port		V_{DS}	-0.5~+17.0	V
GND Terminal Current		I_{GND}	+800	mA
Power Dissipation (On PCB, Ta=25°C)*	GF–type	P_D	2.35	W
	GP–type		1.76	
Thermal Resistance (On PCB, Ta=25°C)*	GF–type	$R_{th(j-a)}$	53.28	°C/W
	GP–type		70.90	
Junction Temperature		$T_{j,max}$	150**	°C
Operating Ambient Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C

*The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

**Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. Users should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

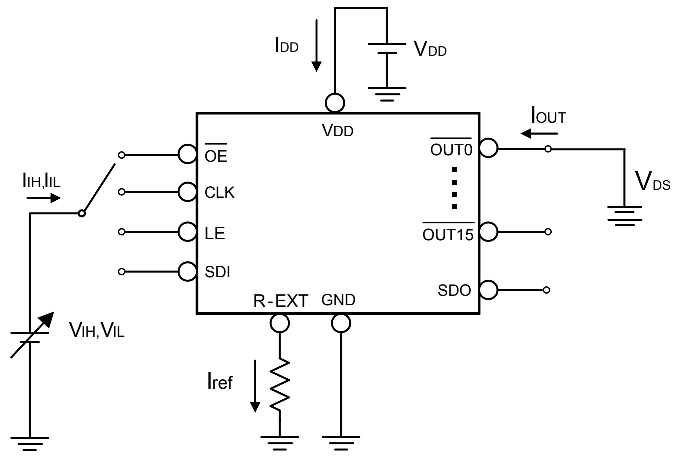
Electrical Characteristics (V_{DD}= 5.0V)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	-	4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports	V_{DS}	$\overline{\text{OUT0}}$~$\overline{\text{OUT15}}$	-	-	17.0	V
Output Current	I_{OUT}	Refer to “Test Circuit for Electrical Characteristics”	3	-	45	mA
Output Current	I_{OH}	SDO	-	-	-1.0	mA
Output Current	I_{OL}	SDO	-	-	1.0	mA
Input Voltage “H” level	V_{IH}	Ta =-40~85ºC	0.7xV_{DD}	-	V_{DD}	V
Input Voltage “L” level	V_{IL}	Ta =-40~85ºC	GND	-	0.3xV_{DD}	V
Output Leakage Current	I_{OH}	V_{DS}=17.0V	-	-	0.5	μA
Output Voltage SDO	V_{OL}	I_{OL}=+1.0mA	-	-	0.4	V
Output Voltage SDO	V_{OH}	I_{OH}=-1.0mA	V_{DD}-0.4	-	-	V
Output Current 1	I_{OUT1}	V_{DS}=0.25V, R_{ext}=930 Ω	-	20	-	mA
Current Skew (Channel)	dI_{OUT1}	I_{OUT}=20mA, V_{DS}=0.25V, R_{ext}=930Ω	-	±1.5	±3.0	%
Current Skew (IC)	dI_{OUT2}	I_{OUT}=20mA, V_{DS}=0.25V, R_{ext}=930Ω	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation	%/dV_{DS}	V_{DS} within 0.5V and 1.5V	-	±0.2	±0.5	%/V
Output Current vs. Supply Voltage Regulation	%/dV_{DD}	V_{DD} within 4.5V and 5.5V	-	±1.0	±2.0	%/V
Low Knee Voltage	V_{DS}	I_{OUT}=20mA	-	0.2	0.25	V
Pull-up Resistor	R_{IN}(up)	$\overline{\text{OE}}$	250	500	800	KΩ
Pull-down Resistor	R_{IN}(down)	LE	250	500	800	KΩ
Supply Current “OFF”	I_{DD}(off) 1	R_{ext}=Open, $\overline{\text{OUT0}}$~$\overline{\text{OUT15}}$ =Off	-	4.0	6.0	mA
Supply Current “OFF”	I_{DD}(off) 2	R_{ext}=6000Ω, $\overline{\text{OUT0}}$~$\overline{\text{OUT15}}$ =Off	-	5.5	7.5	mA
Supply Current “OFF”	I_{DD}(off) 3	R_{ext}=930Ω, $\overline{\text{OUT0}}$~$\overline{\text{OUT15}}$ =Off	-	8.0	10	mA
Supply Current “ON”	I_{DD}(on) 1	R_{ext}=6000Ω, $\overline{\text{OUT0}}$~$\overline{\text{OUT15}}$ =On	-	5.5	7.5	mA
Supply Current “ON”	I_{DD}(on) 2	R_{ext}=930Ω, $\overline{\text{OUT0}}$~$\overline{\text{OUT15}}$ =On	-	8.0	10	mA

Electrical Characteristics (V_{DD}= 3.3V)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to “Test Circuit for Electrical Characteristics”		3	-	30	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	“H” level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	“L” level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		V_{DD}-0.4	-	-	V
Output Current 1		I_{OUT1}	V_{DS}=0.25V	R_{ext}=930 Ω	-	20	-	mA
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=20mA V_{DS}=0.25V	R_{ext}=930Ω	-	±1.5	±3.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=20mA V_{DS}=0.25V	R_{ext}=930Ω	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation		%/dV_{DS}	V_{DS} within 0.5V and 1.5V		-	±0.2	±0.5	%/V
Output Current vs. Supply Voltage Regulation		%/dV_{DD}	V_{DD} within 3.0V and 3.6V		-	±1.0	±2.0	%/V
Low Knee Voltage		V_{DS}	I_{OUT}=20mA		-	0.2	0.25	V
Pull-up Resistor		R_{IN}(up)	$\overline{OE}$		250	500	800	KΩ
Pull-down Resistor		R_{IN}(down)	LE		250	500	800	KΩ
Supply Current	“OFF”	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	3.5	5.5	mA
		I_{DD}(off) 2	R_{ext}=6000Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	5.0	7.0	
		I_{DD}(off) 3	R_{ext}=930Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	7.5	9.5	
	“ON”	I_{DD}(on) 1	R_{ext}=6000Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	5.0	7.5	
		I_{DD}(on) 2	R_{ext}=930Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	7.5	9.5	

Test Circuit for Electrical Characteristics



Switching Characteristics (V_{DD}= 5.0V)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	LE-$\overline{OUT0}$	t_{pLH1}	$V_{IH}=V_{DD}$ V_{IL}=GND Rext=930Ω R_L=150Ω C_L=10PF I_{OUT}=20mA C1=100nF C2=22μF C_{SDO}=10PF V_L=3.3V	-	55	65	ns
	$\overline{OE}$-$\overline{OUT0}$	t_{pLH2}		-	55	65	ns
	CLK-SDO	t_{pLH}		-	-	40	ns
Propagation Delay Time ("H" to "L")	LE-$\overline{OUT0}$	t_{pHL1}		-	35	45	ns
	$\overline{OE}$-$\overline{OUT0}$	t_{pHL2}		-	35	45	ns
	CLK-SDO	t_{pHL}		-	-	40	ns
Staggered Delay of Output*	Output Group 1~ Output Group 2	t_{stag1}		-	5	10	ns
Pulse Width	CLK	$t_{w(CLK)}$		20	-	-	ns
	LE	$t_{w(L)}$		20	-	-	ns
Data Clock Frequency		F_{CLK}		-	-	25	MHz
Hold Time for LE		$t_{h(L)}$		10	10	-	ns
Setup Time for LE		$t_{su(L)}$		10	10	-	ns
Hold Time for SDI		$t_{h(D)}$		5	5	-	ns
Setup Time for SDI		$t_{su(D)}$		3	3	-	ns
Maximum CLK Rise Time		t_r		-	-	500	ns
Maximum CLK Fall Time		t_f		-	-	500	ns
SDO Rise Time		$t_{r,SDO}$		-	10	-	ns
SDO Fall Time		$t_{f,SDI}$		-	10	-	ns
Output Rise Time of Output Ports		t_{or}		-	30	40	ns
Output Fall Time of Output Ports		t_{of}		-	30	40	ns
$\overline{OE}$ Pulse Width		$t_{w(OE)}$		70	100	-	ns

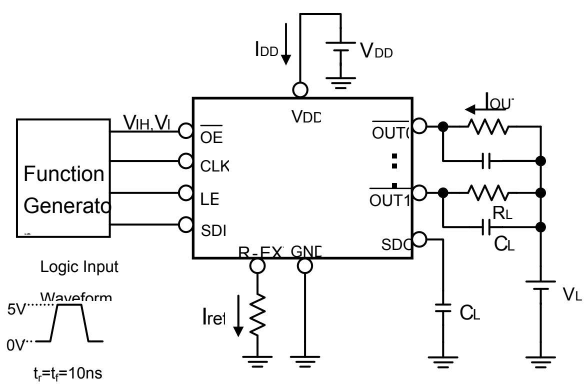
*MBI5035 has a built-in stagger circuit to perform delay mechanism. Among output ports exist a graduated 5ns delay time between $\overline{OUT2n}$ and $\overline{OUT2n+1}$, by which the output ports will be divided to two groups at a different time so that the instant current from the power line will be lowered.

Switching Characteristics (V_{DD}= 3.3V)

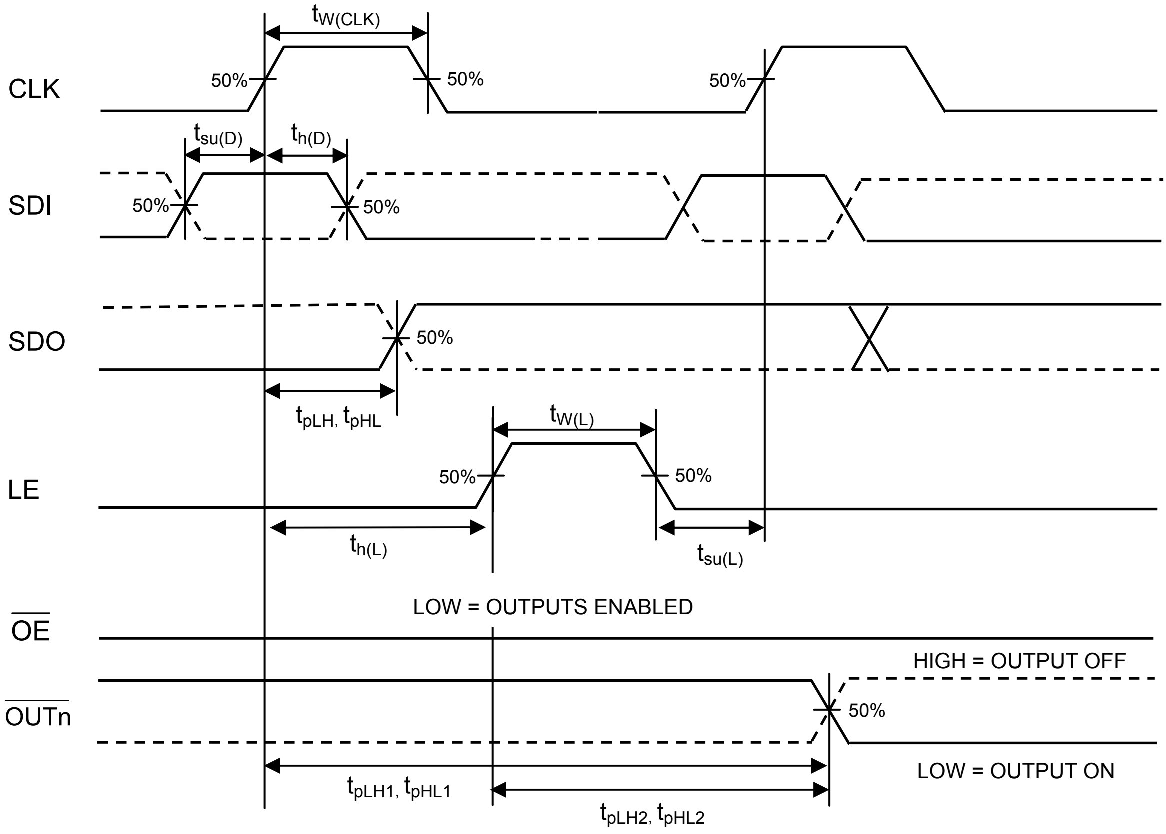
Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	LE-$\overline{OUT0}$	t_{pLH1}	V_{IH}=V_{DD} V_{IL}=GND Rext=930Ω R_L=150Ω C_L=10PF I_{OUT}=20mA C1=100nF C2=22μF C_{SDO}=10PF V_L=3.3V		65	75	ns
	$\overline{OE}$ - $\overline{OUT0}$	t_{pLH2}		-	65	75	ns
	CLK-SDO	t_{pLH}		-	-	50	ns
Propagation Delay Time ("H" to "L")	LE-$\overline{OUT0}$	t_{pHL1}		-	40	50	ns
	$\overline{OE}$ - $\overline{OUT0}$	t_{pHL2}		-	40	50	ns
	CLK-SDO	t_{pHL}		-	-	50	ns
Staggered Delay of Output	Output Group 1~Output Group 2	t_{stag1}		-	10	15	ns
Pulse Width	CLK	$t_{w(CLK)}$		20	-	-	ns
	LE	$t_{w(L)}$		20	-	-	ns
Data Clock Frequency		F_{CLK}		-	-	20	MHz
Hold Time for LE		$t_{h(L)}$		10	-	-	ns
Setup Time for LE		$t_{su(L)}$		10	-	-	ns
Hold Time for SDI		$t_{h(D)}$		5	-	-	ns
Setup Time for SDI		$t_{su(D)}$		3	-	-	ns
Maximum CLK Rise Time		t_r		-	-	500	ns
Maximum CLK Fall Time		t_f		-	-	500	ns
SDO Rise Time		$t_{r,SDO}$		-	10	-	ns
SDO Fall Time		$t_{f,SDI}$		-	10	-	ns
Output Rise Time of Output Ports		t_{or}		-	35	45	ns
Output Fall Time of Output Ports		t_{of}		-	35	45	ns
$\overline{OE}$ Pulse Width		$t_{w(OE)}$		100	130	-	ns

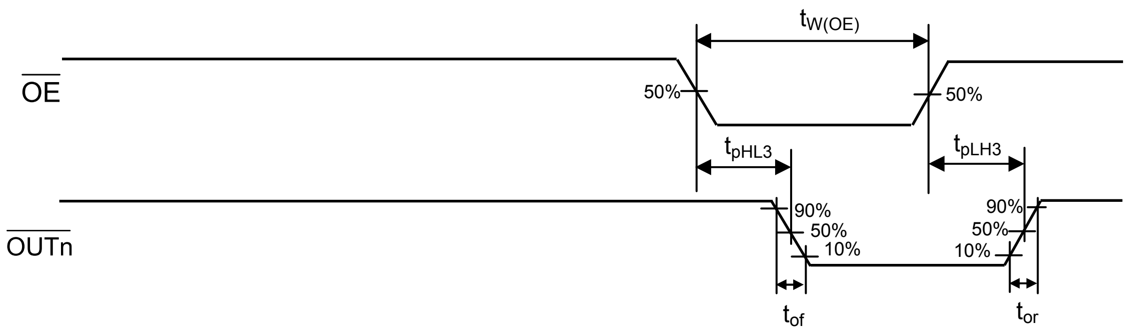
*MBI5035 has a built-in stagger circuit to perform delay mechanism. Among output ports exist a graduated 10ns delay time between $\overline{OUT2n}$ and $\overline{OUT2n+1}$, by which the output ports will be divided to two groups at a different time so that the instant current from the power line will be lowered.

Test Circuit for Switching Characteristics



Timing Waveform



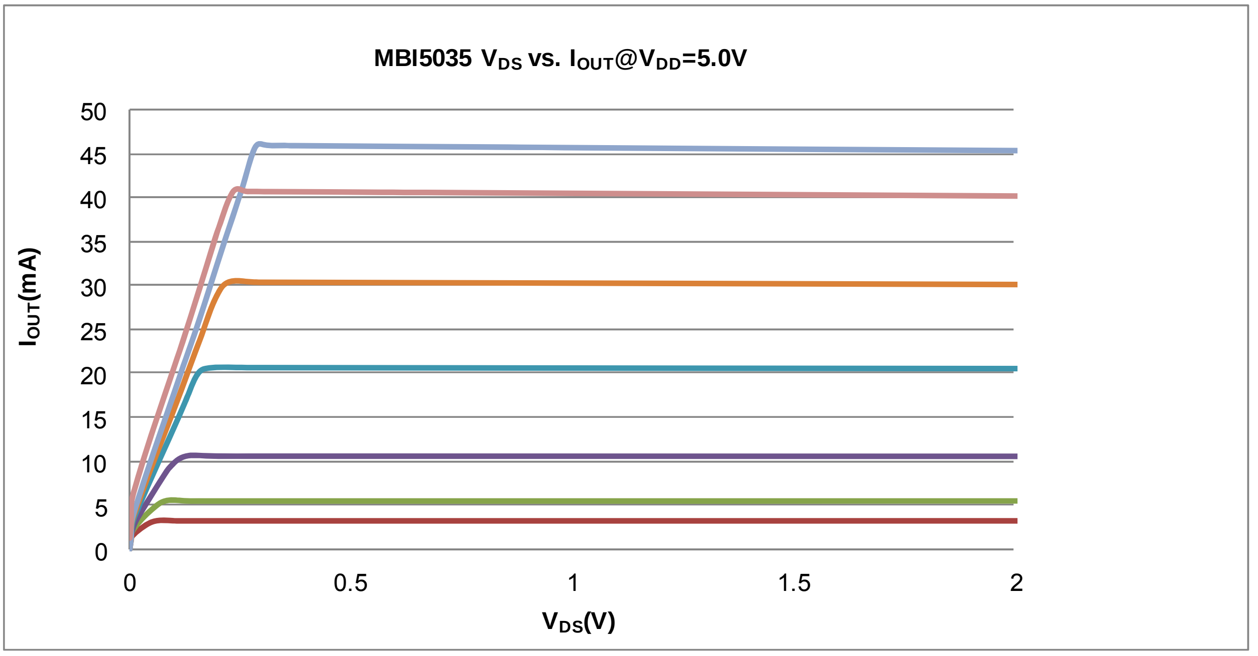


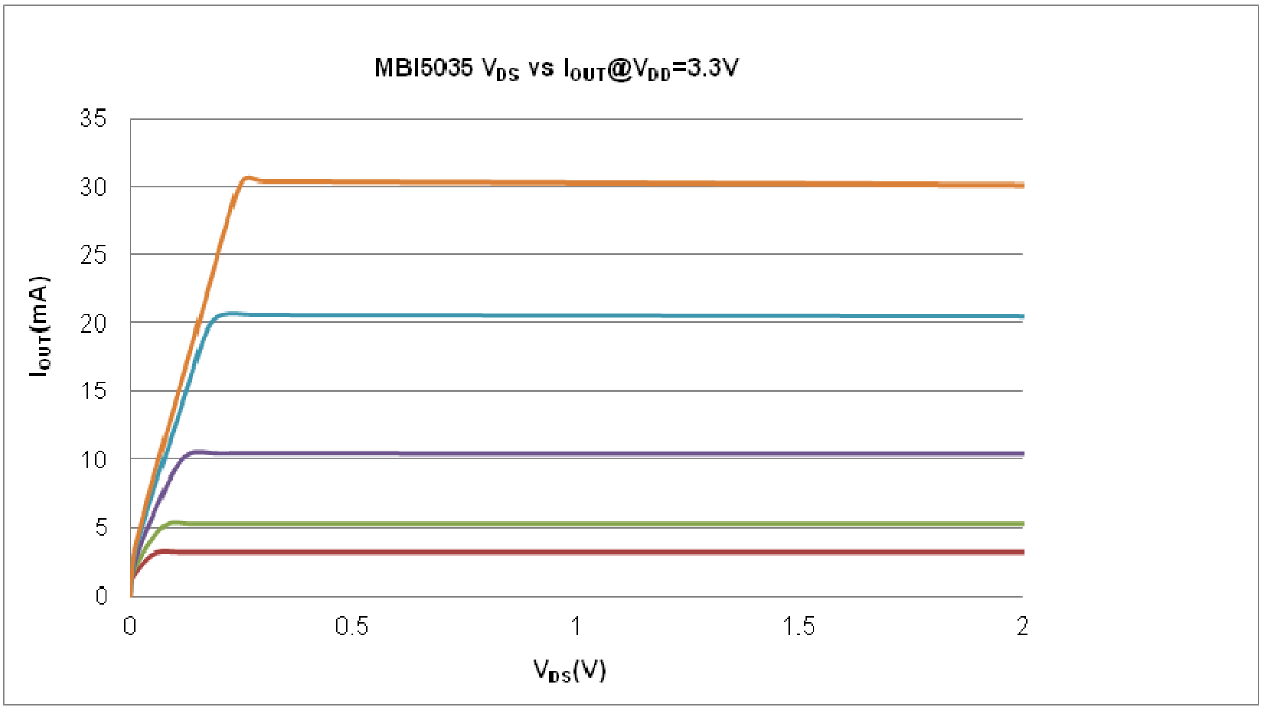
Application Information

Constant Current

To design LED displays, MBI5035 provides nearly no variations in current from channel to channel and from IC to IC. This can be achieved by:

1) The maximum current variation between channels is less than ±3%, and that between ICs is less than ±6%.
2) In addition, the current characteristic of output stage is flat and users can refer to the below figure. The output current can be kept constant regardless of the variations of LED forward voltages(V_F). This performs as a perfect static load regulation.



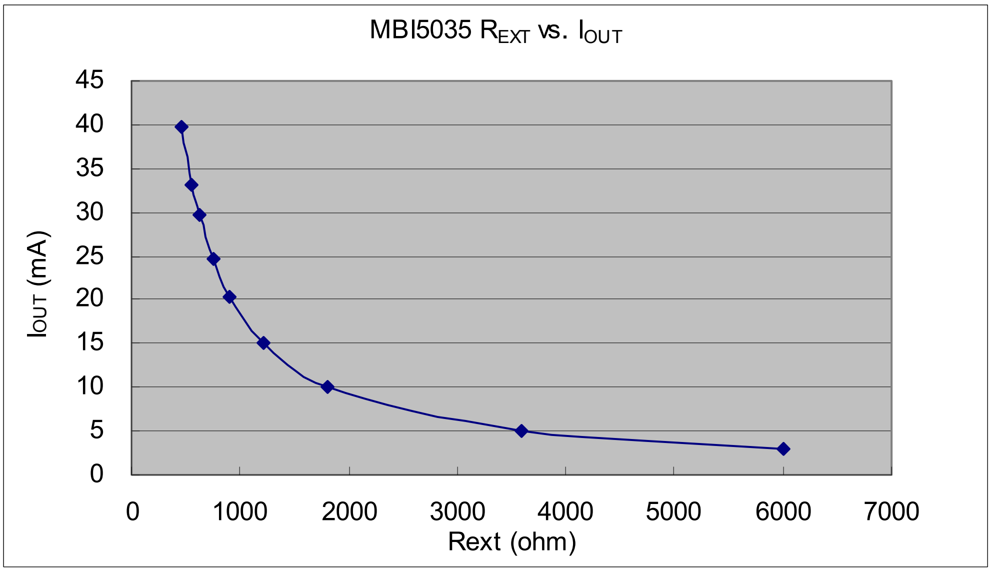


Adjusting Output Current

The output current of each channel (I_{OUT}) is set by an external resistor, R_{ext}. The relationship between I_{OUT} and R_{ext} is shown in the following figure.

Also, the output current can be calculated from the equation:

$V_{R\text{-}EXT}$=1.24V ; I_{OUT}=$V_{R\text{-}EXT}$ *(1/R_{ext})x15; R_{ext} =($V_{R\text{-}EXT}$/I_{OUT})x15



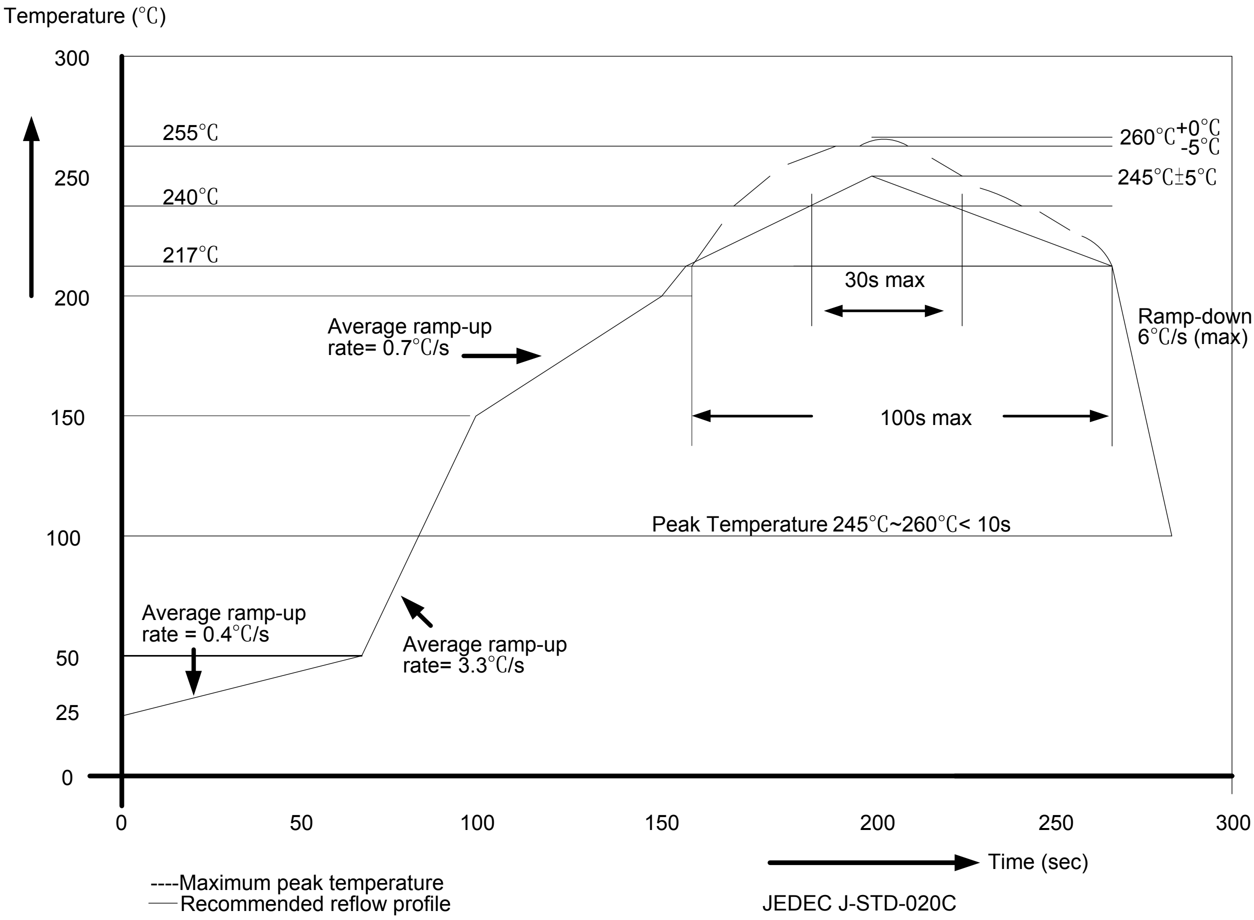
Where R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is the voltage of R-EXT terminal. The magnitude of current (as a function of R_{ext}) is around 20mA at 930Ω and 10mA at 1860Ω.

Staggered Delay of Output

MBI5035 has a built-in staggered circuit to perform delay mechanism. Among output ports exist a graduated 5ns delay time between $\overline{\text{OUT2n}}$ and $\overline{\text{OUT2n+1}}$, by which the output ports will be divided to two groups at a different time so that the instant current from the power line will be lowered.

Soldering Process of “Pb-free” Package Plating*

Macroblock has defined "Pb-Free" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with the higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it adopts tin/lead (SnPb) solder paste, and please refer to the JEDEC J-STD-020C for the temperature of solder bath. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 °C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below.



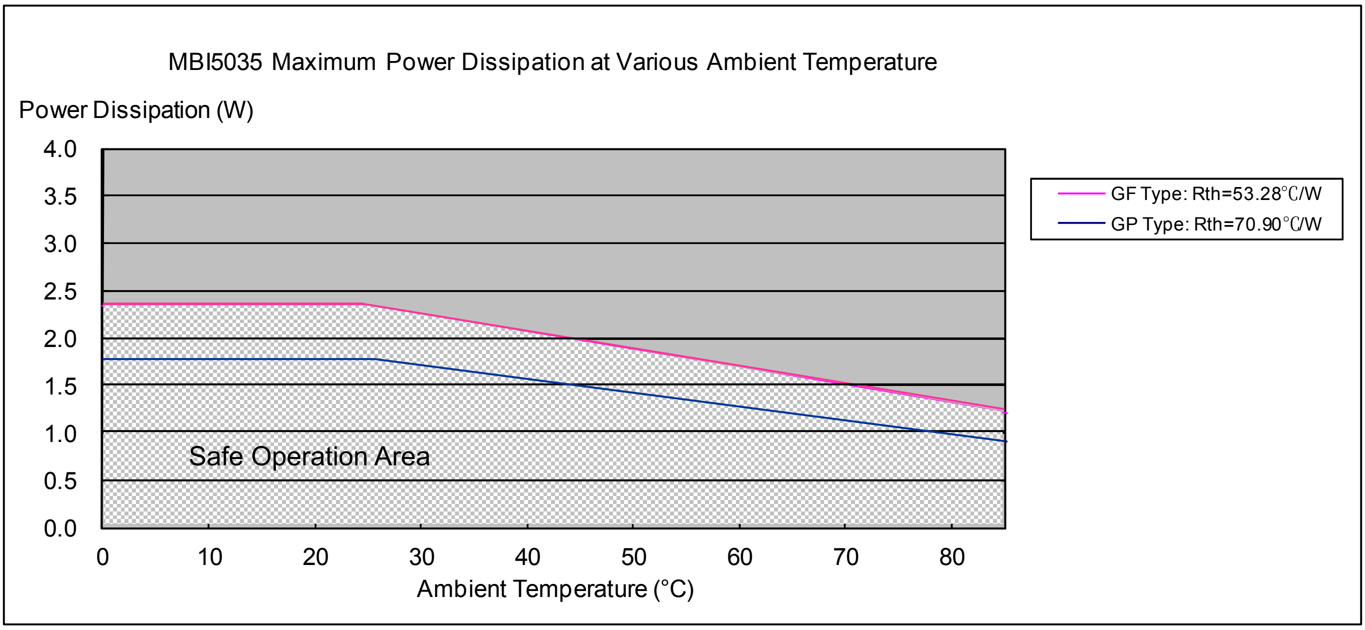
Package Thickness	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

*For details, please refer to Macroblock’s “Policy on Pb-free & Green Package”.

Package Power Dissipation (PD)

The maximum allowable package power dissipation is determined as $P_D(max)=(Tj–Ta)/R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x16)$. Therefore, to keep $P_D(act)\le P_D(max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT}=\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}/Duty/16$, where Tj=150°C.



Condition: I_{OUT}=50mA, 16 output channels	
Device Type	$R_{th(j-a)}$ (°C/W)
GF	53.28
GP	70.90

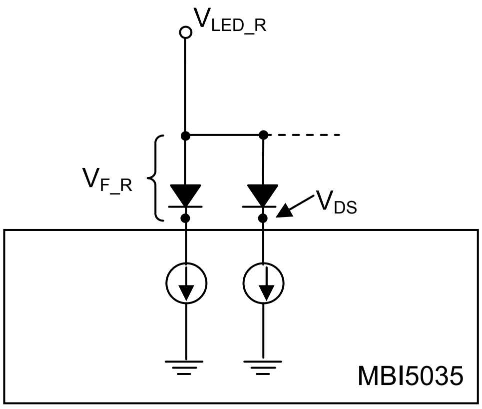
The maximum power dissipation, $P_D(max)=(Tj–Ta)/R_{th(j-a)}$, decreases as the ambient temperature increases.

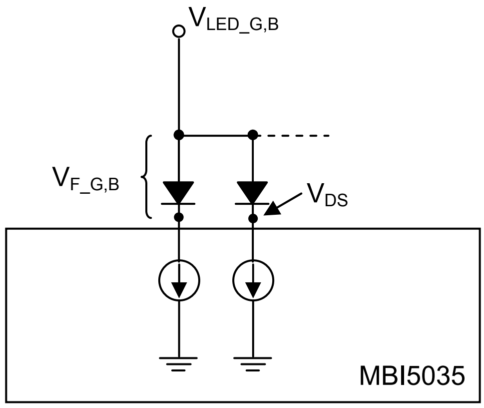
Load Supply Voltage (V_{LED})

MBI5035 are designed to operate with V_{DS} ranging from 0.2V to 0.6V (depending on I_{OUT}=3~45mA) to lower the heat dissipation and reduce the temperature on the package. In this case, it is recommended to use the lowest possible supply voltage $V_{LED.}$ Because the V_F of red LED differs from green and blue LED, we suggest to separate V_{LED_R} from $V_{LED\_G,,B.}$

V_{DS}=V_{LED}–V_F , with V_{DS} ranging from 0.2V to 0.6V

The applications are shown in the following figures.

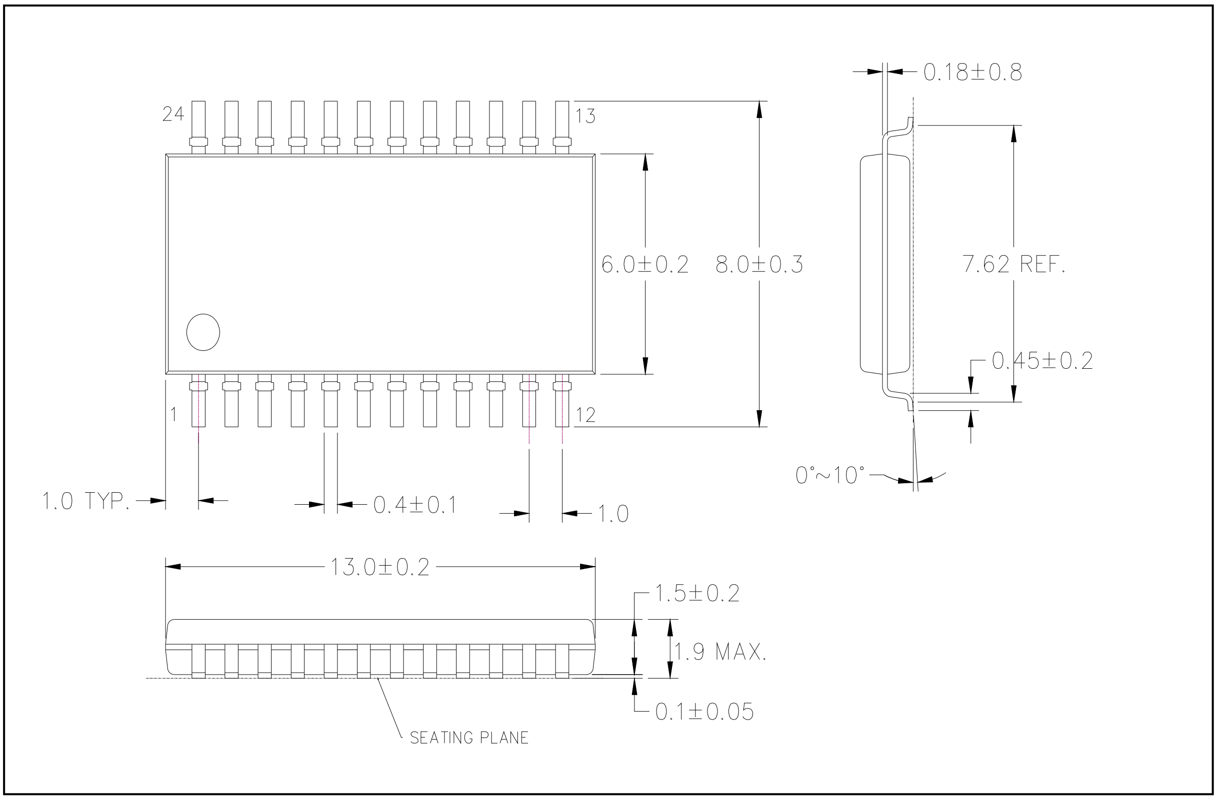




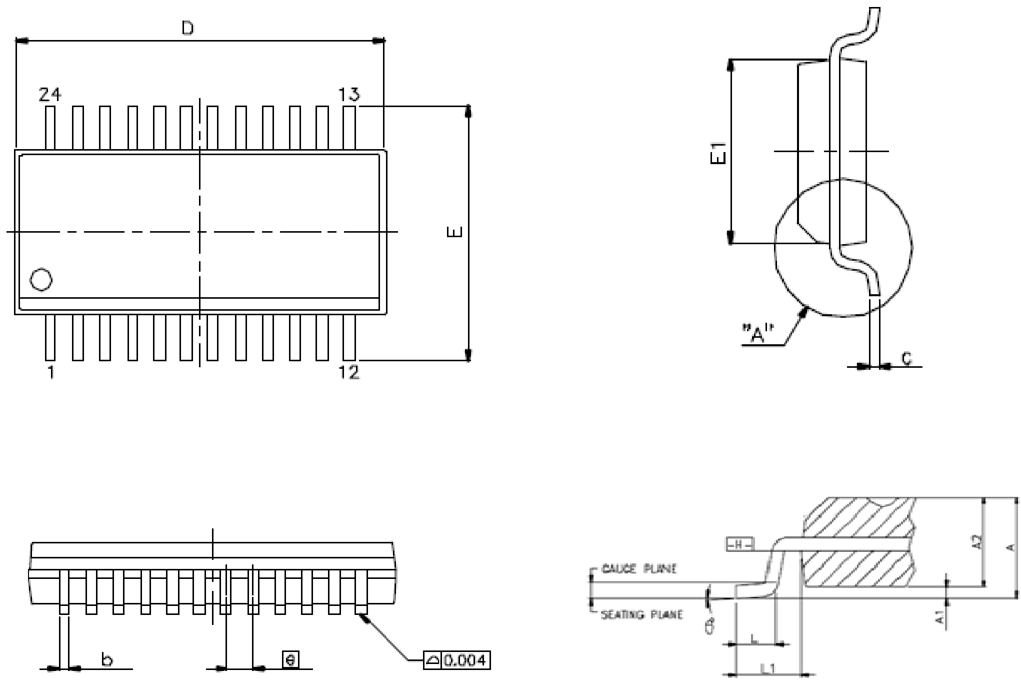
Switching Noise Reduction

LED driver ICs are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to “Application Note for 8-bit and 16-bit LED Drivers- Overshoot”.

Package Outline



MBI5035GF Outline Drawing

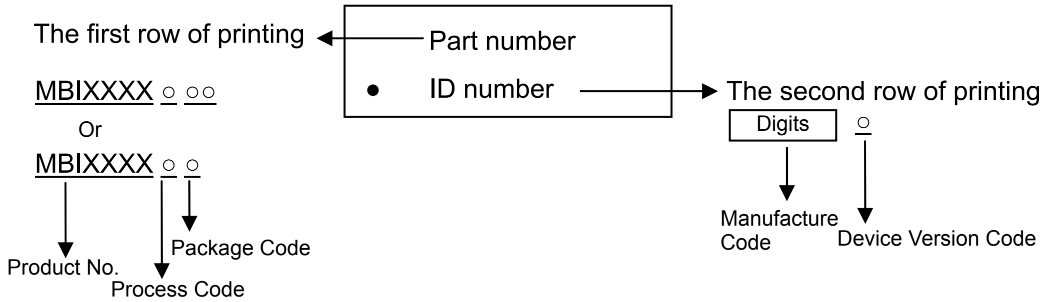


SYMBOLS	Dimensions shown in inches			Dimensions shown in millimeters		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.053	0.064	0.069	1.346	1.626	1.753
A1	0.004	0.006	0.010	0.102	0.152	0.254
A2	—	—	0.059	—	—	1.499
D	0.337	0.341	0.344	8.560	8.661	8.738
E	0.228	0.236	0.244	5.791	5.994	6.198
E1	0.150	0.154	0.157	3.810	3.912	3.988
b	0.008	—	0.012	0.203	—	0.305
c	0.007	—	0.010	0.178	—	0.254
L	0.016	0.025	0.050	0.406	0.635	1.270
e	0.025 BASIC			0.635 BASIC		
L1	0.041 BASIC			1.0414 BASIC		
Θ°	0	—	8	0	—	8

MBI5035 GP Outline Drawing

Note: The unit for the outline drawing is mm.

Product Top-mark Information



Product Revision History

Datasheet version	Device version code
V1.00	A
V1.01	A
V2.00	B

Product Ordering Information

Part Number	"Pb-free & Green" Package Type	Weight (g)
MBI5035GF-B	SOP24L-300-1.00	0.28
MBI5035GP-B	SSOP24L-150-0.64	0.11

*Please place your order with the ***"product ordering number"*** information on your purchase order (PO).

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