EVB71122

300 to 930MHz Receiver

Evaluation Board Description

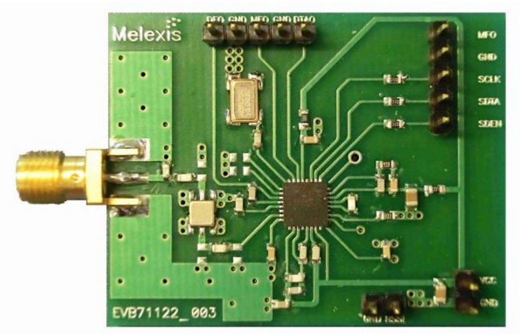
Features

- Programmable PLL synthesizer
- 8-channel preconfigured or fully programmable SPI mode
- Double super-heterodyne receiver architecture with 2nd mixer as image rejection mixer
- Reception of FSK, FM and ASK modulated signals
- Low shut-down and operating currents
- AGC – automatic gain control
- On-chip IF filter
- Fully integrated FSK/FM demodulator
- RSSI for level indication and ASK detection
- 2nd order low-pass data filter
- Positive and negative peak detectors
- Data slicer (with averaging or peak-detector adaptive threshold)
- 32-pin Quad Flat No-Lead Package (QFN)
- EVB programming software is available on Melexis web site

Application Examples

- General digital and analog RF receivers at 300 to 930MHz
- Tire pressure monitoring systems (TPMS)
- Remote keyless entry (RKE)
- Low power telemetry systems
- Alarm and security systems
- Active RFID tags
- Remote controls
- Garage door openers
- Home and building automation

Evaluation board example



Ordering information

EVB71122-315-C
EVB71122-433-C
EVB71122-868-C
EVB71122-915-C

**SPI mode is default population*
***EVB71122-XXX-C with XXX = Reception frequency (315 or 433.92 or 868.3 or 915MHz).*
****The evaluation board is supplied with an SMA connector.*

General Description

The MLX71122 is a multi-channel RF receiver IC based on a double-conversion super-heterodyne architec-ture. It is designed to receive FSK and ASK modulated RF signals either in 8 predefined frequency channels or frequency programmable via a 3-wire serial programming interface (SPI).

The IC is designed for a variety of applications, for example in the European bands at 433MHz and 868MHz or for the use in North America or Asia, e.g. at 315MHz, 447MHz or 915MHz.

Contents

1. Theory of Operation

1.1. General

The MLX71122 receiver architecture is based on a double-conversion super-heterodyne approach. The two LO signals are derived from an on-chip integer-N PLL frequency synthesizer. The PLL reference frequency is derived from a crystal (XTAL). The PLL synthesizer consists of an integrated voltage-controlled oscillator with external inductor, a programmable feedback divider chain, a programmable reference divider, a phase-frequency detector with a charge pump and an external loop filter.

In the receiver's down-conversion chain, two mixers MIX1 and MIX2 are driven by the internal local oscillator signals LO1 and LO2, respectively. The second mixer MIX2 is an image-reject mixer. As the first intermediate frequency (IF1) is very high (typically above 100 MHz), a reasonably high degree of image rejection is provided even without using an RF front-end filter. At applications asking for very high image rejections, cost-efficient RF front-end filtering can be realized by using a SAW filter in front of the LNA.

The receiver signal chain is set up by a low noise amplifier (LNA), two down-conversion mixers (MIX1 and MIX2), an on-chip IF filter (IFF) as well as an IF amplifier (IFA). By choosing the required modulation via an FSK/ASK switch (at pin MODSEL), either the on-chip FSK demodulator (FSK DEMOD) or the RSSI-based ASK detector is selected. A second order data filter (OA1) and a data slicer (OA2) follow the demodulator. The data slicer threshold can be generated from the mean-value of the data stream or by means of the positive and negative peak detectors (PKDET+/-).

In general the MLX71122 can be set to shut-down mode, where all receiver functions are completely turned off, and to several other operating modes. There are two global operating modes that are selectable via the logic level at pin SPISEL:

- 8-channel preconfigured mode (**ABC mode**)
- fully programmable mode (**SPI mode**).

In ABC mode the number of frequency channels is limited to eight but no microcontroller programming is required. In this case the three lines of the serial programming interface (SPI) are used to select one of the eight predefined frequency channels via simple 3-bit parallel programming. Pins ENRX and MODSEL are used to enable/disable the receiver and to select FSK or ASK demodulation, respectively.

SPI mode is recommended for full programming flexibility. In this case the three lines of the SPI are configured as a standard 3-wire bus (SDEN, SDTA and SCLK). This allows changing many parameters of the receiver, for example more operating modes, channels, frequency resolutions, gains, demodulation types, data slicer settings and more. The pin MODSEL has no effect in this mode.

1.2. EVB Data Overview

- Input frequency ranges: 300 to 930MHz
- Power supply range: 3.0 to 5.5V
- Temperature range: -40 to +105°C
- Shutdown current: 50nA
- Operating current: 12mA (typ.)
- Internal IF2: 2MHz with 230kHz 3dB bandwidth
- Maximum data rate: 100kbps NRZ code, 50kbps bi-phase code
- Minimum frequency resolution: 10kHz
- Total image rejection: > 65dB (with external RF front-end filter)
- FSK/FM deviation range: ±2 to ±50kHz
- Spurious emission: < -70dBm
- Linear RSSI range: > 50dB
- FSK input frequency acceptance range: 180kHz (3dB)
- Crystal reference frequency: 10MHz

❒ Input Sensitivity: at 4 kbps NRZ, BER = $3 \cdot 10^{-3}$

Frequency	315 MHZ	433.92 MHz	868.3 MHz	915 MHz
FSK: ±20 kHz deviation	-106dBm	-104dBm	-101dBm	-101dBm
ASK	-108dBm	-108dBm	-106dBm	-106dBm

1.3. Block Diagram

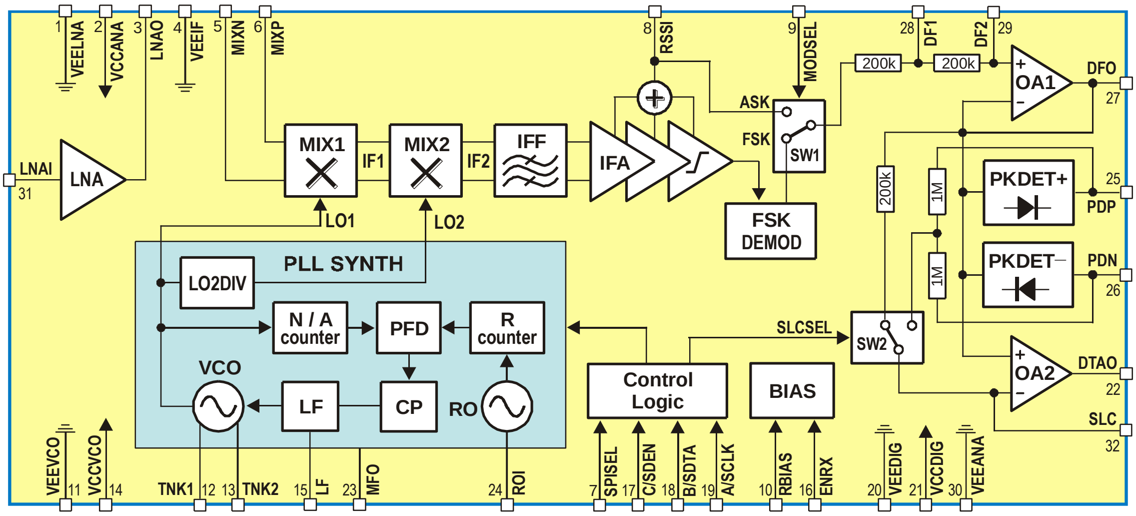


Fig. 1: MLX71122 block diagram

The MLX71122 receiver IC consists of the following building blocks:

- PLL synthesizer (PLL SYNTH) to generate the first and second local oscillator signals LO1 and LO2, parts of the PLL SYNTH are the voltage-controlled oscillator (VCO), the feedback dividers N/A and R, the phase-frequency detector (PFD), the charge pump (CP) and the crystal-based reference oscillator (RO)
- Low-noise amplifier (LNA) for high-sensitivity RF signal reception
- First mixer (MIX1) for down-conversion of the RF signal to the first IF (intermediate frequency)
- Second mixer (MIX2) with image rejection for down-conversion from the first to the second IF
- IF Filter (IFF) with a 2MHz center frequency and a 230kHz 3dB bandwidth
- IF amplifier (IFA) to provide a large amount of voltage gain and an RSSI signal output
- FSK demodulator (FSK DEMOD)
- Operational amplifiers OA1 and OA2 for low-pass filtering and data slicing, respectively
- Positive (PKDET+) and negative (PKDET-) peak detectors
- Switches SW1 to select between FSK and ASK as well as SW2 to chose between averaging or peak detector data slicer
- Control logic with 3-wire bus serial programming interface (SPI)
- Biasing circuit with modes control

For more detailed information, please refer to the latest MLX71122 data sheet revision.

1.4. Enable/Disable in ABC Mode

ENRX	Description
0	Shutdown mode
1	Receive mode

Pin ENRX is pulled down internally. Device is in shutdown by default, after power supply on.
If ENRX = 0 and SPISEL = 1 then operating modes according to OPMODE bit (refer to control word R0).
If ENRX = 1 then OPMODE bit has no effect (hardwired receive mode).

1.5. Demodulation Selection in ABC Mode

MODSEL	Description
0	FSK demodulation
1	ASK demodulation

Pin MODSEL has no effect in SPI mode (SPISEL = 1). We recommend connecting it to ground to avoid a floating CMOS gate.

1.6. Programming Modes

SPISEL	Description
0	ABC mode (8 channels preconfigured)
1	SPI mode (programming via 3-wire bus)

1.7. Preconfigured Frequencies in ABC Mode

A	B	C	Receive Frequency
0	0	0	FSK1: 369.5 MHz
0	1	0	FSK5: 388.3 MHz
1	0	0	FSK2: 371.1 MHz
1	1	0	FSK4: 376.9 MHz
0	0	1	FSK3: 375.3 MHz
0	1	1	FSK7: 394.3 MHz
1	0	1	FSK6: 391.5 MHz
1	1	1	FSK8: 395.9 MHz

As all pins, pins A, B, and C are equipped with ESD protection diodes that are tied to VCC and to VEE. Therefore these pins should not be directly connected to positive supply (a logic “1”) before the supply voltage is applied to the IC. Otherwise the IC will be supplied through these control lines and it may enter into an unpredictable mode. In case the user wants to apply a positive supply voltage to these pins before the supply voltage is applied to the IC, a protection resistor should be inserted in each control line.

2. Functional Description

2.1. Frequency Planning

Because of the double conversion architecture that employs two mixers and two IF signals, there are four different combinations for injecting the LO1 and LO2 signals:

- LO1 high side and LO2 high side: receiving at f_{RF}(high-high)
- LO1 high side and LO2 low side: receiving at f_{RF}(high-low)
- LO1 low side and LO2 high side: receiving at f_{RF}(low-high)
- LO1 low side and LO2 low side: receiving at f_{RF}(low-low)

As a result, four different radio frequencies (RFs) could yield one and the same second IF (IF2). Fig. 2 shows this for the case of receiving at f_{RF}(high-high). In the example of Fig. 2, the image signals at f_{RF}(low-high) and f_{RF}(low-low) are suppressed by the bandpass characteristic provided by the RF front-end. The bandpass shape can be achieved either with a SAW filter (featuring just a couple of MHz bandwidth), or by the tank circuits at the LNA input and output (this typically yields 30 to 60MHz bandwidth). In any case, the high value of the first IF (IF1) helps to suppress the image signals at f_{RF}(low-high) and f_{RF}(low-low).

The two remaining signals at IF1 resulting from f_{RF}(high-high) and f_{RF}(high-low) are entering the second mixer MIX2. This mixer features image rejection with so-called single-sideband (SSB) selection. This means either the upper or lower sideband of IF1 can be selected. In the example of Fig. 2, LO2 high-side injection has been chosen to select the IF2 signal resulting from f_{RF}(high-high).

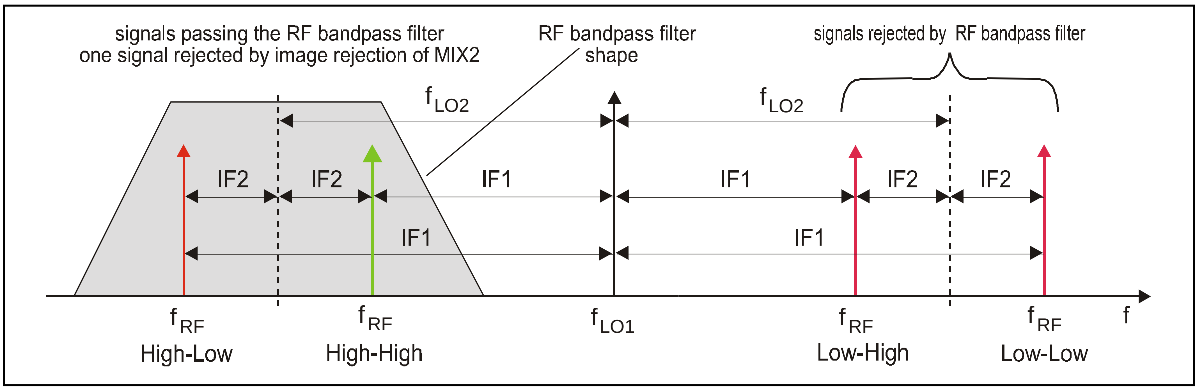


Fig. 2: The four receiving frequencies in a double conversion superhet receiver

It can be seen from the block diagram of Fig. 1 that there is a fixed relationship between the LO1 signal frequency f_{LO1} and the LO2 signal frequency f_{LO2}.

$$\mathrm{LO2DIV} = N_{LO2} = \frac{f_{LO1}}{f_{LO2}} \tag{1}$$

The LO1 signal frequency f_{LO1} is directly synthesized from the crystal reference oscillator frequency f_{RO} by means of an integer-N PLL synthesizer. The PLL consists of a dual-modulus prescaler (P/P+1), a program counter N and a swallow counter A.

$$f_{LO1} = \frac{f_{RO}}{R}(N \cdot P + A) = f_{PFD}(N \cdot P + A) = f_{PFD} \cdot N_{tot} \tag{2}$$

Due to the double superhet receiver architecture, the channel frequency step size f_{CH} is not equal to the phase-frequency detector (PFD) frequency f_{PFD}. For high-side injection, the channel step size f_{CH} is given by:

$$f_{CH} = \frac{f_{RO}}{R}\frac{N_{LO2}-1}{N_{LO2}} = f_{PFD}\frac{N_{LO2}-1}{N_{LO2}} \tag{3}$$

While the following equation is valid for low-side injection:

$$f_{CH} = \frac{f_{RO}}{R}\frac{N_{LO2}+1}{N_{LO2}} = f_{PFD}\frac{N_{LO2}+1}{N_{LO2}} \tag{4}$$

2.2. Calculation of Counter Settings

Frequency planning and the selection of the MLX71122's PLL counter settings are straightforward and can be laid out on the following procedure.

Usually the receive frequency f_{RF} and the channel step size f_{CH} are given by system requirements. The N and A counter settings can be derived from N_{tot} or f_{LO1} and f_{PFD} by using the following equations.

$$N = \mathrm{floor}(\frac{N_{tot}}{P}) = \mathrm{floor}(\frac{N_{tot}}{32})\ ;\ A = N_{tot} - N \cdot P = N_{tot} - N \cdot 32 \tag{5}$$

2.2.1. Calculation of LO1 and IF1 frequency for Low Frequency Bands

High-high injection must be used for the low frequency bands. First of all choose a PFD frequency f_{PFD} according to below table. The R counter values are valid for a 10MHz crystal reference frequency f_{RO}. The PFD frequency is given by $f_{PFD} = f_{RO}$ /R.

Injection Type	f_{CH} [kHz]	f_{PFD} [kHz]	R
h-h	10	13.3	750
h-h	12.5	16.7	600
h-h	20	26.7	375
h-h	25	33.3	300
h-h	50	66.7	150
h-h	100	133.3	75
h-h	250	333.3	30

The second step is to calculate the missing parameters f_{LO1}, f_{IF1}, N_{tot}, N and A. While the second IF (f_{IF2}), the N_{LO2} divider ratio and the prescaler divider ratio P are bound to f_{IF2} = 2MHz, N_{LO2} = 4 (or 8) and P =32.

$$f_{LO1} = \frac{N_{LO2}}{N_{LO2}-1}(f_{RF} - f_{IF2}) \qquad f_{LO1} = \frac{4}{3}(f_{RF} - 2\mathrm{MHz}) \tag{6}$$

$$f_{IF1} = \frac{f_{RF} - N_{LO2} f_{IF2}}{N_{LO2}-1} \qquad f_{IF1} = \frac{f_{RF} - 8\mathrm{MHz}}{3} \tag{7}$$

Finally N and A can be calculated with formula (5).

2.2.2. Calculation of LO1 and IF1 frequency for High Frequency Bands

Typical ISM band operating frequencies like 868.3 and 915MHz can be covered without changing the crystal nor the VCO inductor.
Low-low injection should be used for the high frequency bands. First of all choose a PFD frequency f_{PFD} according to below table. The R counter values are valid for a 10MHz crystal reference. The PFD frequency is given by $f_{PFD} = f_{RO} /R$.

Injection Type	f_{CH} [kHz]	f_{PFD} [kHz]	R
l-l	20	16	625
l-l	25	20	500
l-l	50	40	250
l-l	100	80	125
l-l	250	200	50
l-l	500	400	25

The second step is to calculate the missing parameters f_{LO1}, f_{IF1}, N_{tot}, N and A. While the second IF (f_{IF2}), the N_{LO2} divider ratio and the prescaler divider ratio P are bound to f_{IF2} = 2MHz, N_{Lo2} = 4 (or 8) and P =32.

$$f_{LO1} = \frac{N_{LO2}}{N_{LO2}+1}(f_{RF} - f_{IF2}) \qquad f_{LO1} = \frac{4}{5}(f_{RF} - 2MHz) \tag{8}$$

$$f_{IF1} = \frac{f_{RF} + N_{LO2} f_{IF2}}{N_{LO2}+1} \qquad f_{IF1} = \frac{f_{RF} + 8MHz}{5} \tag{9}$$

Finally N and A can be calculated with formula (5).

2.2.3. Counter Setting Examples for SPI Mode

To provide some examples, the following table shows some counter settings for the reception of the well-known ISM and SRD frequency bands. The channel spacing is assumed to be f_{CH} = 100kHz. In below table all frequency units are in MHz.

Inj	f_{RF}	f_{IF1}	f_{LO1}	N_{tot}	N	P	A	f_{PFD}	R	f_{REF}	f_{LO2}	f_{IF2}
h-h	300	97.3	397.3	2980	93	32	4	0.133	75	10	99.3	2
h-h	315	102.3	417.3	3130	97	32	26	0.133	75	10	104.3	2
h-h	434	142	576	4320	135	32	0	0.133	75	10	144	2
h-h	470	154	624	4680	146	32	8	0.133	75	10	156	2
l-l	850	171.6	678.4	8480	256	32	0	0.08	125	10	169.6	2
l-l	868	175.2	692.8	8660	270	32	20	0.08	125	10	173.2	2
l-l	915	184.6	730.4	9130	285	32	10	0.08	125	10	182.6	2
l-l	930	187.6	742.4	9280	290	32	0	0.08	125	10	185.6	2

2.2.4. Counter Settings in ABC Mode – 8+1 Preconfigured Channels

In ABC mode (SPISEL=0), the counter settings are hard-wired. In below table all frequency units are in MHz.

CH	Inj	f_{RF}	f_{IF1}	f_{LO1}	N_{tot}	N	P	A	f_{PFD}	R	f_{REF}	f_{LO2}	f_{IF2}
1	h-l	369.5	125.8	495.3	3715	116	32	3	0.133	75	10	123.8	2
2	h-l	371.1	126.4	497.5	3731	116	32	19	0.133	75	10	124.4	2
3	h-l	375.3	127.8	503.1	3773	117	32	29	0.133	75	10	125.8	2
4	h-l	376.9	128.3	505.2	3789	118	32	13	0.133	75	10	126.3	2
5	h-l	384.0	130.7	514.7	3860	120	32	20	0.133	75	10	128.7	2
6	h-l	388.3	132.1	520.4	3903	121	32	31	0.133	75	10	130.1	2
7	h-l	391.5	133.2	524.7	3935	122	32	31	0.133	75	10	131.2	2
8	h-l	394.3	134.1	528.4	3963	123	32	27	0.133	75	10	132.1	2
9	h-l	395.9	134.6	530.5	3979	124	32	11	0.133	75	10	132.6	2

List of Mathematical Acronyms	
A	divider ratio of the swallow counter (part of feedback divider)
f_{FB}	frequency at the feedback divider output
$\mathrm{floor}(x)$	The floor function gives the largest integer less than or equal to x. For example, floor(5.4) gives 5, floor(-6.3) gives -7.
f_{PFD}	PFD frequency in locked state
$\frac{f_{RO}}{R} = f_R$	reference frequency of the PLL
f_{RO}	frequency of the crystal reference oscillator
f_{VCO}	frequency of the VCO (equals the LO1 signal of the first mixer)
$N_{tot} = N \cdot P + A$	total divider ratio of the PLL feedback path
N	divider ratio of the program counter (part of feedback divider)
N_{LO2}	LO2DIV divider ratio, to derive the LO2 signal from LO1 (N_1 = 4 or 8)
P	divider ratio of the prescaler (part of feedback divider)
R	divider ratio of the reference divider R

2.2.5. PLL Counter Ranges

In order to cover the frequency range of about 300 to 930MHz the following counter values are implemented in the receiver:

PLL Counter Ranges			
A	**N**	**R**	**P**
0 to 31 (5bit)	3 to 2047 (11bit)	3 to 2047 (11bit)	32

Therefore the minimum and maximum divider ratios of the PLL feedback divider are given by:

$$N_{totmin} = 32 \cdot 32 = 1024 \qquad N_{totmax} = 2047 \cdot 32 + 31 = 65535$$

2.3. SPI Description

2.3.1. General

Serial programming interface (SPI) mode can be activated by choosing SPISEL = 1 (e.g. at positive supply voltage V_{CC}). In this mode, the input pins 17, 18 and 19 are used as a 3-wire unidirectional serial bus interface (SDEN, SDTA, SCLK). The internal latches contain all user programmable variables including counter settings, mode bits etc.

In addition the MFO pin can be programmed as an output (see section 3.1.4) in order to read data from the internal latches and it can be used as an output for different test modes as well.

At each rising edge of the SCLK signal, the logic value at the SDTA terminal is written into a shift register. The programming information is taken over into internal latches with the rising edge of SDEN. Additional leading bits are ignored, only the last bits are serially clocked into the shift register. A normal write operation shifts 16 bits into the SPI, a normal read operation shifts 4 bits into the SPI and reads additional 12 bits from the MFO pin. If less than 12 data bits are shifted into SDTA during the write operation then the control register may contain invalid information.

In general a control word has the following format. Bit 0 is the Read/Write bit that determines whether it is a read (R/W = 1) or a write (R/W = 0) sequence. The R/W bit is preceding the latch address and the corresponding data bits.

Control Word Format															
MSB											LSB	MSB		LSB	Bit 0
Data												**Latch Address**			**Mode**
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A2	A2	A0	R/W

There are two control word formats for read and for write operation. Data bits are only needed in write mode. Read operations require only a latch address and a R/W bit.

Due to the static CMOS design, the serial interface consumes virtually no current. The SPI is a fully separate building block and can therefore be programmed in every operational mode.

2.3.2. Read / Write Sequences

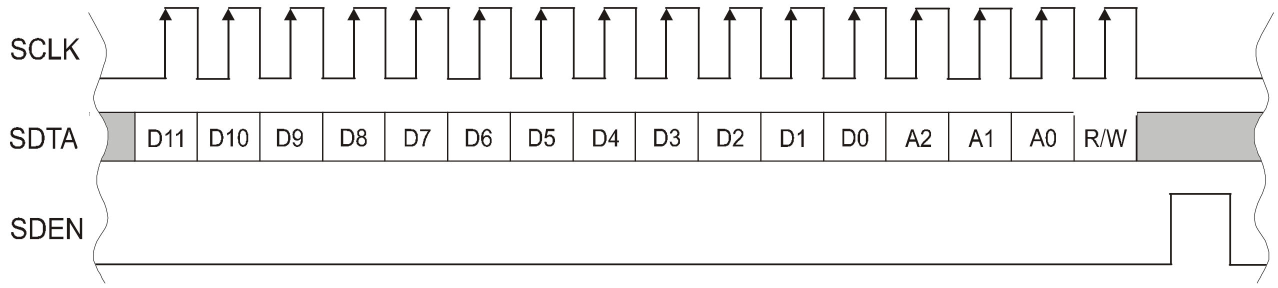


Fig. 6 Typical write sequence diagram

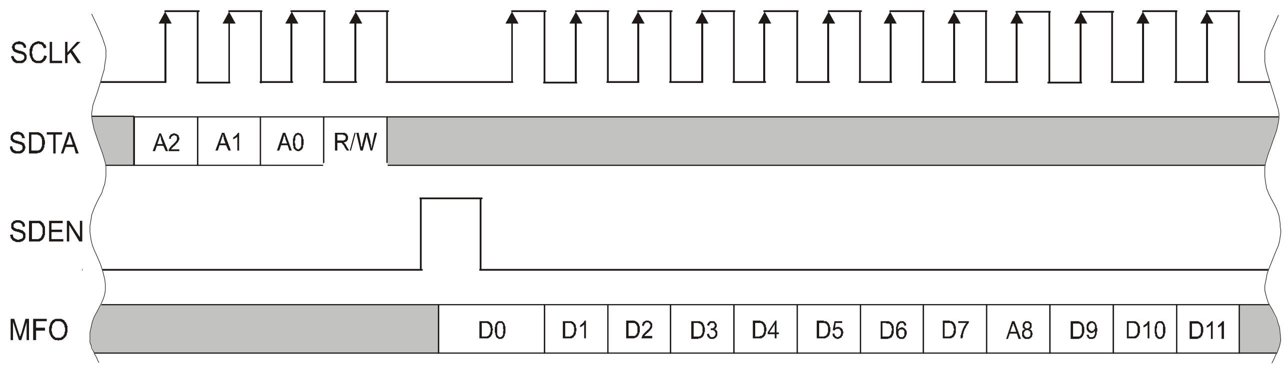


Fig. 7 Typical read sequence diagram

2.3.3. Serial Programming Interface Timing

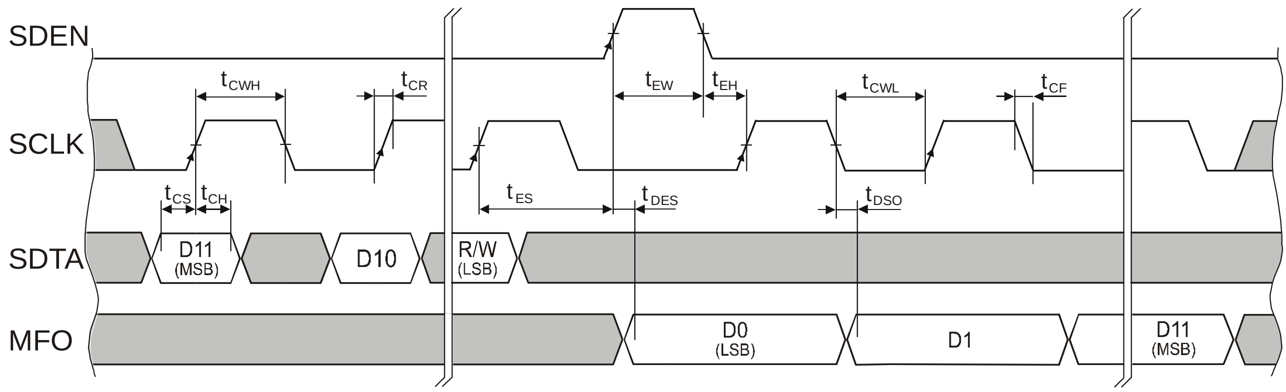


Fig. 8 SPI timing diagram

3. Register Description

The following tables are to describe the functionality of the registers.

Sec. 3.1 provides a register overview with all the control words R0 to R7. The subsequent sections. 3.1.1 to 3.1.8 show the content of the control words in more detail.

Programming the registers requires SPI mode (SPISEL = 1). Default settings are for ABC mode.

3.1. Register Overview

CONTROL WORD	DATA												LATCH ADDRESS		
	MSB											LSB			
Bit No.	11	10	9	8	7	6	5	4	3	2	1	0	MSB		LSB
default	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**
R0	**DTAPOL**	**SLCSEL**	**SSBSEL**	**DEMGAIN**	**IFFGAIN [1 : 0]**		**MIX2GAIN**	**MIX1GAIN**	**LNAGAIN [1 : 0]**		**OPMODE [1 : 0]**		**read/ write**		
Bit No.	11	10	9	8	7	6	5	4	3	2	1	0	MSB		LSB
default	**1**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**1**
R1	**SHOWLD**	**PRESCUR**	**VCOBUF**	**VCOCUR**	**VCORANGE**	**RSSIGAIN**	**LDTIME [1 : 0]**		**LDERR**	**PFDPOL**	**CPCUR [1 : 0]**		**read/ write**		
Bit No.	11	10	9	8	7	6	5	4	3	2	1	0	MSB		LSB
default	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	**0**
R2	**N [6 : 0]**							**A [4 : 0]**					**read/ write**		
Bit No.	11	10	9	8	7	6	5	4	3	2	1	0	MSB		LSB
default	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**
R3	**MFO [3 : 0]**				**AGCDEL [1 : 0]**		**AGCEN**	**LO2DIV**	**N [10 : 7]**				**read/ write**		

CONTROL WORD	DATA												LATCH ADDRESS		
	MSB											LSB			
Bit No.	11	10	9	8	7	6	5	4	3	2	1	0	MSB		LSB
default	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**1**	**1**	**0**	**0**
R4	**AGCMODE**	**R [10 : 0]**											read/ write		
Bit No.	11	10	9	8	7	6	5	4	3	2	1	0	MSB		LSB
default	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**1**
R5	**MODSEL**	**RIFF [10 : 0]**											read/ write		
Bit No.	11	10	9	8	7	6	5	4	3	2	1	0	MSB		LSB
default	**1**	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**1**	**0**
R6	**ROCUR [1 :0]**		**IFFTUNE**	**IFFHLT**	**IFFPRES [7 : 0]**								read/ write		
Bit No.	11	10	9	8	7	6	5	4	3	2	1	0	MSB		LSB
default													**1**	**1**	**1**
R7	**RSSIH**	**LDRSSIL***	**IFFSTATE [1 :0]**		**IFFVAL [7 : 0]**								read-only		

Note: * **depends on bit 11 in R4, 0 = RSSIL, 1 = LD**

3.1.1. Control Word R0

Name	Bits	Description			
OPMODE	[1:0]	operation mode			
		00	**shutdown**		#default
		01	**receive mode**		
		10	**reference oscillator & BIAS only**		
		11	**synthesizer only**		
LNAGAIN	[3:2]	LNA gain			
		00	**lowest gain**	**(default – 20dB)**	
		01	**low gain**	**(default – 6dB)**	
		10	**high gain**	**(default – 2dB)**	
		11	**highest gain**	**(default – 0dB)**	#default
			gain values are relative to gain at default		
MIX1GAIN	[4]	1^{st} Mixer gain			
		0	**high gain**	**(14dB)**	#default
		1	**low gain**	**(0dB)**	
MIX2GAIN	[5]	2^{nd} Mixer gain			
		0	**high gain**	**(9dB)**	#default
		1	**low gain**	**(-2dB)**	
IFFGAIN	[7:6]	intermediate frequency filter gain			
		00	**lowest gain**	**(-14dB)**	
		01	**low gain**	**(-6dB)**	
		10	**high gain**	**(0dB)**	#default
		11	**highest gain**	**(+6dB)**	
DEMGAIN	[8]	demodulator gain			
		0	**low gain**	**(~ 12mV/kHz)**	#default
		1	**high gain**	**(~ 14.5mV/kHz)**	
SSBSEL	[9]	single side band selection			
		0	**upper side band**	**LO2 low-side inj. (IF1 = LO2 + IF2)**	#default
		1	**lower side band**	**LO2 high-side inj. (IF1 = LO2 – IF2)**	
			Internal IF2 = 2MHz		
SLCSEL	[10]	slicer mode select			
		0	**averaging Data Slicer mode**		#default
		1	**peak detector Data Slicer mode**		
DTAPOL	[11]	data output polarity OA2			
		0	**inverted**		#default
			‘1’ for space at ASK or f_{min} at FSK, ‘0’ for mark at ASK or f_{max} at FSK		
		1	**normal**		
			‘0’ for space at ASK or f_{min} at FSK, ‘1’ for mark at ASK or f_{max} at FSK		

3.1.2. Control Word R1

Name	Bits	Description			
CPCUR	[1:0]	charge pump current setting			
		00 **01** **10** **11**	**100µA** **400µA** **400µA static down** **400µA static up**		#default
PFDPOL	[2]	PFD output polarity			
		0 **1**	**negative** **positive**		#default
LDERR	[3]	lock detector time error			
		0 **1**	**15ns** **30ns**		#default
LDTIME	[5:4]	lock detection time			
		00 **01** **10** **11**	**2/f_R** **4/f_R** **8/f_R** **16/f_R**		#default
			minimum time span before lock in f_R is the reference oscillator frequency f_{RO} divided by R, see section 3.1.5 (R4)		
RSSIGAIN	[6]	sensitivity of RSSI voltage			
		0 **1**	**low gain** **high gain**	**(~39mV/dB)** **(~51mV/dB)**	#default
VCORANGE	[7]	VCO range			
		0 **1**	**3V supply** **5V supply**		#default
			VCO range setting for different VCCs.		
VCOCUR	[8]	VCO core current			
		0 **1**	**450µA** **520µA**		#default
VCOBUF	[9]	VCO buffer current			
		0 **1**	**900µA** **1040µA**		#default
PRESCUR	[10]	prescaler 32/33 reference current			
		0 **1**	**20µA** **30µA**		#default
			30µA may be used for f_{RF} = 868/915MHz		
SHOWLD	[11]	function of LDRSSIL bit			
		0 **1**	**RSSIL (RSSI low flag)** **LD (lock detection flag)**		#default
			select output data of LDRSSIL, see section 3.1.8 (R7)		

3.1.3. Control Word R2

Name	Bits	Description		
A	[4:0]	swallow counter value		
		10100	**value is 20**	#default
			swallow counter range: 0 to 31	
N	[11:5]	program counter value (bits 0 – 6)		
		000 0111 1000	**N value is 120**	#default
			N counter range: 3 to 2047	

3.1.4. Control Word R3

N	[3:0]	program counter range (bits 7 – 10)		
		000 0111 1000	**N value is 120**	#default
			N counter range: 3 to 2047	
LO2DIV	[4]	LO2 divider ratio		
		0 **1**	**divide by 4** **divide by 8**	#default
AGCEN	[5]	AGC enable mode		
		0 **1**	**disabled** **enabled**	#default
AGCDEL	[7:6]	AGC delay settings		
		00 **01** **10** **11**	**no delay** **3/f_{IFF}** **15/f_{IFF}** **31/f_{IFF}**	#default
			f_{IFF} is the reference oscillator frequency f_{RO} divided by RIFF, see section 3.1.6 (R6)	
MFO	[11:8]	multi functional output		
		0000 **0001** **0010** **0011** **0100** **0101** **1000**	**MFO is in Z state** **MFO is SPI read-out** **MFO = 0** **MFO = 1** **MFO is analog RO output** **MFO is IFF output** **MFO is lock detector output**	#default

3.1.5. Control Word R4

Name	Bits	Description		
R	[10:0]	reference divider range		
		000 0100 1011	**value is 75**	#default
			R counter range: 3 to 2047	
AGCMODE	[11]	AGC delay mode		
		0 **1**	**gain decrease and increase with delay** **gain decrease without delay, gain increase with delay**	#default
			selects AGC delay mode in combination with AGCDEL bits, see section 3.1.4 (R3)	

3.1.6. Control Word R5

Name	Bits	Description		
RIFF	[10:0]	reference divider value for IFF adjustment		
		010 1010 1100	**value is 684**	#default
			IFF counter range: 4 to 2047	
MODSEL	[11]	demodulation selection		
		0 **1**	**FSK demodulation** **ASK demodulation**	#default
			selects modulation type when chip is controlled via SPI mode	

3.1.7. Control Word R6

Name	Bits	Description		
IFFPRES	[7:0]	IFF preset value		
		0101 1011	**value is 91**	#default
			IFF DAC preset at start of automatic tuning	
IFFHLT	[8]	IFF halt		
		0 **1**	**auto tuning running** **auto tuning halted**	#default
			suspends IFF automatic tuning	
IFFTUNE	[9]	IFF tuning		
		0 **1**	**disable and load DAC with IFFPRES** **enable**	 #default
ROCUR	[11:10]	reference Oscillator core current		
		00 **01** **10** **11**	**85µA** **170µA** **270µA** **355µA**	 #default

3.1.8. Control Word R7 (Read-only Register)

Name	Bits	Description		
IFFVAL	[7:0]	IFF adjustment value		
			see also IFFPRES in section 3.1.7 (R6)	
IFFSTATE	[9:8]	IFF automatic tuning state		
		00	**filter tuned or auto-tuning disabled**	
		01	**tuning up the filter frequency**	
		10	**tuning down the filter frequency**	
		11	**master oscillator of filter does not work**	
LDRSSIL	[10]	lock detector or RSSI low flag		
		0	**PLL not locked or RSSI value in lower region**	
		1	**PLL locked or RSSI value above lower region**	
		depends on SHOWLD in section 3.1.2 (R1)		
RSSIH	[11]	RSSI high flag		
		0	**RSSI value below upper region**	
		1	**RSSI value in upper region**	

4. Application Circuits for SPI Mode

4.1. Averaging Data Slicer Configured for Bi-Phase Codes

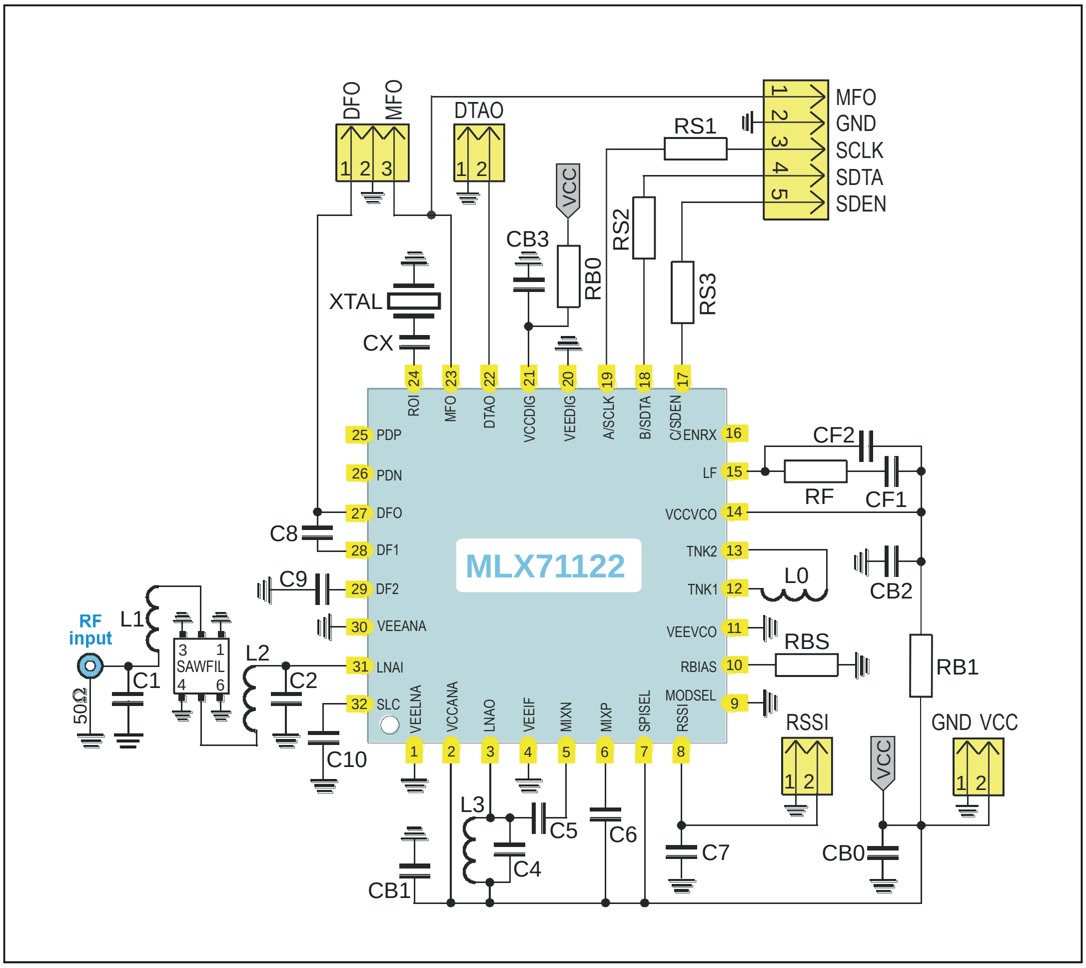


Fig. 6: Application circuit for SPI Mode (averaging data slicer option)

Note

- EVB71122 default population is SPI mode

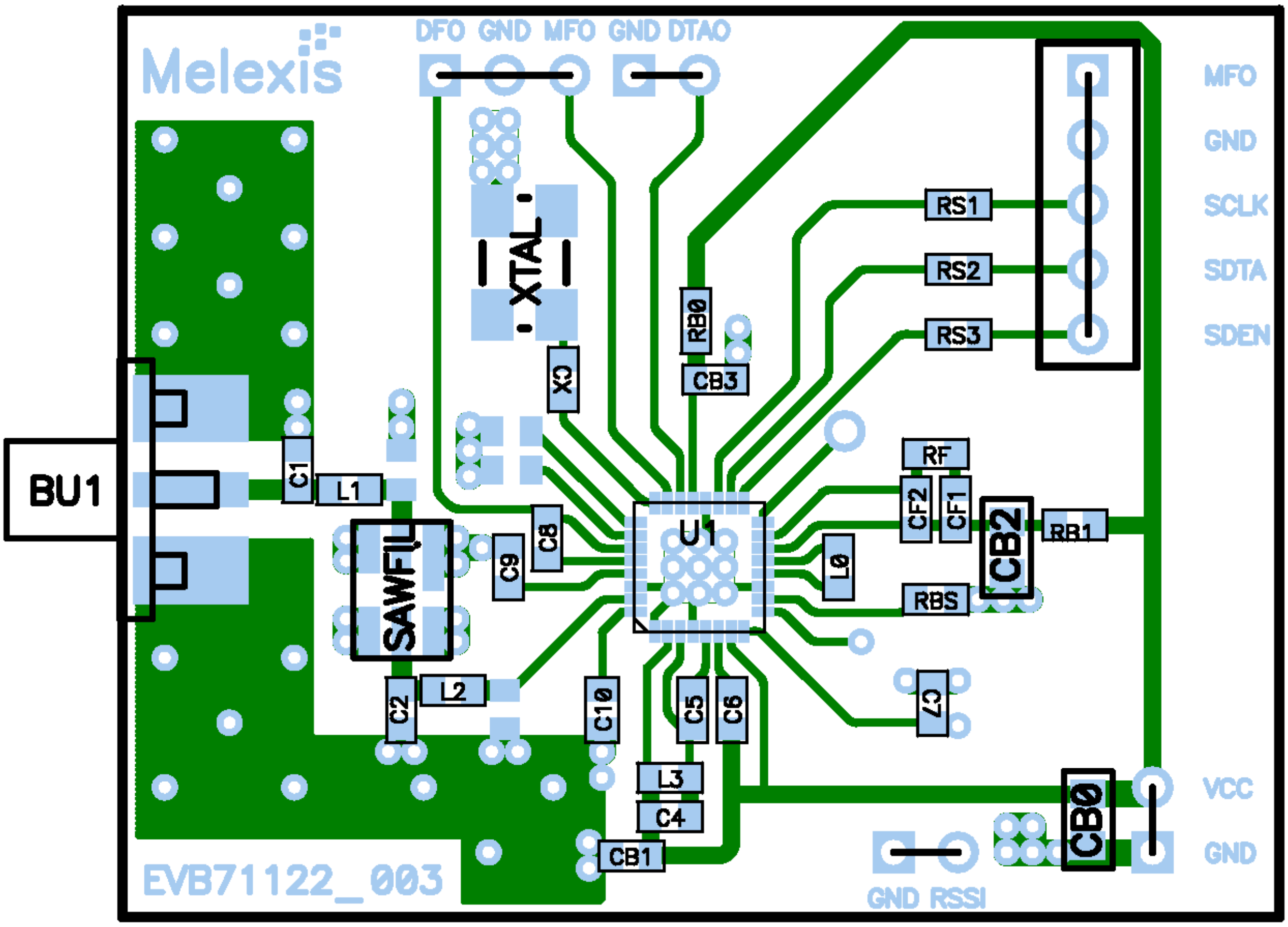


Fig. 7: PCB Top-side view (averaging data slicer option)

4.2. Peak Detector Data Slicer Configured for NRZ Codes

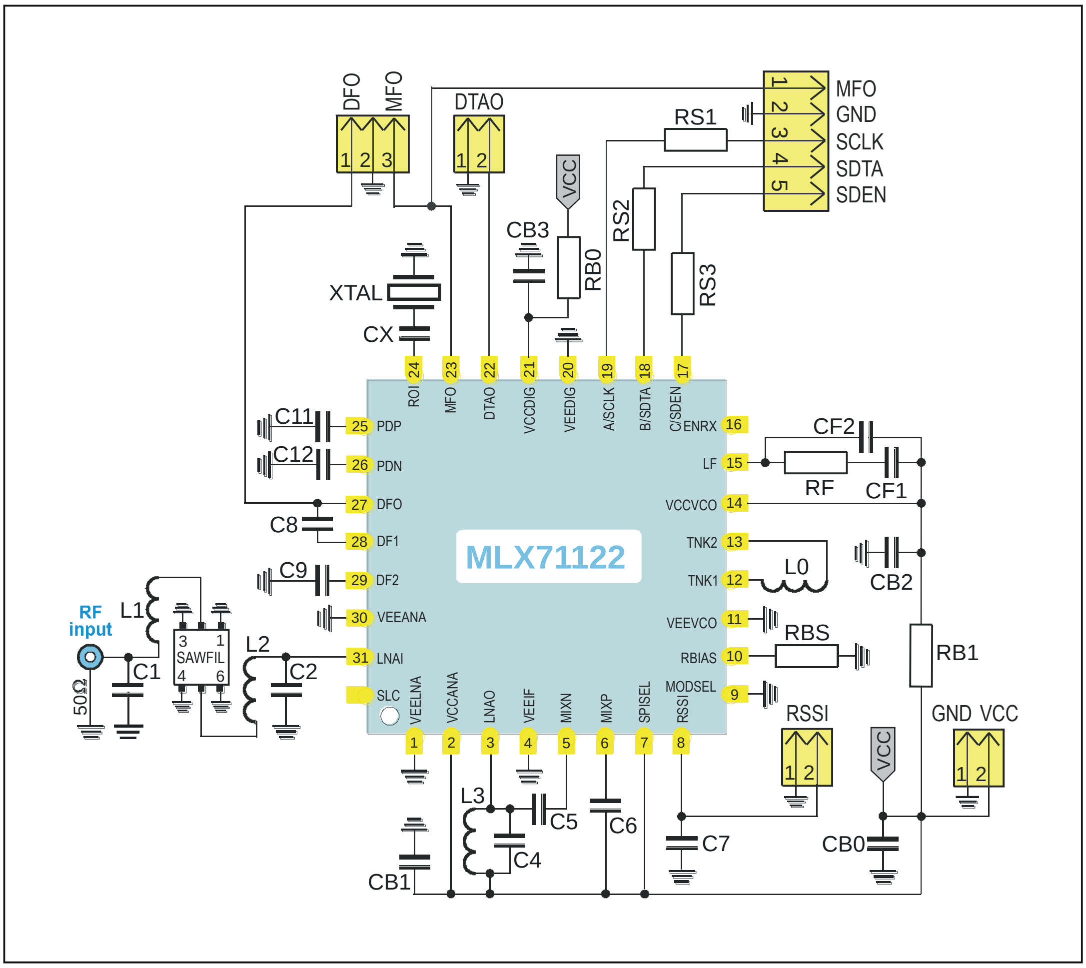


Fig. 8: Application circuit for SPI Mode (peak detector option)

Note

- EVB71122 default population is SPI mode

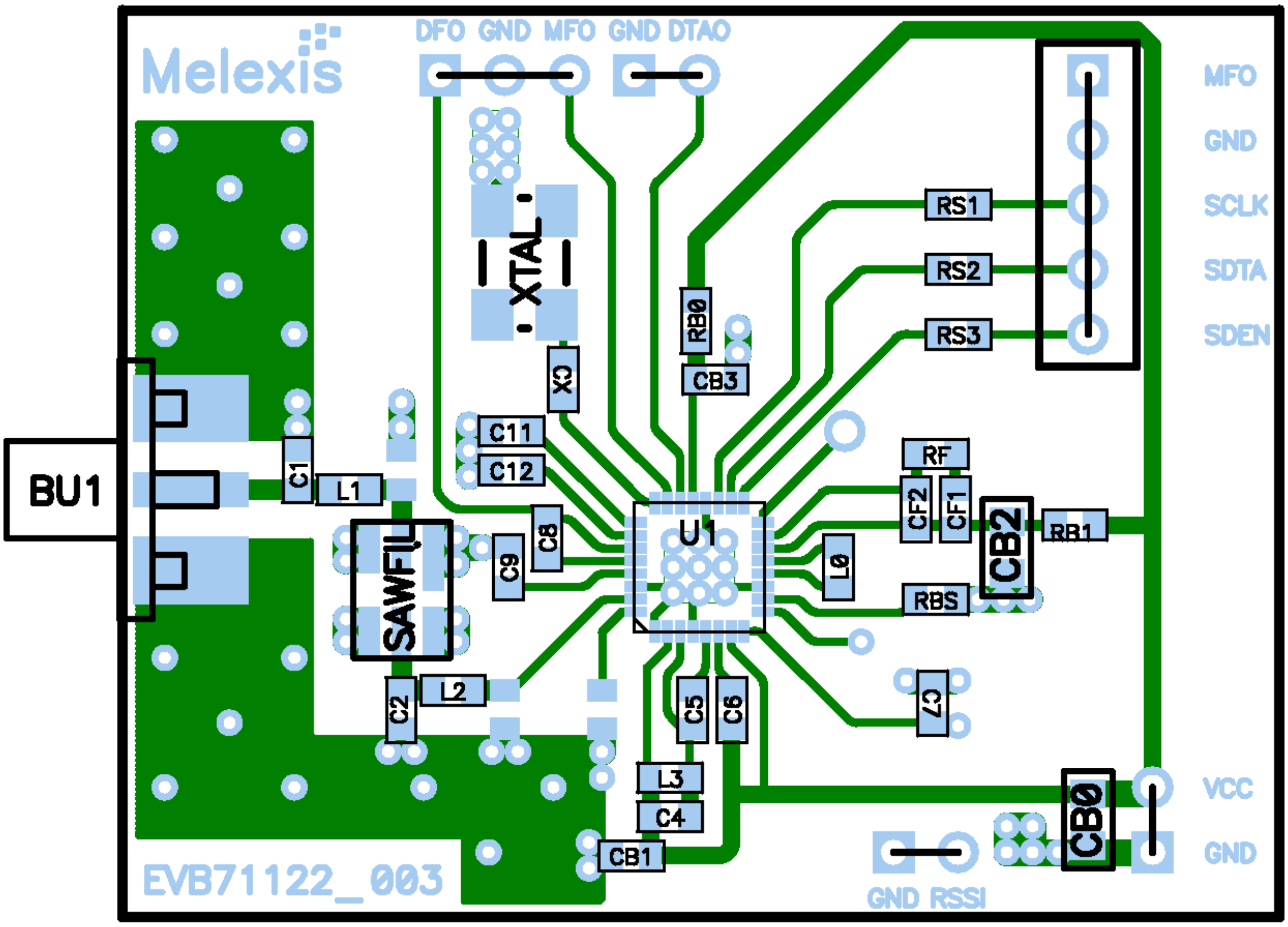


Fig. 9: PCB Top-side view (peak detector option)

4.2.1. Board Component Values List (SPI mode)

Below table is for the application circuits show in Figures 6 and 8

Part	Size	Value @ 315 MHz	Value @ 433.9 MHz	Value @ 868.3 MHz	Value @ 915 MHz	Tol.	Description
C1	0603	NIP	4.7 pF	3.3 pF	NIP	±5%	matching capacitor
C2	0603	NIP	NIP	NIP	NIP	±5%	matching capacitor
C4	0603	4.7 pF	3.3 pF	2.7 pF	2.2 pF	±5%	LNA output tank capacitor
C5	0603	100 pF	100 pF	100 pF	100 pF	±5%	MIX1 negative input matching capacitor
C6	0603	100 pF	100 pF	100 pF	100 pF	±5%	MIX1 negative input matching capacitor
C7	0603	1 nF	1 nF	1 nF	1 nF	±10%	RSSI output low pass capacitor, this value for data rate of 4 kbps NRZ
C8	0603	220 pF	220 pF	220 pF	220 pF	±10%	data low-pass filter capacitor, this value for data rate of 4 kbps NRZ
C9	0603	150 pF	150 pF	150 pF	150 pF	±10%	data low-pass filter capacitor, this value for data rate of 4 kbps NRZ
C10	0603	33 nF	33 nF	33 nF	33 nF	±10%	data slicer capacitor, this value for data rate of 4 kbps NRZ
		not required in Figure 8					
C11	0603	33 nF	33 nF	33 nF	33 nF	±10%	peak detector positive filtering capacitor, this value for data rate of 4 kbps NRZ
		not required in Figures 6					
C12	0603	33 nF	33 nF	33 nF	33 nF	±10%	peak detector negative filtering capacitor, this value for data rate of 4 kbps NRZ
		not required in Figures 6					
CB0	0805	220 nF	220 nF	220 nF	220 nF	±10%	decoupling capacitor
CB1	0603	470 pF	470 pF	470 pF	470 pF	±10%	decoupling capacitor
CB2	0805	10 µF	10 µF	10 µF	10 µF	±10%	decoupling capacitor
CB3	0603	33 nF	33 nF	33 nF	33 nF	±10%	decoupling capacitor
CF1	0603	2.2 nF	2.2 nF	2.2 nF	2.2 nF	±5%	loop filter capacitor
CF2	0603	220 pF	220 pF	220 pF	220 pF	±5%	loop filter capacitor
CX	0603	27 pF	27 pF	27 pF	27 pF	±5%	crystal series capacitor
RB0	0603	10 Ω	10 Ω	10 Ω	10 Ω	±5%	protection resistor
RB1	0603	270 Ω	270 Ω	270 Ω	270 Ω	±5%	protection resistor
RF	0603	27 kΩ	27 kΩ	47 kΩ	47 kΩ	±5%	loop filter resistor
RBS	0603	30 kΩ	30 kΩ	30 kΩ	30 kΩ	±2%	reference bias resistor
RS1…RS3	0603	10 kΩ	10 kΩ	10 kΩ	10 kΩ	±5%	protection resistor
L0	0603	33 nH	15 nH	8.2 nH	8.2 nH	±5%	VCO tank inductor
L1	0603	0 Ω	47 nH	22 nH	0 Ω	±5%	matching inductor
L2	0603	82 nH	82 nH	22 nH	8.2 nH	±5%	matching inductor
L3	0603	33 nH	22 nH	5.6 nH	5.6 nH	±5%	LNA output tank inductor
XTAL	SMD 5x3.2	10.00000 MHz / ±20ppm cal., ±30ppm temp. Telcona HEX24-10.000MHZ-12-50-F-H20-T2075-W2-T					fundamental-mode crystal
SAW FIL	SMD 3x3	SAFDC315MSM 0T00 (315 MHz)	RF3446 (433.92 MHz)	SAFCC868MSL0 X00 (868.3 MHz)	SAFCH915MAL0 N00 (915 MHz)		low-loss SAW filter from Murata or equivalent part

Note: **- NIP – not in place, may be used optionally**

5. Hardware and Software Requirements

The PC programming software has been developed for Windows XP and has been tested for later Windows versions. The program uses TVicPort I/O driver to interface to the parallel port.

The EVB71122 can be used either with a USB-SPI converter connected to the PC's USB port or it can be directly connected to the PC's printer port (LPT). If the LPT port is used then port addresses 0x278, 0x378 and 0x3BC (hexadecimal) are supported. A programming cable with a male 25-pole SUB-D connector can be purchased together with the evaluation board EVB71122.

The following LPT ports can be connected to the corresponding IC pins:

LPT port	Direction	IC pin	Cable pin
BUSY (pin11)	←	**MFO** (pin 23)	**Connected (1)**
GND (pin18-25)	—	GND	**Connected (2)**
D1 (pin3)	→	A/**SCLK** (pin 19)	**Connected (3)**
D2 (pin4)	→	B/**SDTA** (pin 18)	**Connected (4)**
D0 (pin2)	→	C/**SDEN** (pin17)	**Connected (5)**

If the PC's USB port is used, a USB-SPI converter is required (Fig. 10). It is available on request or can be purchased together with the evaluation board EVB71122.

Note that pin 7 of the MLX71122 (SPISEL) is connected to logic HIGH on the EVB71122. This is to set the receiver to SPI mode.

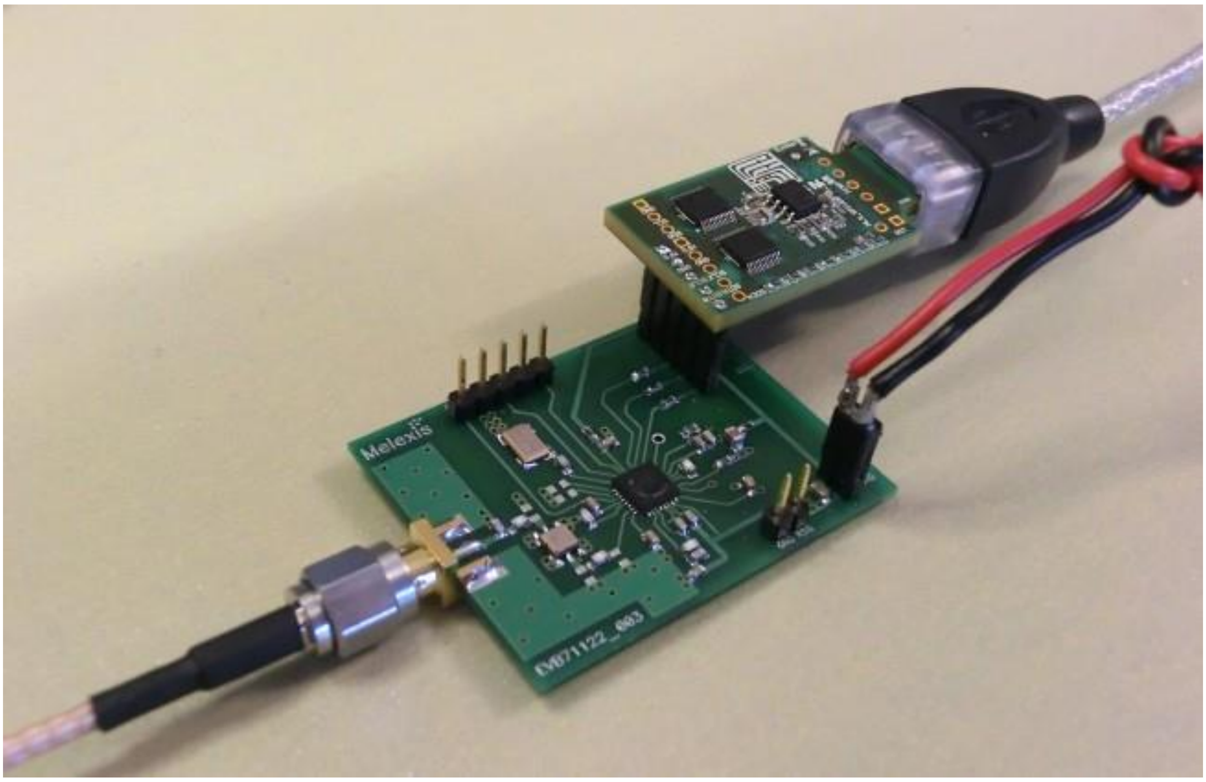


Fig. 10: How to connect the EVB71122 with the USB-SPI convertor

For further information please refer to the Programming Software Manual for MLX71122 RF Receiver .

6. Evaluation Board Layouts

- Board layout data in Gerber format is available, board size is 35.6mm x 45.3mm.

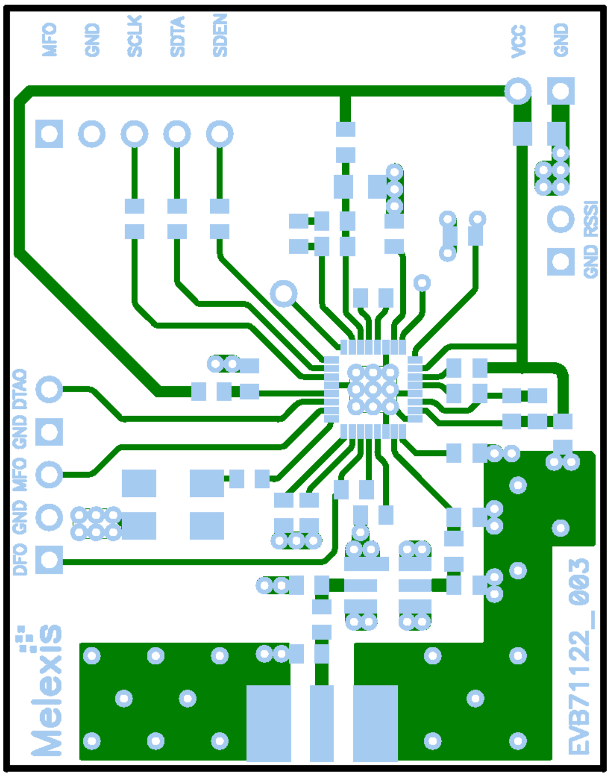


Fig. 11: PCB top view

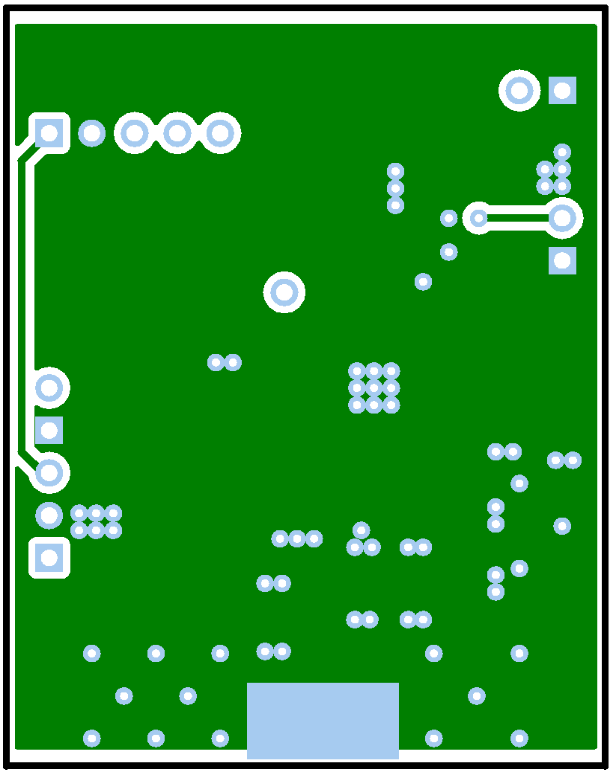
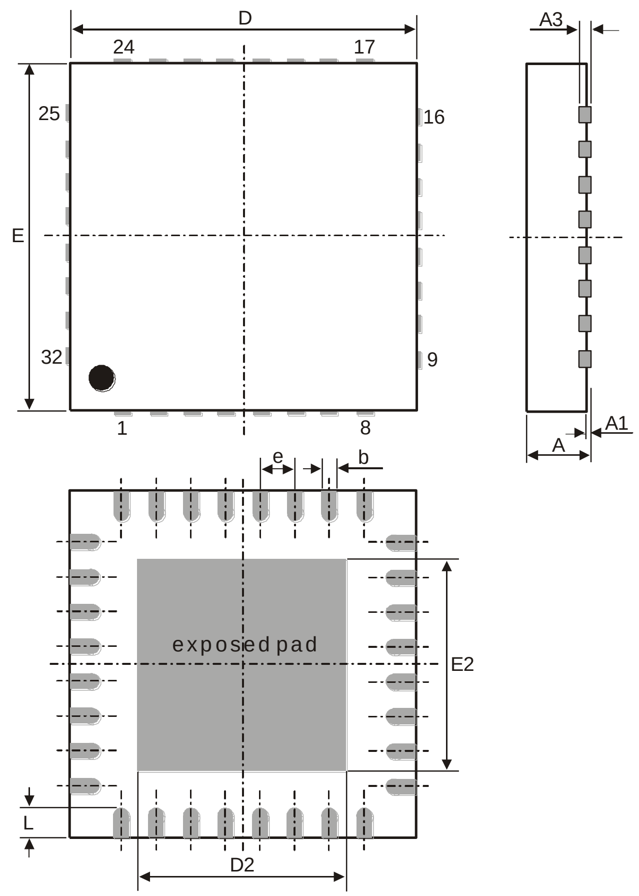


Fig. 12: PCB bottom view

7. Package Description

The device MLX71122 is RoHS compliant.



The "exposed pad" is not connected to internal ground,
it should not be connected to the PCB.

Fig 12: 32L QFN 5x5 Quad

all Dimension in mm										
	D	**E**	**D2**	**E2**	**A**	**A1**	**A3**	**L**	**e**	**b**
min	4.75	4.75	3.00	3.00	0.80	0	0.20	0.3	0.50	0.18
max	5.25	5.25	3.25	3.25	1.00	0.05		0.5		0.30
all Dimension in inch										
min	0.187	0.187	0.118	0.118	0.0315	0	0.0079	0.0118	0.0197	0.0071
max	0.207	0.207	0.128	0.128	0.0393	0.002		0.0197		0.0118

7.1. Soldering Information

- The device MLX71122 is qualified for MSL3 with soldering peak temperature 260 deg C according to JEDEC J-STD-20

8. Reliability Information

This Melexis device is classified and qualified regarding soldering technology, solderability and moisture sensitivity level, as defined in this specification, according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices (classification reflow profiles according to table 5-2)"

Wave Soldering SMD's (Surface Mount Devices)

- EN60749-20
  "Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat"

Solderability SMD's (Surface Mount Devices)

- EIA/JEDEC JESD22-B102
  "Solderability"

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

9. ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

10. Your Notes

11. Contact

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