

# Application Examples

□ Low-power tracking systems

Secure access systems

Passive Keyless Entry / Start (PKES)

# **Related Melexis Products**

| Product            | <b>Temperature</b> | <b>Package</b>    | <b>Option</b> | Packaging Form          |
|--------------------|--------------------|-------------------|---------------|-------------------------|
| MLX73290           | K                  | LQ                | ABA-000       | RE or TU                |
| Legend: K for -40° | C to 105°C         | LQ for 32L QFN5x5 |               | RE for reel (5000 pcs.) |

# Ordering information

| Product    | Option | Comment                 |
|------------|--------|-------------------------|
| EVB73290-A | 433-C  | Evaluation board 433MHz |

## General description

The EVB73290-A is an assembled printed circuit board that simplifies the evaluation of the MLX73290-A device and facilitates the development of wireless applications with this product. It is connected to a specific SPI to USB adaptor for programming the MLX73290-M device through the USB connection of a computer. The EVB73290-A is delivered with GUI-based evaluation software to easily and quickly configure the device.

The MLX73290-A device combines a highly integrated Radio Frequency transceiver for long range, high speed communication and a 3 dimensional low frequency interface (3DLF) for low power wake-up. This unique combination makes the MLX73290-A suitable for applications requiring a very low power wake-up function together with long range, high speed RF feedback.



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## 1 Kit Content

The EVB73290-A is provided with the following hardware:

- 1x Evaluation Board EVB73290-A
- 1x USB-SPI adapter board
- 1x USB cable

The Evaluation Software

• The Evaluation Software GUI73290A is provided directly on the Melexis website (same location as this document).

The following documentation is available on the Melexis website:

- Datasheet MLX73290-A
- EVB73290-A User Manual
- Flyer SmartAntenna Demonstrator

# 2 EVB73290-A Detailed Description



Figure 1: EVB73290-A



### 2.1 Power Supply

Two possible power sources can be used to supply EVB73290-A. The Power supply selection (PWR/BAT) jumper as shown in Figure 1 can be used to select the power supply either from the battery or from the external supply. When setting the PWR/BAT at 1-2 position, the MLX73290-A is supplied through the battery (CR2032) connected at the bottom. When setting the PWR/BAT at 3-4 position, an external power source is needed to supply the EVB to the external 3.3V connector (PWR).

- PWR/BAT jumper in 1-2 position = EVB supplied by the battery (CR2032)
- PWR/BAT jumper in 3-4 position = EVB supplied through 3.3V connector (external supply)

**Important Note:** In case of using an external power supply source, care must be taken to not exceed the absolute maximum voltage of 3.6V to avoid damage to the MLX73290-A device.

### 2.2 Melexis USB-SPI Adapter

The EVB73290-A comes with a USB-SPI adapter board. This board is the interface between the EVB73290-A and a PC. The USB-SPI adapter board embeds the following components:

- A PIC18F4550 microcontroller, flashed for controlling the MLX73290-A through the software.
- A USB interface to connect to a PC.
- Two Level Shifter ICs for driving/receiving the I/O signals.



Figure 2: MLX USB-SPI Adapter



## **3** Evaluation Software

The EVB73290-A is provided with Graphical User Interface software to easily and quickly evaluate the MLX73290-A device. The following chapters describe how to install and use the GUI software.

### 3.1 Installation

The Evaluation Software is delivered as executable files *MLX73290\_A\_setup32.exe* and *MLX73290\_A\_setup64.exe*, respectively for 32 or 64bits operating systems. Once started, this executable will transparently install the USB driver for the Melexis USB-SPI adapter board as well as the MLX73290-A User Interface. The following procedure should be followed to proceed with the installation:

1. Start *MLX73290\_A\_setup32.exe* or *MLX73290\_A\_setup64.exe* according to your Operating System, 32 or 64 bits

- 2. Accept License Agreement
- 3. Select the installation path (42 MB of free disk is required)
- 4. Start installation

When the MLX73290 GUI setup is running it first asks whether to install it for all system users or just your user. If you don't know choose Install for all users.

Next option is to create or not a desktop icon.

In case a problem occurs during the installation, please refer to the chapter Trouble Shooting Notes

#### 3.2 Main Window

The Figure 3 below is a screenshot of the main window of the User Interface. The User Interface Software is composed of 4 essential parts:

- 1. Top-down menus
- 2. The Register Table
- 3. The Setting Configuration
- 4. The Console







### 3.1 Top-Down Menus

- □ File
  - *Import Configuration:* To import a Register Table configuration. A browser window will open, please select the register list (.txt format) you want to upload in the User Interface.
  - *Export Configuration:* To save the Register Table configuration. A browser window will open to save the register list (.txt format) on your computer.
- Device
  - Select Device: To select the EVB73290-A connected to the computer. Please note that the last device connected, is on the top of the list.
  - *Read Device Register:* To update the register table with the register's content of the EVB73290-A.
  - *Write Registers to Device:* To update the register's content of the EVB73290-A with the Register Table
  - *Device Reset:* Perform a Soft reset of the EVB73290-A. Please note that the Register Table and the Setting Configuration will not be automatically updated

#### □ Help

• About: To get the version of the User Interface

### 3.2 Register Table

Figure 4 shows the Register Table of the User Interface. The Register Table is organized into unbanked and bank 0 register tables. Each table is displayed in different tabs individually.

The signification of each byte of the Register Table is detailed in the datasheet of the MLX73290-A product. Each byte can be edited by double clicking on it. The left window below will open with the possibility to modify the complete byte content or the different fields composing the byte.

|                      |          | Unbanked | Regist | ers E | Bank O | Regist  | ers   |    |    |    |
|----------------------|----------|----------|--------|-------|--------|---------|-------|----|----|----|
|                      |          | 0x00     | XX     | XX    | 00     | 00      | 00    | 00 | XX | XX |
| Edit Register        |          | 0x08     | XX     | XX    | 00     | 00      | 00    | 08 | XX | XX |
| Address : 0x20       |          | 0x10     | XX     | XX    | 00     | F1      | 2C    | 34 | 00 | 00 |
| Value : 0x 00        | Doubl    | e click  | 00     | 00    | FE     | 00      | 40    | B8 | 1E | 1B |
| Fields :             | <u> </u> | 0x2      | 09     |       | 33     | 27      | 00    | 07 | 00 | 2E |
| PWRDET2_EN : 0x 00   |          | 0x28     | 90     | 00    | 00     | 00      | 00    | 00 | 00 | 00 |
| PWRDET1_EN : 0x 00   |          | 0x30     | 00     | 00    | 00     | 00      | XX    | XX | XX | XX |
| RF_FE_EN[1:0]: 0x 00 |          | 0x38     | 00     | 00    | 00     | 00      | XX    | XX | XX | XX |
| BAND_SEL[1:0]: 0x 00 |          | 0x40     | XX     | XX    | XX     | XX      | XX    | XX | XX | XX |
| OK Cancel            |          | 0x48     | XX     | XX    | XX     | XX      | XX    | XX | XX | XX |
|                      |          | 0x50     | XX     | XX    | XX     | XX      | XX    | XX | XX | XX |
|                      |          | 0x58     | XX     | XX    | XX     | XX      | XX    | XX | XX | XX |
|                      |          | 0x60     | XX     | XX    | XX     | XX      | XX    | XX | XX | XX |
|                      |          | 0x68     | XX     | XX    | XX     | XX      | XX    | XX | XX | XX |
|                      |          | 0x70     | XX     | XX    | XX     | XX      | XX    | XX | XX | XX |
|                      |          | 0x78     | XX     | XX    | XX     | XX      | XX    | XX | XX | 00 |
|                      |          |          |        | Res   | et Reg | ister T | ables |    |    |    |

Figure 4: MLX73290 evaluation software: Registers table



There are two ways to update the register table:

- 1. Update the Register Table with the register content of the connected EVB73290-A => menu Device->Read Register To Device
- 2. Updating the Register Table with the Setting Configuration => pressing the button Configure Registers

Once updated, the registers which have been modified are marked in Yellow, as shown in the figure 4 above.

The content of the Register Table can be written into the EVB73290-A with the menu *Device->Write Registers to Device*.

The button Reset Register Tables will set all bytes of the Unbanked and Bank0 of the Register Table to zero. Please note that it will not impact the EVB73290-A and the command *Device->Write Registers to Device* will have to be used to also reset the EVB73290-A.



### 3.3 Settings of Configuration Part

The Figure 5 and Figure 6 show the Setting Configuration part, which are a graphical representation of the TX and RX chain of the MLX73290-A device. The Figure 7 shows the Setting Configuration part of the LF part. The settings can be changed and applied to the registers table using the <sup>Configure Registers</sup> button at the bottom left or inversely, updating the settings from the register table with the button <sup>Update Settings from Registers</sup>.

On the top, there are different tabs for each mode RF transmission, RF reception and LF mode.



Figure 5: MLX73290 evaluation software: Settings Configuration Tx & Default values





Figure 6: MLX73290 evaluation software: Settings Configuration Rx & Default values



# EVB73290-A

Evaluation Board of MLX73290-A RF Transceiver



Figure 7: MLX73290 evaluation software: Settings Configuration LF

### 3.4 Console

Figure 8 shows the console which displays error messages in red. More detailed information can be obtained using the debug option which can be selected from the drop-down menu.



#### Figure 8: MLX73290 evaluation software: Console



# 4 **RF Packet Formats**

The following figure shows the packet format for the RF transmission:

| ✓ Packet hand  | ler Edit pag | ket format     |           | Se        | rializer |
|----------------|--------------|----------------|-----------|-----------|----------|
| Packet format: | Preamble     | Sync word      | Length    | Payload   | e CRC    |
|                | 7-byte       | 2-byte         | 1-byte    | 254-byt   | 2-byte   |
| V Pac          | ket handler  | Edit packet fo | ormat     | Deseriali | zer      |
| Packet f       | format: Syn  | c word Le      | ngth Payl | oad C     | RC       |
|                | 2-           | byte 1-        | byte 254- | byte 2-l  | byte     |

Figure 9: Serializer/Deserializer formats.

**Note:** In color are the configurable settings; in grey are the optional settings.

### 4.1 RF Preamble

A preamble can be automatically added to the packet structure. It can be set from 0 to 255 bytes (set to 7 bytes in the default GUI settings). The Preamble is defined in the byte 0x49 of the Bank0 with a default value of 0x55 (0 to 255 time 0x55).

### 4.2 RF Sync Word

Size is 0, 16, 24 or 32 bits. The synchronization word is introduced automatically if the preamble is present. The length of the sync word is given by the scroll-down menu. The sync word is sent MSB first by

default. After a click on Edit packet format button, the Edit Packet format windows appear see the Figure 10 bellow.

| and the ster country |  |                  |                     |                     |                    |
|----------------------|--|------------------|---------------------|---------------------|--------------------|
| Edit Packet          | format                                       |                  |                     |                     | 23                 |
| Sync word            |  |                  |                     |                     |                    |
| 16 bits              | <ul> <li>Sync_wo</li> <li>[31:24]</li> </ul> | ord Syr<br>] [   | nc_word<br>23:16]   | Sync_word<br>[15:8] | Sync_word<br>[7:0] |
|                      | 0x 00  | 0>               | 00                  | 0x 34               | 0x 2C              |
| Fixed pa             | cket length                                  | Pack             | et length:          | 255                 | CRC                |
| Protocol ID:         | 0 byte                                       | • A              | Address: 0x         | 00                  |                    |
| Preamble le          | ngth: 7                                      | Prear            | mble: 0x AA         | 4                   |                    |
| Packet forma         | ıt:  |                  |                     |                     |                    |
| Preamble<br>7-byte   | Sync word<br>2-byte                          | Length<br>1-byte | Payload<br>254-byte | CRC<br>2-byte       |                    |
|                      |  |                  |                     | OK                  | Cancel             |

Figure 10: MLX73290 evaluation software: Edit Packet format window.



### 4.3 RF Packet Length

If the packet handler is enabled, it has to know the length of the packet to be sent/received. This one can be fixed or variable depending on the user settings.

|    | Edit Packet        | format                                       |                   |                   | l                   |                    |
|----|--------------------|--|-------------------|-------------------|---------------------|--------------------|
| I٢ | Sync word          |  |                   |                   |                     |                    |
|    | 32 bits            | <ul> <li>Sync_wo</li> <li>[31:25]</li> </ul> | ord Syno<br>j] [2 | c_word<br>4:16]   | Sync_word<br>[15:8] | Sync_word<br>[7:0] |
|    |                    | 0x E6  | 0x                | D0                | 0x AA               | 0x 3B              |
|    | ✓ Fixed pa         | icket length                                 | Packe             | t length: 8       | 3                   | CRC                |
|    | Protocol ID:       |  | - 🗸 Ad            | ddress: 0x        | 00                  |                    |
|    | Preamble le        | ngth: 7                                      | Pream             | ble: 0x AA        |                     |                    |
|    | Packet forma       | ıt:  |                   |                   |                     |                    |
|    | Preamble<br>7-byte | Sync word<br>4-byte                          | Address<br>1-byte | Payload<br>8-byte | CRC<br>2-byte       |                    |
|    |                    |  |                   |                   | ОК                  | Cancel             |

Figure 11: MLX73290 evaluation software: Edit Packet format window: Packet length

A length between 0 to 255 bytes can be choosing for fixed packet length without protocol ID bytes.

In the case of a variable packet length (Fixed packet length is disabled), the length byte is stored in the FIFO and specified as the first byte of the packet after the protocol ID bytes. See section "Payload" below.

The maximum payload length is reduced by the number of protocol ID bytes and length byte because these bytes need to be stored in the FIFO with the payload. The total size of the FIFO is 256 Bytes (128 for TX and 128 for RX) therefore, 1 byte for the variable length is used and 2 bytes for the Protocol ID, only 252 bytes will be available for the payload.



### 4.4 RF Protocol ID

Protocol ID is used when the data need to be placed before the length byte. For example, for encrypted packet the protocol ID can contain the information if the packet is encrypted or not. A size between 0 to 3 bytes can be chosen for the protocol ID and these bytes will be the first bytes stored in the FIFO.

|   | Edit Packet        | format                                      |                        |                  |                     | ×                 |
|---|--------------------|---|------------------------|------------------|---------------------|-------------------|
|   | Sync word          |   |                        |                  |                     |                   |
|   | 16 bits            | <ul> <li>Sync_wo</li> <li>[31:24</li> </ul> | ord Sync_w<br> ] [23:1 | ord Syr<br>6]    | nc_word S<br>[15:8] | ync_word<br>[7:0] |
|   |                    | 0x 00                                       | 0x 00                  | 0>               | 34                  | 0x 2C             |
|   | Fixed pa           | cket length                                 | Packet le              | ngth: 255        | ✓ CR                | с                 |
|   | Protocol ID:       | 2 bytes                                     | - Addr                 | ess: 0x 00       |                     |                   |
| 1 | Preamble le        | ngth: 7                                     | Preamble               | e: 0x AA         |                     |                   |
|   | Packet forma       | t:  |                        |                  |                     |                   |
|   | Preamble<br>7-byte | Sync word<br>2-byte                         | Protocol ID<br>2-byte  | Length<br>1-byte | Payload<br>252-byte | CRC<br>2-byte     |
|   |                    |   |                        |                  | ОК                  | Cancel            |

Figure 12: MLX73290 evaluation software: Edit Packet format window: Protocol ID

### 4.5 RF Address

An address byte can be inserted automatically after the packet length. The value of this byte is stored in a specific register, not in the FIFO.

| Edit Packet        | format                                       |                   |                     |                     |                    |   |
|--------------------|--|-------------------|---------------------|---------------------|--------------------|---|
| Sync word          |  |                   |                     |                     |                    |   |
| 16 bits            | <ul> <li>Sync_wo</li> <li>[31:25]</li> </ul> | rd Syna<br>] [2   | c_word 9<br>24:16]  | Sync_word<br>[15:8] | Sync_word<br>[7:0] |   |
|                    | 0x 00  | 0x                | 00                  | 0x 00               | 0x 00              |   |
| V Fixed pa         | acket length                                 | Packe             | t length: 2         | 55 🗸                | CRC                |   |
| Protocol ID:       |  | - 🗸 A             | ddress: 0x 0        | 00                  |                    |   |
| Preamble le        | ngth: 7                                      | Pream             | ible: Ux AA         |                     |                    |   |
| Packet forma       | at:  |                   |                     |                     |                    |   |
| Preamble<br>7-byte | Sync word<br>2-byte                          | Address<br>1-byte | Payload<br>255-byte | CRC<br>2-byte       |                    |   |
|                    |  |                   |                     | ОК                  | Cancel             | ] |

Figure 13: MLX73290 evaluation software: Edit Packet format window: Address



### 4.6 RF Payload

The Payload is set after a click on is shown in Figure 14.

, an example for a variable length with 2 bytes protocol ID

| Start Tra                | smission 🗆 🗆 🖾  |   |
|--------------------------|---|---|
| Source:<br>FIFO<br>data: | Serializer<br>B2-D6 <mark>03</mark> -AA-BB-CC-  |   |
|                          | B2-D6: Protocol ID (2 bytes)<br>03: Packet length (1 byte)<br>AA-BB-CC: Payload (3 bytes) |   |
| Repeat:                  | 10  |   |
| Delay:                   | 100 milliSecon  | d |
|                          | Transmit Close  |   |

Start Tx

Figure 14: MLX73290 evaluation software start transmission. FIFO data

**Note:** the Payload length depends on the packet length register if it is fixed. If it is variable, it depends on the **length byte** which is the first byte after the **Protocol ID** (see above); while the value set in the length register becomes a maximum value for the length byte.



See Figure 15 for the settings of the packet format with variable length.

| Edit Packet        | format              |                        |                  |                     |                    |
|--------------------|---------------------|------------------------|------------------|---------------------|--------------------|
| Sync word          |                     |                        |                  |                     |                    |
| 16 bits            | Sync_wo<br>[31:24   | ord Sync_w<br>4] [23:1 | ord Syr<br>6]    | nc_word 5<br>[15:8] | Sync_word<br>[7:0] |
|                    | 0x 00               | 0x 00                  | 0>               | 34                  | 0x 2C              |
| Fixed pa           | cket length         | Packet le              | ngth: 255        | V CR                | C                  |
| Protocol ID:       | 2 bytes             | - Addr                 | ess: 0x 00       |                     |                    |
| Preamble ler       | ngth: 7             | Preamble               | e: Ox AA         |                     |                    |
| Packet forma       | t:                  |                        |                  |                     |                    |
| Preamble<br>7-byte | Sync word<br>2-byte | Protocol ID<br>2-byte  | Length<br>1-byte | Payload<br>252-byte | CRC<br>2-byte      |
|                    |                     |                        |                  | ОК                  | Cancel             |

Figure 15: MLX73290 evaluation software Edit Packet format window.

Example packet:

#### AA-AA-AA-AA-AA-AA-34-2C-B2-D6-03-AA-BB-CC-CRC

Preamble: AA-AA-AA-AA-AA-AA-AA (7 Bytes) Sync word: 34-2C (2 bytes) Protocol ID: B2-D6 (2 bytes) Packet length: 03 (1 byte) Payload: AA-BB-CC (3 bytes according to the Packet length) And the CRC



In Figure 16, there are packet settings with fixed packet length:

| ~                           |                               |                                |                  |               |                   | _     |                   |
|-----------------------------|-------------------------------|--------------------------------|------------------|---------------|-------------------|-------|-------------------|
| -Sync w                     | vord—                         |                                |                  |               |                   |       |                   |
| 16 bit                      | s •                           | Sync_word<br>[31:24]           | Sync_<br>[23:    | word<br>16]   | Sync_wo<br>[15:8] | rd Sy | ync_word<br>[7:0] |
|                             |                               | 0x 00                          | 0x 0             | 0             | 0x 34             |       | Dx 2C             |
| ✓ Fixe                      | d packet                      | length                         | Packet I         | ength:        | 8                 | CR(   | C                 |
| Protoco                     | ID: 0                         | byte 🔻                         | Add              | lress: 0x     | 00                |       |                   |
| Preamb                      | le length                     | : 7                            | Preamb           | le: 0x A      | A                 |       |                   |
| acket fo                    | ormat:                        |                                |                  |               | -                 |       |                   |
| Preamb<br>7-byte            | ole Sy<br>e 2                 | nc word P<br>2-byte 8          | ayload<br>3-byte | CRC<br>2-byte |                   |       |                   |
|                             |                               |                                |                  |               | ОК                |       | Cancel            |
| Str                         | art Trans                     | mission                        |                  |               |                   | _ 0   | 23                |
|                             |                               |                                |                  |               | _                 |       |                   |
|                             |                               |                                |                  |               |                   |       |                   |
| So                          | urce: S                       | Serializer                     |                  |               |                   |       |                   |
| So<br>FIF<br>da             | urce: S<br>O<br>ta:           | Serializer<br>AA-BB-CC-E       | )D-11-22-        | 33-           |                   |       |                   |
| So<br>FIF<br>da             | urce: S<br>O<br>ta:           | Serializer<br>AA-BB-CC-E       | )D-11-22-        | 33-           |                   |       |                   |
| So<br>FIF<br>da<br>Re       | peat:                         | Serializer<br>AA-BB-CC-E<br>10 | )D-11-22-        | 33-           |                   |       |                   |
| So<br>FIF<br>da<br>Re<br>De | urce: S<br>To<br>ta:<br>peat: | AA-BB-CC-E                     | )D-11-22-        | 33-           |                   | milli | iSecond           |

#### Figure 16: MLX73290 evaluation software: Edit Packet format and Start Transmission windows.

Example packet:

#### AA-AA-AA-AA-AA-AA-34-2C- AA-BB-CC-DD-00-11-22-33-CRC

Preamble: AA-AA-AA-AA-AA-AA-AA (7 Bytes) Sync word: 34-2C (2 bytes) Payload: AA-BB-CC-DD-00-11-22-33 (8 bytes) And the CRC



### 4.7 RF Checksum

A checksum CRC16 can be automatically computed and added/compared to the packet sent/received, by enabling the CRC setting.

| 💽 Edit Packe  | t format                                    |                 |                    |                     | Σ                  | 3 |  |  |
|---|---|-----------------|--------------------|---------------------|--------------------|---|--|--|
| Sync wor  | d   |                 |                    |                     |                    | 1 |  |  |
| 16 bits   | <ul> <li>Sync_w</li> <li>[31:24]</li> </ul> | ord Syr<br>4] [ | nc_word<br>[23:16] | Sync_word<br>[15:8] | Sync_word<br>[7:0] |   |  |  |
|   | 0x 00                                       | 0>              | 00                 | 0x 34               | 0x 2C              |   |  |  |
| Fixed packet length Packet length: 255 CRC                        |   |                 |                    |                     |                    |   |  |  |
| Protocol II   | D: 0 byte                                   | • A             | Address: 0x        | 00                  |                    |   |  |  |
| Preamble  | length: 7                                   | Prear           | mble: 0x A         | 4                   |                    |   |  |  |
| Packet format:  |   |                 |                    |                     |                    |   |  |  |
| PreambleSync wordLengthPayloadCRC7-byte2-byte1-byte254-byte2-byte |   |                 |                    |                     |                    |   |  |  |
| OK Cancel   |   |                 |                    |                     |                    |   |  |  |

Figure 17: MLX73290 evaluation software: Edit Packet format window: CRC

### 4.8 LF Operation mode

LF operation mode: Rx only 👻



Two LF operation modes are available:

- **Rx only**, LF data can be received with the EVB73290-A
- RSSI measure only, to check the RSSI levels on the 3 antennas of the 3DLF antenna



### 4.9 LF Header



#### Figure 19: MLX73290 evaluation software: LF Header

The size of the header can be selected through the scroll down menu. The Bit order LSB first or MSB first can be changed, and also the bit polarity. The default polarity (LFRX\_POL = 0) Manchester pattern 01 will yield 0 as data bit. The standby time between two LF Rx polling can be modified with the scroll down menu.



# 5 GPIO

The hardware default values of GPIOs after power-on reset (POR) are:

| GPIO0 | READY     | MLX73290-A is ready after start-up sequence (POR)    |
|-------|-----------|--|
| GPIO1 | READY_NOT |  |
| GPIO2 | TMR_FLAG  | Programmable timer flag                              |
| GPIO3 | BATTOK    | Battery level measured above the minimum level 2.1V. |

#### Figure 20: Default GPIO values table after POR

These are the values of the GPIO when the MLX73290-A device has just been supplied or when GPIOs registers were not overwritten. The digital signals are active high (unless otherwise specified).

### 5.1 RX GPIO

This is the default values of the GPIO set by the MLX73290 Tool when the EVB is running in Rx.

| GPIO0 | RFRX_CLOCK    | RF Clock output after data-handler        |
|-------|---------------|---|
| GPIO1 | RFRX_DATA     | RF Data output after data-handler         |
| GPIO2 | RXRF_WAIT_HDR | RF state-machine waiting for valid Header |
| GPIO3 | RFRX_PAYLOAD  | RF state-machine receiving the payload    |

#### Figure 21: MLX73290 evaluation software: Default GPIO values table for Rx



# 6 Timing diagram

This is an example frame to show the signal timing (Fixed packet length disabled, CRC enabled):

|              |           |           | Start Rx |         |     |   |
|--------------|-----------|-----------|----------|---------|-----|---|
|              | Preamble  | Sync word | Length   | Payload | CRC | Preamble  |
|              | 'AIT_HDR: | ·         |          |         |     |   |
| RFRX_P.<br>♠ | AYLOAD:   |           |          |         |     | 1   |
| RFRX_P       | KT:       |           |          |         |     | Stay high until<br>the read access<br>to the FIFO |

#### Figure 22: GPIO outputs timing diagram

t



# 7 Tutorial for the Communication Modes

### 7.1 Crystal Frequency Correction

The crystal frequency correction is a correction factor to compensate the frequency variation between crystals. The required frequency correction parameter is printed on your EVB.

First, take your EVB73290-A and import the original parameters. Then change the frequency correction parameter accordingly.

**Note:** When the crystal frequency correction is not adjusted, the chip will still work (i.e. packet exchange done in previous section) because MLX73290-A embeds a carrier recovery feature in RX mode such that it will compensate for the mismatch between the TX and RX carrier up to a certain level. For optimal performances in narrow-band applications, the crystal frequency correction should be adjusted for each board because the carrier frequency is slightly different depending on the crystal, therefore, this value can be set to get the exact carrier frequency desired. The following formula applies:

$$f_{\rm Corr} = \frac{fOutMeas}{fOut} fRef - fRef$$

Where  $f_{Corr}$  is the crystal frequency correction,  $f_{Out Meas}$  is the measured carrier frequency,  $f_{Out}$  is is the desired output carrier frequency and  $f_{Ref:}$  is the Ideal crystal frequency, e.g. 32MHz for EVB73290-A.

### 7.2 Continuous Wave (CW) Mode

After the operating frequency is fine adjusted (chapter above), it is needed to choose the desired output power with the two settings above. The first one is a number of PA stages between 1 to 4 the second one is a power tuning word between 8 to 55.



#### Figure 23: MLX73290 evaluation software: Stages and Tuning settings.

Therefore, the minimum is: Stages = 1 and Tuning = 8 and the maximum: Stages = 4 and Tuning = 55.

**Note:** a target output power can be achieve with fewer stages and a higher power tuning word, this is better in terms of current consumption.

To continuously transmit at the required frequency, the OOK modulation type must be selected. If FSK is selected, the transmit frequency will be equal to the selected operating frequency +/- the frequency deviation (depending on the logical data selected, fixed 0 or 1). Please select OOK as shown below.





### Figure 24: MLX73290 evaluation software: Modulation.

The Source must be selected to Fixed1, in order to continuously send logic 1.



#### Figure 25: MLX73290 evaluation software: Source select.

### 7.3 Continuous Modulation

To send a continuous modulation, the Source can be selected either to Fixed0, Fixed1 or signal from a GPIO (see explanation below).



Figure 26: MLX73290 evaluation software: Source select.

After, it is required to select Manchester coding or data whitening, respectively alternating 1 and 0 or pseudo random data based on PN9 sequence, to see the modulation on the spectrum analyzer:

|   | Encoder              |  |  |  |  |  |  |
|---|----------------------|--|--|--|--|--|--|
|   | ✓ Manchester coding  |  |  |  |  |  |  |
|   | Data white           |  |  |  |  |  |  |
| _ | Interpolator         |  |  |  |  |  |  |
|   | Inverte bit polarity |  |  |  |  |  |  |
|   | LSB first            |  |  |  |  |  |  |
|   | Data rate: 19 2 kbps |  |  |  |  |  |  |

Figure 27: MLX73290 evaluation software: Encoder.



|              | Manchester<br>coding | Data<br>white |
|--------------|----------------------|---------------|
| PN9 sequence | enable               | disable       |
| 101010       | disable              | enable        |

Figure 28: Encoding table.

To control the data, it is possible to send a modulating signal on a GPIO input by selecting one of the GPIO as the modulation source.



Figure 29: MLX73290 evaluation software: Source select.

After selecting one of the GPIO, be careful to set this GPIO as a digital input (pull-up or pull-down options are available) as shown in Figure 28.



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Figure 30: MLX73290 evaluation software: GPIO.

After, it is needed to choose between FSK and OOK:





**Note:** When a modulating signal is used it is possible to do the desired modulation and Manchester coding or data whitening become optional to see the continuous modulation.



### 7.4 RF Tx example

### 7.4.1 Setup

Bellow, an example of a transmitting setup for the EVB73290-A



#### Figure 32: Packets exchange schematic.

On the computer install the tool. After that, select the tab on the top of the interface and configure it with the right settings.

#### 7.4.2 Packet Exchange Example

Before all, it is needed to select the device. For that, connect the EVB73290 through the USB-SPI adapter and select the device:



Note: The last device connected, is on the top of the list.

After selecting the right mode (through top tab), and once the settings are configured, there are three steps to start the communication (shown below).



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#### Figure 34: MLX73290 evaluation software: Steps for communication example.

**Note:** It is a good practice to read the device registers before configuring the register to highlight the registers changes from the current registers that have just been read.

**Step 1:** Configure the Register List by clicking on the button highlights the changes in yellow upon successful configuration.

| Unbanked Registers Bank 0 Registers |    |    |    |    |    |    |    |    |
|-------------------------------------|----|----|----|----|----|----|----|----|
| 0x00                                | XX | XX | 00 | 00 | 00 | 00 | XX | XX |
| 0x08                                | XX | XX | 00 | 00 | 00 | 08 | XX | XX |
| 0x10                                | XX | XX | 00 | F1 | 2C | 34 | 00 | 00 |
| 0x18                                | 00 | 00 | FE | 00 | 40 | B8 | 1E | 1B |
| 0x20                                | 09 | 01 | 33 | 27 | 00 | 07 | 00 | 2E |
| 0x28                                | 90 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x30                                | 00 | 00 | 00 | 00 | XX | XX | XX | XX |
| 0x38                                | 00 | 00 | 00 | 00 | XX | XX | XX | XX |
| 0x40                                | XX |

Figure 35: MLX73290 evaluation software: Registers table.

**Step 2:** Then, update the EVB73290-A with the Register List by clicking "Write Registers to Device" in Device menu or Ctrl+W key.

Configure Registers

The register table





Figure 36: MLX7320 evaluation software: Write Registers to Device.

Step 3: Start Transmission and Reception by clicking on Start Tx for the transmitter and

Start Rx for the receiver. On the transmitter, the FIFO data (payload), the number of time to repeat the message and the delays between 2 packets must be specified.

| Start Tran    | smission                          |
|---------------|-----------------------------------|
| Source:       | Serializer                        |
| FIFO<br>data: | dq-00-00-00-5D-E6-40-00-48-C6-60- |
| Repeat:       | 10                                |
| Delay:        | 100 milliSecond                   |
|               | Transmit Close                    |

Figure 37: MLX73290 evaluation software: Transmit Payload.

On the console, the packets transmit are displayed.



Figure 38: MLX73290 evaluation software: A console example



### 7.5 RF Rx example

Bellow, an example of a receiving setup for the EVB73290-A



#### Figure 39: Packets exchange schematic.

On the computer install the tool. After that, select the Rx 2 Settings tab on the top of the interface and configure it with the right settings. After that, the same process can be followed to receive in RF mode.

The packets received are displayed in the console.

| DEBUG -   | Scroll to End Pause Clear Save log  |  |  |  |  |  |
|---|---|--|--|--|--|--|
| Watting for th  | CWT OCNCESS   |  |  |  |  |  |
| MLX73290: V   | Vriting unbanked register 0x2F : 0xFC   |  |  |  |  |  |
| MLX73290: D<br>Waiting for N  | ata received: packet count(4) : 0a 00 00 00 5d e6 40 00 4b c6 60<br>ew Packet |  |  |  |  |  |
| MLX73290: V   | Vriting unbanked register 0x2F : 0xFC   |  |  |  |  |  |
| MLX73290: Data received: packet count(5) : 0a 00 00 00 5d e6 40 00 4b c6 60<br>Waiting for New Packet |   |  |  |  |  |  |
| MLX73290: Writing unbanked register 0x2F : 0xFC   |   |  |  |  |  |  |
| MLX73290: Data received: packet count(6) : 0a 00 00 00 5d e6 40 00 4b c6 60<br>Waiting for New Packet |   |  |  |  |  |  |
| MLX73290: V   | Vriting unbanked register 0x2F : 0xFC   |  |  |  |  |  |
| MLX73290: D   | ata received: packet count(7) : 0a 00 00 00 5d e6 40 00 4b c6 60              |  |  |  |  |  |

Figure 40: MLX73290 evaluation software: The receiver console (DEBUG mode)



### 7.6 Summary of Modulation Settings

|   | Modulation source                        | FSK/OOK | Manchester           | Datawhite            | Comment  |
|---|--|---------|----------------------|----------------------|--|
| Continuous<br>wave                          | Fixed logic 1                            | ООК     | disable              | disable              |  |
| Continuous modulation FSK<br>Manchester     | Fixed logic 1 or<br>Fixed logic 0        | FSK     | enable               | disable              |  |
| Continuous modulation FSK data whitening    | Fixed logic 1 or<br>Fixed logic 0        | FSK     | disable              | enable               |  |
| Continuous modulation FSK<br>GPIO           | GPIO 0:<br>GPIO 1:<br>GPIO 2:<br>GPIO 3: | FSK     | enable or<br>disable | enable or<br>disable | If it is needed to<br>encode data. It is<br>necessary to<br>modulate data<br>either Manchester<br>coding or data<br>whitening. |
| Continuous modulation OOK<br>Manchester     | Fixed logic 1 or<br>Fixed logic 0        | ООК     | enable               | disable              |  |
| Continuous modulation OOK<br>data whitening | Fixed logic 1 or<br>Fixed logic 0        | OOK     | disable              | enable               |  |
| Continuous modulation OOK<br>GPIO           | GPIO 0:<br>GPIO 1:<br>GPIO 2:<br>GPIO 3: | ООК     | enable or<br>disable | enable or<br>disable | If it is needed to<br>encode data. It is<br>necessary to<br>modulate data<br>either Manchester<br>coding or data<br>whitening. |

Figure 41: Summary of modulation settings table.

**Note**: For continuous modulation through GPIOs, the selected GPIO need to be set as a digital input.



# 8 LF examples

To configure the LF mode in the tool, select the 3rd tab.

| Rx 2 Settings Tx 2 Settings LF Settings |          |  |  |  |  |  |  |  |
|---|----------|--|--|--|--|--|--|--|
| LF Rx<br>LF Field                       | Preamble |  |  |  |  |  |  |  |
| Coil1_Listen Pay                        |          |  |  |  |  |  |  |  |
| Figure 42: LF mode selection.           |          |  |  |  |  |  |  |  |

Two different modes are possible: "Rx only" to receive LF data and "RSSI measure only" to measure the RSSI levels one the 3DLF antenna

### 8.1 Rx only example

The Rx only mode is used to receive data in LF. First, "**Rx only**" needs to be selected.



Figure 43: Rx only LF operating mode selection.

Once the "**Rx only**" operating mode is selected, the header has to be configured.







Figure 44: LF header configuration.

In Rx "Rx only" operating mode 3 other settings can be changed in the tool:

- Invert bit polarity: 3D LF RX polarity by default polarity (LFRX\_POL = 0) Manchester pattern 01 will yield 0 as data bit.
- LSB first: Bit order LSB first or MSB first.
- **T standby**: Standby interval between two 3D LF RX polling.

To configure the chip, it is important to first select the right device:



After that the register table needs to be updated. By clicking on the Then write the register in the chip.

button

**Configure Registers** 



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Figure 46: LF start receiving.

**Note:** It is a good practice to read the device registers before configuring the register to highlight the registers changes from the current registers that have just been read.

**Step 1:** Configure the Register List by clicking on the button highlights the changes in yellow upon successful configuration.

| Configure | Registers |
|-----------|-----------|
|-----------|-----------|

. The register table

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| Unbanked Registers Bank 0 Registers |    |    |    |    |    |    |    |    |  |  |
|-------------------------------------|----|----|----|----|----|----|----|----|--|--|
| 0x00                                | XX | XX | 00 | 00 | 00 | 00 | XX | XX |  |  |
| 0x08                                | XX | XX | 00 | 00 | 00 | 08 | XX | XX |  |  |
| 0x10                                | XX | XX | 00 | F1 | 2C | 34 | 00 | 00 |  |  |
| 0x18                                | 00 | 00 | FE | 00 | 40 | B8 | 1E | 1B |  |  |
| 0x20                                | 09 | 01 | 33 | 27 | 00 | 07 | 00 | 2E |  |  |
| 0x28                                | 90 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |  |  |
| 0x30                                | 00 | 00 | 00 | 00 | XX | XX | XX | XX |  |  |
| 0x38                                | 00 | 00 | 00 | 00 | XX | XX | XX | XX |  |  |
| 0x40                                | XX |  |  |

Figure 47: MLX73290 evaluation software: Registers table.

**Step 2:** Then, update the EVB73290-A with the Register List by clicking "Write Registers to Device" in Device menu or Ctrl+W key.



#### Figure 48: MLX73290 evaluation software: Write Registers to Device.

**Step 3:** Start Transmission and Reception by clicking on "Start LF". Once the "Start LF" button is pressed, the 3DLF Sate machine is configured according to the LF operation mode. For example, in case of RX mode, the scanning operation will start only when the "Start LF" button is pressed.



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Figure 49: LF start receiving.

After starting the reception, the receiving data can be seen in the console.

| INFO    Scroll to End Pause Clear Save log                   |  |  |  |  |  |
|--|--|--|--|--|--|
| MLX73290: Waiting for LF telegram                            |  |  |  |  |  |
| MLX73290: Data received: packet count(5) : b3 22 33 44 55 66 |  |  |  |  |  |
| MLX73290: Waiting for LF telegram                            |  |  |  |  |  |
| MLX73290: Data received: packet count(6) : b3 22 33 44 55 66 |  |  |  |  |  |
| MLX73290: Waiting for LF telegram                            |  |  |  |  |  |
| MLX73290: Data received: packet count(7) : b3 22 33 44 55 66 |  |  |  |  |  |
| MLX73290: Waiting for LF telegram                            |  |  |  |  |  |

Figure 50: LF start receiving.



### 8.2 RSSI measure (only) example

It is also possible to measure the RSSI levels on the 3 LF antennas by selecting the "**RSSI measure** only" LF operating mode.



Figure 51: LF start receiving.

Then, after start the reception, the levels can be seen in the dynamic chart.



#### Figure 52: LF start receiving.

The levels are update only if they cross the red line of the "Trig. Level". The red line can be moved with the cursor.



# 9 Trouble Shooting Notes

| Unable to start Transceiver                     | <ul> <li>Check if the jumper PWR is connected on the right power supply source</li> <li>In case of EXT, check that a supply between 2.1 and 3.6V is applied between +PWR and GND</li> <li>Check the voltage level and verify the initial value of the GPIO pins</li> </ul>   |
|---|--|
| Issue during the installation of the USB driver | <ul> <li>The Evaluation Software setup tries to install the USB driver automatically. If the driver installation was not completed successfully, you can follow procedure below:</li> <li>Manually open the driver installation dialogue that pops up after plug in the USB-SPI adapter.</li> <li>Browse to the Melexis Framework installation folder (e.g. C:\Program Files\Melexis\ MLX73290 Evaluation Software) and choose the MLX_SPIUSB_Driver folder.</li> <li>If automatic detection for the USB-SPI adapter fails you have to open System Properties and choose Device Manager.</li> <li>Select the device MLX-SPI-Adapter and click right mouse button on it if there is an exclamation mark.</li> <li>Choose Update driver and browse to the path for MLX_SPIUSB_Driver.</li> </ul> |



# 10 Appendix

### 10.1 EVB Schematic



Figure 53: EVB Schematic 1

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**Evaluation Board of MLX73290-A RF Transceiver** 



Figure 54: EVB Schematic 2



# **EVB73290-A** Evaluation Board of MLX73290-A RF Transceiver

10.1.1 EVB Layout









# 11 EVB Bill of Materials (BOM)

### 11.1 EVB73290-A

| Component               | Size               | Value    | Tolerance   | Description                                    |
|-------------------------|--------------------|----------|-------------|--|
| C1                      |                    | 10u      | ±20%        | De-coupling capacitor                          |
| C2,C3, C7, C8, C10, C13 | 0603               | 470p     | <b>±20%</b> | Impedance matching capacitor                   |
| C4, C6, C9 ,C11         | 0805               | 1u       | <b>±20%</b> | De-coupling capacitor                          |
| C5, C26                 | 0603               | 220p     | ±5%         | Impedance matching capacitor                   |
| C16, C24                | 0603               | 10p      | ±5%         | Impedance matching capacitor                   |
| C14, C15                | 0603               | 22p      | ±5%         | Impedance matching capacitor                   |
| C17, C23                | 0603               | 0.75p    | ±5%         | Impedance matching capacitor                   |
| C18, C20                | 0603               | 5.1p     | ±10%        | Impedance matching capacitor                   |
| C19, C21                | 0603               | 57.5p    | ±5%         | Impedance matching capacitor                   |
| C32, C34, C36           | 0603               | 470p     | ±1%         | Impedance matching capacitor                   |
| C33, C35, C37           | 0603               | 180p     | ±1%         | Impedance matching capacitor                   |
| L1, L6                  | 0603               | 13nH     | <b>±2%</b>  | WE-KI Wire Wound Ceramic Inductor              |
| L2, L5                  | 0603               | 27nH     | ±2%         | WE-KI Wire Wound Ceramic Inductor              |
| L3, L4                  | 0805               | 33nH     | <b>±2%</b>  | WE-KI Wire Wound Ceramic Inductor              |
| L8                      |                    | 7.2mH    |             | 3DLF coil                                      |
| R1                      | 0603               | 100R     | ±1%         |  |
| R3, R4, R5              | 0603               | 47K      | ±1%         |  |
| X1                      | XTAL200x<br>160x45 | NX2016SA | 10ppm       | 32MHz Crystal from NDK, NX2016SA 10 ppm, 12 pF |

Figure 56: BOM EVB73290-A



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www.melexis.com

Or for additional information contact Melexis Direct:

Europe, Africa, Asia:

America:

Phone: +32 1367 049 E-Mail: sales\_europe@melexis.com Phone: +1 248 306 5400 E-Mail: sales\_usa@melexis.com

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