MLX75024 Time-of-Flight Sensor Array

Preliminary datasheet

All specifications subject to change without notice

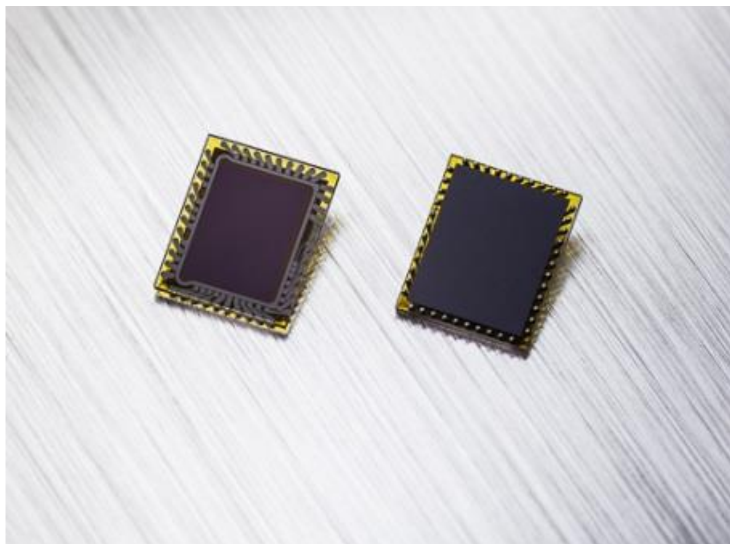
Features & Benefits

- 1/3” optical Time-of-Flight sensor (optical area = 4.8 x 3.6 mm^2)
- QVGA resolution, 320 x 240 pixels
- 15 x 15 µm DepthSense® pixels
- Demodulation frequency up to 40 MHz
- Two dual channel analog outputs
- Pixel rate up to 80 MSPS
- 960 us minimum image readout time
- Gain modes for amplified signal
- 22% external quantum efficiency (850 nm wavelength)
- 15% external quantum efficiency (940 nm wavelength)
- Over 93% AC contrast (20 MHz modulation frequency)
- Over 85% AC contrast (40 MHz modulation frequency)
- Built-in temperature sensor
- Wafer level glass BGA package (Dimensions : 6.6 x 5.5 x 0.6 mm)
- AEC-Q100 qualified (grade 2)
- Ambient operating temperature ranges of -20 +85°C and -40 to +105°C

Description

MLX75024 is an optical time-of-flight (TOF) image sensor. Potential use cases include gesture recognition, automotive in-cabin monitoring, surveillance, people counting and robot vision. The sensor features 320 x 240 (QVGA) time-of-flight pixels based on DepthSense® pixel technology. MLX75024 is the successor of MLX75023, with enhanced sensitivity and reduced power consumption. In combination with MLX75123, Melexis’ dedicated TOF companion chip provides a complete ToF sensor solution.
The sensor is available in automotive and industrial grades, both in a small glass BGA wafer level package form factor which offers many integration possibilities.

Figure 1: MLX75024 top (left) and bottom (right)



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1. Datasheet Changelog

Version	Date	Changes
0.10.5	12/Nov/2018	Preliminary release version

Table 1: Changelog

2. Glossary of terms

Term	Definition
CAPD	Current Assisted Photon Demodulator.
DC contrast	Capability of the sensor to capture electrons under a constant light source.
AC contrast	Capability of the sensor to capture electrons under a modulated light source.
Full well capacity	Maximum number of electrons which can be collected on a tap of the pixel.
T_{INT}	Integration time. Period of time when DMIX signals are toggling, illumination is activated and electrons are captured in the pixels.
$T_{COOLDOWN}$	Period of time after integration when illumination is off and can decrease its temperature.
T_{READ}	Period of time required to readout the values of all the pixels of the array.
PDNU	Pixel depth non uniformity
PNNU	Pixel norm non uniformity

Table 2: Glossary of terms

3. Ordering Information

Ordering example: MLX75024RTF-GAA-001-TR

Product	Temperature Code	Package	Option Code	Packing Form
MLX75024	R	TF	GAA-000	TR
MLX75024	S	TF	GAA-000	TR
MLX75024	R	TF	GAA-001	TR
MLX75024	S	TF	GAA-001	TR
MLX75024	R	TF	GAA-000	SP

Table 3: Product ordering code(s)

Legend:

Temperature Code	R : -40°C to 105°C S : -20°C to 85°C
Package Code	TF : Glass BGA Package, 44pins
Option Code	GAA-000 : without cover tape GAA-001 : with cover tape[1]
Packing Form	TR : Tray SP : Samples

Table 4: Option code(s)

[1] Shelf life of samples with cover tape is of 3 months.

4. Application System Architecture

A complete TOF system or camera module typically includes the following main components:

- MLX75123 + MLX75024 TOF chipset
- A high bandwidth near infrared (NIR) illumination source (LED or laser)
- Beam shaping optics for the light distribution
- A receiving sensor lens, optimized for maximum NIR transmittance
- A microcontroller or DSP to calculate and process the data

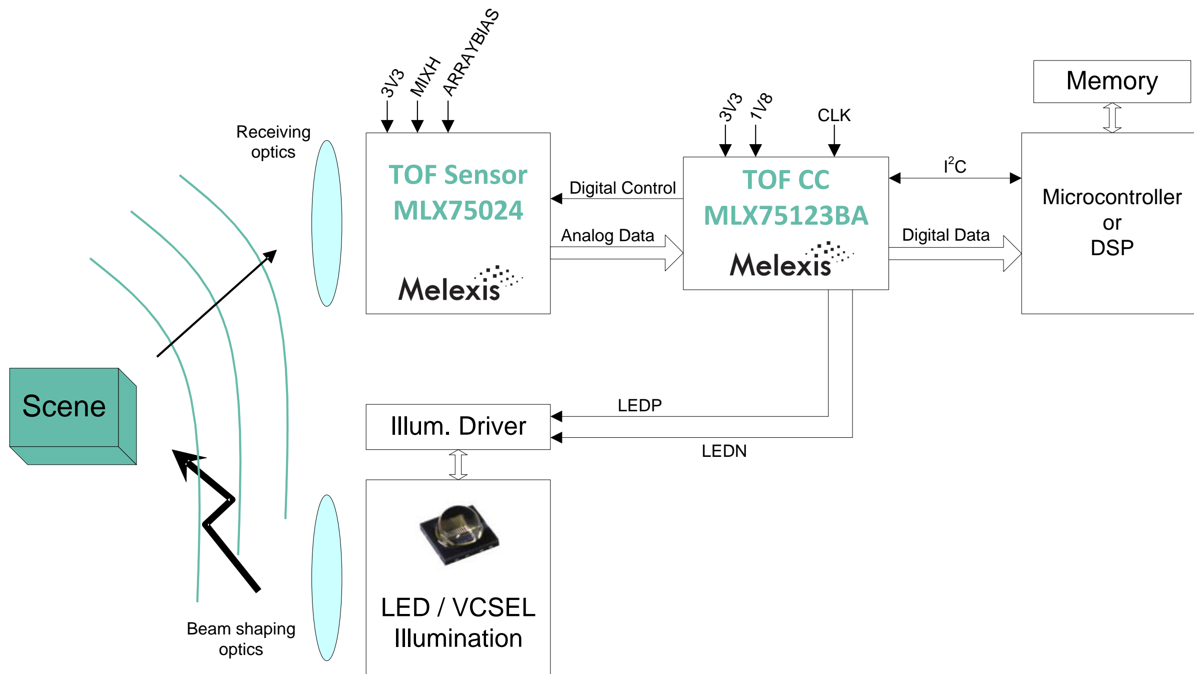


Figure 2: System architecture

5. Pinout Description

Designator	Pin #	Function	Description
ROW[7] ROW[6] ROW[5] ROW[4] ROW[3] ROW[2] ROW[1] ROW[0]	1 2 3 4 5 6 7 8	Dynamic Digital Input	These inputs are used to apply the pixel row address bits signals coming from the MLX75123BA.
ARRAYBIAS	9	Voltage Bias	Bias of CAPD terminal.
PIXELVDD	10	Pixel voltage pin	Output pin for testing PIX_{VDD} voltage levels.
VDDA	11	Analog Supply	
AGND	12	Ground	
OUT3	13	Analog Output	
OUT2	14	Analog Output	
OUT0	15	Analog Output	
OUT1	16	Analog Output	
LATCH_ENABLE	17	Dynamic Digital Input	Enables the configuration of the sensor. Active high.
PIXELFLUSH	18	Dynamic Digital Input	Used to remove the remaining charges in the pixel substrate.
CORE_RESET	19	Dynamic Digital Input	Detector reset signal.
SHUTTER	20	Dynamic Digital Input	Control signal of the pixel.
CS	21	Digital Input	Chip select. Active High.
DGND	22	Ground	
VDDD	23	Digital Supply	
COLUMN[0] COLUMN[1] COLUMN[2] COLUMN[3] COLUMN[4] COLUMN[5] COLUMN[6] COLUMN[7]	24 25 26 27 28 29 30 31	Dynamic Digital Input	These inputs are used to apply the pixel column address bits signals coming from the MLX75123BA.
DGND	32	Ground	
VDDD	33	Digital Supply	
DMIX[1] DMIX[0]	34 35	Dynamic Digital Input	Digital MIX1&0. Active High.
DGND	36	Ground	
MIXH	37	TOF Supply	Supply pin for the V_{MIXH} voltage
MIXH	38	TOF Supply	Supply pin for the V_{MIXH} voltage
DGND	39	Ground	
DGND	40	Ground	
MIXH	41	TOF Supply	Supply pin for the V_{MIXH} voltage
MIXH	42	TOF Supply	Supply pin for the V_{MIXH} voltage
DGND	43	Ground	
VDDD	44	Digital Supply	

Table 5: MLX75024 Pinout

6. Typical Connection Diagram

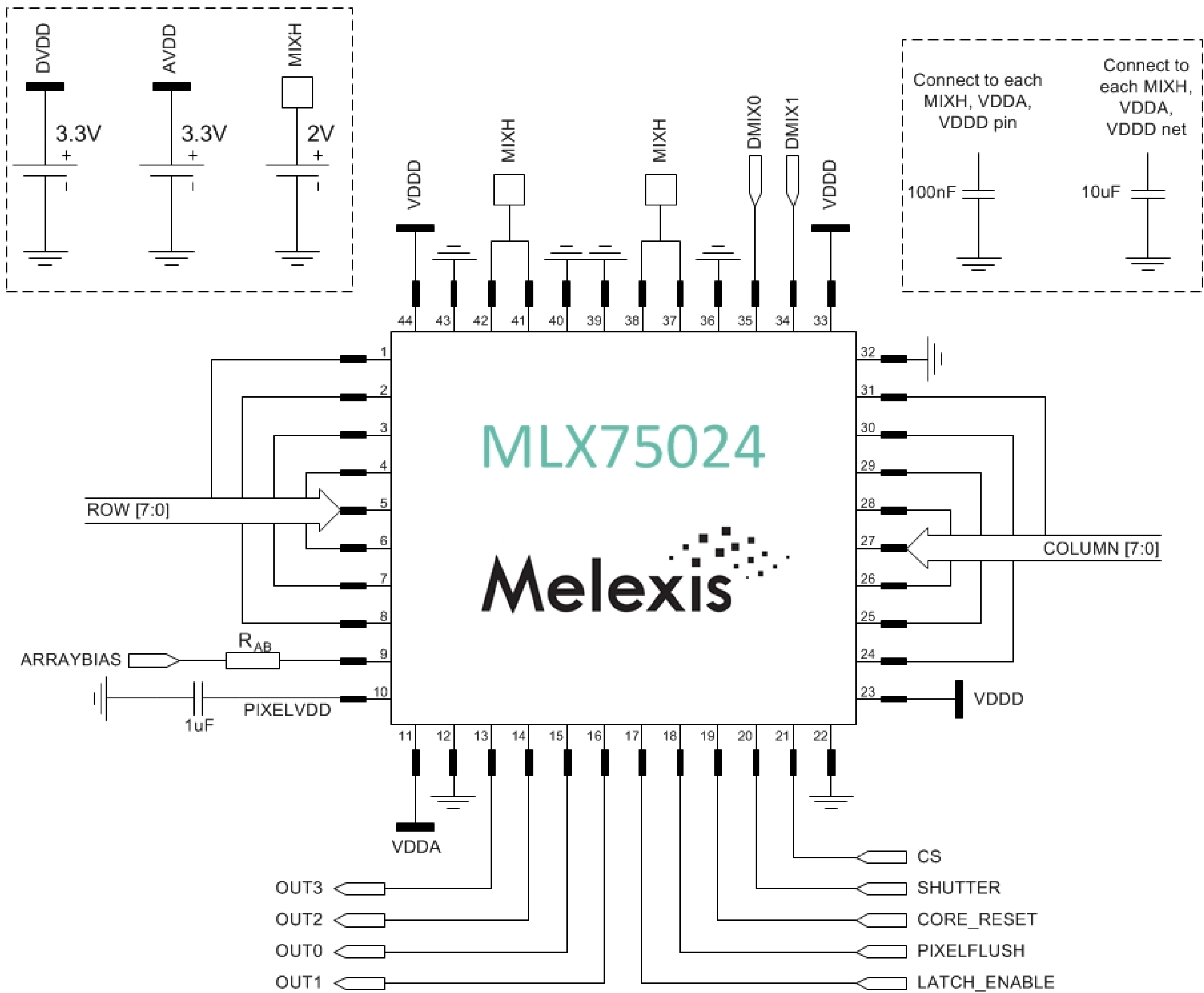


Figure 3: Typical connection diagram[2]

[2] R_{AB} value will influence the demodulation contrast of the sensor. We recommend using 68Ω resistor in combination with -3V3 ARRAYBIAS voltage for optimal performance.

7. Block diagram

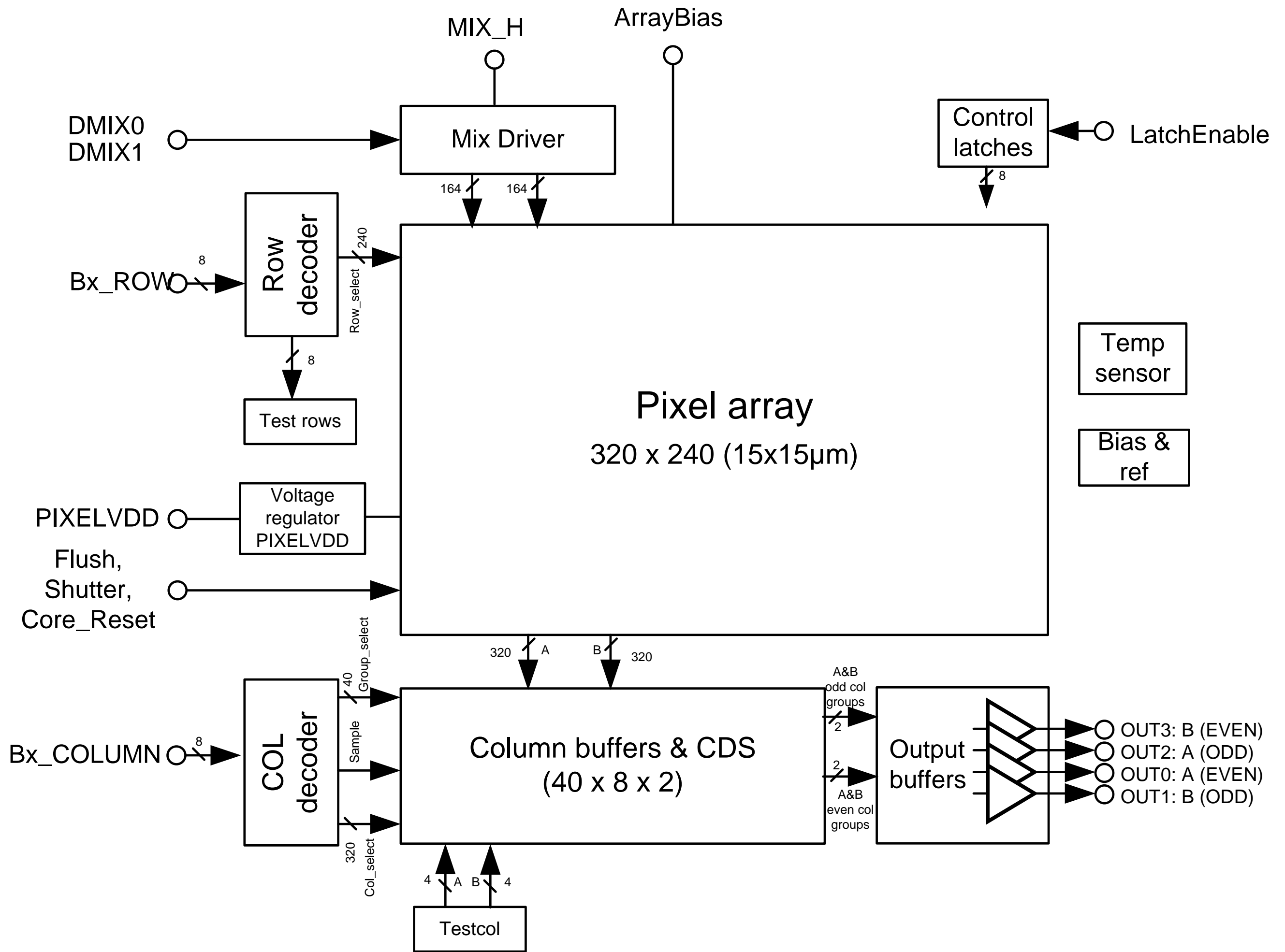


Figure 4: MLX75024 block diagram

8. Electrical Characteristics

8.1. Absolute Maximum Ratings[3]

Parameter	Symbol	Min.	Max.	Unit
3V3 supply voltage range	$V_{DD_33_X}$	-0.3	4.5	V
3V3 DC input voltage: $V_{DDA,}$ V_{DDD}	V_{DDX}	-0.3	4.5	V
MIXH input voltage : MIXH	V_{MIXH}		2.5	V
MIXH DC input current	I_{MIXH}		1000	mA
Storage temperature	T_{stg}	-50	125	°C
Junction temperature	T_J		125	°C

Table 6: Absolute maximum ratings[2]

8.2. Digital IO Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital input threshold level high	V_{IH}	0.7* V_{DDD}			V
Digital input threshold level low	V_{IL}			0.3* V_{DDD}	V
Input hysteresis	V_{HYST}	0.5			V
Digital input leakage current	I_{DIN}			1	µA
Digital input pin capacitance	C_{DIN}		10		pF
Pull down resistor at DMIX	R_{PD_MIX}		50		kΩ

Table 7: Digital IO characteristics

[3] Absolute maximum ratings must not be exceeded to prevent permanent damage to the device. The device is not guaranteed to be functional while applying the absolute maximum stress.

8.3. Current consumption in operating conditions

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
VDDA supply voltage		V_{DDA}	3.0	3.3	3.6	V
VDDA supply current	Integration	$I_VDDA_{INTEGRATION_CS_H}$		38		mA
VDDA supply current	Readout, slew rate = 0[4]	$I_VDDA_{READOUT_SR_L}$		47		mA
VDDA supply current	Readout, slew rate = 1[4]	$I_VDDA_{READOUT_SR_H}$		70		mA
VDDA supply current	Readout, CS low	$I_VDDA_{READOUT_CS_L}$		22		mA
VDDA supply current	Power down, DISABLE_VREG[5]	$I_VDDA_{POWER_DOWN}$		15		uA
VDDD supply voltage		V_{DDD}	3.0	3.3	3.6	V
VDDD supply current	During Idle time, after readout	I_VDDD_{IDLE}		2		µA
VDDD supply current	Integration, f_{MIX} = 20 MHz	$I_VDDD_{INTEGRATION_20MHZ}$		8	10	mA
VDDD supply current	Integration, f_{MIX} = 40 MHz	$I_VDDD_{INTEGRATION_40MHZ}$		16	20	mA
VDDD supply current	Readout	$I_VDDD_{READOUT}$		300		uA
ARRAYBIAS supply voltage		$V_{ArrayBias}$	-5	-3.3	0	V
ARRAYBIAS supply current	V_{MIXH} = 2V, $V_{ArrayBias}$ = -3V	$I_{ArrayBias}$		17	30	mA
MIXH supply voltage		V_{MIXH}	1.5	2	2.5	V
MIXH supply current	Integration, V_{MIXH} = 1.5V	$I_{MIXH_1.5V}$		480	900	mA
MIXH supply current	Integration, V_{MIXH} = 2V	$I_{MIXH_2.0V}$		720	1000	mA
MIXH supply current	Integration, V_{MIXH} = 2.5V	$I_{MIXH_2.5V}$		760	1100	mA
Junction temperature		T_{jnt}		125		°C
PIXELVDD voltage[6]	CDS_CTRL = 00b	PIX_{VDD_CDS1}		2.85		V
PIXELVDD voltage[6]	CDS_CTRL = 11b	$PIX_{VDD_CDS_bypass}$		2.7		V

Table 8: Electrical operation conditions

[4] See 9.1

[5] See 9.1

[6] PIXELVDD doesn't need to be provided externally. Values indicated here can be used when debugging to check if the sensor is working properly.

8.4. Dynamic Characteristics

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Column addressing frequency	Slew rate = 0[7]	f_{COL}			25[8]	MSPS
Column addressing frequency	Slew rate = 1[7]	f_{COL}			40	MSPS
Row addressing frequency		f_{ROW}			0.5	MSPS
DMIX frequency		f_{MIX}		20	40	MHz
Delay row/column to analog output settled	Slew rate = 0[7]	t_{VAL}		26	30	ns
Delay row/column to analog output settled	Slew rate = 1[7]	t_{VAL}		18.2	25	ns
Output ready after CS high		T_{SETTLE_CS}			60	ns
OUTx output swing		$RANGE_{OUT}$		1.55		V
OUTx output voltage		V_{OUT}	0		1.9	V
OUTx load capacitance		C_{OUT}		20	40[9]	pF

Table 9: Dynamic characteristics

8.5. Temperature sensor characteristics

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Gain of temperature sensor		K_{PTAT}	1.74	1.79	1.85	mV/K
Differential PTAT output voltage	Calibrated at 35°C	V_{PTAT}		563.5		mV
Temperature error with 35°C calibration	$T_{JUNCTION}$ = 35°C	$ERROR_{TEMP_35}$	-3.00		3.00	K
Temperature error with 35°C calibration	$T_{JUNCTION}$ = 85°C	$ERROR_{TEMP_85}$	-4.80		4.80	K
Temperature error with 35°C calibration	$T_{JUNCTION}$ = 105°C	$ERROR_{TEMP_105}$	-5.50		5.50	K
Temperature error with 35°C calibration	$T_{JUNCTION}$ = 0°C	$ERROR_{TEMP_0}$	-4.10		4.10	K
Temperature error with 35°C calibration	$T_{JUNCTION}$ = -40°C	$ERROR_{TEMP_-40}$	-5.50		5.50	K

Table 10: Temperature sensor characteristics

[7] See 9.1.

[8] Column addressing above 25 MHz can create image artefacts due to settling errors.

[9] Driving capability of the output buffer can be doubled using high power mode (OUT_DRIVE_2X), see 9.1 for more information.

8.6. Sensor Optical and Physical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External quantum efficiency	EQE_{850}	No optical BP filter, 850 nm		23		%
External quantum efficiency	EQE_{940}	No optical BP filter, 940 nm		13		%
DC contrast	C_{DC_850}	850 nm		95		%
AC contrast	$C_{AC_850_20MHz}$	20 MHz, 850 nm		87		%
AC contrast	$C_{AC_850_40MHz}$	40 MHz, 850 nm		84		%
DC contrast	C_{DC_940}	940 nm		95		%
AC contrast	$C_{AC_940_20MHz}$	940 nm, 20 MHz		87		%
AC contrast	$C_{AC_940_40MHz}$	940 nm, 40 MHz		85		%
Full well capacity	FWC	CDS_CTRL = 11b		458		ke-
Full well capacity	FWC	CDS_CTRL = 00b		483		ke-
Full well capacity	FWC	CDS_CTRL = 01b		246		ke-
Full well capacity	FWC	CDS_CTRL = 10b		137		ke-
Horizontal resolution	h			320		pixels
Vertical resolution	v			240		pixels
Pixel pitch	pp			15		µm
PDNU local	$PDNU_{LOCAL_20MHZ}$	20 MHz		0.38		cm
PDNU global	$PDNU_{GLOBAL_20MHZ}$	20 MHz		7.41		cm
PDNU local	$PDNU_{LOCAL_40MHZ}$	40 MHz		0.34		cm
PDNU global	$PDNU_{GLOBAL_40MHZ}$	40 MHz		9.5		cm
PNNU local	$PNNU_{LOCAL_20MHZ}$	20 MHz		1.2		%
PNNU global	$PNNU_{GLOBAL_20MHZ}$	20 MHz		7		%
PNNU local	$PNNU_{LOCAL_40MHZ}$	40 MHz		1.05		%
PNNU global	$PNNU_{GLOBAL_40MHZ}$	40 MHz		11.9		%

Table 11: Optical & physical characteristics

8.7. Signal Chain, Noise and Gain Modes Characteristics

Parameter	Symbol	Condition	Typ.	Unit
Camera gain	$C_GAIN_{CDS_bypass}$	CDS_CTRL = 11b	3.47	uV/e-
Camera gain	$C_GAIN_{CDS_1}$	CDS_CTRL = 00b	3.2	uV/e-
Camera gain	$C_GAIN_{CDS_2}$	CDS_CTRL = 01b	5.9	uV/e-
Camera gain	$C_GAIN_{CDS_3}$	CDS_CTRL = 10b	10.3	uV/e-
Dark voltage	$V_DARK_{CDS_bypass}$	CDS_CTRL = 11b, Hard Reset	1.75	V
Bright voltage	$V_BRIGHT_{CDS_bypass}$	CDS_CTRL = 11b, Hard Reset	0.2	V
Dynamic Range	$D_RANGE_{CDS_bypass}$	CDS_CTRL = 11b, Hard Reset	1.55	V
Dark voltage	$V_DARK_{CDS_1}$	CDS_CTRL = 00b	1.7	V
Bright voltage	$V_BRIGHT_{CDS_1}$	CDS_CTRL = 00b	0.2	V
Dynamic Range	$D_RANGE_{CDS_1}$	CDS_CTRL = 00b	1.5	V
Dark voltage	$V_DARK_{CDS_2}$	CDS_CTRL = 01b	1.65	V
Bright voltage	$V_BRIGHT_{CDS_2}$	CDS_CTRL = 01b	0.2	V
Dynamic Range	$D_RANGE_{CDS_2}$	CDS_CTRL = 01b	1.45	V
Dark voltage	$V_DARK_{CDS_3}$	CDS_CTRL = 10b	1.55	V
Bright voltage	$V_BRIGHT_{CDS_3}$	CDS_CTRL = 10b	0.2	V
Dynamic Range	$D_RANGE_{CDS_3}$	CDS_CTRL = 10b	1.35	V
Dark noise	DN_{CDS_bypass}	CDS_CTRL = 11b	130	e-
Dark noise	DN_{CDS_1}	CDS_CTRL = 00b	156	e-
Dark noise	DN_{CDS_2}	CDS_CTRL = 01b	135	e-
Dark noise	DN_{CDS_3}	CDS_CTRL = 10b	128	e-

Table 12 : Signal chain, noise and gain modes characteristics.

9. Device programming interface

9.1. Configuration latches

LATCH_ENABLE allows to program latches which control the general behaviour of the circuitry.

When LATCH_ENABLE is set to high, the pixel ROW and pixel COL inputs are the latch inputs, called ROW_LATCH_CONTROL and COLUMN_LATCH_CONTROL.

There exist 16 latches (8 on the row address lines and 8 on the column lines) which generally configure some functions of the device. The usage of the output latches are described in the following table:

Latch number	Function	
ROW_LATCH_CONTROL[7]	Reserved – Should be set to zero	Reserved
ROW_LATCH_CONTROL[6]	Reserved – Should be set to zero	Reserved
ROW_LATCH_CONTROL[5]	High slew rate mode of analog output buffer[10]	OUT_SR_2X
ROW_LATCH_CONTROL[4]	High power mode of analog output buffer[11]	OUT_DRIVE_2X
ROW_LATCH_CONTROL[3]	CDS control bit 1	CDS_CTRL<1>
ROW_LATCH_CONTROL[2]	CDS control bit 0	CDS_CTRL<0>
ROW_LATCH_CONTROL[1]	The first and last 4 column will be replaced by the test pixels	TEST_COLUMN_OUT
ROW_LATCH_CONTROL[0]	Power device down	POWER_DOWN

Table 13: Column Latch usage table

Latch number	Function	
COLUMN_LATCH_CONTROL[7]	Read the column backwards	REVERSE
COLUMN_LATCH_CONTROL[6]	Reset and start fuse readout[12]	FUSE_READOUT_LATCHED
COLUMN_LATCH_CONTROL[5]	Read the rows backwards	REVERSE_ROW
COLUMN_LATCH_CONTROL[4]	Reserved – Should be set to zero	Reserved
COLUMN_LATCH_CONTROL[3]	Reserved – Should be set to zero	Reserved
COLUMN_LATCH_CONTROL[2]	Reserved – Should be set to zero	Reserved
COLUMN_LATCH_CONTROL[1]	Reserved – Should be set to zero	Reserved
COLUMN_LATCH_CONTROL[0]	Reserved – Should be set to zero	Reserved

Table 14: Row Latch usage table

NB: An event at LATCH_EN might cause a change of operation mode (for instance power down) during normal application. It is recommended to initialize the image sensor after each frame read procedure to recover the system and set again the desired mode of operation.

[10] OUT_SR_2X must be used in case of f_{COL} > 25 MSPS. This will increase the power consumption of sensor by 10 mA.

[11] OUT_DRIVE_2X is used to double the driving capability of the output buffer in order to be able to drive 40 pF load compared to standard 20 pF load. It is necessary in situations where one MLX75123 companion chip is driving 2 MLX75024 sensors where PCB tracks load is expected to be higher than in standard mode.

[12] FUSE_READOUT_LATCHED triggers the read out of the FUSE. At the end of the read cycle, the FUSE read system is switched to power down mode. At minimum 64 clock cycles on ROW[1] (or two phases readout cycles) are required to complete one fuse cycle)

9.2. Control of the CDS function

CDS control bits 0 and 1 are used to select the gain of the CDS stage or bypass the CDS function depending of their values:

- CDS_CTRL<1:0> = 00b: CDS_mode = 1
- CDS_CTRL<1:0> = 01b: CDS_mode = 2
- CDS_CTRL<1:0> = 10b: CDS_mode = 3
- CDS_CTRL<1:0> = 11b: CDS function is bypassed or CDS_BYPASS = 1

10. Interface

10.1. Timing Diagrams[13]

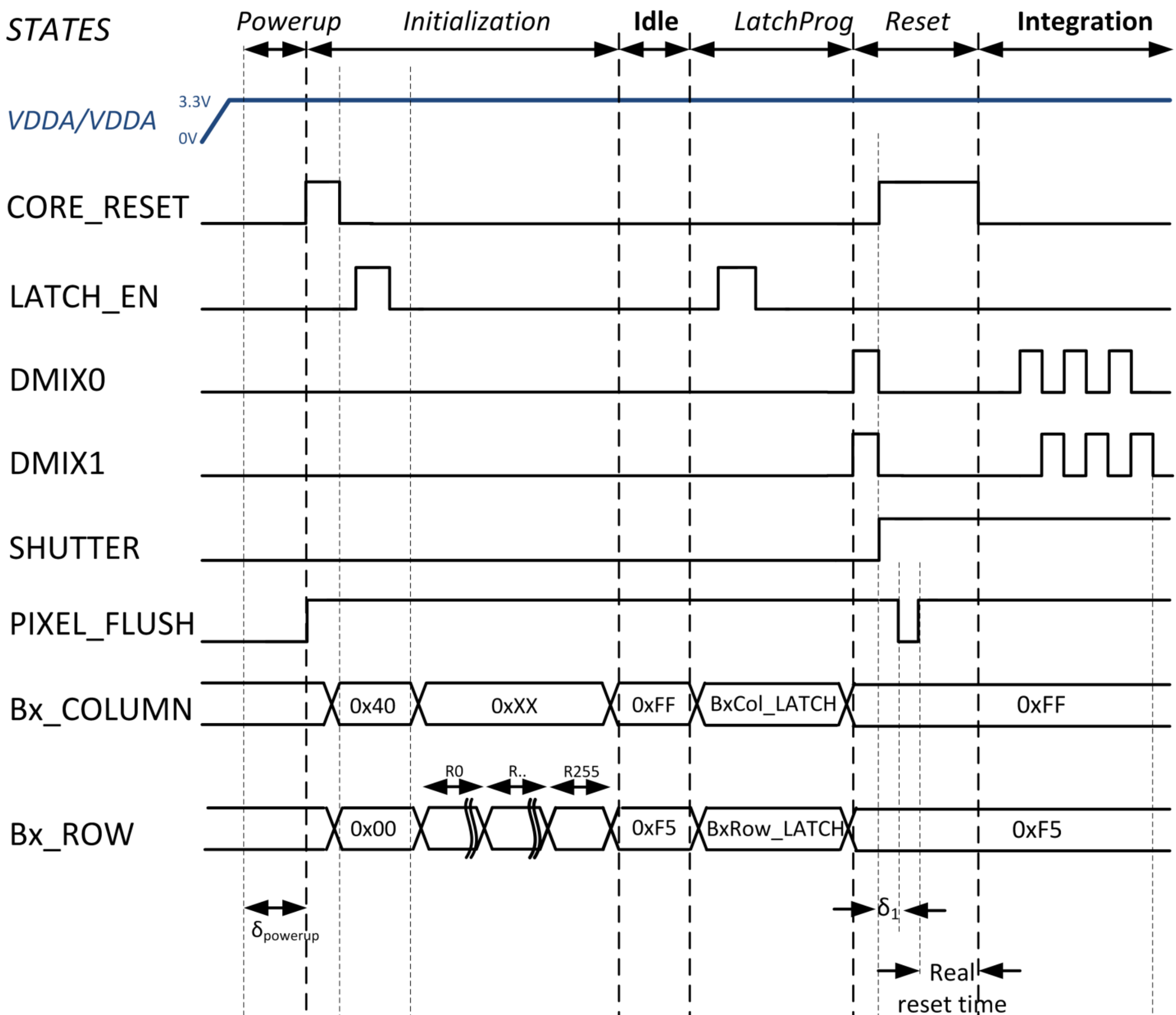


Figure 5: Global timing diagram from power up to integration. Each cycle consists of a reset phase, an integration phase and a read-out phase. $\delta 1 \geq 0.1us$, $\delta_{powerup} \geq 5ms$

[13] This timing diagram is a typical communication and timing flow for operation the MLX75024. The MLX75123BA is managing all these timings and durations automatically or by the use of programmable registers.

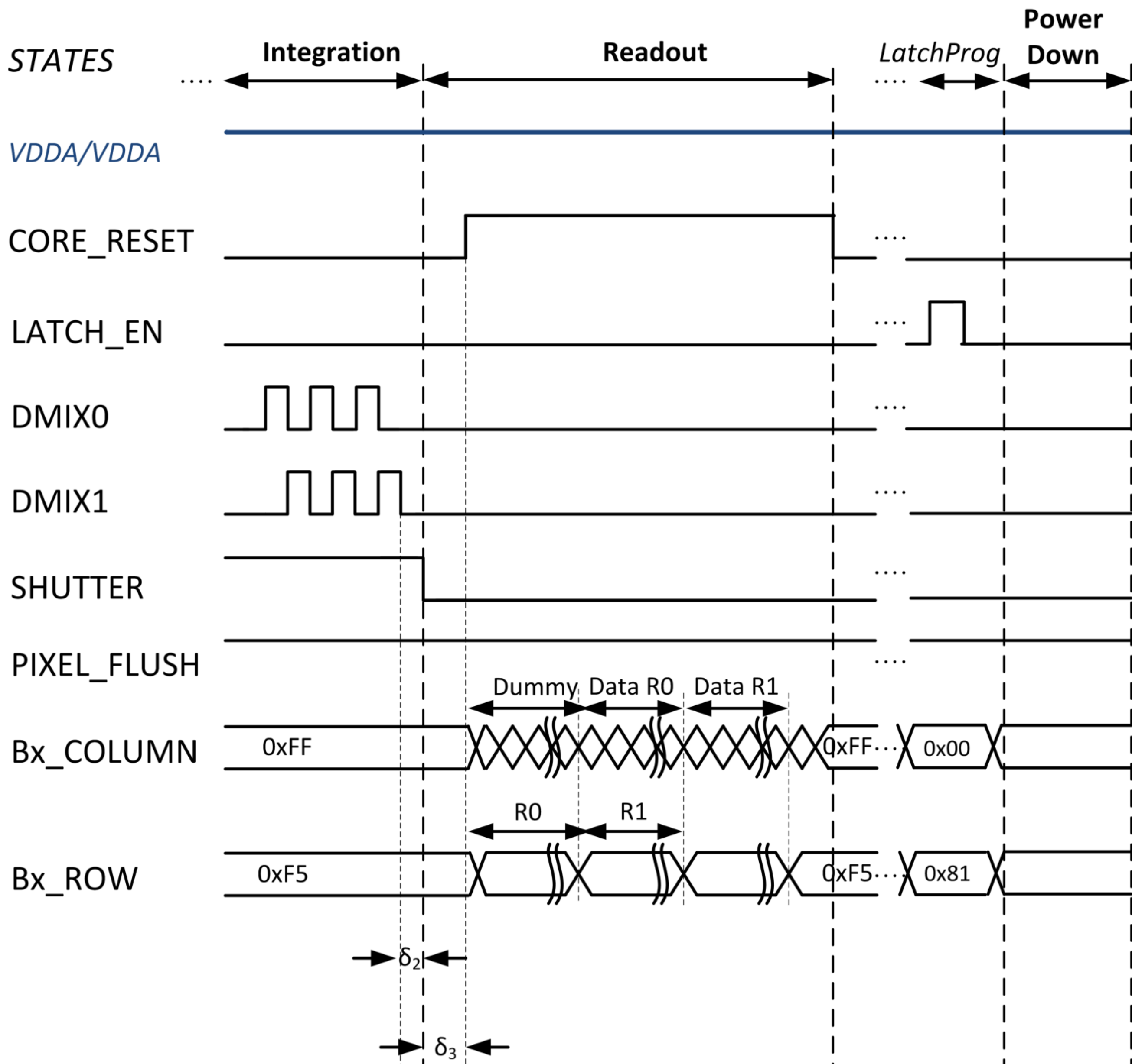


Figure 6: Global timing diagram from integration to power down. Each cycle consists of a reset phase, an integration phase and a read-out phase. $\delta 2 \geq 0.1us$, $\delta 3 \geq 1us$.

10.2. Power Up

The power up phase should last at least for 5ms after the supply reached the nominal value. This is indicated on the timing diagram by the $\delta_{powerup}$ value. After this power up phase, the MLX75024 will be able to be programmed using the LATCH values[14]. To initiate normal operating mode, a code of 0x00 should be applied to the ROW[X] bus and a code of 0x40 should be applied to the COL[X] bus at the falling edge of the LATCH_ENABLE signal.

ATTENTION: The first frame readout after power up contains invalid data thus should be discarded.

[14] See 9.1 for additional details about the programming of the device.

10.3. Latch Programming

Latch programming is used to change the behaviour of the MLX75024 by using the LATCH_ENABLE input. Latch programming phase should happen before integration. The CDS gain can be programmed during this phase, for example.

10.4. Reset

This Reset phase will happen at the beginning of every phase capture. The reset is organized in 3 steps. CORE_RESET is HIGH during all three steps. The electronic shutter should be opened by setting SHUTTER to HIGH.

- Step 1 : Substrate flush

During step 1, mix signals DMIX0 and DMIX1 are pulled HIGH for at least 100 ns.
The step ends by pulling DMIX0 and DMIX1 terminal LOW.

- Step 2 : Pixel flush

The second phase implements a flushed reset by switching PIXELFLUSH low during 5 us of CORE_RESET HIGH.

- Step 3 : Reset

The 3rd phase of the reset period lasts another 5 us, where the PIXELFLUSH is asserted.
During the 2nd and 3rd phase of the reset, DMIX0 and DMIX1 states should be LOW.

The real reset time is the time from the rising edge of the PIXEL_FLUSH until the falling edge of Reset. In application, the Reset should be programmed in such way that it is closest to:

$$\left(\frac{Total\ number\ of\ columns}{2} - 39\right) \times Column\ time$$

10.5. Integration

After the reset cycle, the integration cycle is started. The electronic shutter should be kept open (keep SHUTTER HIGH). The mix signals DMIX0/1 are alternated using the Time-of-Flight modulation pattern. When the integration is completed, the mix signals DMIX0/1 should be again put in idle state LOW. The electronic shutter can be closed by setting SHUTTER to LOW.

10.6. Read-out

Reading out the sensor is done by toggling both Row and Column address. Both addresses have 8 bit width. The Row binary word is directly mapped to the row number. The column binary word is toggled from 00h to 9Fh (0 to 159).

When row 0 is addressed the data from the pixels in row 0 is stored on a column-level memory Mem0. After this, row 1 is addressed and the data from the pixels in row 1 is stored in a second column-level memory Mem1. Simultaneously, after row 0 to row 1 transition, the data from row 0 previously stored in Mem0 can be read at the outputs OUT0 to OUT3 by selecting the columns sequentially. The Mem0-Mem1 shadow buffer switching is controlled by the B0_ROW signal; when reading out the matrix the B0_ROW signal must change its state every row.

When selecting column 0, OUT0 and OUT3 offer the data from pixel 0, while OUT1 and OUT2 offer the data from pixel 8. As such, the data is read out in blocks of 8. (Pixel 0 is located in the bottom right corner as indicated on Figure 16)
When selecting column 1, OUT0/3 offer the data from pixel 1, while OUT1/2 offer the data from pixel 9.
When selecting column 8, OUT0/3 offer the data from pixel 16, while OUT1/2 offer the data from pixel 24.
As such when selecting column N, the data at

OUT0/3 is coming from pixel (N MOD 8) + 16*FLOOR(N/8)
OUT1/2 is coming from pixel (N MOD 8) + 16*FLOOR(N/8) + 8

Parameter	OUT0/3 : Pixel #	OUT1/2 : Pixel #
0	0	8
1	1	9
…	…	…
6	6	14
7	7	15
8	16	24
9	17	25
…	…	…
15	23	31
16	32	40
17	33	41
…	..	…

Table 15: Read-out table

The row data can only be shifted out in the next row after it has been addressed. For CDS operation, the column signal needs to toggle in order to have CDS sampling working, so it is required to toggle the column already when addressing the first row (R0), even though there might be no meaningful data (Dummy) shifted out. This is not required in CDS_BYPASS mode.

The minimum number of columns which need to be read out is 160 columns in CDS mode. This is not required in CDS_BYPASS mode.

10.7. Test Rows Specification

MLX75024 has built in test patterns (The first 5 rows of the 8 test rows) that can be used to debug the analog to digital conversion or verify if the chipset and communication between the MLX75024 and the MLX75123 is working properly. Test rows are always enabled and can be read-out and addressed like any other pixel row. Test rows contain a chess pattern corresponding for each pixel to the value of the COL[X] signal for that pixel (high or low):

Row No.		Col 0	Col 1	…	Col 255	Col 256	Col 257	…	Col319
240	Tap A	!COL[0]	!COL[0]	…	!COL[0]	!COL[0]	!COL[0]	…	!COL[0]
241	Tap A	COL[1]	COL[1]	…	COL[1]	COL[1]	COL[1]	…	COL[1]
242	Tap A	COL[3]	COL[3]	…	COL[3]	COL[3]	COL[3]	…	COL[3]
243	Tap A	COL[5]	COL[5]	…	COL[5]	COL[5]	COL[5]	…	COL[5]
244[15]	Tap A	COL[7]	COL[7]	…	COL[7]	COL[7]	COL[7]	…	COL[7]
240	Tap B	COL[8]	COL[8]	…	COL[8]	COL[8]	COL[8]	…	COL[8]
241	Tap B	COL[0]	COL[0]	…	COL[0]	COL[0]	COL[0]	…	COL[0]
242	Tap B	COL[2]	COL[2]	…	COL[2]	COL[2]	COL[2]	…	COL[2]
243	Tap B	COL[4]	COL[4]	…	COL[4]	COL[4]	COL[4]	…	COL[4]
244[9]	Tap B	COL[6]	COL[6]	…	COL[6]	COL[6]	COL[6]	…	COL[6]

Table 16: Test row description

[15] Test row 244 test pattern can only be read-out in reverse mode using the REVERSE_ROW option setting the COLUMN_LATCH_CONTROL[5] to 1. See 8.1.1 for additional information.

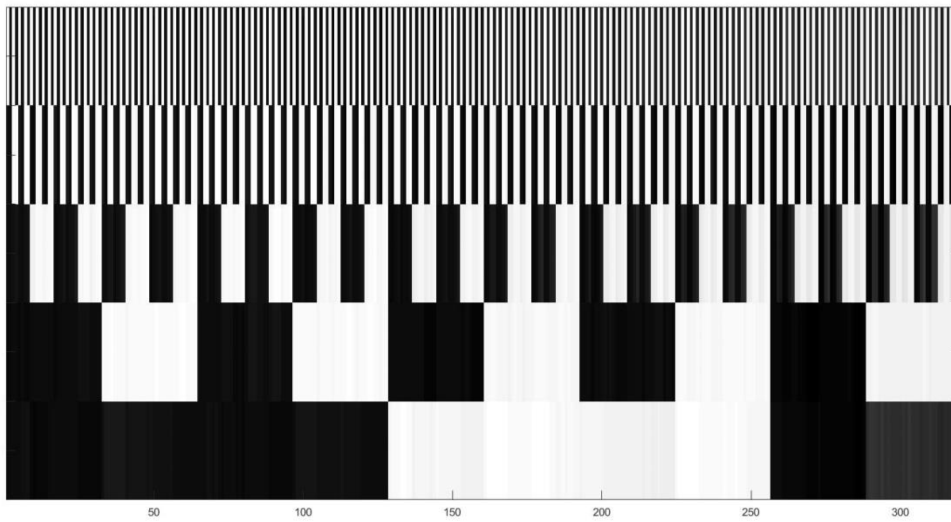


Figure 7 : Raw tap A image of the test rows readout in reverse mode. Top row being row 240, bottom one being row 244.

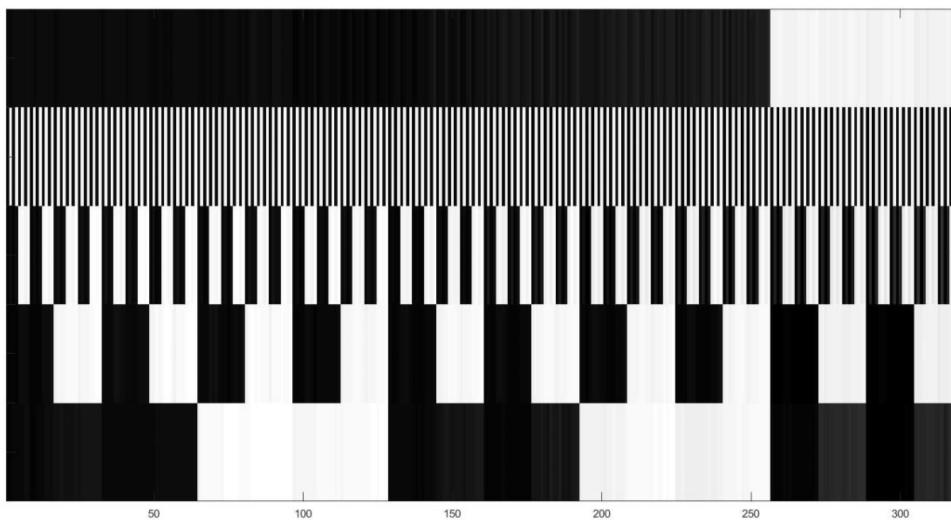


Figure 8: Raw tap B image of the test rows readout in reverse mode. Top row being row 240, bottom one being row 244.

10.8. Test Columns Specification

When TEST_COLUMN_OUT (ROW_LATCH_CONTROL[1], see 9.1) is high the first 4 columns of the array will be switched into the row ID addresses, or the row number presented in a binary way. It is used to test the row decoder.

The last 4 columns of the pixel array will also be switched into the row ID addresses, or the row number presented in a binary way. It is used to test the row decoder. The reason to duplicate this is to be able to read the pattern with another set of the output buffers.

Col No.		Row 0	Row 1	...	Row 200	Row 201	Row 202	...	Row 239
0	Tap A	ROW[1]	ROW[1]	...	ROW[1]	ROW[1]	ROW[1]	...	ROW[1]
1	Tap A	ROW[3]	ROW[3]	...	ROW[3]	ROW[3]	ROW[3]	...	ROW[3]
2	Tap A	ROW[5]	ROW[5]	...	ROW[5]	ROW[5]	ROW[5]	...	ROW[5]
3	Tap A	ROW[7]	ROW[7]	...	ROW[7]	ROW[7]	ROW[7]	...	ROW[7]
316	Tap A	ROW[1]	ROW[1]	...	ROW[1]	ROW[1]	ROW[1]	...	ROW[1]
317	Tap A	ROW[3]	ROW[3]	...	ROW[3]	ROW[3]	ROW[3]	...	ROW[3]
318	Tap A	ROW[5]	ROW[5]	...	ROW[5]	ROW[5]	ROW[5]	...	ROW[5]
319	Tap A	ROW[7]	ROW[7]	...	ROW[7]	ROW[7]	ROW[7]	...	ROW[7]

Col No.		Row 0	Row 1	...	Row 200	Row 201	Row 202	...	Row 239
0	Tap B	ROW[0]	ROW[0]	...	ROW[0]	ROW[0]	ROW[0]	...	ROW[0]
1	Tap B	ROW[2]	ROW[2]	...	ROW[2]	ROW[2]	ROW[2]	...	ROW[2]
2	Tap B	ROW[4]	ROW[4]	...	ROW[4]	ROW[4]	ROW[4]	...	ROW[4]
3	Tap B	ROW[6]	ROW[6]	...	ROW[6]	ROW[6]	ROW[6]	...	ROW[6]
316	Tap B	ROW[0]	ROW[0]	...	ROW[0]	ROW[0]	ROW[0]	...	ROW[0]
317	Tap B	ROW[2]	ROW[2]	...	ROW[2]	ROW[2]	ROW[2]	...	ROW[2]
318	Tap B	ROW[4]	ROW[4]	...	ROW[4]	ROW[4]	ROW[4]	...	ROW[4]
319	Tap B	ROW[6]	ROW[6]	...	ROW[6]	ROW[6]	ROW[6]	...	ROW[6]

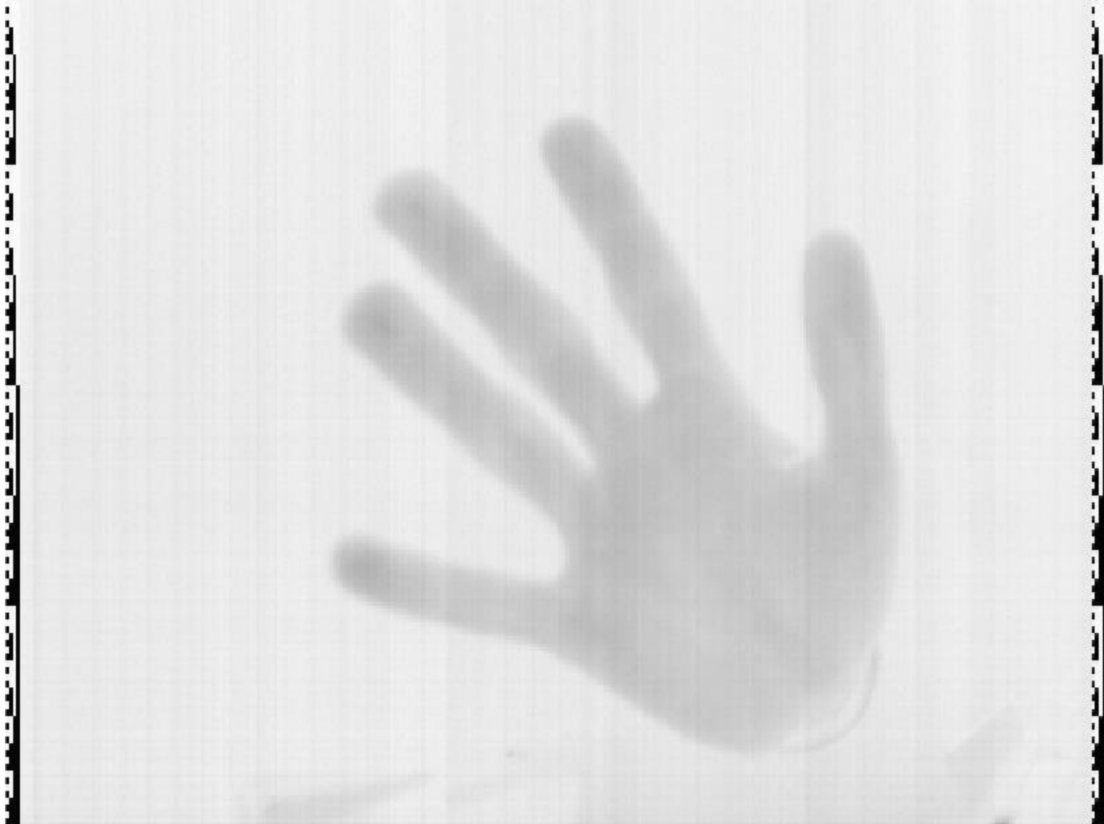
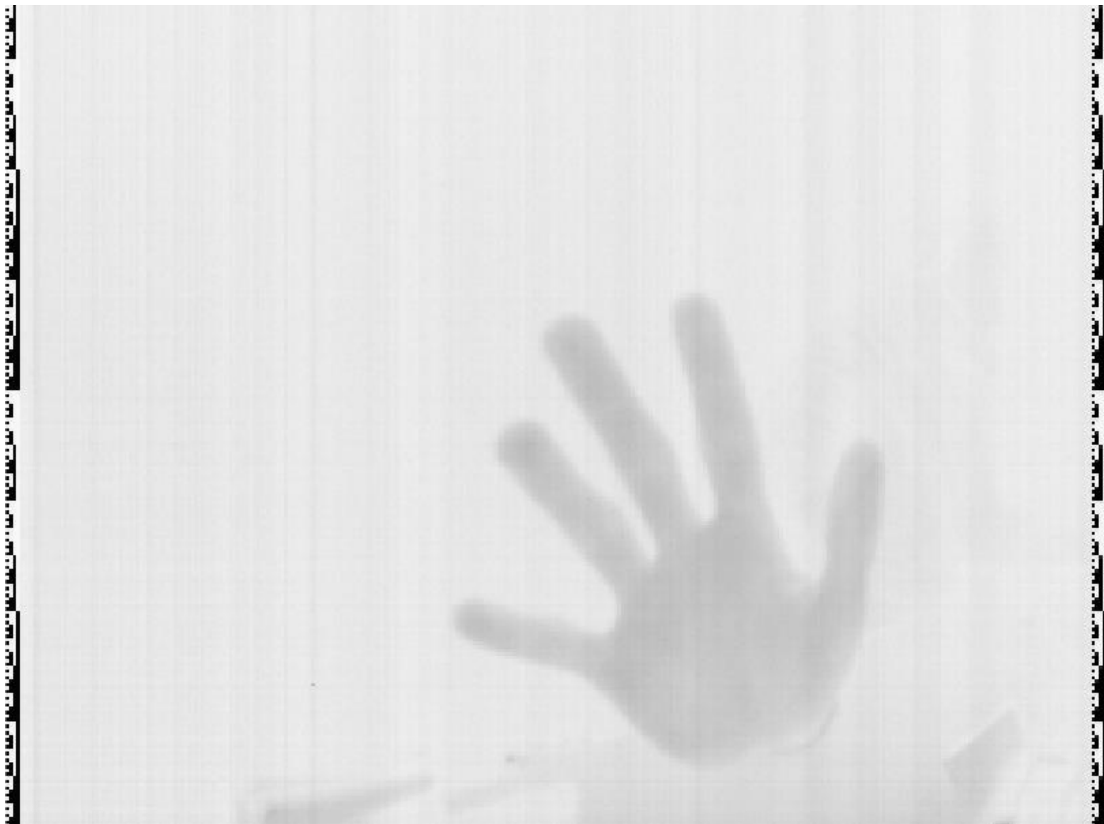


Figure 9: Raw tap A image with visible test columns.

Figure 10: Raw tap B image with visible test columns.



11. Recommendations for EMC

In order to improve further the electromagnetic compatibility of the sensor used together with the MLX75123 TOF companion chip, some additional recommendations could be applied:

Pin designator	Pin number	Recommendation	Capacitors values
VDDA	11	Decoupling	100nF &10 nF & 1 nF
PIXELVDD	10	Decoupling	100nF & 10 nF & 1 nF
ARRAYBIAS	9	Decoupling	100nF & 10 nF & 1 nF
VDDD	23	Decoupling	100 nF & 10 nF
VDDD	44	Decoupling	10 nF & 1 nF
MIXH	41, 42	Decoupling to DGND pin 43	10 uF, 100nF &10 nF & 1 nF
MIXH	37, 38	Decoupling to DGND pins 36 and 39	10 nF & 1 nF

Additional recommendations:

- Using a power plane for 3V3 power supply.
- Using the top layer for digital and analog grounds, and avoiding vias to connect ground pins of the image sensor.
- Use vias to route power supply to top layer.
- Place decoupling capacitors as close as possible to VDDD pins, with the lowest capacitance closest to the pin.
- Use 0201 components for 1 nF and 10 nF decoupling capacitors if possible.

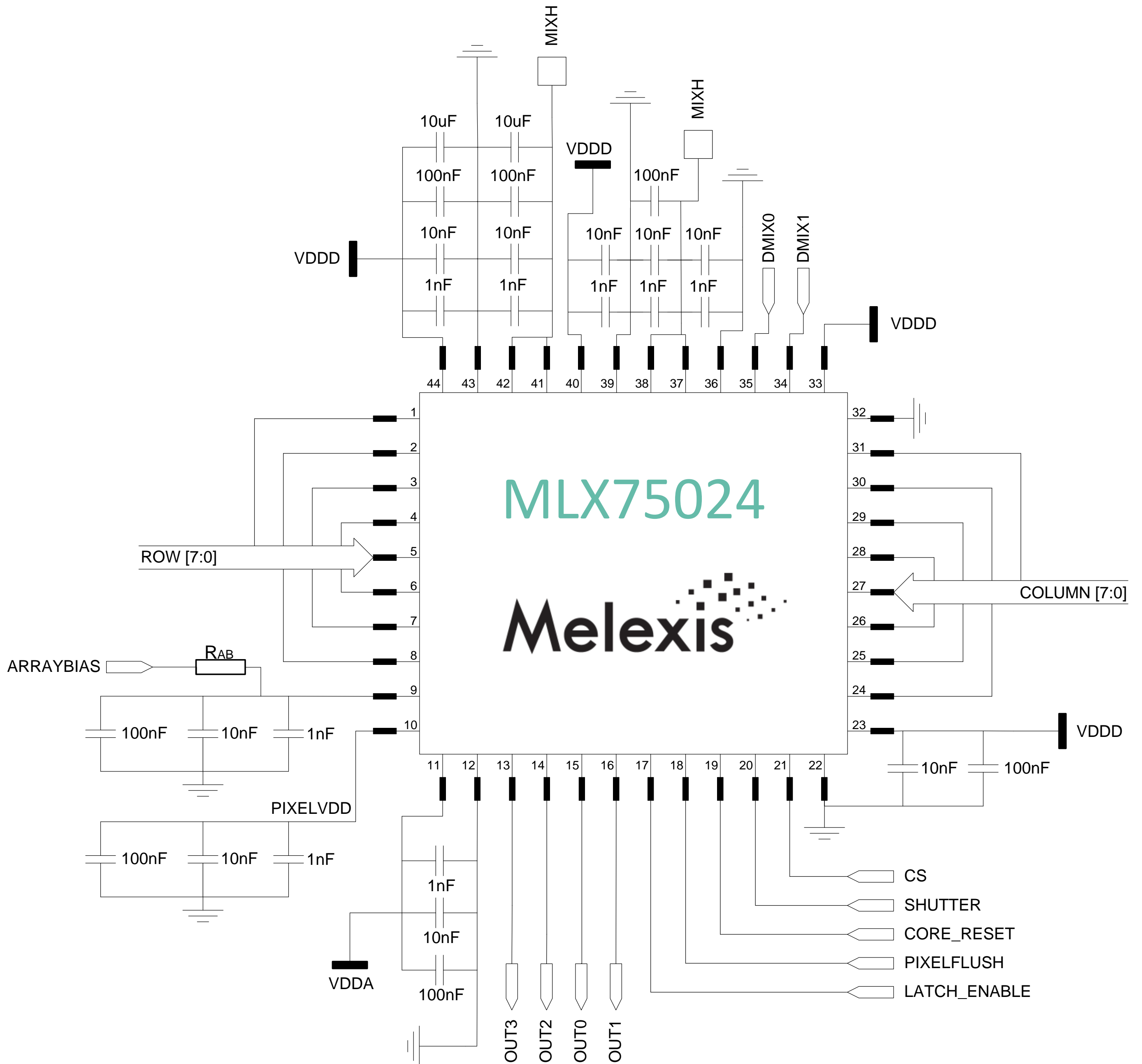


Figure 11: Recommended connection diagram for high EMC performance.

12. Depth & Confidence Calculation

12.1. Correlation Measurement

A depth and confidence measurement can be realized by a sequence of 4 correlation measurements, followed by a digital processing step. In one implementation, a single correlation measurement is realized by synchronous demodulation of the light signal of the active illumination source: during the integration time T_{int}, the active illumination source should be turned on while the TOF pixel responsivity and the light signal are amplitude modulated at a frequency f_{MIX}. Between the illumination source and the TOF pixel modulation signal, a fixed phase delay $\phi \in \{0, 180, 90, 270\}$ degrees should be applied per correlation measurement. After each integration time, the light source should be switched off to cool down for a time $T_{cooldown}$. During this cool down time, there is a time T_{read} to read out the TOF pixel correlation values S_{ϕ}. In an N-tap TOF pixel design, multiple correlations $S_{k,\phi}$, where $k \in 1..N$ can be measured in parallel.

Figure 12 shows the sequence of 4 correlation measurements and the synchronization between the pixel and active illumination timings.

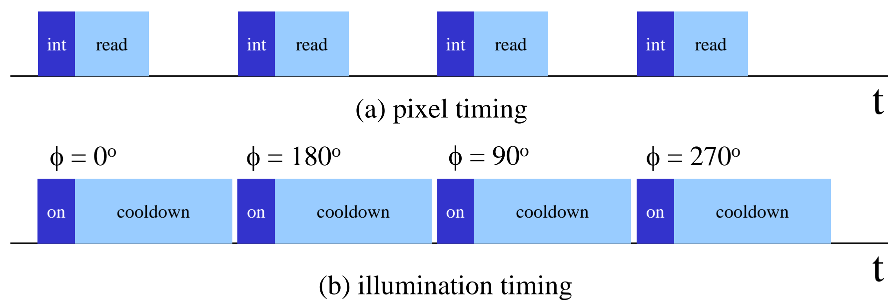


Figure 12: Pixel and illumination timing sequence(s)

The MLX75024 features a two-tap TOF pixel design. One tap measures the in-phase correlation, while the other tap measures the counter phase correlation. Following the described sequence, there will be 8 correlation values available per depth measurement sequence, per pixel: $S_{k,\phi}$ where $k \in \{0,1\}$ denotes the in-phase and counter phase correlation respectively, and $\phi \in \{0, 180, 90, 270\}$.

The MLX75024 features two dual-ended outputs. The dual ended output terminal pairs are (OUT0, OUT3) and (OUT1, OUT2). During readout of the sensor, each dual ended pair will output the voltages of a two-tap pixel. Each output pair can be assigned to readout one half of the pixel array. For columns 0 … 7, 16 … 23, … :

$$OUT_0 \rightarrow S_{0,\phi}$$

$$OUT_3 \rightarrow S_{1,\phi}$$

For columns 8 … 15, 24 … 33, … :

$$OUT_1 \rightarrow S_{1,\phi}$$

$$OUT_2 \rightarrow S_{0,\phi}$$

The MLX75024 features digital mix input terminals DMIX0 (pin 35) and DMIX1 (pin 34). During the integration time T_{int}, the modulation reference signal should be applied differentially to these terminals. During the remainder of the time, the timing requirements as detailed in Section 10.1 should be followed.

12.2. Active Illumination

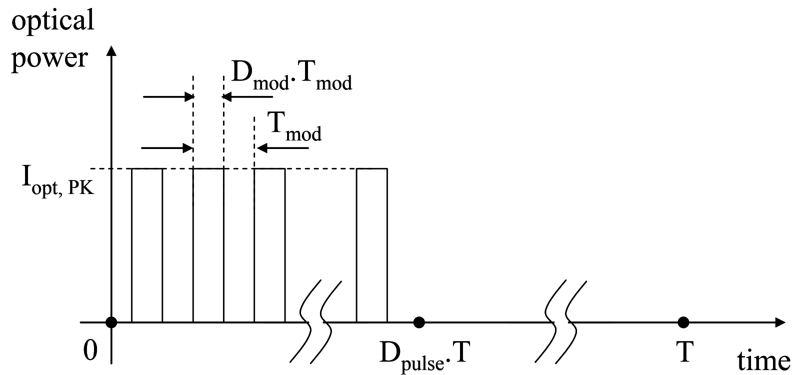


Figure 13: Active illumination waveform

A typical active illumination waveform is shown in Figure 13. The waveform consists of two parts: during the first, a pulse train of active illumination is emitted and during the second, no active light is emitted. During this time, the active light source can cool down and the pixel values can be read out.

The symbols in the graph have the following meaning:

- T is the time between consecutive measurements
- D_{pulse} is the ratio between the time that active pulses should be emitted and the total time of the measurement
- T_{mod} is the duration of each active pulse
- D_{mod} is the ratio between the duration of an active pulse and the time between consecutive pulses
- $I_{opt,PK}$ is the peak optical power or intensity level of the active pulse
- The average optical power or intensity $I_{opt,AVG}$ can be calculated as
- $I_{opt,AVG} = I_{opt,PK} * D_{mod} * D_{pulse}$
- The average duty cycle $D_{mod} * D_{pulse}$ should be chosen such that the active illumination can operate reliably i.e. does not exceed its critical temperature, while aiming for maximum peak power $I_{opt,PK}$ to achieve the best measurement SNR in high ambient light conditions.

Referring to Section 12.1, we note that:

- The integration time T_{int} equals $D_{pulse} * T$
- The cool down time $T_{cooldown}$ equals $\left(1 - D_{pulse}\right) * T$

- The modulation frequency f_{MIX} equals $1/T_{mod}$
- The modulation duty cycle D_{mod} equals 50% in case of square wave or sine modulation

12.3. Depth and Confidence Calculation

The depth data per pixel in degrees can be calculated by following formula

$$\phi = \begin{cases} 90 * (1 - x) & \text{if } y < 0 \\ 90 * (3 + x) & \text{if } y \geq 0 \end{cases}$$

Where x, y are average quadrature values calculated as:

$$x = \frac{X_0}{2N_0} - \frac{X_1}{2N_1}$$
$$y = \frac{Y_0}{2N_0} - \frac{Y_1}{2N_1}$$

Where X_0, Y_0, N_0 and X_1, Y_1, N_1 are the quadrature and norm values measured by the first and second pixel tap, respectively. They can be calculated from the correlation values by following formula:

$$X_k = S_{k,0} - S_{k,180}$$

$$Y_k = S_{k,270} - S_{k,90}$$

$$N_k = |X_k| + |Y_k|$$

Where $k \in \{0,1\}$ is the pixel tap index. A good measure of the depth value confidence is the total norm $N_0 + N_1$.

13. Package and Handling

13.1. Mechanical Dimensions

To avoid dust accumulation, scratches or other sources of damage during component storage, logistics or the assembly process(es) we offer product variants that include a plastic cover tape to protect the sensitive area of the sensor.
In order to focus the lens over the sensor and capture the light in the most efficient way it's important to have the sensor sensitive part at the focal length of the lens. The top of the glass package is not directly the sensitive area of the pixel which is around 550 microns under the top surface of the sensor (not visible in Figure 14 below).

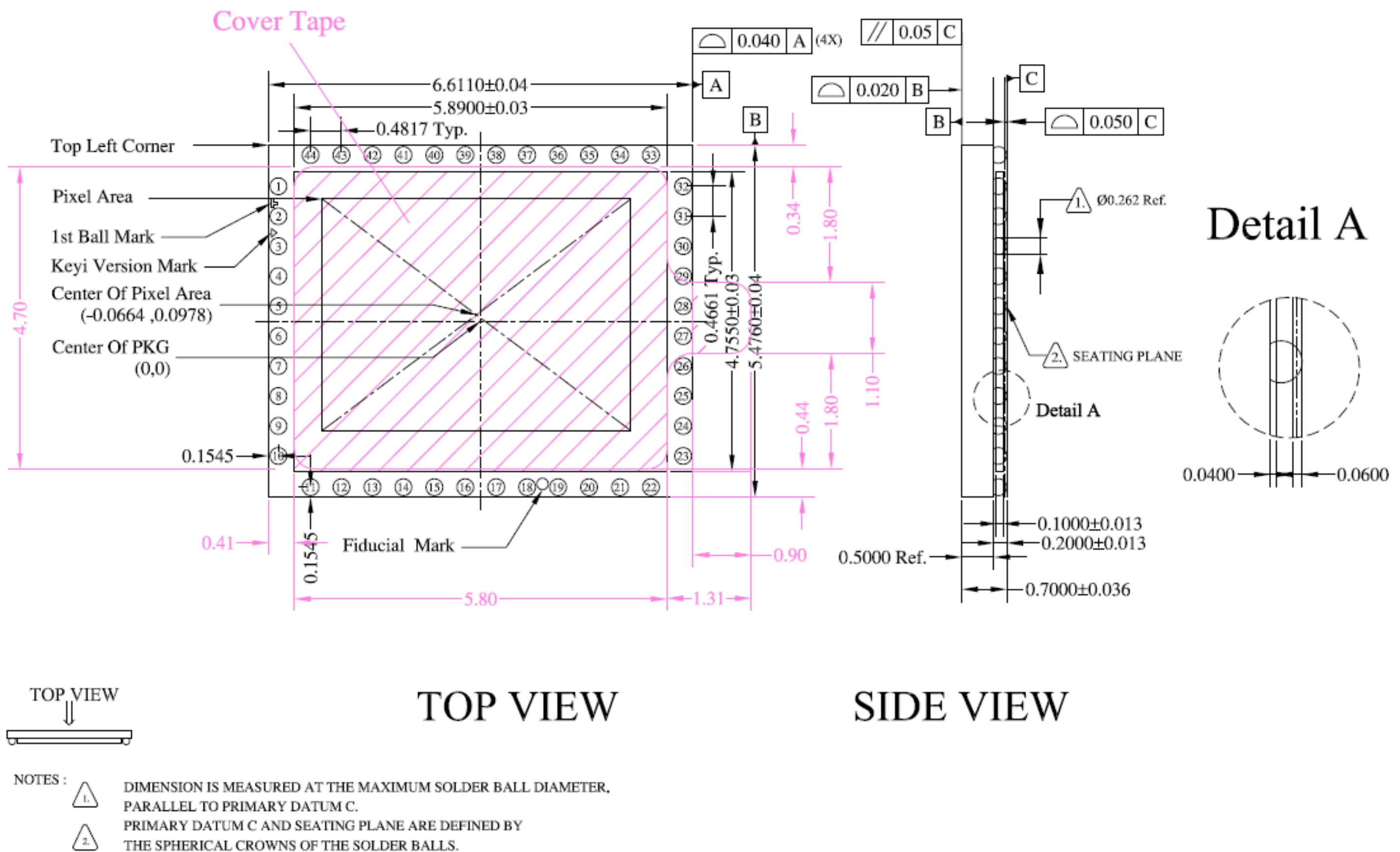


Figure 14: Mechanical dimensions

13.2. PCB Footprint Recommendations

It’s recommended to use NSMD (Non Solder Mask Defined) type of pads on the PCB. In order to prevent the solder balls of the sensor to get in contact with each other after reflow, it’s also recommended to shift the solder ball pads 50 um outward from the package position, as illustrated in Figure 15 and Figure 16.

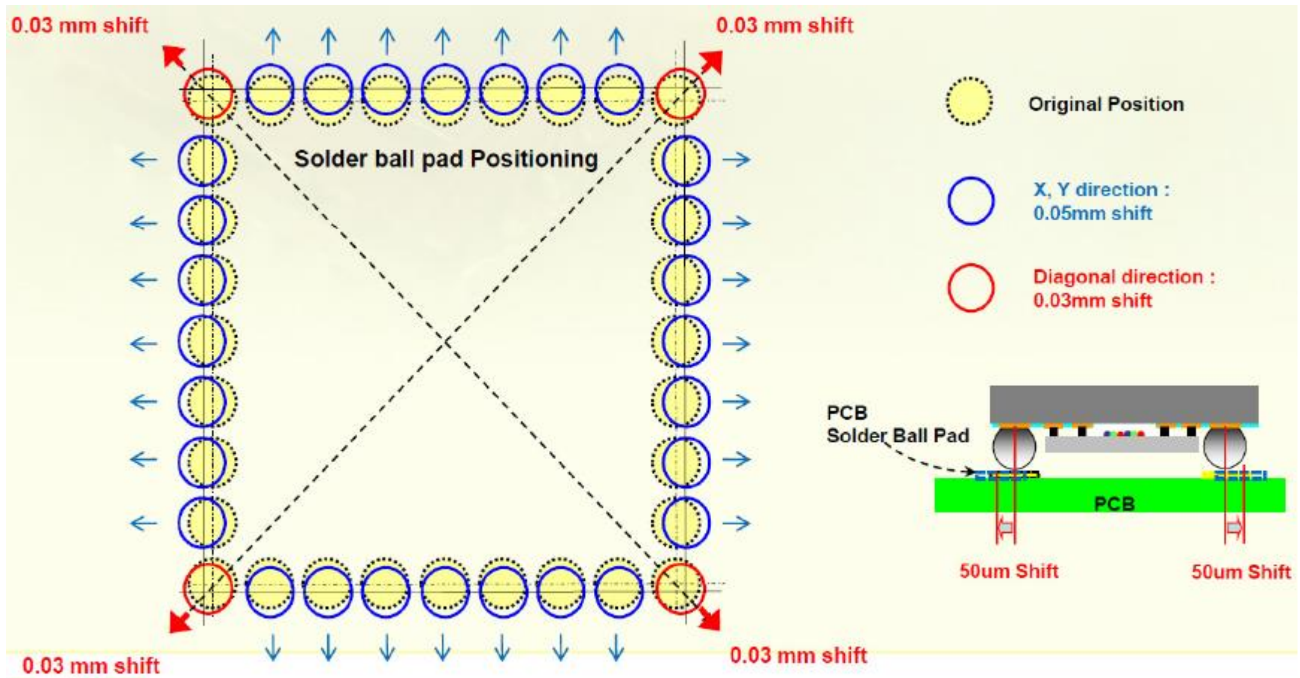


Figure 15: Recommended solder pad shift

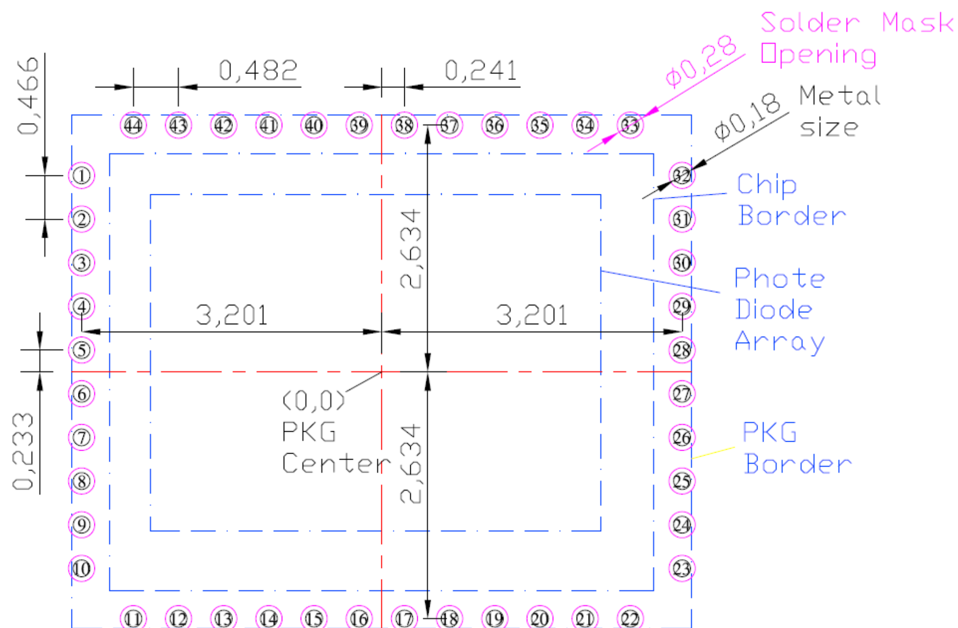


Figure 16: Recommended PCB land pattern (dimensions in mm), Pixel (0,0) is located on the top right corner of the pixel array here, close to pin 31.

13.3. PCB Trace Layout Recommendation

It is mandatory to route the traces connected to the solder balls outside of the solder ball perimeter (see Figure 17, left). In case that traces should be routed inside of the solder ball perimeter, the trace angle should be greater than 45 deg (see Figure 17, right). It is recommended to use NSMD (none solder mask defined) type of pads.

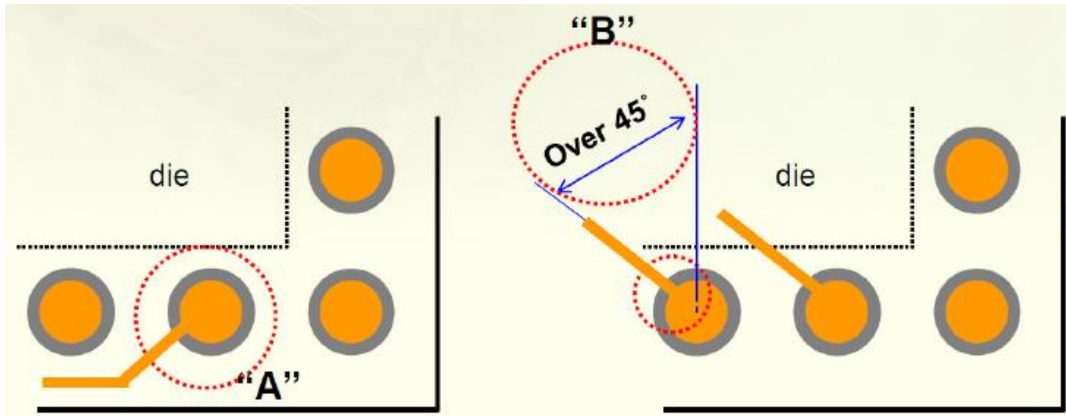


Figure 17: Recommended trace layout

13.4. Sensor Reflow Profile

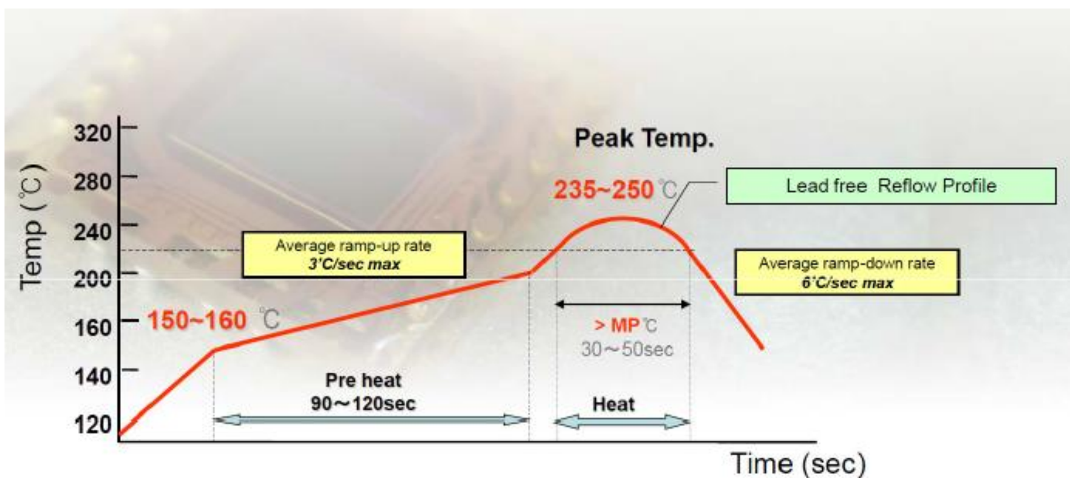


Figure 18: Recommended reflow profile

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