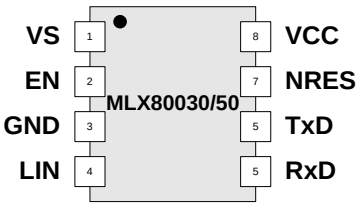
MLX80050/51/30/31

LIN System Basis ICs

Datasheet

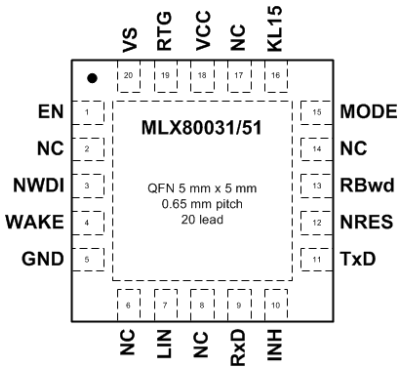


Features

- LIN 2.x / SAE J2602 compliant
- Operating voltage V_{SUP} = 5 ... 27 V
- 3 modes: Normal, Silent and Sleep
- Linear low drop voltage regulator:

  MLX80030/31:
  - Normal mode 3.3V/70mA ±2%
  - Silent mode 3.3V/20mA ±2%

  MLX80050/51:
  - Normal mode 5V/70mA ±2%
  - Silent mode 5V/20mA ±2
- Low current consumption (typ)
  - Sleep mode 20 µA
  - Silent mode “noload” 45 µA
- Output current limitation
- LIN-Bus Transceiver
  - Baud rate up to 20 kBaud
  - Slew rate control for best EME behaviour
  - Low slew mode for optimized SAE J2602 transmission
  - High impedance LIN pin in case of loss of ground or battery
- Remote and local wake up source recognition
- VCC undervoltage detection at NRES output (start-up delay 4ms)
  - Vres threshold 3.0 V (MLX80030/31); Vres threshold 4.1V (MLX80050/51)
- Programmable Window Watchdog (only MLX80031/51)
- VSUP undervoltage detection (POR), Over temperature shutdown
- TxD dominant time out function, Standby mode time out after 350ms
- Automotive temperature range of –40°C to 125°C
- Interface I/O’s independent from voltage regulator output
- Enhanced ESD robustness according to IEC 61000-4-2
  - Direct discharge for pin LIN >20kV (only Lin cap connected) and for pin VBAT >15kV
  - Indirect discharge for pin LIN >15kV
- Load dump protected (40V)



Order Code	Temp. Range	Package	Delivery	Remark
MLX80050KDC-CAA-100-RE	-40 - 125 °C	SOIC8	Reel	Silent Mode enabled
MLX80051KLW-CAA-100-RE	-40 - 125 °C	QFN_WF20/5x5	Reel	Silent Mode enabled
MLX80030KDC-CAA-100-RE	-40 - 125 °C	SOIC8	Reel	Silent Mode enabled
MLX80031KLW-CAA-100-RE	-40 - 125 °C	QFN_WF20/5x5	Reel	Silent Mode enabled

Short Description

The MLX8005x/3x consist of a low-drop voltage regulator 5V/3.3V/70mA combined with a Reset/Watchdog unit and a LIN bus transceiver. The LIN transceiver is suitable for LIN bus systems conform to LIN specification revision 2.x and SAE J2602. The watchdog times of the integrated window watchdog can be adapted on application needs via external resistors. With the help of an external bipolar transistor it is possible to extend the output current of the integrated voltage regulator. The combination of voltage regulator and bus transceiver as well as watchdog unit makes it possible to develop simple, but powerful and cheap slave nodes in LIN Bus systems.

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All voltages are referenced to ground (GND), positive currents flow into the IC.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage at VS	V_S	Respective to GND	-0.3	40	V
Transient voltage ISO 7637/2		pulse 1, 2	-100	100	V
Transient voltage ISO 7637/2		pulse 3A; 3B, coupling 1nF	-150	100	V
DC voltage LIN	V_{LIN_DC}	Respective to GND and VS Loss of Ground (VGND = VS)	-20 -30	40 40	V
DC voltage WAKE	V_{WAKE_DC}	Respective to GND and VS Loss of Ground (VGND = VS)	-20 -30	40 40	V
DC voltage INH	V_{INH_DC}		-0.3	V_S+0.3	V
DC voltage VCC	V_{VCC_DC}		-0.3	7	V
DC voltage RTG	V_{RTG_DC}		-0.3	7	V
Input voltage at low voltage I/O's (EN, TxD, RxD, NRES, WDI, RB_{WD}, MODE)	V_{IN}		-0.3	7	V
ESD voltage	V_{ESDIEC}	IEC 61000-4-2, direct ESD Pin LIN with LIN cap 220pF Pin VS to GND	20 15		kV
	$V_{ESDIECind}$	IEC 61000-4-2, indirect ESD Pin LIN with LIN cap 220pF	15		kV
	V_{ESDHBM}	HBM (CDF-AEC-Q100-002) Pin LIN Pin WAKE, KL15, VS Other pins	 ±6 ±4 ±2		 kV kV kV
	V_{ESDCDM}	CDM (AEC-Q100-011)	±500		V
Power dissipation	P_0		Internal limited, see also chapter 9.1		
Thermal resistance from junction to ambient	R_{THJA_SOIC8}	JEDEC 1s0p board, no air flow		150	K/W
	R_{THJA_QFN20}	JEDEC 1s0p board, no air flow		50	K/W
Junction temperature	T_J		-40	150	°C
Storage temperature	T_{STG}		-55	150	°C

Table 1: Absolute maximum ratings

3.1. DC Characteristics

Unless otherwise specified all values in the following tables are valid for V_S = 5 to 27V and T_{AMB} = -40 to 125°C. All voltages are referenced to ground (GND), positive currents flow into the IC.
For MLX80031/51 apply: RTG connected to VCC.

Table 2: Voltage Regulator and Reset Unit

	Parameter	Symbol	Condition	Min	Typ	Max	Unit	T[1]
Supply Voltage Pin VS								
	Nominal DC operating voltage	V_S		5		27	V	A
1.01	V_S under voltage reset	V_{SUVR_OFF}	V_S ramp up	4.1		5.0	V	A
1.02	V_S under voltage reset	V_{SUVR_ON}	V_S ramp down	3.7		4.8	V	A
1.03	V_S under voltage reset hysteresis	V_{SUVR_HYS}	V_{SUVR_OFF} - V_{SUVR_ON}	0.04	0.3	0.7	V	A
Supply currents MLX80030, MLX80050								
2.00	Supply current, normal mode	I_{VS_nor}	$V_S \leq$ 14V, V_{EN} > 2V , LIN recessive, no load at VCC	400	750	1500	µA	A
2.01	Supply current, sleep mode	I_{VS_sleep}	$V_S \leq$ 14V T_A = -40 °C T_A = 25 °C $T_A \leq$ 85 ° C $T_A \leq$ 125 °C		15	 30 20 30 45	µA	A
2.02	Supply current, silent mode	I_{VS_sil}	$V_S \leq$ 14V, LIN recessive no load at VCC T_A = -40 °C T_A = 25 °C $T_A \leq$ 85 ° C $T_A \leq$ 125 °C		65	 85 95 100 125	µA	A
Supply currents MLX80031, MLX80051								
2.00	Supply current, normal mode	I_{VS_nor}	$V_S \leq$ 14V, V_{EN} > 2V ,RB_{WD} = 60k LIN recessive, no load at VCC	400	750	1500	µA	A
2.01	Supply current, sleep mode	I_{VS_sleep}	$V_S \leq$ 14V T_A = -40 °C T_A = 25 °C $T_A \leq$ 85 ° C $T_A \leq$ 125 °C		15	 30 20 30 45	µA	A
2.02	Supply current, silent mode	I_{VS_sil}	$V_S \leq$ 14V, LIN recessive no load at VCC T_A = -40 °C T_A = 25 °C $T_A \leq$ 85 ° C $T_A \leq$ 125 °C		65	 85 95 100 125	µA	A

Voltage Regulator Pin VCC								
MLX80050, MLX80051 (RTG connected to VCC)								
3.01	Output voltage VCC	V_{CCn5}	$6V \le V_S \le 18V$ $1mA \le I_{LOAD} \le 70mA$ $T_A = 25°C$ $T_A = -40°C$ to $125°C$	4.90 4.85	5.0	5.10 5.15	V	A
	Output voltage VCC under disturbances functional state A	$V_{CCndis5}$	$6V \le V_S \le 18V$, $T_A = 25°C$ $R_{LOAD} = 330\ \Omega$	4.75		5.25	V	C
3.02	Drop-out voltage [2]	V_{D10_5}	$V_S > 4V$, $I_{VCC} = 10mA$		75	120	mV	C
3.03		V_{D30_5}	$V_S > 4V$, $I_{VCC} = 30mA$		220	350	mV	C
3.04		V_{D70_5}	$V_S > 4V$, $I_{VCC} = 70mA$		500	800	mV	C
3.05	Line regulation	V_{LNR5}	$6V \le V_S \le 18V$, $I_{VCC} = 30mA$ $6V \le V_S \le 18V$, $I_{VCC} = 70mA$			20 100	mV	A
3.06	Load regulation	V_{LDR10_5}	$1\ mA < I_{LOAD} < 10\ mA$			50	mV	A
3.07		V_{LDR30_5}	$1\ mA < I_{LOAD} < 30\ mA$			90	mV	A
3.08		V_{LDR70_5}	$1\ mA < I_{LOAD} < 70\ mA$			150	mV	A
3.09	Output current limitation [3]	I_{VCCLIM_5}	$V_S > 6V$ $T_A = -40\ °C$ $25\ °C \le T_A \le 125\ °C$	-135 -150	-110	-75 -80	mA	A
3.10	Load capacity	C_{LOAD}		2.2	22		µF	D
MLX80030, MLX80031 (RTG connected to VCC)								
3.01	Output voltage VCC	V_{CCn3}	$4\ V \le V_S \le 18\ V$ $1m\ A \le I_{LOAD} \le 70\ mA$ $T_A = 25\ °C$ $T_A = -40\ °C$ to $125\ °C$	3.234 3.201	3.3	3.366 3.399	V	A
	Output voltage VCC under disturbances functional state A	$V_{CCndis3}$	$6\ V \le V_S \le 18\ V$, $T_A = 25\ °C$ $R_{LOAD} = 330\ \Omega$	3.135		3.465	V	C
3.02	Drop-out voltage [2]	V_{D10_3}	$V_S > 3\ V$, $I_{VCC} = 10\ mA$			100	mV	C
3.03		V_{D30_3}	$V_S > 3\ V$, $I_{VCC} = 30\ mA$			300	mV	C
3.04		V_{D70_3}	$V_S > 3\ V$, $I_{VCC} = 70\ mA$			700	mV	C
3.05	Line regulation	V_{LNR_3}	$5\ V \le V_S \le 18\ V$, $I_{VCC} = 30mA$ $5V \le V_S \le 18V$, $I_{VCC} = 70mA$			20 100	mV	A
3.06	Load regulation	V_{LDR10_3}	$1\ mA < I_{LOAD} < 10\ mA$			50	mV	A
3.07		V_{LDR30_3}	$1\ mA < I_{LOAD} < 30\ mA$			90	mV	A
3.08		V_{LDR70_3}	$1\ mA < I_{LOAD} < 70\ mA$			150	mV	A
3.09	Output current limitation [3]	I_{VCCLIM_3}	$V_S > 4\ V$ $T_A = -40\ °C$	-135	-110	-75	mA	A

			25 °C ≤ T_A ≤ 125 °C	-150		-80		
3.10	Load capacity	C_{LOAD}		2.2	22		µF	D

Output Pin NRES								
4.01	Output voltage low	V_{OL_NRES}	I_{NRES} = 1 mA			0.25	V	A
4.02	Leakage current low	I_{leak_RxD}	V_{NRES} = 0 V	-5		5	µA	A
4.03	Leakage current high	I_{leak_RxD}	V_{NRES} = V_{CC}	-5		5	µA	A
	Output voltage high NRES under disturbances to fulfil functional state A	V_{OH_NRES}	R_{load} = 2.7 k to VCC	V_{CC} -1			V	C
MLX80050, MLX80051								
5.01	VCC reset threshold on NRES pin	V_{RES5V}	t > t_{rr}	3.9	4.10	4.3	V	A
5.02	V_{RES} Hysteresis V_{RESHYS} = |$V_{RES(ON)}$ – $V_{RES(OFF)}$|	$V_{RESHYS5V}$				200	mV	C
MLX80030, MLX80031								
5.01	VCC reset threshold on NRES pin	V_{RES3V}	t > t_{rr}	2.75	2.95	3.15	V	A
5.02	V_{RES} Hysteresis V_{RESHYS} = |$V_{RES(ON)}$ – $V_{RES(OFF)}$|	$V_{RESHYS3V}$				100	mV	C
Input Pin EN								
6.01	Input voltage low	V_{IL_EN}				0.8	V	A
6.02	Input voltage high	V_{IH_EN}		2.0			V	A
6.03	Hysteresis	V_{HYS_EN}		50	100	700	mV	C
6.04	Pull-down resistor	R_{pd_EN}	V_{EN} =VCC	50	125	250	kΩ	A
Input Pin WAKE (MLX80031, MLX80051)								
7.01	High level input voltage	V_{IH_WAKE}	Sleep mode	V_S-1V			V	A
7.02	Low level input voltage	V_{IL_WAKE}	Sleep mode			V_S-3.3V	V	A
7.03	Pull up current WAKE	I_{WAKE_PU}	Normal & sleep	-30	-15	-1	µA	A
7.04	Leakage current WAKE high	I_{WAKE_lk}	V_S = 18V	-5		5	µA	A
Input Pin KL15 (MLX80031, MLX80051)								
8.01	High level input voltage	V_{IH_KL15}	Rv = 50kΩ	4		V_S+0.3V	V	A
8.02	Low level input voltage	V_{IL_KL15}	Rv = 50kΩ	-1		2	V	A
8.03	Pull down current KL15	I_{KL15_PD}			30	65	µA	A
Input Pin MODE (MLX80031, MLX80051)								
23.01	Input voltage low	V_{IL_MODE}				0.8	V	A
23.02	Input voltage high	V_{IH_MODE}		2.0			V	A

23.03	Hysteresis	V_{HYS_MODE}		50	100	600	mV	C
23.04	Pull-down resistor	R_{pd_MODE}	V_{MODE} = VCC	200		600	kΩ	A

Input Pin NWDI (MLX80031, MLX80051)								
9.01	Input voltage low	V_{IL_NWDI}				0.8	V	A
9.02	Input voltage high	V_{IH_NWDI}		2.0			V	A
9.03	Hysteresis	V_{HYS_NWDI}		50	100	600	mV	C
9.04	Pull-up resistor to VCC	R_{pu_NWDI}	VN_{WDI} = 0V	125	250	375	kΩ	A
9.05	Min low pulse width	T_{minlow_NWDI}	one WD_OSC clock period	1			1	D
Watchdog Oscillator pin RBWD (MLX80031, MLX80051)								
10.01	Voltage at RB_{WD}	V_{RBwd}	I_{OUT} = -50 µA		1.2		V	A
10.02	Range of RB_{WD} resistance	RB_{WD}		20		60	kΩ	B
10.03	RB_{WD} short resistance threshold to enable fail-safe state	RB_{WDSH}	see paragraph 7.3	0		330	Ω	B
Output INH (MLX80031, MLX80051)								
11.01	ON Resistance	R_{ON_INH}	V_S = 12V		20	60	Ω	A
11.02	Leakage current INH high	I_{leakH_INH}	Sleep Mode, V_{INH} = 18V, V_S = 18V	-5		5	µA	A
11.03	Leakage current INH low	I_{leakL_INH}	Sleep Mode, V_{INH} = 0V, V_S = 18V	-5		5	µA	A
Thermal Protection								
	Thermal shutdown	T_{JSHD}		155	170	190	°C	D
	Thermal hysteresis	T_{JHYS}			10	30	°C	D

Notes:

[1] A = 100% serial test, B = Operating parameter, C = characterization data,
D = Value guaranteed by design

[2] The nominal VCC voltage is measured at VSUP = 12V. If the VCC voltage is 100mV below its nominal value then the voltage drop is VD = VSUP – VCC

[3] Functionality range of current limitation at silent mode is limited by reset threshold VRES. Below them the IC change to normal mode.
Validity for IVCC_MAXsil: VCCn (min) ≤ VCC ≤ VRES

Table 3: LIN DC Characteristics

Parameter		Symbol	Condition	Min	Typ	Max	Unit	T[1]
General								
12.01	Pull up current LIN (recessive)	$I_{INLINpu}$	V_{LIN} = 18 V, V_S = 6V			80	µA	A
12.02	Pull up resistor LIN	R_{LINpu}	V_S = 12V, V_{LIN} = 0V	20	30	60	kΩ	A
12.03	Reverse current LIN (dominant)	$I_{INLINdom}$	V_S = 12V, V_{LIN} = 0V	-400			µA	A
12.04	Reverse current LIN (recessive)	$I_{INLINrec}$	$V_{LIN} \geq V_S$, 8V ≤ V_{LIN} ≤ 18V, 8V ≤ V_S ≤ 18V	0		23	µA	A
12.05	Reverse current LIN (loss of battery)	I_{INLIN_lob}	V_S = 0V, 0V ≤ V_{LIN} ≤ 18V	0		23	µA	A
12.06	Reverse current LIN (loss of ground)	I_{INLIN_log}	V_S= 12V, 0V ≤ V_{LIN} ≤ 18V	-10		50	µA	A
	Voltage drop serial Diode	$V_{SerDiode}$		0.4	0.7	1.0	V	D
	Battery Shift	V_{Shift_BAT}	related to VS	0		11.5	%	D
	Ground Shift	V_{Shift_GND}	related to VS	0		11.5	%	D
	Ground-Battery shift difference	V_{Shift_diff}	related to VS	0		8	%	D
Receiver								
12.07	Receiver dominant voltage	V_{BUSdom}	7.0 V ≤ V_S ≤ 18 V			0.4*V_S	V	A
	Receiver recessive voltage	V_{BUSrec}		0.6*V_S				A
12.08	Centre point of receiver threshold V_{thr_cnt} = (V_{thr_rec}+V_{thr_dom})/2	V_{thr_cnt}		0.475*V_S	0.5*V_S	0.525*V_S		A
12.09	Receiver Hysteresis V_{hys} = V_{thr_rec}-V_{thr_dom}	V_{hys}			0.15*V_S	0.175*V_S		A
Transmitter								
12.10	Transmitter dominant voltage	Vol_{bus}	R_{load} = 500Ω, V_S = 5V	0		1.2	V	D
			R_{load} = 500Ω, V_S >= 7V	0		0.2*V_S		A
12.11	Current limitation LIN	I_{LIM}	V_{LIN} = V_S, TxD = 0V	40	120	200	mA	A
12.12	Transmitter recessive voltage	Voh_{BUS}	No load, V_{EN} = 0/5V, VTxD = 5V	0.8*V_S		V_S	V	A

Input/Output Pin TxD								
13.01	Input voltage low TxD	V_{IL_TxD}	rising			0.8	V	A
13.02	Input voltage high TxD	V_{IH_TxD}		2			V	A
13.03	Hysteresis	V_{HYS_TxD}		50		700	mV	C
13.04	Pull-up resistor to VCC	R_{pu_TxD}	V_{TxD} = 0V	125	250	375	kΩ	A

13.06	Low level output current	I_{OL_TxD}	local wake-up request; standby mode; V_{TxD} = 0.4V	1.5			mA	A
Output Pin RxD								
14.01	Output voltage low RxD	V_{OL_RxD}	I_{RxD} = 2 mA			0.6	V	A
14.02	Pull-up resistor to VCC	R_{pu_RxD}	V_{RxD} = 0V	3	5	7	kΩ	A
14.03	Leakage current high	I_{leak_RxD}	V_{RxD} = VCC	-5		5	µA	A
	Output voltage high RxD under disturbances to fulfil functional state A	V_{OH_RxD}	R_{load} = 2.7k to VCC	V_{CC} -1			V	C

Notes:

[1] A = 100% serial test, B = Operating parameter, C = characterization data, D = Value guaranteed by design

3.2. AC Characteristics

6V ≤ V_S ≤ 27V, -40°C ≤ T_A ≤ 125°C, RTG connected to VCC, unless otherwise specified

Table 4: AC Characteristics

Parameter		Symbol	Condition	Min	Typ	Max	Unit	T[1]
Reset parameter on NRES								
16.01	Reset time	t_{Res}	V_S = 14V	2.5	4	5.5	ms	A
16.02	Reset rising time	t_{rr}	V_S = 14V	3.0	6.5	12	µs	A
Watchdog parameter on NRES (MLX80031, MLX80051)								
17.01	Watchdog-Oscillator Period	$t_{WDOSC20}$	RB_{WD} = 20kΩ ±1%	7.0	8.05	9.0	µs	A
17.02		$t_{WDOSC60}$	RB_{WD} = 60kΩ ±1%	19.0	23.05	25.2	µs	A
	Watchdog Close Window	t_{CW}	tCW = cycles * tWDOSC		1053		cycles	D
	Watchdog Open Window	t_{OW}	tOW = cycles * tWDOSC		1105		cycles	D
17.05	Watchdog Reset Low Time	t_{WDres}		3	4	5	ms	A
	Watchdog Lead Window	t_{LDT}	tOWS = cycles * tWDOSC		7895		cycles	D
17.06	Watchdog Safety Oscillator	$t_{WDsafety}$	RBWD open / RBWD gnd	30	50	75	µs	A

Wake-up and Mode Control								
18.01	Remote Wake-up filter time	t_{wu_remote}		30	70	150	µs	A
18.02	Wake-up filter time on WAKE (only MLX80051,MLX80031)	t_{wu_WAKE}	Sleep or Silent Mode, WAKE falling edge	10		50	µs	A
18.03	Wake-up filter time on KL15 (only MLX80051,MLX80031)	t_{wu_KL15}	Sleep or Silent Mode, KL15 rising edge	80	168	250	µs	A
18.04	Propagation delay from Normal Mode to Sleep Mode via EN	t_{pd_sleep}	V_{EN} = 0V	5	15	20	µs	A
18.05	Propagation delay from Standby Mode to Normal Mode via EN	t_{pd_norm}	V_{EN} = 5V	5	15	20	µs	A
18.06	Propagation delay from Silent Mode to Normal Mode via EN	$t_{pd\_sil\_n}$	V_{EN} = 5V Silicon Revision C	5	15	40	µs	A
18.07	Propagation delay: go to silent mode after EN=H/L	t_{pd_sil}	check falling edge on RBwd, EN = 0V Silicon Revision C			20	µs	A
	Setup time TxD to EN for low slew mode	$t_{set\_TxD\_EN}$		5			µs	B
	Hold time TxD after EN for low slew mode	$t_{hold\_TxD\_EN}$		20			µs	B
	TXD hold time for mode change	$t_{hold\_TxD\_MCH}$				2	µs	D
18.08	Debouncing time EN	t_{deb_EN}		2	5	20	µs	A
18.09	TxD dominant time out	t_{TxD_to}	Normal Mode, V_{TxD} = 0V	27		60	ms	A
18.10	Standby time out	t_{sby_to}	Standby Mode, V_{EN}= 0V	150		500	ms	A
18.11	Wake up time vs. EN	t_{wu_EN}	Wake form sleep via EN=L/H	2	5	20	µs	A
General LIN Parameter								
19.01	Receiver propagation delay LIN -> RxD	t_{dr_RxD} t_{df_RxD}	$C_{L(RXD)}$ = 50 pF			6	µs	A
19.02	Symmetry prop. delay LIN->RxD	t_{dsym_RxD}	t_{dr_RXD} - t_{df_RXD}	-2		2	µs	A
19.03	Receiver debouncing time	t_{deb_LIN}		1.5	2.8	4.0	µs	D

19.04	slew rate rising edge LIN	dV/dTrise	Normal Mode LIN-Load: 1kΩ/1nF	1.0	1.5	2.5	V/µs	C
19.05	slew rate falling edge LIN	dV/dTfall		-2.5	-1.5	-1.0	V/µs	C
19.06	slew rate rising edge LIN	dV/dTrise	Low Slew Mode LIN-Load: 1kΩ/1nF	0.3	0.8	1.3	V/µs	C
19.07	slew rate falling edge LIN	dV/dTfall		-1.3	-0.8	-0.3	V/µs	C
	Internal capacity	C_{LIN}	Pulse at LIN via 10kOhm with 0/10V; VS = open		25	35	pF	D
LIN transceiver parameter according to LIN Physical Layer Spec. rev. 2.0, table 3.4 (20kbit/s)								
Conditions:	Normal slew mode; V_S =7.0V to 18V; LIN loads: 1kΩ/1nF; 660Ω/6.8nF; 500Ω/10nF TxD signal: t_{Bit} = 50µs, $t_{wH} = T_{wL} = t_{Bit}$; $t_{rise} = t_{fall}$ < 100ns							
	Minimal recessive bit time	$t_{rec(min)}$		40	50	58	µs	
	Maximum recessive bit time	$t_{rec(max)}$		40	50	58	µs	
20.01	Duty cycle 1	D_1	$D_1 = t_{rec(min)} / (2*t_{Bit})$	0.396				A
20.02	Duty cycle 2	D_2	$D_2 = t_{rec(max)} / (2*t_{Bit})$			0.581		A
Transceiver parameter according to LIN Physical Layer Spec. rev. 2.0, table 3.4 (10.4kbit/s)								
Conditions:	Low slew mode; V_S =7.0V to 18V; LIN loads: 1kΩ/1nF; 660Ω/6.8nF; 500Ω/10nF TxD signal: t_{Bit} = 96µs, $t_{wH} = T_{wL} = t_{Bit}$; $t_{rise} = t_{fall}$ < 100ns							
	Minimal recessive bit time	$t_{rec(min)}$		80	96	113	µs	
	Maximum recessive bit time	$t_{rec(max)}$		80	96	113	µs	
21.01	Duty cycle 1	D_3	$D_3 = t_{rec(min)} / (2*t_{Bit})$	0.417				A
21.02	Duty cycle 2	D_4	$D_4 = t_{rec(max)} / (2*t_{Bit})$			0.590		A
LIN transceiver parameter according to SAE J2602 (10.4kbit/s)								
Conditions:	Low slew mode; V_S =7.0V to 18V; LIN loads: 1kΩ/1nF;660Ω/6.8nF;500Ω/10nF TxD signal: t_{Bit} = 96µs, $t_{wH} = T_{wL} = t_{Bit}$; $t_{rise} = t_{fall}$ < 100ns							
22.01	Minimal recessive delay TxD -> LIN	$t_{x\_rec\_min}$				48	µs	A
22.02	Maximum recessive delay TxD -> LIN	$t_{x\_rec\_max}$				48	µs	A
22.03	Minimal dominant delay TxD -> LIN	$t_{x\_dom\_min}$				48	µs	A
22.04	Maximum dominant delay TxD -> LIN	$t_{x\_dom\_max}$				48	µs	A
22.05	Maximum rec. to dom. delay	$T_{r\_d\_max}$	$t_{x\_rec\_max} - t_{x\_dom\_min}$			15.9	µs	A
22.06	Maximum dom. to rec. delay	$T_{d\_r\_max}$	$t_{x\_dom\_max} - t_{x\_rec\_min}$			17.2	µs	A

Notes:

[1] A = 100% serial test, B = Operating parameter, C = characterization data, D = Value guaranteed by design

3.3. Timing diagrams

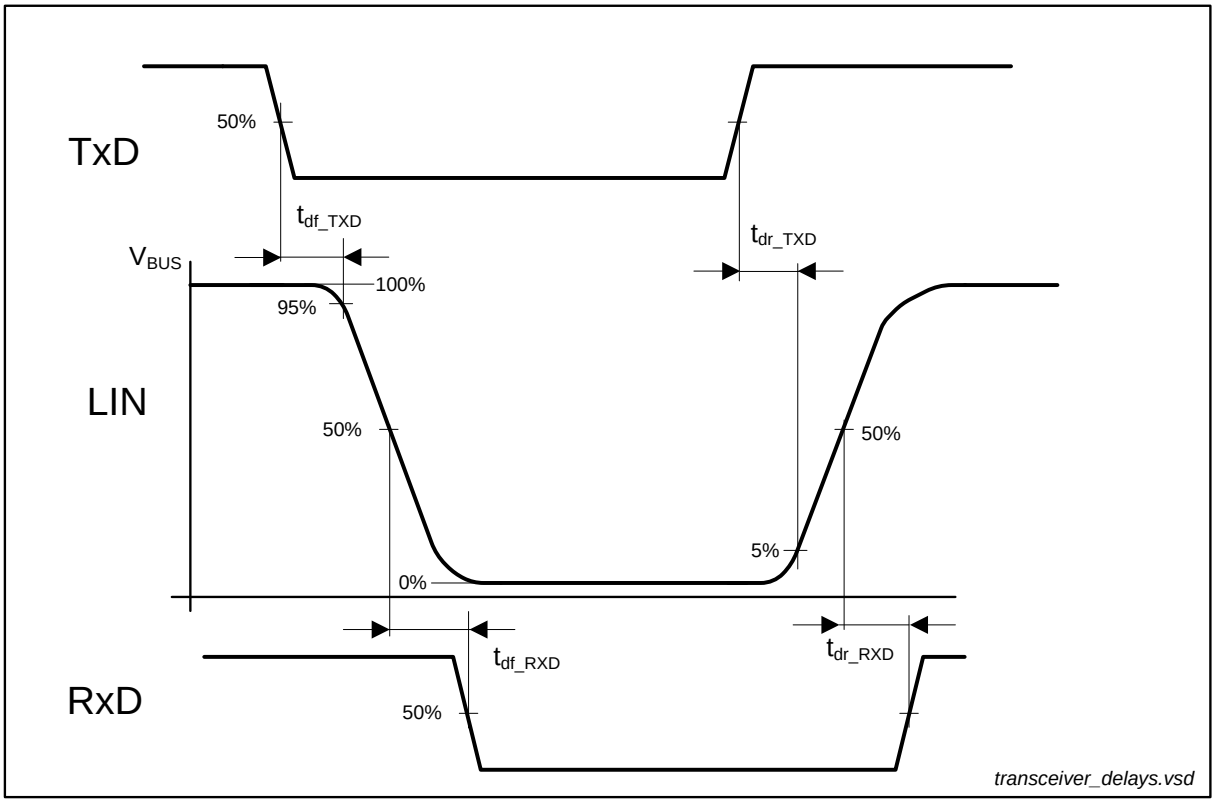


Figure 1: LIN propagation delays

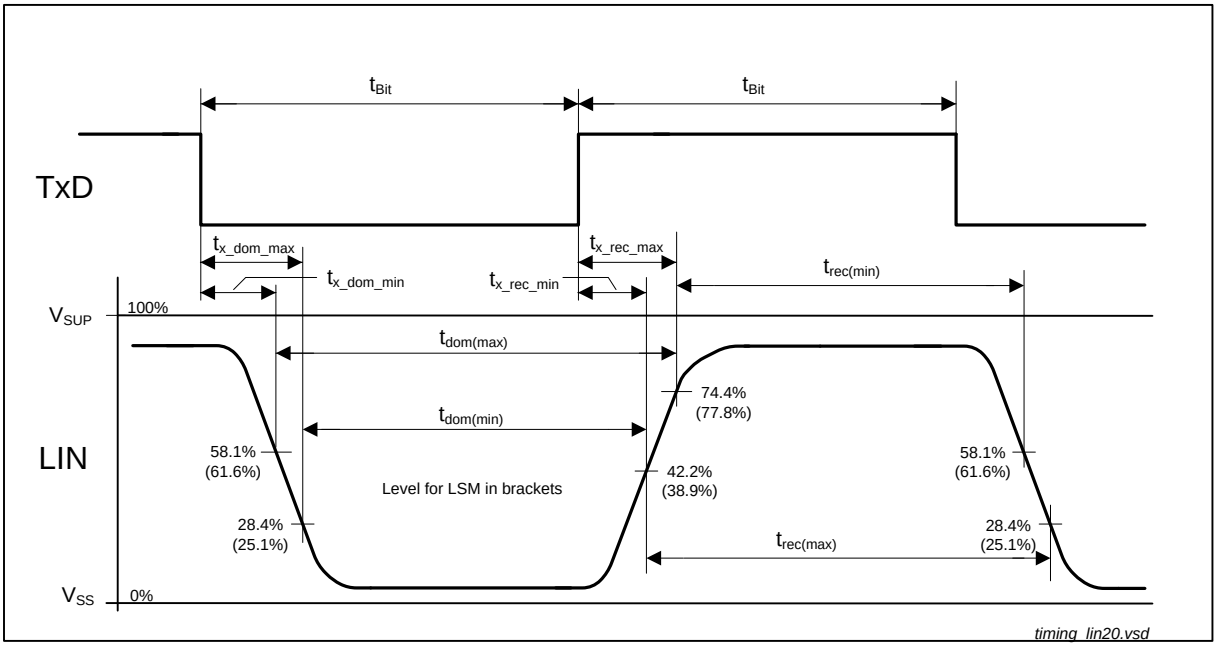
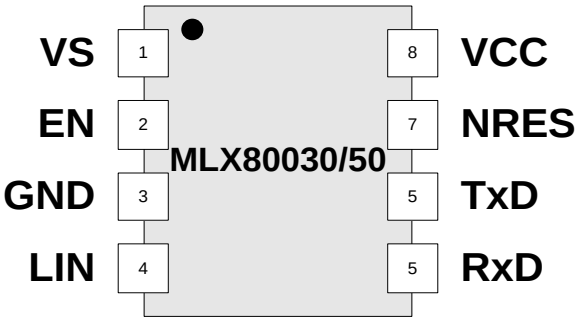


Figure 2: LIN duty cycles

4. Pin Configuration

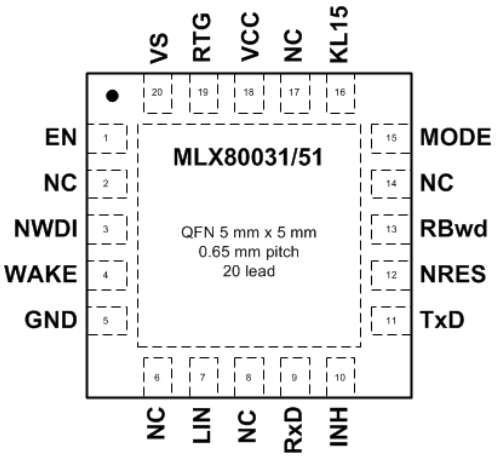
4.1. MLX80030 and MLX80050 - SOIC8



Pin	Name	IO-Typ	Description
1	VS	P	Battery supply voltage
2	EN	I	Mode control pin, enables the normal operation mode when HIGH
3	GND	G	Ground
4	LIN	I/O	LIN bus transmitter/receiver pin, (low = dominant)
5	RxD	I/O	Received data from LIN bus, low in dominant state; internal pull-up resistor
6	TxD	I/O	Transmit data input (low = dominant)
7	NRES	O	Undervoltage reset output (open drain), low active
8	VCC	P	Voltage regulator output

Table 5: MLX80050/30 pin list in SOIC8

4.2. MLX80031 and MLX80051 in QFN20



Pin	Name	IO-Typ	Description
1	EN	I	Mode control pin, enables the normal operation mode when HIGH
2	NC		not connected
3	NWDI	I	Watchdog trigger input; negative edge; pull-up
4	WAKE	I	High voltage input for local wake up, negative edge triggered
5	GND	G	Ground
6	NC		not connected
7	LIN	I/O	LIN bus transmitter/receiver pin, (low = dominant)
8	NC		not connected
9	RxD	I/O	Received data from LIN bus, low in dominant state; internal pull-up resistor
10	INH	O	High side switch; High voltage
11	TxD	I/O	Transmit data input (low = dominant)
12	NRES	O	Reset output (open drain), low active
13	RB_{WD}	I/O	Bias resistor for watchdog oscillator
14	NC		not connected
15	MODE	I	Input to control window watchdog
16	KL15	I	High voltage input for local wake up, positive edge triggered
17	NC		not connected
18	VCC	I	Voltage regulator sense input
19	RTG	P	Voltage regulator output
20	VS	P	Battery supply voltage
	EP	G	Exposed pad should be connected to Ground

Table 6: MLX80051/31 pin list in QFN20

3. Functional Description

The MLX8003x/5x consists of a low drop 3.3V/5V voltage regulator capable to drive 70mA and a LIN bus transceiver, which is a bi-directional bus interface for data transfer between LIN bus and the LIN protocol controller. Additionally integrated is a Window-Watchdog/RESET unit with a fixed power-on-reset delay of 4 ms and an adjustable watchdog time defined by an external bias resistor.

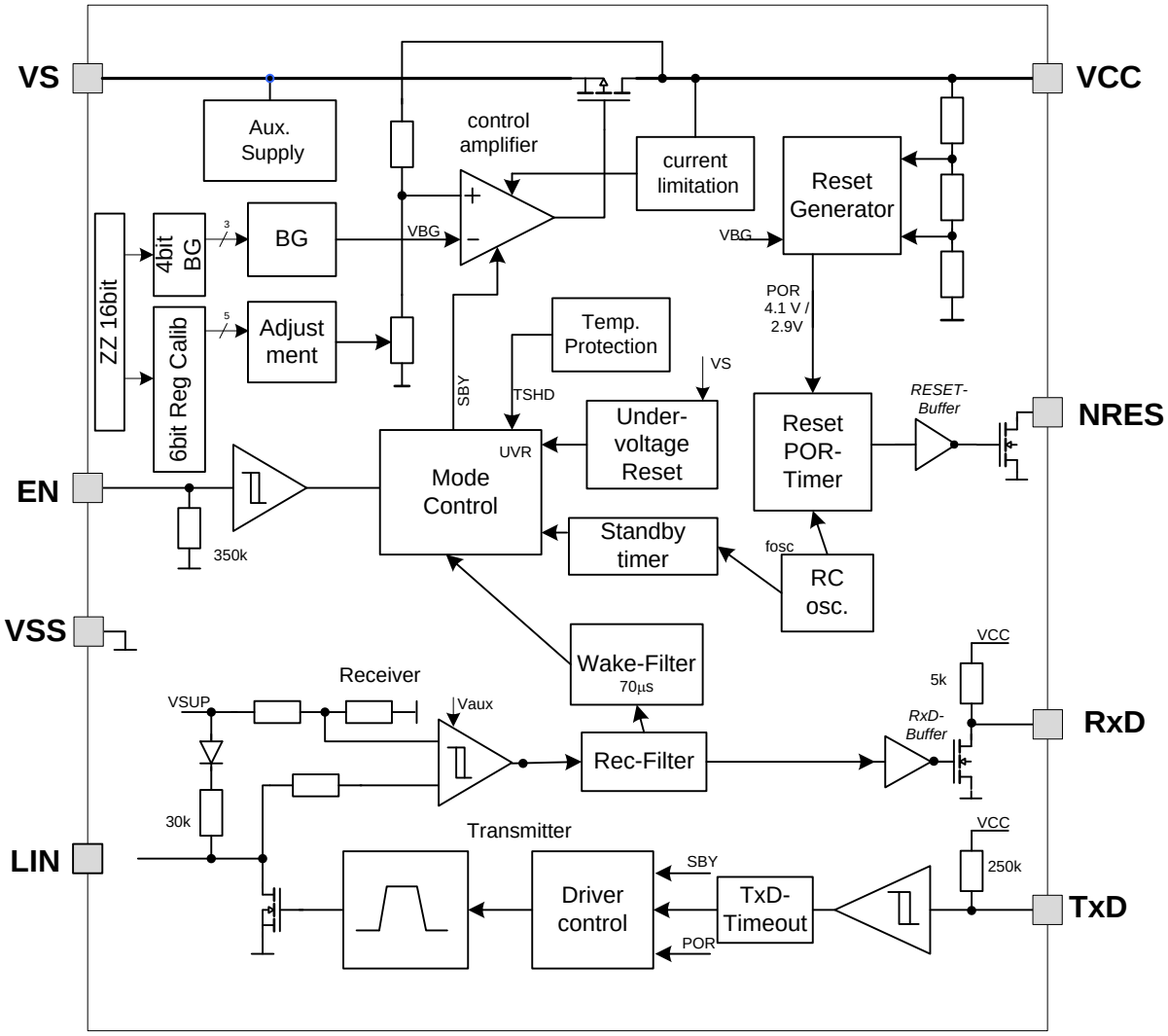


Figure 3: MLX80050/30 Block Diagram

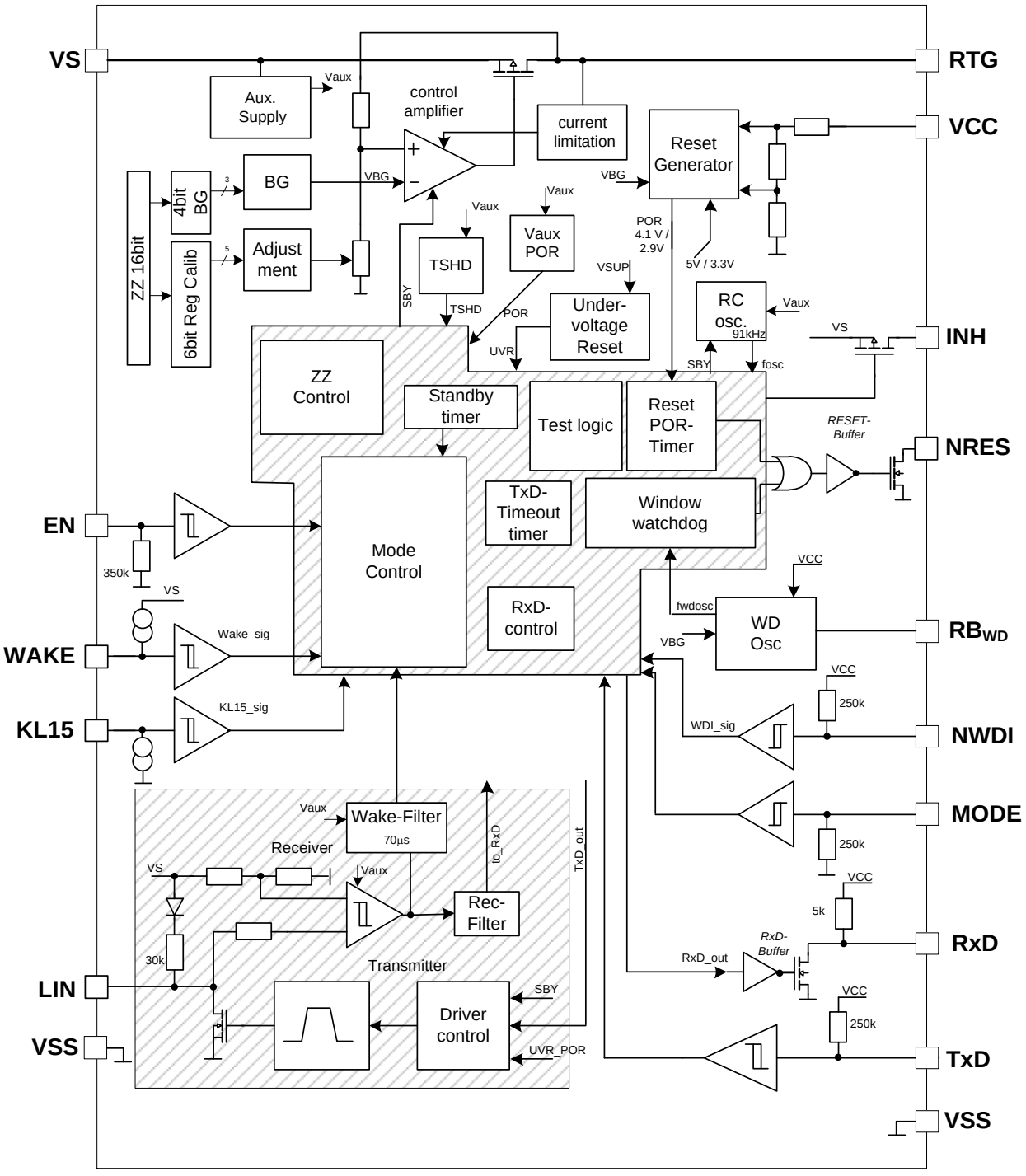


Figure 4: MLX80051/31 Block Diagram

3.1. Supply Pin VS

VS is the operational voltage pin of MLX8005x/3x. The voltage range is VS = 6 to 18V. After switching on VS, the MLX8003x/5x starts at Standby Mode and the VCC voltage regulator ramps up. An undervoltage detection unit prevent an undefined operation for Vs < 4V.

VS- Power-ON

If VS is switched on, the MLX8003x/5x starts in Standby Mode. A combination of dynamic POR and under voltage reset circuitry generates a POR signal, which switches the MLX8003x/5x on. This power on behaviour is independent from the status of the EN-pin.

Power-on reset and under-voltage reset operate independent from each other, which secures the independence from the rise time of VS.

3.2. EN input pin

The ENable input is the mode control pin of MLX8003x/5x in combination with the TxD input.

The MLX8003x/5x is switched into the Sleep Mode with a falling edge and into normal mode with a rising edge at the EN pin. The state machine goes to Normal Mode after t_{Res} (see also Table 4: AC Characteristics). The Normal Mode will be kept as long as EN remains high.

The Normal Mode can be entered from Standby Mode, when the pin EN is driven HIGH. To prevent unwanted mode transitions, the EN input contains a debounce filter as specified (t_{EN_deb}).

The pin EN contains a weak pull down resistor. The input thresholds are compatible to 3.3V and 5V supply systems.

MLX80031/51:

Additionally the positive edge on pin EN results in an immediate reset of the active low interrupt on pin RxD as well as the wake-up source recognition flag on pin TxD.

3.3. Ground pin GND

This is the reference pin of the IC. The absence of GND connection will not influence or disturb the communication between other LIN bus nodes.

3.4. LIN

This bidirectional pin consists of a low side driver in the output path and a high-voltage comparator in the input path. Furthermore is integrated a LIN pull-up resistor between LIN and VS pin. Low side driver consist a current limitation.

3.5. Receiver Output RxD

The pin RxD is a buffered open drain output. Output signals can be shifted by the external pull up resistor to 3.3V and 5V supply systems.

3.6. Transmit Input TxD

The transmit data stream of the LIN protocol controller applied to the pin TxD is converted into the LIN bus signal with slew rate control in order to minimize electromagnetic emissions.
The pin TxD contains a weak pull up resistor. The input thresholds are compatible to 3.3V and 5V supply systems. To enable the transmit path, the TxD pin has to be driven recessive (HIGH) after or during the normal mode has been entered.

3.6.1. TxD dominant time-out feature

With the first dominant level on pin TxD after the transmit path has been enabled, the dominant time-out counter is started. In case of a faulty blocked permanent dominant level on pin TxD the transmit path will be disabled after the specified time t_{TxD_to}. The time-out counter is reset by the first negative edge on pin TxD.

3.7. Output NRES

The NRES pin outputs the reset state as well as the watchdog condition in MLX80031 and MLX80051.

3.8. Voltage regulator pins VCC and RTG

The MLX80030/50 has an integrated low drop linear regulator with a p-channel-MOSFET as driving transistor. This regulator outputs a voltage of 5V ±2% (MLX80050/51) or 3.3V ±2% (MLX80030/31) with a load current of max. 70mA. The current limitation unit limits the output current for short circuits or overload to 130mA by decreasing the VCC voltage. This way the power dissipation is held constant at a maximum value.

The voltage regulator has two pins, output pin RTG and sense input pin VCC. For MLX80030/50 both, RTG and VCC, are commonly bonded to pin VCC on the package.

Devices MLX80031/51 has both pins bonded and provides the possibility to use an external npn transistor to boost the maximum load current. In this case the basis of the npn transistor has to be connected to the RTG pin and the emitter to the VCC pin. In case of using the internal voltage regulator, both pins have to be connected to each other.

3.9. INH Output (only MLX80031/51)

INH switches to high (VS connected to INH) in case of Standby or Normal Mode. INH is switched off at Silent and Sleep Mode. The pin will be used for switch on an external power supply or for switch off the external 1k master resistor in master node applications.

3.10. WAKE Input (only MLX80031/51)

High voltage input pin for local wake-up functionality. With a falling edge on WAKE the IC wakes-up from Silent Mode or Sleep Mode to Standby Mode.
The pin WAKE provides a weak pull up current source towards Vs which provides a HIGH level on the pin in case of open circuit failures or if no local wake-up feature is required. In such applications it is recommended to connect the pin WAKE directly to pin Vs in order to prevent influences due to EMI.

3.11. KL15 Input (only MLX80031/51)

High voltage input pin for local wake-up functionality. With a rising edge on KL15 the IC wakes-up from Silent Mode or Sleep Mode to Standby Mode.

The pin KL15 provides a weak current sink towards GND which provides a LOW level on the pin in case of open circuit failures or if no local wake-up feature is required. In such applications it is recommended to connect the pin KL15 directly to GND in order to prevent influences due to EMI. KL15 is typically connected to the ignition terminal and generates a local wake-up at start of ignition.

3.12. Watchdog Trigger Input NWDI (only MLX80031/51)

This input is used to trigger the integrated window watchdog in MLX80031/51. Every falling edge on NWDI in watchdog open window is used to reset the watchdog timer. An internal pull up resistor of 250k secures a stable high condition if this pin is open. The NWDI input is a low voltage CMOS input. The minimum low time of NWDI is one WD_OSC clock period to allow falling edge detection.

3.13. Watchdog Oscillator Resistor RB_{WD} (only MLX80031/51)

A resistor between RBWD and GND defines the window watchdog times as trigger time.

3.14. Mode Input MODE (only MLX80031/51)

Special pin for to disable the window watchdog function. For normal watchdog operation connect the MODE pin to GND directly or via external resistor. With MODE pin on 3.3V/5V the window watchdog is switched off.

4. Operational Modes

The MLX8003x/5x provides four main operating modes “Standby”, “Normal”, “Silent” and “Sleep”. The main modes are fixed states defined by basic actions (VS start, EN or wake-up).

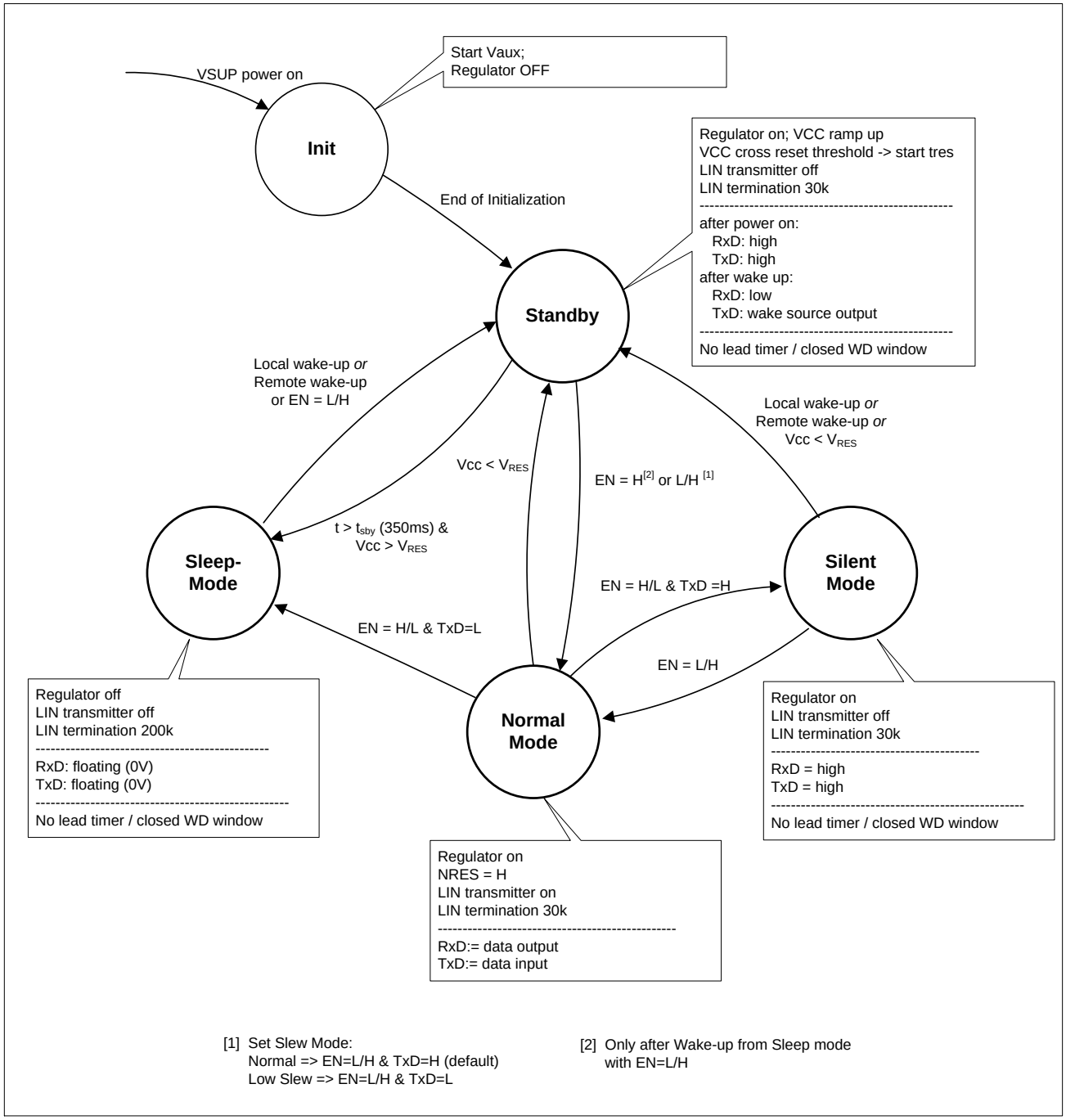


Figure 5: MLX8005x3x state diagram of modes of operation

4.1. Modes Overview

Mode	VCC	TxD	RxD	LIN	remarks
Standby	3.3V/5V	high	high	recessive	entered after power on or wake up
Normal	3.3V/5V	input for transmit data stream	output for LIN data stream	follows TxD	[1]
Silent	3.3V/5V	high	high	recessive	high = 3.3V/5V
Sleep	0	floating	floating	recessive	remote wake up to enter Standby Mode, EN = H to go to Normal Mode

Table 7: MLX80050/30 Operation Modes

[1] Normal mode will be entered form Standby Mode by a low -> high transition on pin EN and from Sleep Mode by EN = H after startup of the regulator. When recessive level (high) on pin TxD is present the transmit path will be enabled

Mode	VCC	TxD	RxD	LIN	INH	Watchdog	remarks
Standby	3.3V/5V	High/ active low[1]	high/ active low[2]	recessive	ON	ON	entered after power on or wake up
Normal	3.3V/5V	input for transmit data stream	output for LIN data stream	follows TxD	ON	ON	[3] [4] [5]
Silent	3.3V/5V	high	high	recessive	OFF	OFF	
Sleep	0	floating	floating	recessive	OFF	OFF	Local or remote wake up to enter Standby Mode, EN = H to go to Normal Mode

Table 8: MLX80051/31 Operation Modes

[1] Indicates the wake up flag in case of local wake up
[2] After power on RxD is going high via pull-up to Vcc. If any wake up(local or remote) occurs it will be indicated by active low
[3] Active low interrupt at pin RxD will be removed when entering normal mode
[4] Wake up source flag at pin TxD will be removed when entering normal mode
[5] Normal mode will be entered from Standby Mode by a low -> high transition on pin EN and from Sleep Mode by EN = H after startup of the regulator. When recessive level (high) on pin TxD is present the transmit path will be enabled

4.2. Initialisation and Standby mode

When the battery supply voltage VS exceeds the specified threshold V_{SUVR_OFF}, the MLX8003x/5x automatically enters the Standby Mode. Following internal procedure is running:

First:

- Start of internal supply Vaux and POR of Vaux
- Start of internal RC oscillator

Second and parallel after POR:

- Start of voltage regulator

The output voltage V_{CC} ramps up to nominal value. The pin RxD is floating and the integrated slave pull up resistor with decoupling diode pulls the pin LIN. The transmitter as well as the receiver is disabled.

If there occurs no mode change to Normal Mode via an EN LOW to HIGH transition within the time stated (typically 350ms), the IC enters the most power saving Sleep Mode.

Furthermore the standby mode will be entered after a valid local or remote wake up event, when the MLX8003x/5x is in Sleep or Silent mode. The entering of the standby mode after wake up will be indicated by an active LOW interrupt on pin RxD.

4.3. Normal Mode

This mode is the base mode. The bus transceiver is able to send with a max baud rate of 20kbit/s.

The whole MLX8003x/5x is active. The incoming bus traffic is detected by the receiver and transferred via the RxD output pin to the microcontroller.

Exit the Normal Mode with one of the following conditions:

1. High-to-low edge on EN pin with TxD = H -> switch to Silent Mode
2. High-to-low edge on EN pin with TxD = L -> switch to Sleep Mode
3. Undervoltage monitor on VCC detects a low voltage reset condition (VCC < V_{RES}) -> switch back to stand-by mode.

Low Slew Mode

The first rising edge on EN after power-on defines the slew rate of the device. With TxD = High at this point works the MLX8003x/5x with normal slew rate (default state). TxD = Low activates the Low Slew Mode, as long as VS > V_{SUVR_OFF}.

In this mode the slew rate is switched from the normal value of typ. 1.6V/µs to a low value of typ. 0.8V/µs. This mode is optimized to send with a maximum baud rate of 10.4kbit/s (acc. to SAE J2602). Because of this reduction of the slew rate the EME behaviour is improved especially in the frequency range of 100 kHz to 10MHz.

4.4. Silent Mode

The Silent Mode is a special mode for application with active Sleep Mode on LIN, but the connected MCU still needs to be supplied with VCC.

With a falling edge on EN input in combination with TxD=high switches the MLX8003x/5x from Normal Mode to the Silent Mode with reduced internal current consumption.

In Silent Mode the voltage regulator is on with a 2% tolerance. The transmitter is disabled and the pin RxD is disconnected from the receive path and is floating. The slave termination resistor (LIN pull up resistor with decoupling diode between pins LIN and VS) is disconnected; only a weak current source is applied to the LIN bus. Value is typical -75uA, limits -20…-100uA.

Exit the silent mode with one of the following conditions:

1. Low-to-high edge on the EN pin -> switch back to normal mode
2. Remote wake up (all versions) or local wake up request (MLX80031/51 only) -> switch to standby mode
3. Undervoltage monitor on VCC detects a low voltage reset condition (VCC < V_{RES}) -> switch back to stand-by mode.

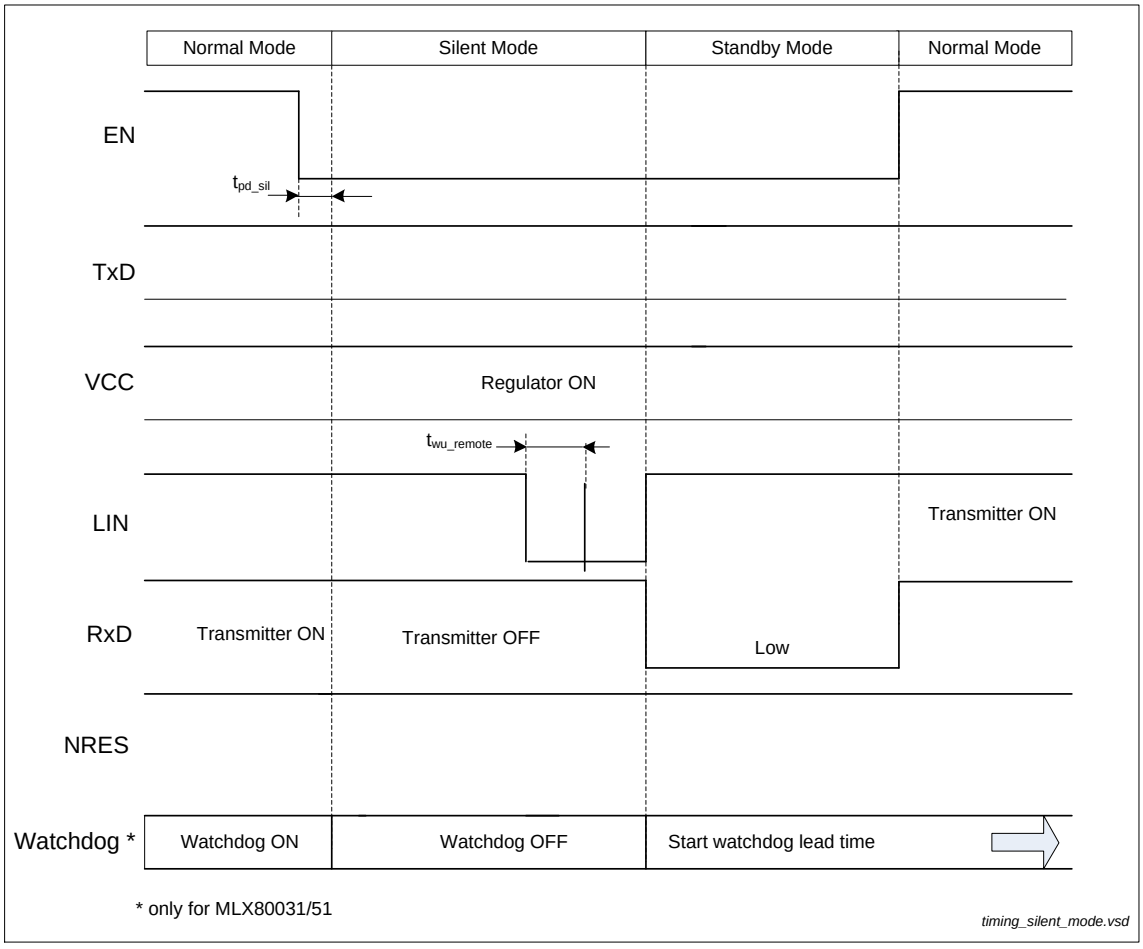


Figure 6: LIN wake-up from Silent Mode

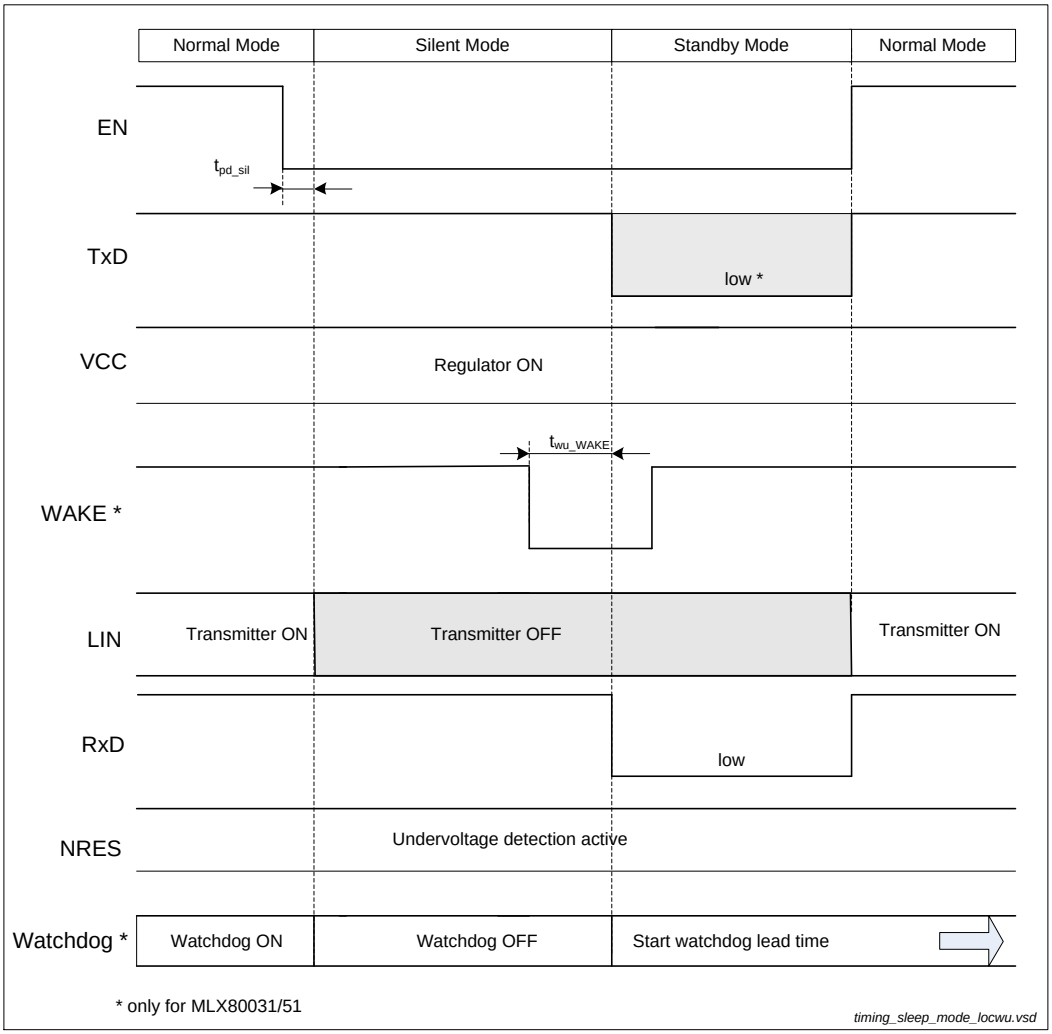


Figure 7 Local Wake-up from Silent Mode via WAKE

4.5. Sleep Mode

The most power saving mode of the MLX8003x/5x is the Sleep Mode. The MLX8003x/5x offers two procedures to enter the sleep mode:

- The mode is selected from normal mode with a falling edge on EN in combination with TxD = L.
- If the MLX8003x/5x is in Standby Mode after power-on or wake-up, a sleep counter is started and switches the transceiver into Sleep Mode after the specified time (typ. 350ms) even when the microcontroller of the ECU will not confirm the normal operation by setting the EN pin to logic HIGH. This new feature allows faulty blocked LIN nodes to reach always the most power saving mode.

Being in Sleep Mode the voltage regulator switched off in order to minimize the current consumption of the complete LIN node. The transmitter is disabled and the pin RxD is disconnected from the receive path and is low (follows VCC). The slave termination resistor (LIN pull up resistor with decoupling diode between pins LIN and VS) is disconnected, only a weak current source is applied to the LIN bus (see chapter 8 fail-safe features)
Exit the Sleep Mode with the following condition:

1. Remote (all versions) or local wake up request (MLX80031/51 only) -> Switch to Standby Mode
2. EN = L/H -> Switch to Standby Mode

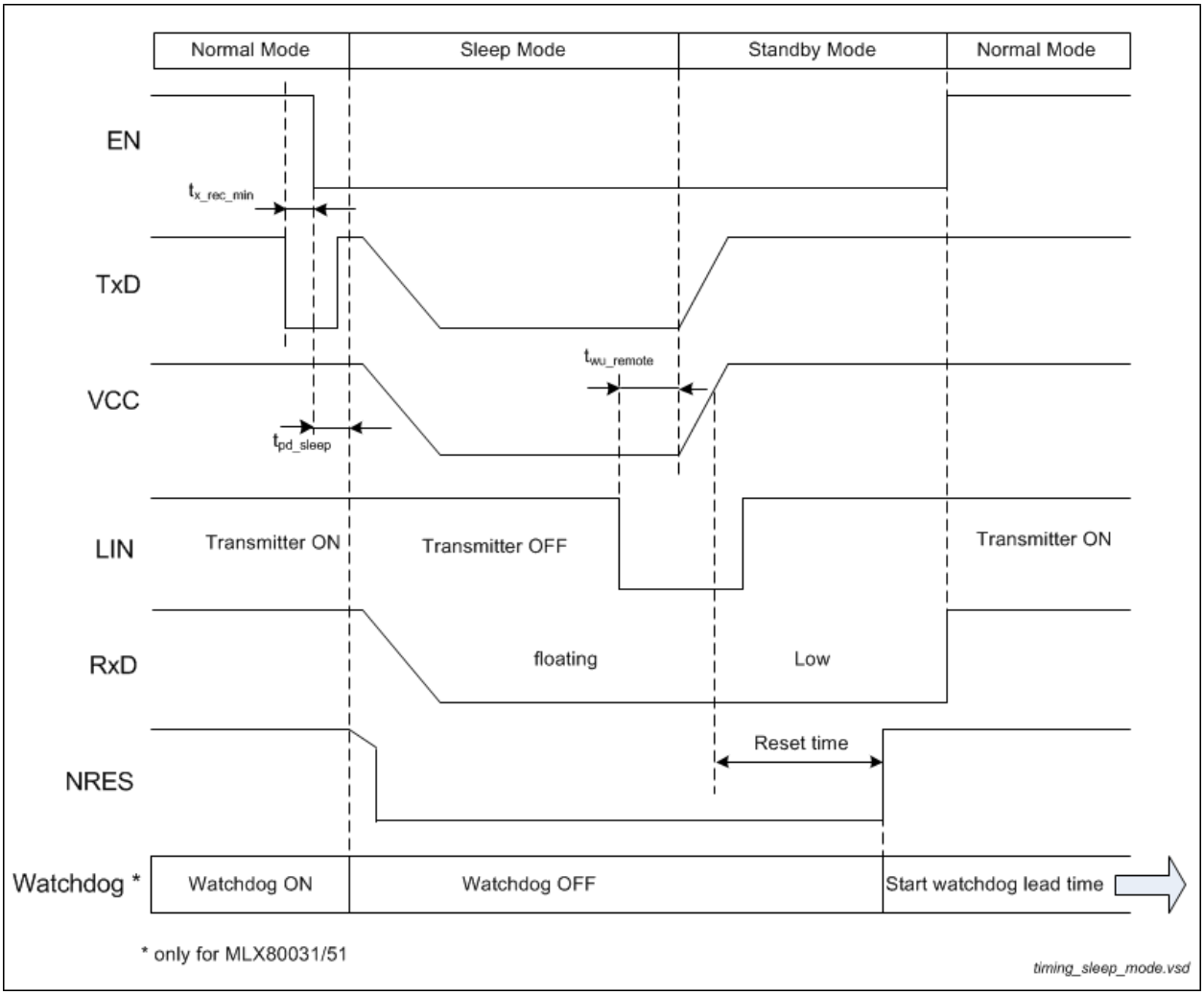


Figure 8: Remote wake-up from Sleep Mode

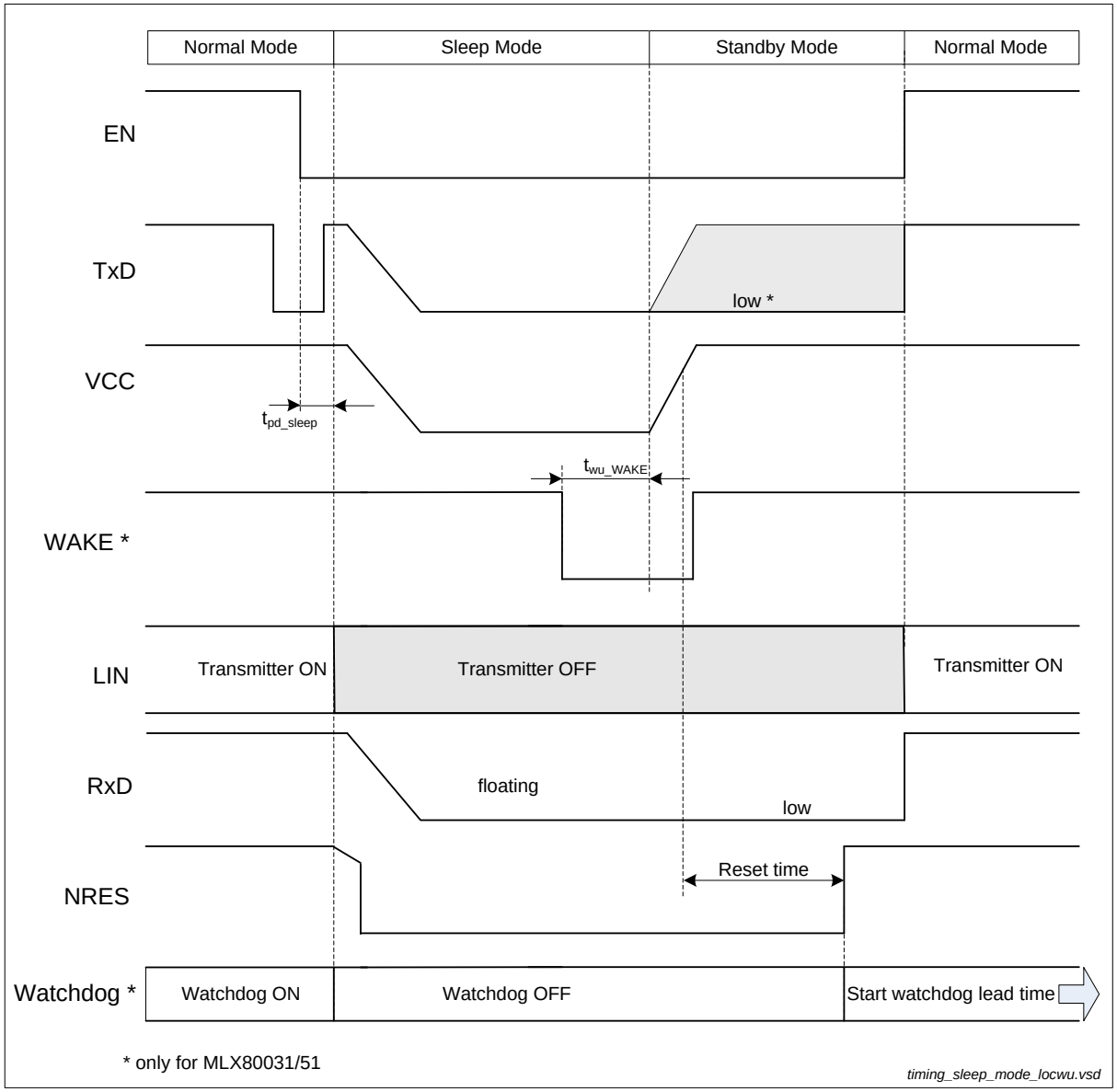


Figure 9: Local wake-up from Sleep Mode

4.6. Init-State

This is an intermediate state, which will pass through after switch on of VS or after undervoltage detection VS with VS < V_{SUVR_ON}. The internal supply voltage Vaux ramp up and the initial readout procedure of zenerzap storage are started. At the end of this phase the VCC voltage definition and the definition of MLX8003x5x version is established. This Init-State changes to Standby Mode with the start of VCC regulator.

5. Wake Up Procedures

The MLX80030/50 versions offer only remote wake-up:

After a falling edge on the LIN bus followed by a dominant voltage level for longer than the specified value (t_{wu_remote}) and a rising edge on pin LIN will cause a remote wake up. The device switches to Standby Mode and the wake-up request is indicated by an active LOW on pin RxD.

The MLX80031/51 versions offer three wake-up procedures:

- In applications with continuously powered ECU a wake up via mode transition to normal mode is possible (see chapter 4.3 Normal Mode).
- Remote wake-up via LIN bus traffic
  After a falling edge on the LIN bus followed by a dominant voltage level for longer than the specified value(t_{wu_remote}) and a rising edge on pin LIN will cause a remote wake up.
- Local wake-up via a falling edge on pin WAKE
  A falling edge on the pin WAKE and a dominant voltage level for longer than the specified time (t_{wu_WAKE}) will cause a local wake-up. The current for an external switch has to be provided by an external pull up resistor R_{WK}. For a reverse current limitation in case of a closed external switch and a negative ground shift or an ECU loss of ground a protection resistor R_{WK_prot} between pin WAKE and the switch is recommended.
- Local wake-up via a rising edge on pin KL15
  A positive edge on the pin KL15 followed by a high voltage level for a time period t_{wu_KL15} > 250µs results in a local wake-up request. The MLX80031/51 switches to the Standby Mode. The long debouncing time on KL15 suppresses unintentional transients. A high level on KL15 has no influence of switching between modes with EN input. Before a new local wake-up request via KL15 can be started, KL15 have to be switched to low level for a time > 250µs.

5.1. Wake Up Source Recognition in MLX80031/51

The device can distinguish between a local wake-up event (pin WAKE or pin KL15) and a remote wake-up event. The wake-up source flag is set after a local wake-up event and is indicated by an active LOW on pin TxD.
The wake-up flag can be read if an external pull up resistor towards the microcontroller supply voltage has been added and the MLX80031/51 is still in standby mode:

- LOW level indicates a local wake-up event
- HIGH level indicates a remote wake up event

The wake-up request is indicated by an active LOW on pin RxD and can be used for an interrupt.
When the microcontroller confirms a normal mode operation by setting the pin EN to HIGH, both the wake-up request on pin RxD as well as the wake-up source flag on pin TxD are reset immediately.

6. Functionality

6.1. RESET behaviour of MLX8003x/5x

The MLX8003x/5x contains a reset unit which controls the initialization and generation of the reset signal. The *NRES* pin flags the reset state of the MLX8003x/5x. The POR timer will be started if V_S is switched on and $V_{CC} > V_{RES}$ threshold. After the time t_{Res} the *NRES* output is switched from low to high.
The reset unit combines a VCC low voltage detection unit with fixed reset timer. This output is switched from low to high if V_S is switched on and after the time t_{Res} is $V_{CC} > V_{RES}$.
A drop of the V_{CC} voltage will be detected by the low voltage reset unit which generates a reset signal. The MLX8003x/5x will be reinitialized if the V_{CC} voltage rises above the low voltage limit.
If the voltage V_{CC} drops below V_{RES} then the *NRES* output is switched from high to low after the time t_{rr}. This filters short breaks of the V_{CC} voltage and avoids uncontrolled reset generation.

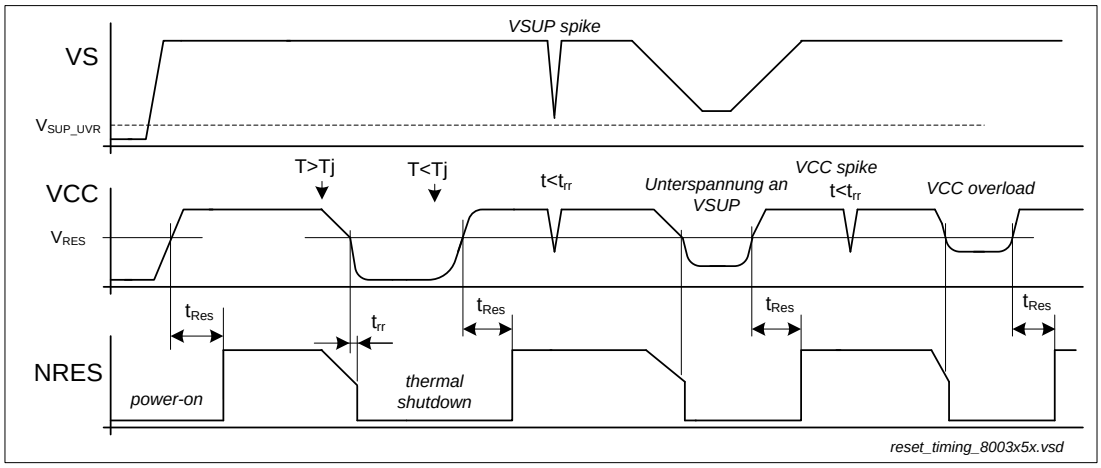


Figure 10: VCC reset behavior

The MLX80031/51 version combines the reset behaviour described above with a window-watchdog unit.
The NRES pin outputs the reset state as well as the watchdog condition. The POR timer will be started if V_{SUP} is switched on and V_{CC} > POR threshold. After the time t_{Res} the RESET output is switched from low to high. The watchdog is disabled during this POR procedure. After the POR delay, the NRES output is switched from low to high and the watchdog starts. In normal mode the NRES pin flags the status of the window watchdog.

6.2. Thermal Shutdown

If the junction temperature T_J is higher than T_{JSHD}, the MLX8003x/5x switches from any mode into Standby Mode. During TSD all functions are switched-off. The transceiver and the voltage regulator are completely disabled; no wake-up functionality is available.
If T_J falls below the thermal recovery temperature T_{JREC}, MLX8003x/5x resumes operation starting from Standby Mode. If EN=H at recovery, chip switches to NORMAL after VCC>VRES and tres. SBY-timeout timer is disabled during TSD.

6.3. VS under voltage reset

The under voltage detection unit prevents an undefined behaviour of the MLX8003x/5x under low voltage condition (VS < V_{SUVR_ON}). If VS drops below V_{SUVR_ON}, the under voltage detection becomes active and the IC will be switched from every state to Init-State followed by Standby Mode with the same behaviour like after VS power-on. With the following increase of VS above V_{SUVR_OFF} the MLX8003x5x remains in Standby Mode and the voltage regulator starts with the initialization sequence (Vcc available). If EN=H at power-up, the chip switches to NORMAL after VCC>VRES and tres.

Remark: In case Vs drops below 5V but still remains above V_{SUVR_ON} , Vcc follows Vs. Vcc is switched off during Vs Undervoltage reset.

6.4. LIN-Transceiver

The MLX8003x/5x has an integrated bi-directional bus interface device for data transfer between LIN bus and the LIN protocol controller.
The transceiver consists of a driver with slew rate control, wave shaping and current limitation and a receiver with high voltage comparator followed by a debouncing unit.

Transmit Mode

During transmission the data at the pin TxD will be transferred to the LIN driver to generate a bus signal. To minimize the electromagnetic emission of the bus line, the LIN driver has an integrated slew rate control and wave shaping unit.
Transmitting will be interrupted in the following cases:

- Sleep Mode
- Silent Mode
- Thermal Shutdown active
- Power on Reset

The recessive LIN bus level is generated from the integrated 30k pull up resistor in serial with an active diode This diode prevents the reverse current of V_{LIN} during differential voltage between VS and LIN ($V_{LIN}>V_S$).
No additional termination resistor is necessary to use the MLX8003x/5x in LIN slave nodes. If this ICs are used for LIN master nodes it is necessary that the LIN pin is terminated via an external 1kΩ resistor in series with a diode to VBAT.

Receive Mode

The data signals from the LIN pin will be transferred continuously to the pin RxD. Short spikes on the bus signal are suppressed by the implemented debouncing circuit.

Slew Modes and Data rates

The MLX8003x/5x consists a ***constant slew rate*** transceiver which means that the bus driver works with a mode depended slew rate. In normal mode the slew rate is typical 1.6 V/µs (max. baud rate 20kbit/s) and in low slew mode typical 0.8 V/µs. The lower slew rate in low slew mode associated with a baud rate of 10.4kbit/s improves the EME behaviour.
The LIN transceiver of MLX8003x/5x is compatible to the physical layer specification according to LIN 2.x specification for data rates up to 20kbit/s and the SAE specification J2602 for data rates up to 10.4kbit/s.
The constant slew rate principle is very robust against voltage drops and can operate with RC- oscillator systems with a clock tolerance up to ±2% between 2 nodes.

Low Slew Mode

In this mode the slew rate is switched from the normal value of typical 1.6V/µs to a low value of typical 0.8V/µs. This mode is optimized to send with a maximum baud rate of 10.4kbit/s (acc. to SAE J2602). Because of this reduction of the slew rate the EME behaviour is improved especially in the frequency range of 100 kHz to 10MHz.

6.5. Voltage Regulator

The MLX8003x/5x has an integrated low drop linear regulator with a p-channel-MOSFET as driving transistor. This regulator outputs a voltage of 3.3V/5V ±2% and a current of ≤70mA within an input voltage range of $6V \leq V_{SUP} \leq 18V$. The current limitation unit limits the output current for short circuits or overload to 130mA respectively drop-down of the V_{CC} voltage.

7. Window-Watchdog (only MLX80031/51)

The integrated window watchdog unit observes the correct function of the connected Microcontroller. The required timing can be programmed with an external resistor connected to the pin RB_{WD}. This resistor defines together with an internal capacitor the watchdog oscillator frequency. The watchdog is re-triggered by the Microcontroller via the NWDI input. The watchdog status is represented by the NRES pin.
Negative edges on NWDI reset the watchdog timer. If no pulse is received at NWDI, the MLX80051/31 generates low pulses on the NRES output with a pulse width of t_{WDres} and a period of t_{WDper}.

7.1. MLX80031/51 Watchdog Behaviour

After power-on and elapsed reset time t_{res}, the window watchdog starts operation with a rising edge on pin NRES. This start is independent from Standby or Normal Mode.

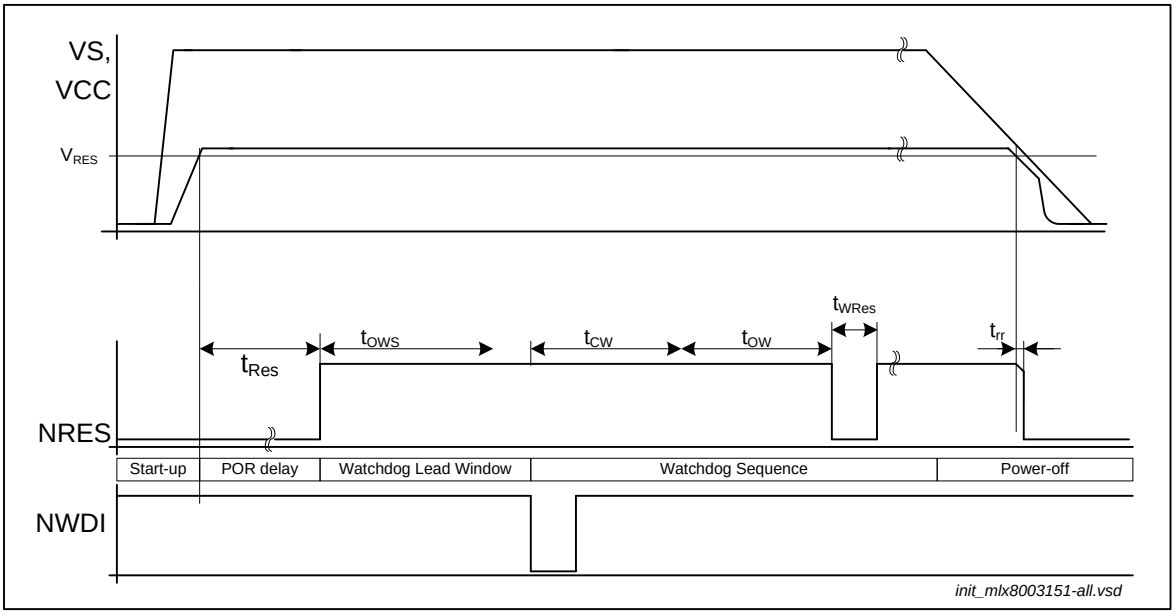


Figure 11: MLX80031/51 Watchdog behavior

After t_{res} the window watchdog unit starts with the Lead Time State. In this state the watchdog clock periods ($1/f_{wdosc}$) are counted 7895(=nlead) times. A falling edge on NWDI pin within this lead time stops the lead counter and activates the Closed Window State with ncw=1053. Thereafter follows the Open Window State with counter start value of now=1105. In case the lead counter elapses, the watchdog enters the Reset State and starts the reset timer with time tres.

Close Window State and Open Window State are the normal states of the window watchdog. At each of these states runs a counter with the watchdog clock signal. The CWT counter runs always to the end. The watchdog does not trigger when the NWDI trigger signal arrives within the Open Window State.
A NWDI trigger pulse outside the Open Window State generates a reset condition and the NRES output switches to low for the time t_{WDres} (see Figure 12).

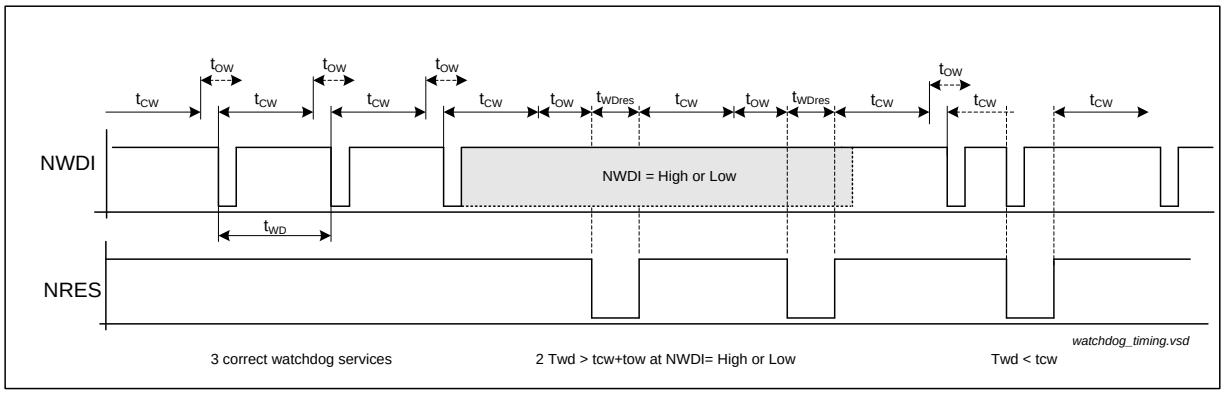


Figure 12: Watchdog timing

7.2. All watchdog start-up scenarios

7.2.1. After power-on and initialization

Watchdog starts after VCC ramp up and elapsed time of reset timer (typ. 4ms) with Lead Time State. MLX80031/51 is in Standby or Normal Mode.

7.2.2. Wake up indicated transition to Standby Mode from Sleep or Silent Mode

Watchdog starts immediately with activation of Standby Mode (SBY_MODE = 1). Waking up from Sleep Mode the VCC regulator ramps up and the reset timer starts. The reset timer has in this case no influence on the watchdog start.

7.2.3. Undervoltage reset on VCC on Normal Mode or Silent Mode

MLX80031/51 goes to Standby Mode. Running watchdog process is stopped and cleared. With active undervoltage reset the signal the output pin NRES goes to low. Leaving undervoltage reset starts the reset timer (4ms) and thereafter starts a new watchdog cycle.

7.2.4. EN indicated transition from Silent Mode to Normal Mode

Mode control changes from Silent Mode to Normal Mode. Watchdog starts immediately with activation of Normal Mode in Closed Window State.

7.3. Calculation of Watchdog Period

The RC-oscillator of MLX80031/51 which generates the responsible timing of the watchdog has a tolerance of ±15%. This has the consequence that also the watchdog window times t_{CW} and t_{OW} variants with this tolerance.

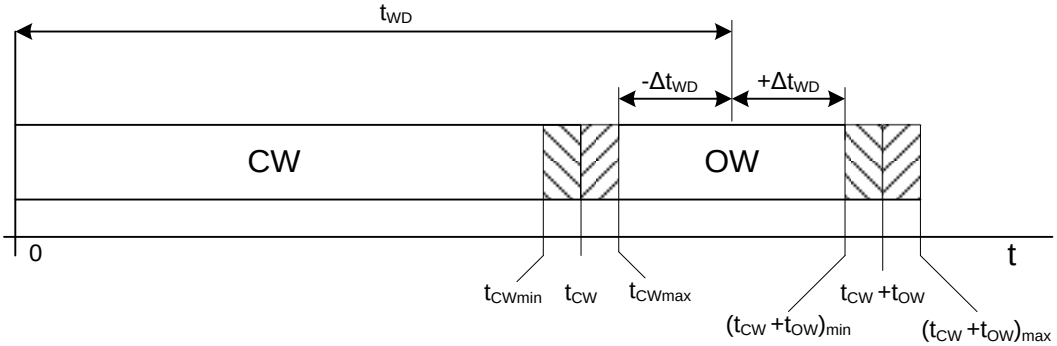


Figure 13: Watchdog open and close window tolerances

The ideal watchdog period can be calculated with:

$$t_{WD\_id} = t_{CW} + \frac{1}{2} * t_{OW}$$

The average value t_{WD} of the real usable watchdog trigger time under consideration of the oscillator tolerance is:

$$t_{WD} = (t_{CW\,min} + t_{OW\,min} + t_{CW\,max})/2 \qquad \text{[EQ1]}$$

The allowed tolerance Δt_{WD} is:

$$\Delta t_{WD} = (t_{CW\,min} + t_{OW\,min} - t_{CW\,max})/2 \qquad \text{[EQ2]}$$

With the definition of t_{CW} = ncw * (1± TOL) * t_{WDOSC} and t_{OW} = now * (1± TOL) * t_{WDOSC} from [EQ1] t_{WD} can be calculated with:

$$t_{WD} = t_{WDOSC}(2 \cdot ncw + now \cdot (1 - TOL))/2 \qquad \text{[EQ3]}$$

and with [EQ2]:

$$\Delta t_{WD} = t_{WDOSC}(now \cdot (1 - TOL) - 2 \cdot TOL \cdot ncw)/2 \qquad \text{[EQ4]}$$

The variation Δt_{WD} will be normalized to the mean value t_{WD} and both counter values set in a relationship of a=now/ncw, then follows for the relative deviation:

$$t_{WDTOL} = \frac{a \cdot (1 - TOL) - 2 \cdot TOL}{2 + a \cdot (1 - TOL)} \qquad \text{[EQ5]}$$

The watchdog trigger time as well as the tolerance depends only on the oscillator frequency respectively the period t_{WDOSC}, if there are fixed values for both counters (ncw and now) and oscillator tolerance.

Implemented in MLX80031/51 is a precision RC oscillator with a tolerance of TOL = ±15%. Combined with the relation of counter values a=1.04 reached them a tolerance of trigger time of ±20%.

Symbol	Parameter	Value
TOL	Tolerance WD oscillator	±15%
ncw	Close window counter	1053
now	Open window counter	1105
t_{WDTOL}	Tolerance WD-trigger time	±20%

Table 9: Parameters of Window Watchdog

With the predefined counter values (ncw and now) and the oscillator tolerance TOL are the trigger time of watchdog and them tolerance only be calculated by the selection of oscillator frequency, or their period t_{WDOSC}.

Fort the used precision RC-oscillator the oscillator period is shown as a linear function of the external resistor RB_{WD}.

$$tWDosc\ [\mu s] = 0.37505 * RBWD\ [k\Omega] + 0.547 \qquad \text{[EQ6]}$$

The trigger period can be calculated with the help of EQ3 together with Table 9 – Parameter of Window Watchdog

$$tWD\ [ms] = 0.571061 * RBWD\ [k\Omega] + 0.832879 \qquad \text{[EQ7]}$$

Or convert to RB_{WD}:

$$RBWD\ [k\Omega] = 1.75113 * twd\ [ms] - 1.45847 \qquad \text{[EQ8]}$$

Some typical samples of different RD_{WD} values and the corresponding watchdog times for 35°C:

RB_{WD} [kΩ]	t_{WDOSC} [µs]	Close Window t_{CW} [ms]	Open Window t_{OW} [ms]	Trigger Period t_{WD} [ms]
20	8.06	8.47	8.89	12.25
30	11.79	12.42	13.04	17.96
40	15.54	16.37	17.18	23.68
50	19.30	20.32	21.33	29.39
60	23.05	24.27	25.47	35.10

Table 10: Window Watchdog Timing Selection.

8. Fail-safe features

Loss of battery

If the ECU is disconnected from the battery, the LIN bus pin is in high impedance state. There is no impact to the bus traffic and to the ECU itself. Reverse current is limited to < 20µA

Loss of Ground

In case of an interrupted ECU ground connection there is no influence to the bus line. The current from the ECU to the LIN bus is limited by the weak pull up resistor of the pin LIN. The slave termination resistor is disconnected in order to fulfil the SAE J2602 requirements for the loss of ground current (<100µA @12V).

Short circuit to battery

The transmitter output current is limited to the specified value in case of short circuit to battery in order to prevent high current densities and thermal hot spots in the LIN driver.

Short circuit to ground

If the LIN bus wiring is shorted to negative shifted ground levels, there is no current flow from the ECU ground to the bus and no distortion of the bus traffic occurs.

If the controller detects a short circuit of the LIN bus to ground the transceiver can be set into sleep mode. Additionally the internal slave termination resistor is switched off and only a weak pull up termination is applied to the LIN bus (typ. 50µA). If the failure disappears, the bus level will become recessive again and will wake up the system even if no local wake up occurs or is possible.

Thermal overload

All MLX8003x/5x versions are protected against thermal overloads. If the chip temperature exceeds the specified value, the transmitter is disabled until thermal recovery and the following recessive to dominant transition on pin TxD. The receiver is still working while thermal shutdown.

Undervoltage lock out

If the battery supply voltage is missing or decreases below the specified value (VS_UV), the transmitter is disabled to prevent undefined bus traffic. While in sleep mode, the MLX8003x/5x enters the Standby Mode if Vs drops below the internal power on reset threshold.

Open Circuit protection

- The pin TxD provides a pull up resistor to VCC. The transmitter cannot be enabled.
- The pin EN provides a pull down resistor to prevent undefined normal mode transitions.
- The pin NWDI provides a pull up resistor to VCC. The window watchdog generates NRES pulse.
- The pin MODE provides a pull down resistor to GND. No influence on window watchdog.
- If the battery supply voltage is disconnected, the pin RxD is floating.
- The pin WAKE provides a weak pull up current towards supply voltage Vs to prevent local wake-up requests.
- The pin KL15 provides a weak pull down current towards GND to prevent local wake-up requests.

Short circuit RxD, NRES against GND or VCC

Both outputs are short circuit proof to VCC and ground.

9. Application Hints

9.1. Safe Operating Area

The linear regulator of the MLX8003x/5x operates with input voltages up to 27 V and can output a current of 70 mA. The maximum power dissipation limits the maximum output current at high input voltages and high ambient temperatures. The output current of 70 mA at an ambient temperature of T_A = 125°C is only possible with small voltage differences between V_S and V_{CC}.

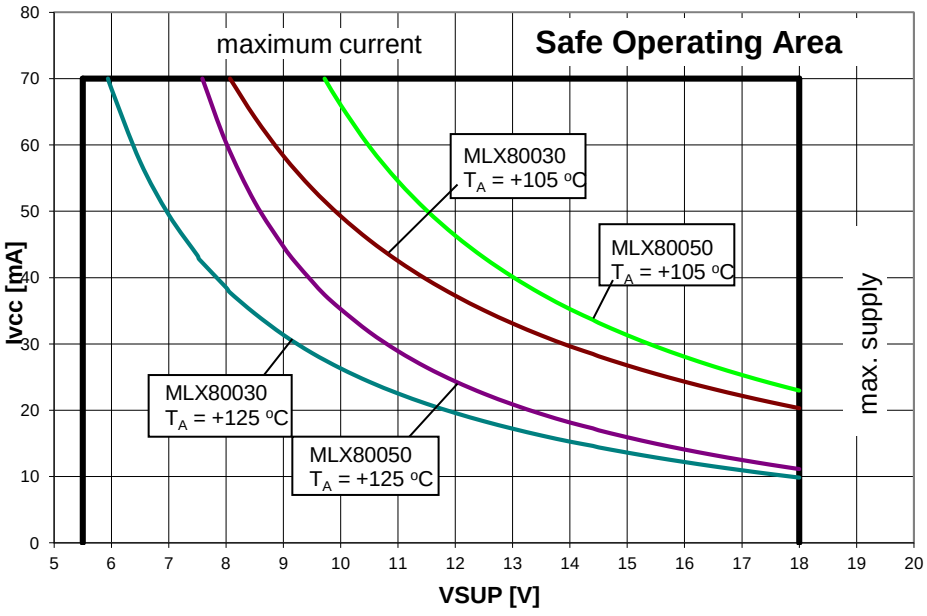


Figure 14: Safe operating area for MLX80030/50 in SOIC-8 for Vsup up to 18V

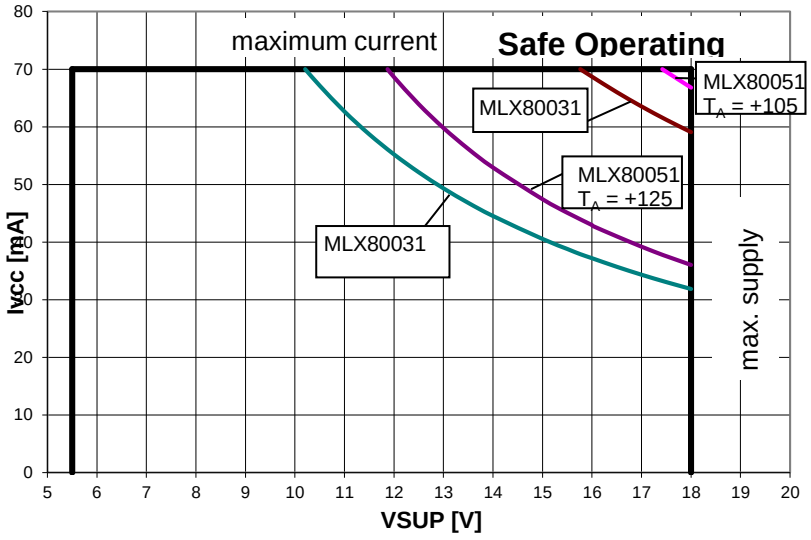


Figure 15: Safe operating area for MLX80031/51 in QFN20 for Vsup up to 18V

9.2. Application Circuitry

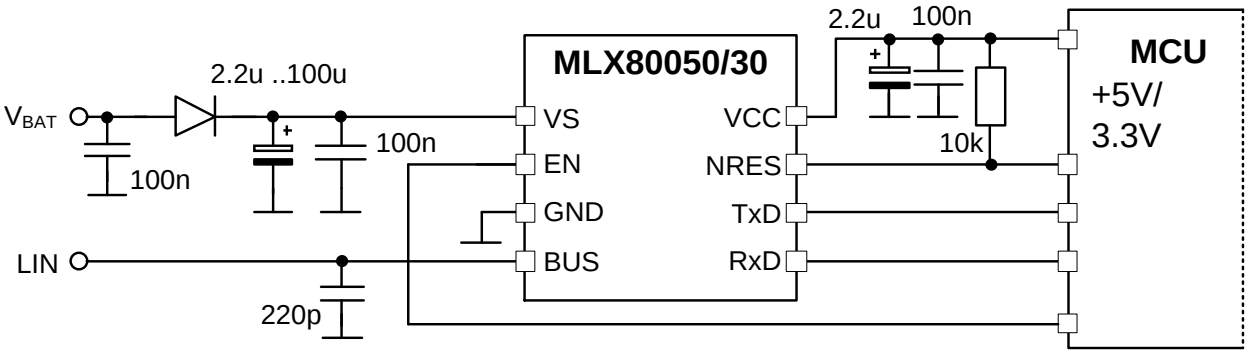


Figure 16: Application circuit with MLX80050 or MLX80030 (slave node)

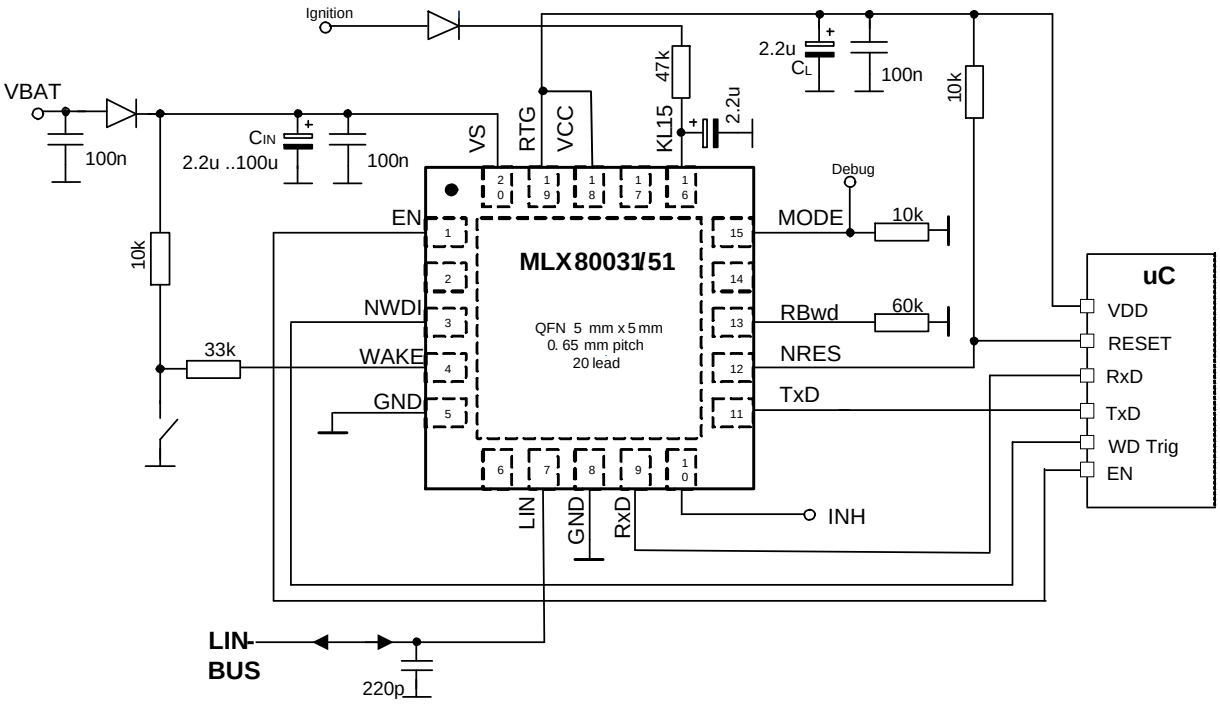


Figure 17: Application circuit with MLX80031 or MLX80051 (slave node)

To minimize the influence of EMI on the bus line an 220pF capacitor should be connected directly to the LIN pin (see Figure 17). This EMI-Filter assures that the RF injection into the IC from the LIN bus line has no effect or will be limited. It is also possible to use LC- or RC-filters. The dimensions of C-L or R-L depend on the corner frequency, the maximum LIN bus capacitance (10nF) and the compliance with the DC- and AC LIN bus parameters.

10. ESD and EMC

10.1. Recommendations for Actuator products

In order to minimize EMC influences, the PCB has to be designed according to EMC guidelines. Actuators products are ESD sensitive devices and have to be handled according to the rules in IEC61340-5-2.
Actuators products will apply the requirements in the application according to the specification, to ISO7637-2, -3 and ISO16750-2.

Prototype samples of actuators products will be evaluated according AEC-Q100-002. The result will be published after qualification. After ESD stress single parameters may be shifted out of their limit, but IC function will still be correctly.

10.1.1. Automotive Qualification Test Pulses

That means that automotive test pulses are applied to the module in the application environment and not to the single IC. Therefore attention must be taken, that only protected pins (protection by means of the IC itself or by means of external components) are wired to a module connector. In the recommended application diagrams, the reverse polarity diode together with the capacitors on supply pins, the protection resistors in several lines and the load dump protected IC itself will protect the module against the below listed automotive test pulses. The exact value of the capacitors for the application has to be figured out during design-in of the product according to the automotive requirements.

For the LIN pin the specification “LIN Physical Layer Spec 2.1 (Nov. 24, 2006)” is valid.
Supply Pin VS is protected via the reverse polarity diode and the supply capacitors. No damage will occur for defined test pulses. A deviation of characteristics is allowed during pulse 1 and 2; but the module will recover to the normal function after the pulse without any additional action. During test pulse 3a, 3b, 5 the module will work within characteristic limits.

10.1.2. Test Pulses On supply Lines

Parameter	Symbol	Min	Max	Dim	Coupling	test condition, functional status
Transient test pulses in accordance to ISO7637-2 (supply lines) & , VS=13.5V, TA=(23 ± 5)°C & (Document: “Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications”; Audi, BMW, Daimler, Porsche, VW; 2009-12-02)						
Test pulse #1	vpulse1	-100		V	Direct	5000 pulses, functional state C
Test pulse #2a	vpulse2a		75	V	Direct	5000 pulses, functional state A
Test pulse #3a	vpulse3a	-150		V	Direct	1h,functional state A
Test pulse #3b	vpulse3b		100	V	Direct	1h,functional state A
Load dump test pulse in accordance to ISO16750-2 (supply lines), VS=13.0V, TA=(23 ± 5)°C						
Test pulse #5b	vpulse5b	65 (+13V (VS))	87 (+13V (VS))	V	Direct	1 pulse clamped to 27V (+13V (VS)), (32V (+13V (VS))for applications for north America), functional state C

Table 11: Test pulses Supply Line

10.1.3. Test pulses on Pin LIN

Parameter	Symbol	Min	Max	Dim	Coupling	test condition, functional status
Transient test pulses in accordance to ISO7637-3, VS=13.5V, TA=(23 ± 5)°C & (Document: "Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications"; Audi, BMW, Daimler, Porsche, VW; 2009-12-02)						
Test pulse 'DCC slow –'	Vpulse_ slow+	-100		V	Direct capacitive coupled: 1nF	1000 pulses, functional state D
Test pulse 'DCC slow +'	Vpulse_ slow-		75	V	Direct capacitive coupled: 1nF	1000 pulses, functional state D
Test pulse 'DCC fast a'	Vpulse_ fast_a	-150		V	Direct capacitive coupled: 1nF	10 min, functional state D
Test pulse 'DCC fast b'	Vpulse_ fast_b		100	V	Direct capacitive coupled: 1nF	10 min, functional state D

Table 12: Test pulses LIN

10.1.4. Test pulses on signal lines

Parameter	Symbol	Min	Max	Dim	Coupling	test condition, functional status
Transient test pulses in accordance to ISO7637-3 (signal lines). VS=13.5V, TA=(23 ± 5)°C						
Test pulse 'DCC slow –'	Vpulse_ slow+	-30	-8	V	Direct capacitive coupled: 100nF	1000 pulses, functional state C
Test pulse 'DCC slow +'	Vpulse_ slow-	+8	+30	V	Direct capacitive coupled: 100nF	1000 pulses, functional state A
Test pulse 'DCC fast a'	Vpulse_ fast_a	-60	-10	V	Direct capacitive coupled: 100pF	10 min, functional state A
Test pulse 'DCC fast b'	Vpulse_ fast_b	10	40	V	Direct capacitive coupled: 100pF	10 min, functional state A

Table 13: Test pulses signal lines

Description of functional state

A: All functions of the device are performed as designed during and after the disturbance occurs.

B: All functions of the device are performed as designed during the disturbance occurs. One or more functions can violate the specified tolerances. All functions return automatically within their normal limits after the disturbances is removed..

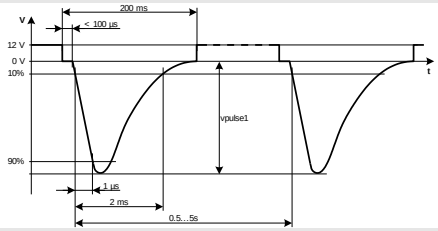
C: A function of a device does not perform as designed during the disturbance occurs but returns automatically to the normal operation after the disturbances is removed.

D: A function of a device does not perform as designed during the disturbance occurs and does not return automatically to the normal operation after the disturbances is removed. The device needs to be reset by a simple operation/action to return to the specified limits/function.

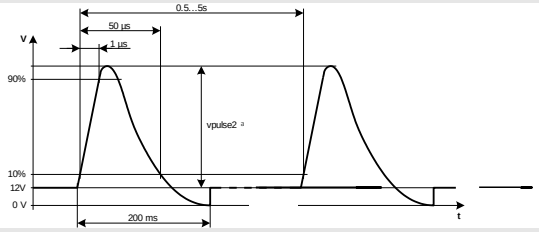
E: One or more functions of a device do not perform as designed during and after the disturbance occurs and does not return automatically to the normal operation after the disturbances is removed. After a reset of the device, it does not return to the specified limits/function. The device needs to be repaired or replaced.

10.1.5. EMV Test pulse definition

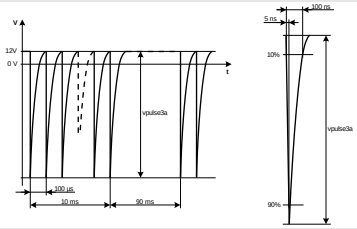
Test Pulse 1
Ri = 10 Ohm



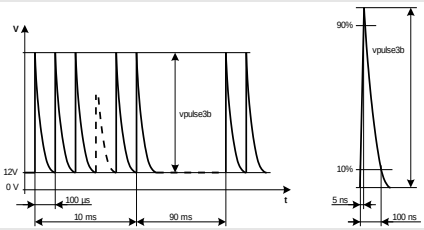
Test pulse 2a
Ri = 2 Ohm



Test Pulse 3a
Ri = 50 Ohm



Test Pulse 3b
Ri = 50 Ohm



Test Pulse 5a (Load Dump)
Ri = 0.5Ohm (clamped to 45V during test)

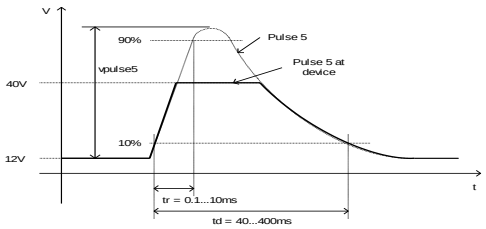
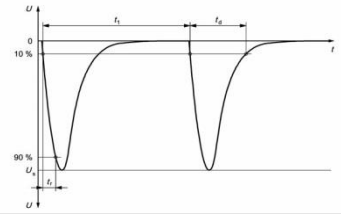


Table 14: Test pulses shapes ISO7637-2

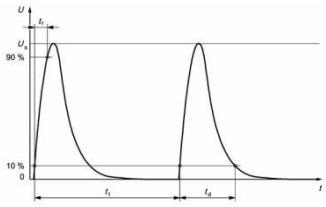
EMV Test Pulse shapes (ISO7637-3 (non-supply lines))

Test Pulse 'DCC slow -'
Ri = 2 Ohm



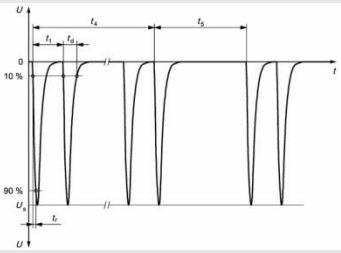
Parameters	
U_s	To be defined in test plan
t_r	⩽1 µs
t_d	0,05 ms
t_1	0,5 s to 5 s
R_i	2 Ω

Test pulse 'DCC slow +'
Ri = 2 Ohm



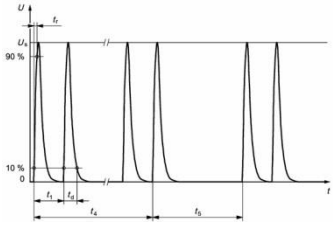
Parameters	
U_s	To be defined in test plan
t_r	⩽1 µs
t_d	0,05 ms
t_1	0,5 s to 5 s
R_i	2 Ω

Test Pulse 'Fast a, DCC'
Ri = 50 Ohm



Parameters	12 V system
U_s in V	See Table B.1
t_r in ns	5
t_d in µs	0,1
t_1 in µs	100
t_4 in ms	10
t_5 in ms	90
R_i in Ω	50

Test Pulse 'Fast b, DCC'
Ri = 50 Ohm

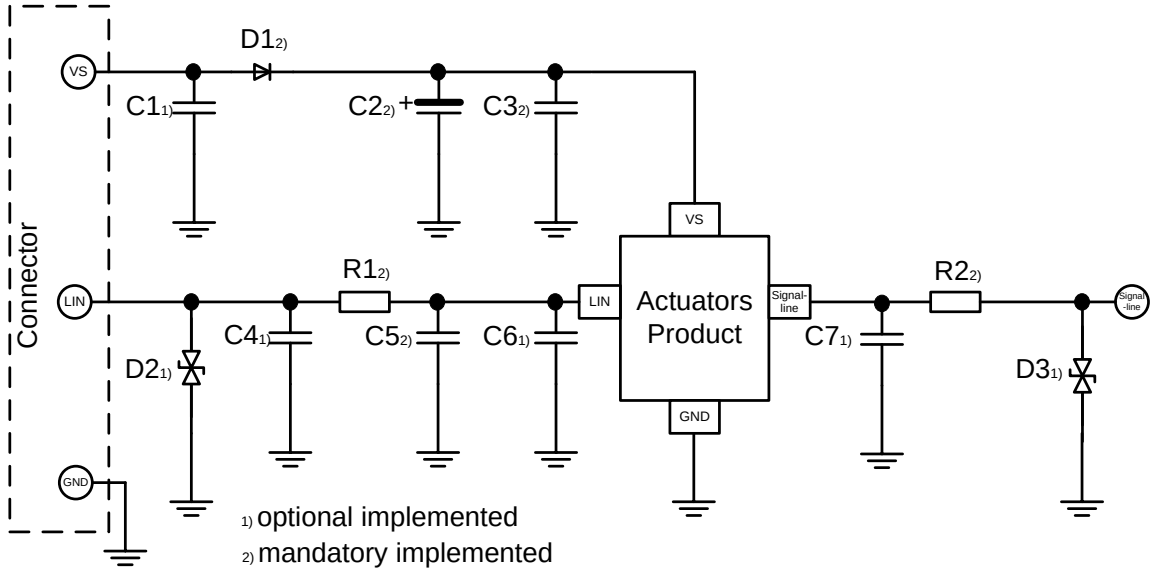


Parameters	12 V system
U_s in V	See Table B.1
t_r in ns	5
t_d in µs	0,1
t_1 in µs	100
t_4 in ms	10
t_5 in ms	90
R_i in Ω	50

Table 15: Test pulses shapes ISO7637-3

10.2. Typical Application Circuitry

In order to minimize EMC influences, the external application circuitry shall be designed as followed:



10.2.1. External Circuitry on Supply Lines

In order to minimize EMC influences, the external application circuitry shall be designed as followed:

Name	Mounting	Min	Recommended	Max	Dim	Comment
C1	recommended	-	100	-	nF	Ceramic SMD: 10%, 0805, ≥50V; close to the connector
D1	mandatory					Inverse-polarity protection diode
C2	mandatory	1	22	100	µF	Tantal SMD: 10%, 7343, 35V
C3	mandatory	-	100	-	nF	Ceramic SMD: 10%, 0805, ≥50V; close to the pin

10.2.2. External Circuitry on LIN Lines

In order to minimize EMC influences, the external application circuitry shall be designed as followed:

Name	Mounting	Min	Recommended	Max	Dim	Comment
D2	no	-	PESD1LIN	-		ESD protection Diode: SOD323 close to the connector; optional part
C4	no	-	-	-	pF	Ceramic SMD: 10%, 0805, ≥50V; $C_{Slave} \leq C_{D2}+C_4+C_5+C_6+C_{IC}$ $C_{Slave} \leq 250pF$; optional part
R1	mandatory	-	0	-	Ω	Serial resistor: 0805; or optional Ferrite
C5	mandatory	-	220	-	pF	Ceramic SMD: 10%, 0805, ≥50V; $C_{Slave} \leq C_{D2}+C_4+C_5+C_6+C_{IC}$ $C_{Slave} \leq 250pF$
C6	no	-	-	-	pF	Ceramic SMD: 10%, 0805, ≥50V; $C_{Slave} \leq C_{D2}+C_4+C_5+C_6+C_{IC}$ $C_{Slave} \leq 250pF$; optional part

10.2.3. External Circuitry on Signal Lines

In order to minimize EMC influences, the external application circuitry shall be designed as followed:

Name	Mounting	Min	Recommended	Max	Dim	Comment
C7	no	0.1	1	100	nF	Ceramic SMD: 10%, 0805, ≥50V; optional part
R2	mandatory	0	560	1000	Ω	Serial resistor: 0805; or optional Ferrite
D3	no	-	PESD1LIN	-		ESD protection Diode: SOD323 close to the connector; optional part

11. Mechanical Specification

11.1. SOIC8 package

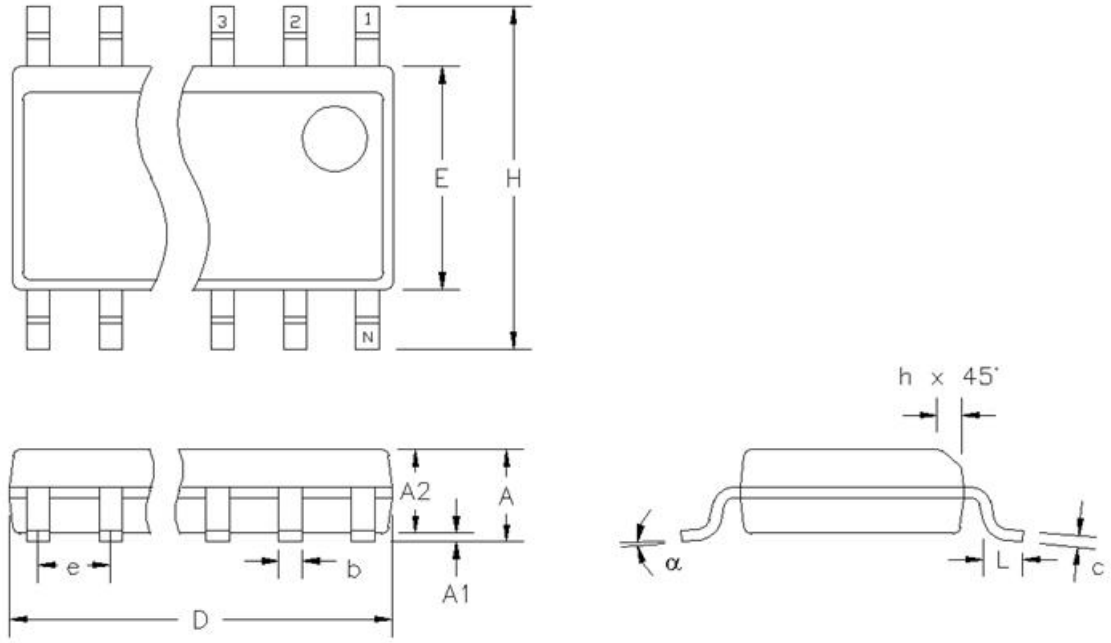


Figure 18: SOIC8 Drawing

Small Outline Integrated Circuit (SOIC), SOIC8, 150mil

N		A	A1	A2	D	E	H	L	b	c	e	h	α	
8	min	1.52	0.10	1.37	4.80	3.81	5.80	0.41	0.35	0.19	1.27	0.25	0°	[1]
	max	1.73	0.25	1.57	4.98	3.99	6.20	1.27	0.49	0.25	BSC	0.50	8°	[2]

Table 16: SOIC8 dimensions

11.2. QFN20 5x5 package

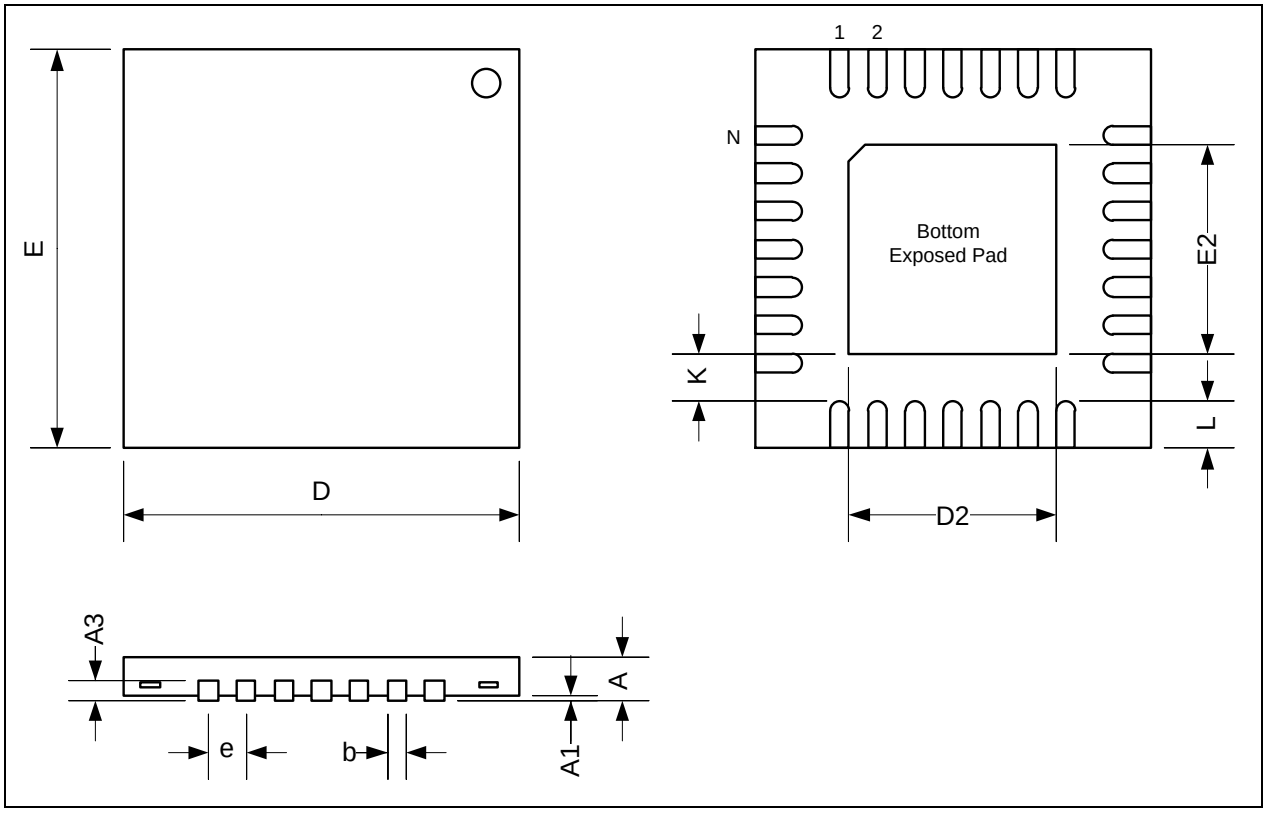


Figure 19: QFN20 Drawing

Symbol	A	A1	A3	b	D	D2	E	E2	e	K	L	N [3]	ND [4]	NE [4]	
min	0.80	0	0.20	0.25	5.00	3.00	5.00	3.00	0.65	0.20	0.45	20	5	5	[1] [2]
max	1.00	0.05		0.35		3.25		3.25			0.65				

Table 17: QFN20 Package Dimensions

[1] Dimensions and tolerances conform to ASME Y14.5M-1994
[2] All dimensions are in Millimeters. All angels are in degrees
[3] N is the total number of terminals
[4] ND and NE refer to the number of terminals on each D and E side respectively

12. Revision History

Version	Changes	Remark	Date
001	First Release	1st Release	April 2012
002	• For TSD added: "If EN=H at recovery, chip switches to NORMAL after VCC>VRES and tres" and "SBY-timeout timer is disabled during TSD" • For TSD removed explicit values and kept parameter name only. • For Vs_uvr added: "If EN=H at power-up, chip switches to NORMAL after VCC>VRES and tres" • Changed state diagram: sleep mode can be left with EN = H (was a L-H transition in A version of the device), refers to Errata 80050AA-07.		June 2012
003	• ESD robustness level adapted to Conformance Test Report • Static Characteristics adapted to CPK-Values • Block Diagram updated • Corrected short description of product		Dec 2012
004	• Removed 06.05, 09.05, 13.05 • Changed 05.02 to 200mV (5V) and 100mV (3.3V) • Changed 06.03 and 13.03 to 700mV • Changed 09.03 to 600mV • Added MODE pin to parameter list • Changed 15.05 to LL = 2.7V and UL to 3.3V • Changed 14.01 to 0.6V at 2mA • Changed 08.03 to LL = 30 • Changed 02.00 to LL = 400 and UL to 1500 • Changed Tjshd to 155/170/190°C • Changed 12.04 and 12.05 UL to 20uA • Changed 03.05 to relevance “C” (only for characterization) • Added 17.06 Watchdog safety oscillator • Changed 3.01 for 80030/31 to UL = 3.201 and UL = 3.399		Mar 2013
005	• Corrected value “e” of QFN package data to “0.65”		Apr 2013
006	• Changed 15.01 • Changed 1.03 LL to 40mV • Changed 3.09 LL to -135mA and UL to -75mA • Changed ESD capability of LIN pin to +/-6kV		July 2013
007	• Changed operating voltage to max. 27V • Changed table 2, nominal operating voltage, max to 27V • Update 3.09: split temperature ranges • Changed 12.03 to min: -400µA • Changed 12.06 to min: -10µA, max: 50µA • Changed 6.04 to typ: 125 kΩ, max: 250 kΩ • Changed 12.01 to 80µA		Feb 2014
008	• Added condition for thermal resistance • Updated chapter 4.1, tables 7 and 8 for TxD and RxD values depending on the mode and EN = H transition from Sleep Mode to Normal Mode		April 2014

	• Changed operating voltage to 27V max in application hints 9.1 • Re-phrased information to EMC compliance in 9.2.2 • LIN: Changed parameter 12.10 and added parameter 12.12 to Lin spec 2.x and compatible to SAE J2602, split parameter 12.07 into dominant and recessive		
009	• Updated product codes to “wettable flanks”		Nov 2014
010	• Silent Mode for Silicon Version B not supported • Silicon Version C added, support of silent mode		Feb 2015
011	• Silicon Version B removed • Changed 1.01, 1.02 VS under voltage reset • Changed 2.01 supply current sleep mode • Changed 2.02 supply current silent mode • Addition of 18.11 Wake up time vs. EN • Update state diagram (Fig 5) • Update of paragraph ESD and EMC		Jun 2016
012	• Update of disclaimer • Update of paragraph 6.2 Thermal shutdown • Update of paragraph 7.3 Calculation of Watchdog Period • Update of paragraph 8 Fail-safe features • Changed R_{BWD} max to 60kΩ and updated all references to it • Changed product order code from -000 to – 100 • Updated SOIC8 drawing and dimensions table (Table 16) • Updated Figure 5 – Operational modes • Updated EQ6 , EQ7, EQ8 on page 34 • Added Parameter TXD hold time for mode change in AC parameter table		Aug 2019
013	• Updated product order codes to latest IC version		Nov 2019

13. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis recommends reviewing on our web site the General Guidelines soldering recommendation (http://www.melexis.com/Quality_soldering.aspx) as well as trim&form recommendations (http://www.melexis.com/Assets/Trim-and-form-recommendations-5565.aspx).

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/quality.aspx

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