TH71221

27 to 930MHz FSK/FM/ASK Transceiver

Features

- ❒ Single chip solution with only a few external components
- ❒ Stand-alone fixed-frequency user mode
- ❒ Programmable multi-channel user mode
- ❒ Low current consumption in active mode and very low standby current
- ❒ PLL-stabilized RF VCO (LO) with internal varactor diode
- ❒ Lock detect output in programmable user mode
- ❒ On-chip AFC for extended input frequency acceptance range
- ❒ 3wire bus serial control interface
- ❒ FSK/ASK mode selection
- ❒ FSK for digital data or FM for analog signal reception
- ❒ RSSI output for signal strength indication and ASK reception
- ❒ Peak detector for ASK detection
- ❒ Switchable LNA gain for improved dynamic range
- ❒ Automatic PA turn-on after PLL lock
- ❒ ASK modulation achieved by PA on/off keying
- ❒ 32-pin Quad Flat Lead Package (QFN)

Ordering Code

Product Code	**Temperature Code**	**Package Code**	**Option Code**	**Packing Form Code**
TH71221	E	LQ	BAA-000	RE
TH71221	E	LQ	BAA-000	TU

Legend:

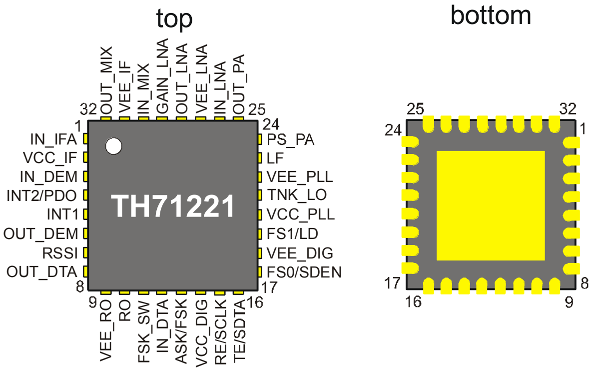
Temperature Code:	E for Temperature Range -40°C to 85°C
Package Code:	LQ for QFN,
Packing Form:	RE for Reel, TU for Tube

Ordering example: TH71221ELQ-BAA-000-RE

Application Examples

- ❒ General bi-directional half duplex digital data RF signaling or analog signal communication
- ❒ Remote Keyless Entry (RKE)
- ❒ Low-power telemetry systems
- ❒ Alarm and security systems
- ❒ Wireless access control
- ❒ Garage door openers
- ❒ Networking solutions
- ❒ Active RFID tags
- ❒ Remote controls
- ❒ Home and building automation

Pin Description



General Description

The TH71221 is a single chip FSK/FM/ASK transceiver IC. It is designed to operate in low-power multi-channel programmable or single-channel stand-alone, half-duplex data transmission systems. It can be used for applications in automotive, industrial-scientific-medical (ISM), short range devices (SRD) or similar applications operating in the frequency range of 300 MHz to 930 MHz. In programmable user mode, the transceiver can operate down to 27 MHz by employing an external VCO varactor diode.

Table of Content

1 Theory of Operation

1.1 General

The main building block of the transceiver is a programmable PLL frequency synthesizer that is based on an integer-N topology. The PLL is used for generating the carrier frequency during transmission and for generating the LO signal during reception. The carrier frequency can be FSK-modulated either by pulling the crystal or by modulating the VCO directly. ASK modulation is done by on/off keying of the power amplifier. The receiver is based on the principle of a single conversion superhet. Therefore the VCO frequency has to be changed between transmit and receive mode. In receive mode, the default LO injection type is low-side injection.

The TH71221 transceiver IC consists of the following building blocks:

- Low-noise amplifier (LNA) for high-sensitivity RF signal reception with switchable gain
- Mixer (MIX) for RF-to-IF down-conversion
- IF amplifier (IFA) to amplify and limit the IF signal and for RSSI generation
- Phase-coincidence FSK demodulator with external ceramic discriminator or LC tank
- Operational amplifier (OA1), connected to demodulator output
- Operational amplifier (OA2), for general use
- Peak detector (PKDET) for ASK detection
- Control logic with 3wire bus serial control interface (SCI)
- Reference oscillator (RO) with external crystal
- Reference divider (R counter)
- Programmable divider (N/A counter)
- Phase-frequency detector (PFD)
- Charge pump (CP)
- Voltage controlled oscillator (VCO) with internal varactor diode
- Power amplifier (PA) with adjustable output power

1.2 Technical Data Overview

- Frequency range: 300 MHz to 930 MHz in programmable user mode
- Extended frequency range with external VCO varactor diode: 27 MHz to 930 MHz
- 315 MHz, 433 MHz, 868 MHz or 915 MHz fixed-frequency settings in stand-alone mode
- Power supply range: 2.2 V to 5.5 V
- Temperature range: -40 °C to +85 °C
- Standby current: 0.05 µA
- Operating current in receive: 6.5 mA (low gain)
- Operating current in transmit: 12 mA (at -2 dBm)
- Adjustable RF power range: -20 dBm to +10dBm
- Sensitivity: -105 dBm at FSK with 180 kHz IF filter BW
- Sensitivity: -107 dBm at ASK with 180 kHz IF filter BW
- Max. data rate with crystal pulling: 20 kbps NRZ
- Max. data rate with direct VCO modulation: 115 kbps NRZ
- Max. input level: -10 dBm at FSK and -20 dBm at ASK
- Input frequency acceptance: ± 10 to ± 150 kHz (depending on FSK deviation)
- FM/FSK deviation range: ±2.5 to ±80 kHz
- Analog modulation frequency: max. 10 kHz
- Crystal reference frequency: 3 MHz to 12 MHz
- External reference frequency: 1 MHz to 16 MHz

1.3 Note on ASK Operation

Optimum ASK performance can be achieved by using an 8-MHz crystal for operation at 315 MHz, 434 MHz and 915 MHz. For details please refer to the software settings shown in sections 7.4 and 7.6. FSK operation is the preferred choice for applications in the European 868MHz band.

1.4 Block Diagram

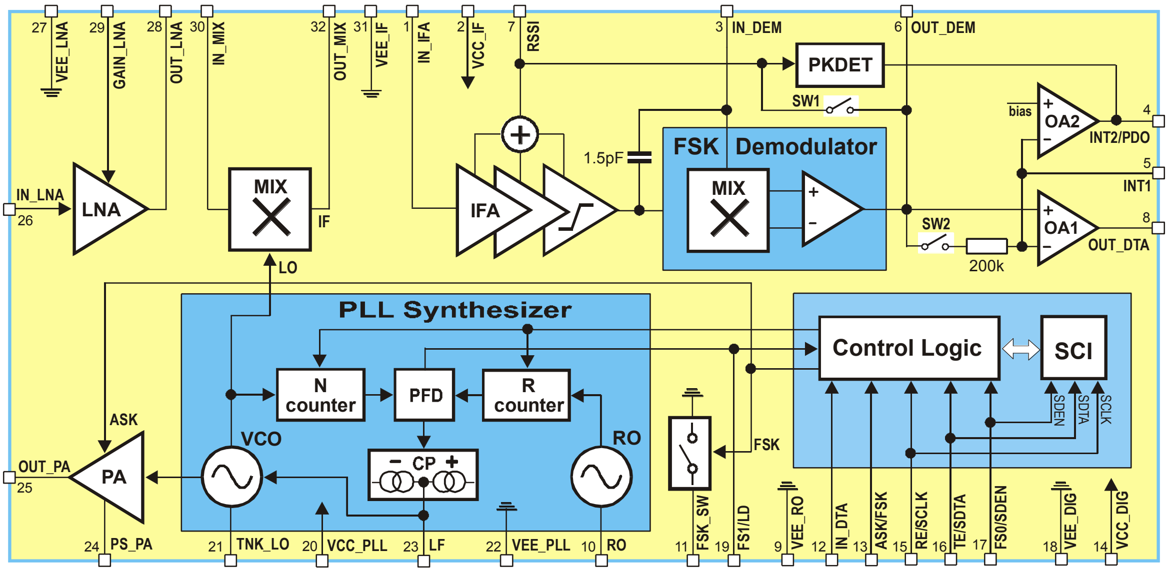


Fig. 1: TH71221 block diagram

1.5 User Mode Features

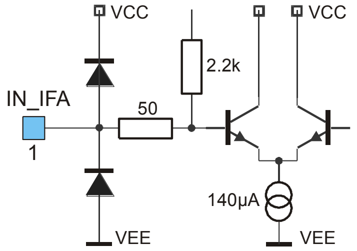
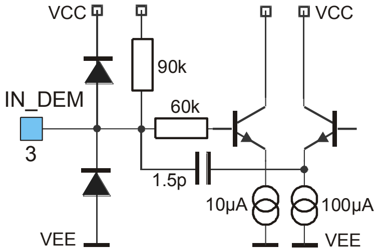
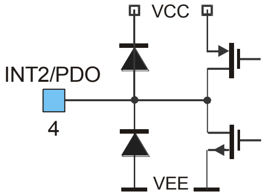
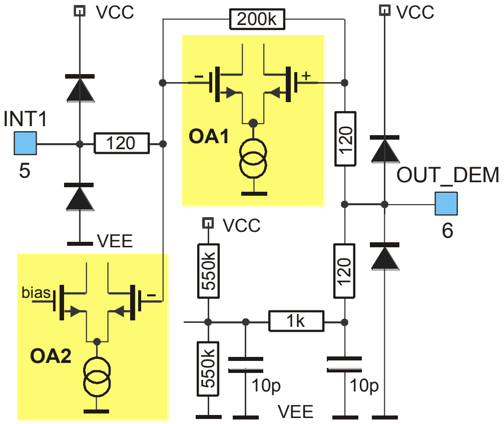
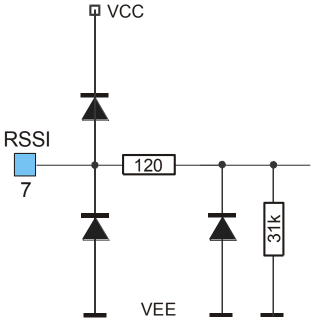
The transceiver can operate in two different user modes. It can be used either as a 3wire-bus-controlled programmable or as a stand-alone fixed-frequency device. After power up, the transceiver is set to Stand-alone User Mode (SUM). In this mode, pins FS0/SDEN and FS1/LD must be connected to V_{EE} or V_{CC} in order to set the desired frequency of operation. There are 4 pre-defined frequency settings: 315MHz, 433.92MHz, 868.3MHz and 915MHz. The logic level at pin FS0/SDEN must not be changed after power up in order to remain in fixed-frequency mode.

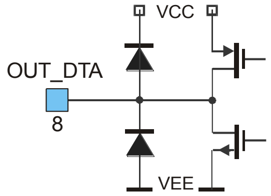
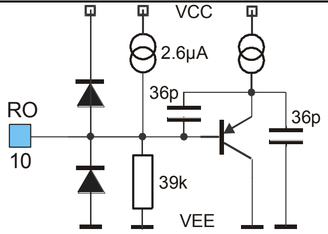
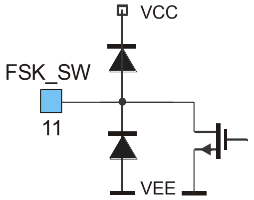
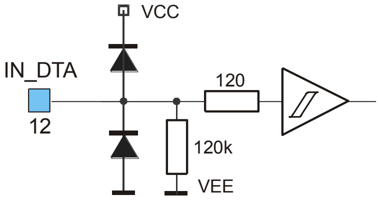
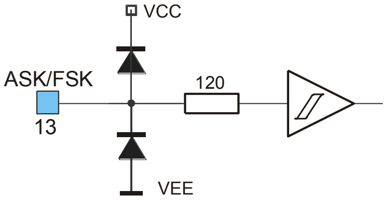
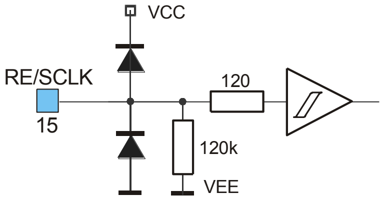
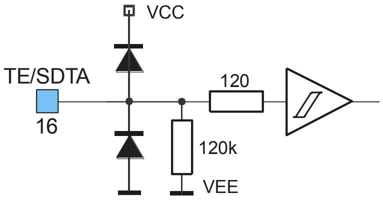
After the first logic level change at pin FS0/SDEN, the transceiver enters into Programmable User Mode (PUM). In this mode, the user can set any PLL frequency or mode of operation by the SCI. In SUM pins FS0/SDEN and FS1/LD are used to set the desired frequency, while in PUM pin FS0/SDEN is part of the 3-wire serial control interface (SCI) and pin FS1/LD is the look detector output signal of the PLL synthesizer.

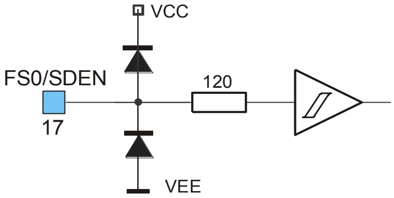
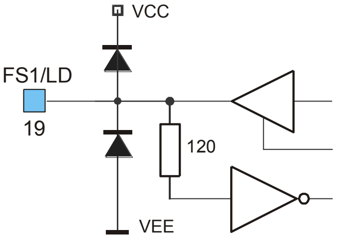
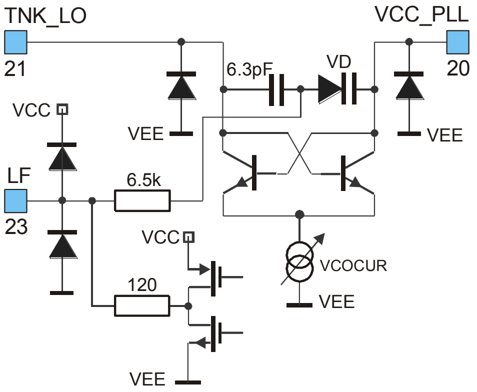
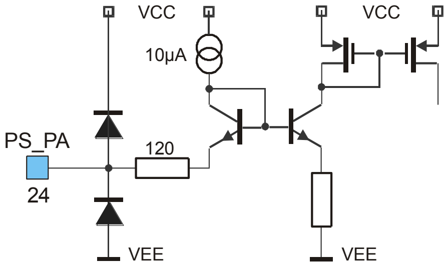
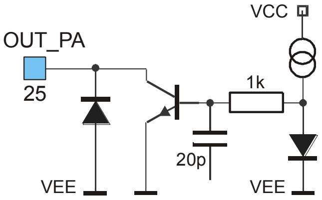
A mode control logic allows several operating modes. In addition to standby, transmit and receive mode, two idle modes can be selected to run either the reference oscillator only or the whole PLL synthesizer. The PLL settings for the PLL idle mode are taken over from the last operating mode which can be either receive or transmit mode.

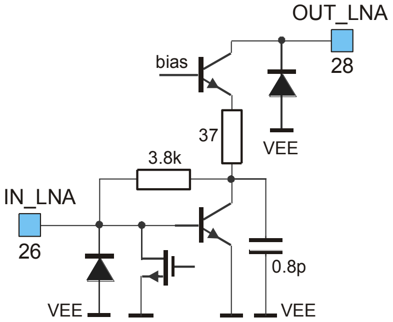
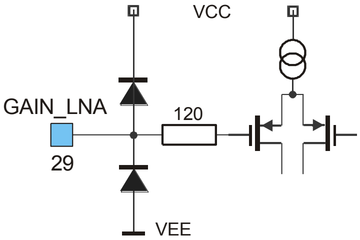
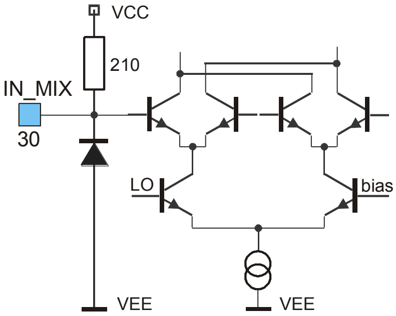
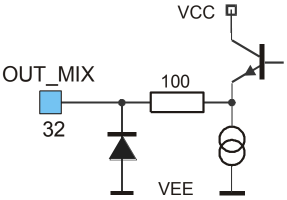
The different operating modes can be set in SUM and PUM as well. In SUM the user can program the transceiver via control pins RE/SCLK and TE/SDTA. In PUM the register bits OPMODE are used to select the modes of operation while pins RE/SCLK and TE/SDTA are part of the SCI.

2 Pin Definitions and Descriptions

Pin No.	Name	I/O Type	Functional Schematic	Description
1	IN_IFA	input		IF amplifier input, approx. 2 kΩ single-ended
2	VCC_IF	supply		positive supply of LNA, MIX, IFA, FSK Demodulator, PA, OA1 and OA2
3	IN_DEM	analog I/O		IF amplifier output and demodulator input, connection to external ceramic discriminator or LC tank
4	INT2/PDO	output		OA2 output or peak detector output, high impedance in transmit and idle mode
5	INT1	input		inverting inputs of OA1 and OA2
6	OUT_DEM	analog I/O		demodulator output and non-inverting OA1 input, high impedance in transmit and idle mode
7	RSSI	output		RSSI output, approx. 31 kΩ

Pin No.	Name	I/O Type	Functional Schematic	Description
8	OUT_DTA	output		OA1 output, high impedance in transmit and idle mode
9	VEE_RO	ground		ground of RO
10	RO	analog I/O		RO input, base of bipolar transistor
11	FSK_SW	analog I/O		FSK pulling pin, switch to ground or OPEN The switch is open in receive and idle mode
12	IN_DTA	input		ASK/FSK modulation data input, pull down resistor 120kΩ
13	ASK/FSK	input		ASK/FSK mode select input
14	VCC_DIG	supply		positive supply of serial port and control logic
15	RE/SCLK	input		receiver enable input / clock input for the shift register, pull down resistor 120kΩ
16	TE/SDTA	input		transmitter enable input / serial data input, pull down resistor 120kΩ

Pin No.	Name	I/O Type	Functional Schematic	Description
17	FS0/SDEN	input		frequency select input / serial data enable input
18	VEE_DIG	ground		ground of serial port and control logic
19	FS1/LD	input / output		frequency select input / lock detector output
20	VCC_PLL	analog I/O		VCO open-collector output, connection to VCC or external LC tank
21	TNK_LO	analog I/O		VCO open-collector output, connection to external LC tank
23	LF	analog I/O		charge pump output, connection to external loop filter
22	VEE_PLL	ground		ground of PLL frequency synthesizer
24	PS_PA	analog I/O		power-setting input
25	OUT_PA	output		power amplifier open-collector output

Pin No.	Name	I/O Type	Functional Schematic	Description
27	VEE_LNA	ground		ground of LNA and PA
28	OUT_LNA	output		LNA open-collector output, connection to external LC tank at RF
26	IN_LNA	input		LNA input, single-ended
29	GAIN_LNA	input		LNA gain control input
30	IN_MIX	input		mixer input, approx. 200Ω single-ended
31	VEE_IF	ground		ground of IFA, Demodulator, OA1 and OA2
32	OUT_MIX	output		mixer output, approx. 330Ω single-ended

3 Functional Description

3.1 PLL Frequency Synthesizer

The TH71221 contains an integer-N PLL frequency synthesizer. A PLL circuit performs the frequency synthesis via a feedback mechanism. The output frequency f_{VCO} is generated as an integer multiple of the phase detector comparison frequency f_R .This reference frequency f_R is generated by dividing the output frequency f_{RO} of a crystal oscillator. The phase detector utilizes this signal as a reference to tune the VCO and in the locked state it must be equal to the desired output frequency, divided by the feedback divider ratio N.

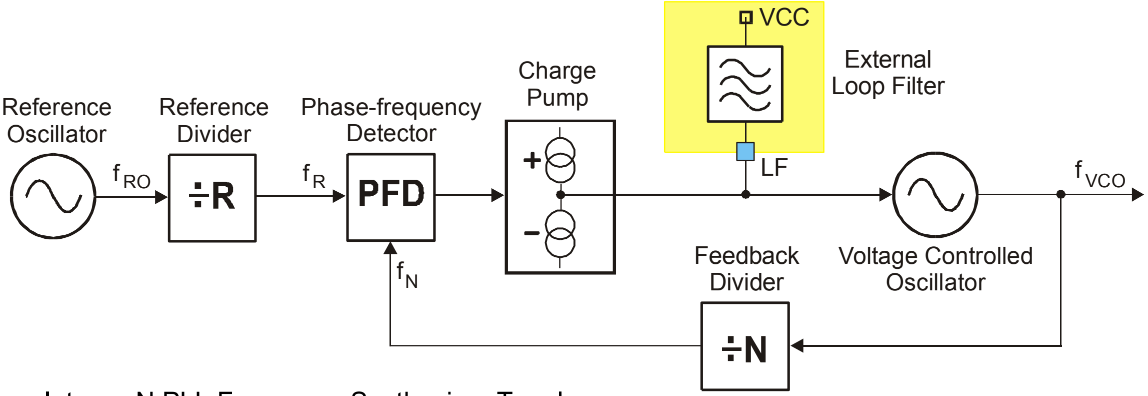


Fig. 2: Integer-N PLL Frequency Synthesizer Topology

The output frequency of the synthesizer f_{VCO} can be selected by programming the feedback divider and the reference divider. The only constraint for the frequency output of the system is that the minimum frequency resolution, or the channel spacing, must be equal to the PFD frequency f_R, which is given by the reference frequency f_{RO} and the reference divider factor R:

$$f_R = \frac{f_{RO}}{R}. \qquad (1)$$

When the PLL is unlocked (e.g. during power up or during reprogramming of a new feedback divider ratio N), the phase-frequency detector PFD and the charge pump create an error signal proportional to the phase difference of the two input signals. This error signal is low-pass filtered through the external loop filter and input to the VCO to control its frequency. A very low frequency resolution increases the settling time of the PLL and reduces the ability to cancel out VCO perturbations, because the loop filter is updated every $1/f_R$. After the PLL has locked, the VCO frequency is given by the following equation:

$$f_{VCO} = N \cdot \frac{f_{RO}}{R} = N \cdot f_R. \qquad (2)$$

There are four registers available to set the VCO frequencies in receive (registers RR and NR) and in transmit mode (registers RT and NT). These registers can be programmed using the Serial Control Interface in Programmable User Mode (PUM). In case of Stand-alone User Mode (SUM), the registers are set fixed values (refer to para. 4.1.1).

The VCO frequency is equal to the carrier frequency in transmit mode. While in receive mode the VCO frequency is offset by the intermediate frequency IF. This is because of the super-heterodyne nature of the receive part.

3.1.1 Reference Oscillator (XOSC)

The reference oscillator is based on a Colpitts topology with two integrated functional capacitors as shown in figure 3. The circuitry is optimized for a load capacitance range of 10 pF to 15 pF. The equivalent input capacitance CRO offered by the oscillator input pin RO is about 18pF.

To ensure a fast and reliable start-up and a very stable frequency over the specified supply voltage and temperature range, the oscillator bias circuitry provides an amplitude regulation. The amplitude on pin RO is monitored in order to regulate the current of the oscillator core I_{RO}. There are two limits ROMAX and ROMIN between the regulation is maintained. These values can be changed via serial control interface in Programmable User Mode (PUM). In Stand-alone User Mode (SUM), ROMAX and ROMIN are set to default values (refer to para. 5.1.3). ROMAX defines the start-up current of the oscillator. The ROMIN value sets the desired steady-state current. If ROMIN is sufficient to achieve an amplitude of about 400 mV on pin RO, the current I_{RO} will be set to ROMIN. Otherwise the current will be permanently regulated between ROMIN and ROMAX. If ROMIN and ROMAX are equal, no regulation takes place. For most of the applications ROMIN and ROMAX should not be changed from default.

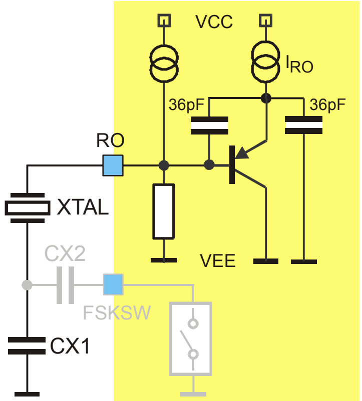


Fig. 3: Reference oscillator circuit

3.1.2 Reference Divider

The reference divider provides the input signal of the phase detector by dividing the signal of the reference oscillator. The range of the reference divider is

$$4 \le R \le 1023 \ . \tag{3}$$

3.1.3 Feedback Divider

The feedback divider of the PLL is based on a pulse-swallow topology. It contains a 4-bit swallow A-counter, a 13-bit program B-counter and a prescaler. The divider ratio of the prescaler is controlled by the program counter and the swallow counter. During one cycle, the prescaler divides by 17 until the swallow A-counter reaches its terminal count. Afterwards the prescaler divides by 16 until the program counter reaches its terminal count. Therefore the overall feedback divider ratio can be expressed as:

$$N = 17 \cdot A + 16 \cdot (B - A) . \tag{4}$$

The A-counter configuration represents the lower bits in the feedback divider register ($N_{0-3} = A_{0-3}$) and the upper bits the B-counter configuration ($N_{4-16} = B_{0-12}$) respectively. According to that, the following counter ranges are implemented:

$$0 \le A \le 15; \quad \mathbf{4 \le B \le 8191} \text{ whereas } \mathbf{B > A} \tag{5}$$

and therefore the range of the overall feedback divider ratio results in:

$$64 \le N \le 131071 \ . \tag{6}$$

The user does not need to care about the A- and B-counter settings. It is only necessary to know the overall feedback divider ratio N to program the register settings.

3.1.4 Frequency Resolution and Operating Frequency

It is obvious from (2) that, at a given frequency resolution f_R, the maximum operating frequency of the VCO is limited by the maximum N-counter setting. The table below provides some illustrative numbers. Please also refer to section 4.4.1 for the pre-configured settings in Stand-alone User Mode (SUM).

Crystal frequency f_{RO}	Frequency resolution f_R	R counter	N counter	Operating frequency f_{VCO}
3.0000MHz	2.93kHz	1023	13107	38.437MHz
3.0000MHz	2.93kHz	1023	131071	384.372MHz
8.0000MHz	12.5kHz	640	35812	447.65MHz
8.0000MHz	25kHz	320	34746	868.65MHz
8.0000MHz	250kHz	32	3660	915.0MHz

3.1.5 Phase-Frequency Detector

The phase-frequency detector creates an error voltage proportional to the phase difference between the reference signal f_R and f_N. The implementation of the phase detector is a phase-frequency type. That circuitry is very useful because it decreases the acquisition time significantly. The gain of the phase detector can be expressed as:

$$K_{PD} = \frac{I_{CP}}{2\pi}, \qquad (7)$$

where I_{CP} is the charge pump current which is set via register CPCUR. In the TH7122 design the VCO frequency control characteristic is with negative polarity. This means the VCO frequency increases if the loop filter output voltage decreases and vice versa. When an external varactor diode is added to the VCO tank, the tuning characteristic can be changed between positive and negative depending on the particular varactor diode circuitry. Therefore the PDFPOL register can be used to define the phase detector polarity.

3.1.6 Lock Detector

In Programmable User Mode a lock-detect signal LD is available at pin FS1/LD (pin 19). The lock detection circuitry uses Up and Down signals from the phase detector to check them for phase coherency. Figure 4 shows an overview of the lock signal generation. The locked state and the unlock condition will be decided on the register settings of LDTM and ERTM respectively. In the start-up phase of the PLL, Up and Down signals are quite unbalanced and counter CNT_LD receives no clock signal. When the loop approaches steady state, the signals Up and Down begin to overlap and CNT_LD counts down. Herein register LDTM sets the number of counts which are necessary to set the lock detection signal LD. If an unlock condition occurs, the counter CNT_LD will be reloaded and therefore its CARRY falls back.

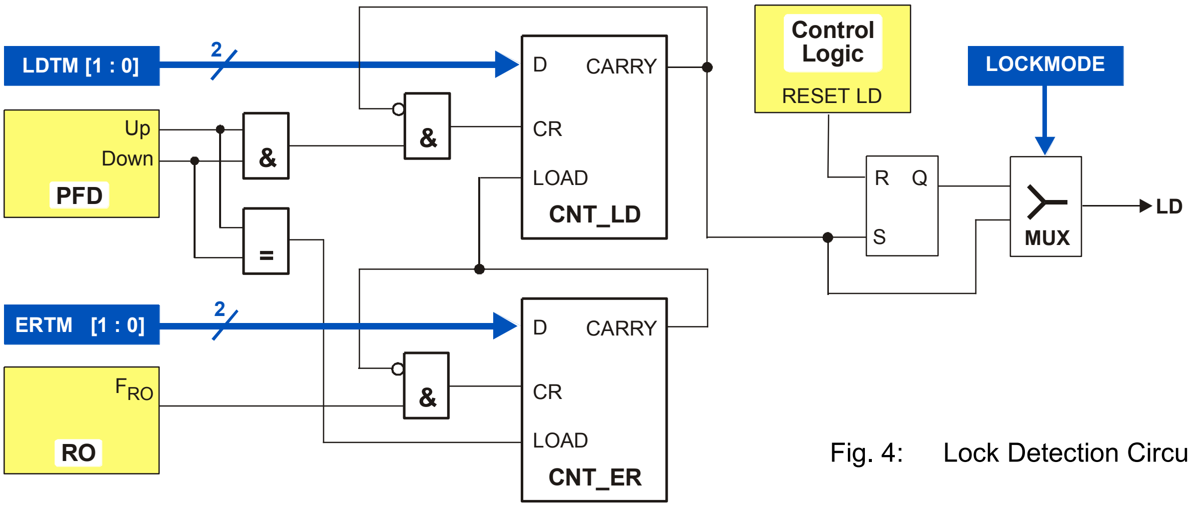


Fig. 4: Lock Detection Circuit

The CNT_ER supervises the unlock condition. If Up and Down are consecutive, the counter CNT_ER will be reloaded permanently and its CARRY will not be set, otherwise the counter level of CNT_ER will be reduced by the reference oscillator clock ($1/f_{RO}$). The register ERTM decides on the maximum number of clocks during Up and Down signals can be non-consecutive without loosing the locked state.

The transceiver offers two ways of analyzing the locked state. If the register LOCKMODE is set to '0', only one occurrence of the locked state condition is needed to remain LD = 1 during the whole active mode, otherwise the state of the PLL will be observed permanently.

3.1.7 Voltage Controlled Oscillator with external Loop Filter

The transceiver provides a LC-based voltage-controlled oscillator with an external inductance element connected between VCC and pin TNK_LO. An internal varactor diode in series with a fixed capacitor forms the variable part of the oscillator tank. The oscillation frequency is adjusted by the DC-voltage at pin LF. The tuning sensitivity of the VCO is approximately 20MHz/V for 433MHz operations and 40MHz/V at 868MHz. Since the internal varactor is connected to VCC, a lower voltage on pin LF causes the capacitance to decrease and the VCO frequency to increase. For this reason the phase detector polarity should be negative (PFDPOL = 0). If the operation frequency is below 300MHz, an external varactor diode between pin TNK_LO and VCC_PLL is necessary. The corresponding application schematic is shown in section 8. The VCO current VCOCUR can be adjusted via serial control interface in order to ensure stable oscillations over the whole frequency range. For lowest LO emission in receive mode, VCOCUR should be set to the lowest value.

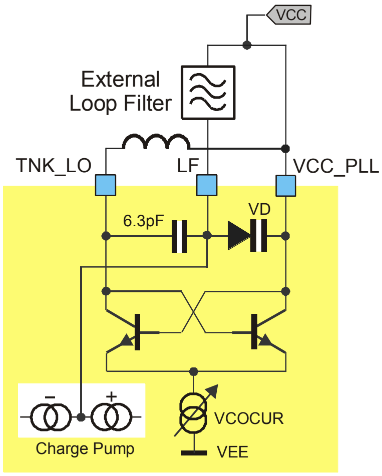


Fig. 5: VCO schematic

3.1.8 Loop Filter

Since the loop filter has a strong impact on the function of the PLL, it must be chosen carefully. For FSK operation the bandwidth of the loop filter must be selected wide enough for a fast relock of the PLL during crystal pulling. The bandwidth must of course also be larger than the data rate. In case of ASK or OOK the bandwidth should be extended even further to allow the PLL to cancel out VCO perturbations that might be caused by the PA on/off keying. The suggested filter topology is shown in Fig. 6. The dimensions of the loop filter elements can be derived using well known formulas in application notes and other reference literature.

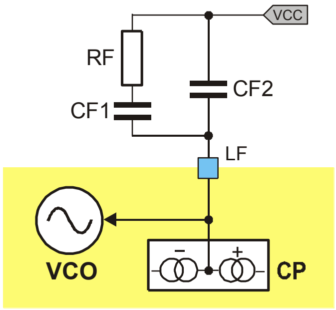


Fig. 6: 2nd order Loop filter

3.2 Receiver Part

The RF front-end of the receiver part is a super-heterodyne configuration that converts the input radio-frequency (RF) signal into an intermediate frequency (IF) signal. The most commonly used IF is 10.7 MHz, but IFs in the range of 0.4 to 22 MHz can also be used. According to the block diagram, the front-end consists of a LNA, a Mixer and an IF limiting amplifier with received signal strength indicator (RSSI). The local oscillator (LO) signal for the mixer is generated by the PLL frequency synthesizer.

As the receiver constitutes a superhet architecture, there is no inherent suppression of the image frequency. It depends on the particular application and the system's environmental conditions whether an RF front-end filter should be added or not. If image rejection and/or good blocking immunity are relevant system parameters, a band-pass filter must be placed either in front or after the LNA. This filter can be a SAW (surface acoustic wave) or LC-based filter (e.g. helix type).

3.2.1 LNA

The LNA is based on a cascode topology for low-noise, high gain and good reverse isolation. The open collector output has to be connected to an external resonance circuit which is tuned to the receive frequency. The gain of the LNA can be changed in order to achieve a high dynamic range. There are two possibilities for the gain setting which can be selected by the register bit LNACTRL. External control can be done via the pin GAIN_LNA, internal control is given by the register bit LNAGAIN. In case of external gain control, a hysteresis of about 340 mV can be chosen via the register bit LNAHYST. This configuration is useful if an automatic gain control loop via the RSSI signal is established. In transmit mode the LNA-input is shorted to protect the amplifier from saturation and damaging.

3.2.2 Mixer

The mixer is a double-balanced mixer which down converts the receive frequency to the IF. The default LO injection type is low side ($f_{VCO} = f_{RX} – f_{IF}$). But also high side injection is possible ($f_{VCO} = f_{RX} + f_{IF}$). In this case, the data signal´s polarity is inverted due to the mixing process. To avoid this, the transmitted data stream can be inverted too by setting DTAPOL to ‘1’.
The output impedance of the mixer is about 330Ω in order to match to an external IF filter.

3.2.3 IF Amplifier

After passing the channel select filter which sets the IF bandwidth the signal is limited by means of an high gain limiting amplifier. The small signal gain is about 80 dB. The RSSI signal is generated within the IF amplifier. The output of the RSSI signal is available at pin RSSI. The voltage at this pin is proportional to the input power of the receiver in dBm. Using this RSSI output signal the signal strength of different transmitters can be distinguished.

3.2.4 ASK Demodulator

The receive part of the TH7122 allows for two ASK demodulation configurations:

- standard ASK demodulation or
- ASK demodulation with peak detector.

The default setting is standard ASK demodulation. In this mode SW1 and SW2 are closed and the RSSI output signal directly feeds the data slicer setup by means of OA1. The data slicer time constant equals to

$$T = 200\mathrm{k}\Omega \cdot C3\,, \qquad (8)$$

with C3 external to pin INT1. This time constant should be larger than the longest possible bit duration of the data stream. This is required to properly extract the ASK data’s DC level. The purpose of the DC (or mean) level at the negative input of OA1 is to set an adaptive comparator threshold to perform the ASK detection.

Alternatively a peak detector can be used to define the ASK detection threshold. In this configuration the peak detector PKDET is enabled, SW1 is closed and SW2 is open, and the peak detector output is multiplexed to pin INT2/PDO. This way the peak detector can feed the data slicer, again constituted by OA1 and a few external R and C components. The peak detection mode is selectable in programmable user mode.

3.2.5 FSK Demodulator

The implemented FSK demodulator is based on the phase-coincidence principle. A discriminator tank, which can either consist of a ceramic discriminator or an LC tank, is connected to pin IN_DEM. If FSK mode is selected SW1 is open, SW2 is closed and the output of OA2 is multiplexed to pin INT2/PDO.

The demodulator output signal directly feeds the data slicer setup by means of OA1. The data slicer time constant can be calculated using (8). This time constant should be larger than the longest possible bit duration of the data stream as described in the previous paragraph.

An on-chip AFC circuit tolerates input frequency variations. The input frequency acceptance range is proportional to the FSK or FM deviation. It can be adjusted by the discriminator tank. The AFC feature is disabled by default and can be activated in programmable mode.

3.3 Transmitter Part

The output of the PLL frequency synthesizer feeds a power amplifier (PA) in order to setup a complete RF transmitter. The VCO frequency is identical to the carrier frequency.

3.3.1 Power Amplifier

The power amplifier (PA) has been designed to deliver about 10 dBm in the specified frequency bands. Its pin OUT_PA is an open collector output. The larger the output voltage swing can be made the better the power efficiency will be. The PA must be matched to deliver the best efficiency in terms of output power and current consumption.

The collector must be biased to the positive supply. This is done by means of an inductor parallel tuned with a capacitor. Or it is made large enough in order not to affect the output matching network. S-parameters of pin OUT_PA are not useful because the output is very high resistive with a small portion of parallel capacitance. Since the open-collector output transistor can be considered as a current source, the only parameters needed to design the output matching network are the output capacitance, the supply voltage V_{CC}, the transistor's saturation voltage and the power delivered to the load P_O.

In order to avoid saturation of the output stage, a saturation voltage VCE_{SAT} of about 0.7 V should be considered. The real part of the load impedance can then be calculated using

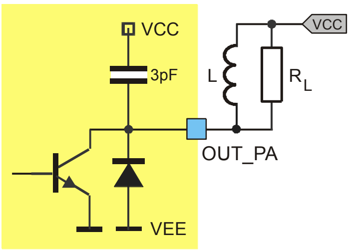


Fig. 7: OUT_PA schematic

$$R_L = \frac{(V_{CC} - VCE_{SAT})^2}{2 \cdot P_O}. \qquad (9)$$

The output capacitance is typically 3 pF.

3.3.2 Output Power Adjustment

The maximum output power is adjustable via the external resistor RPS as shown in Figure 8. There are four predefined power settings in programmable user mode which can be set in the register TXPOWER. The maximum power setting P4 is the default setting.

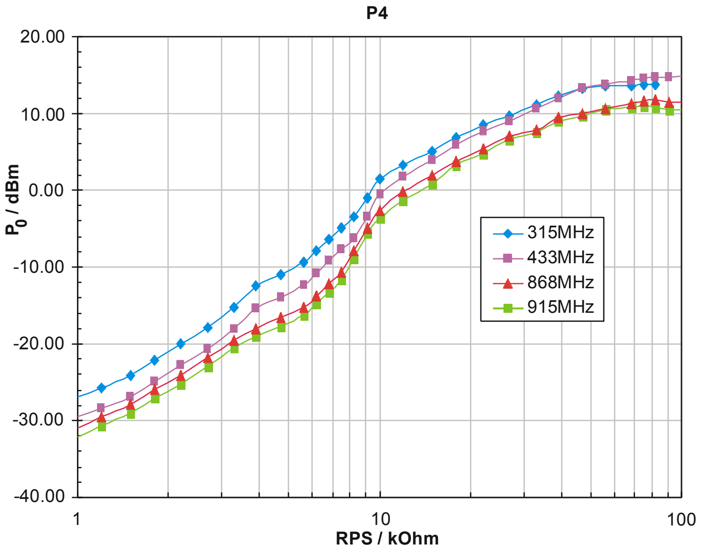


Fig. 8: Output power vs. RPS

3.3.3 Modulation Schemes

The RF carrier generated by the PLL frequency synthesizer can be ASK or FSK modulated. Depending on the selected user mode, the modulation type can be selected either by the ASK/FSK pin or via the serial control interface. Data is applied to pin IN_DTA. The data signal can be inverted by the bit DTAPOL. The following tables for ASK and FSK modulation are valid for non-inverted data (DTAPOL = 0)

3.3.4 ASK Modulation

IN_DTA	Description
0	Power amplifier is turned off
1	Power amplifier is turned on (according to the selected output power)

The transceiver is ASK-modulated by turning on and off the power amplifier. Please also refer to para. 1.3 for ASK modulation limits.

3.3.5 FSK Modulation

- FSK modulation via crystal pulling

FSK modulation can be achieved by pulling the crystal oscillator frequency. A CMOS-compatible data stream applied at pin IN_DTA digitally modulates the XOSC via an integrated NMOS switch. Two external pulling capacitors CX1 and CX2 allow the FSK deviation Δf and center frequency f_c to be adjusted independently. At IN_DTA = LOW CX2 is connected in parallel to CX1 leading to the low-frequency component of the FSK spectrum (f_{min}); while at IN_DTA = HIGH CX2 is deactivated and the XOSC is set to its high frequency, leading to f_{max}.

IN_DTA	Description
0	$f_{min} = f_c - \Delta f$ (FSK switch is closed)
1	$f_{max} = f_c + \Delta f$ (FSK switch is open)

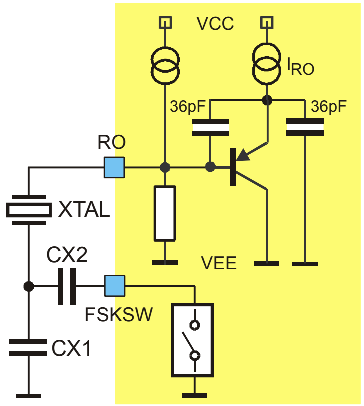


Fig. 9: Crystal Pulling Circuit

An external reference signal can be directly AC-coupled to the reference oscillator input pin RO. Then the transceiver is used without a XTAL. Now the reference signal sets the carrier frequency and has to contain the FSK (or FM) modulation

- FSK modulation via direct VCO modulation

Alternatively FSK or FM can be achieved by injecting the modulating signal into the loop filter to directly control the VCO frequency. Fig. 10 shows a circuit proposal for direct VCO modulation. This circuit is recommended for data rates in excess of about 20 kbps NRZ. An external VCO tuning varactor should be added for narrow-band applications, for example at channel spacings of 25 kHz. For details please refer to the application notes “TH7122 and TH71221 High Speed Data Communication” and “TH7122 and TH71221 Used In Narrow Band FSK Applications” as well as to the “TH7122 and TH71221 Cookbook”

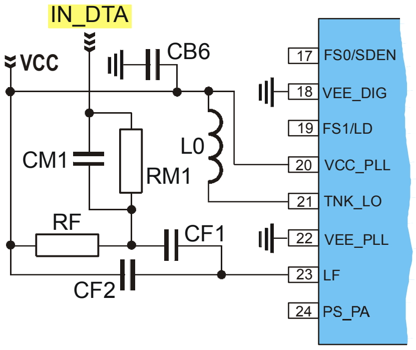


Fig. 10: Circuit schematic for direct VCO modulation

3.3.6 Crystal Tuning

A crystal is tuned by the manufacturer to the requested oscillation frequency f_0 for a certain load capacitance CL within the specified calibration tolerance. The only way to tune this oscillation frequency is to vary the effective load capacitance CL_{eff} seen by the crystal.
Figure 8 shows the oscillation frequency of a crystal in dependency on the effective load capacitance. This capacitance changes in accordance with the logic level of IN_DTA around the specified load capacitance. The figure illustrates the relationship between the external pulling capacitors and the frequency deviation.

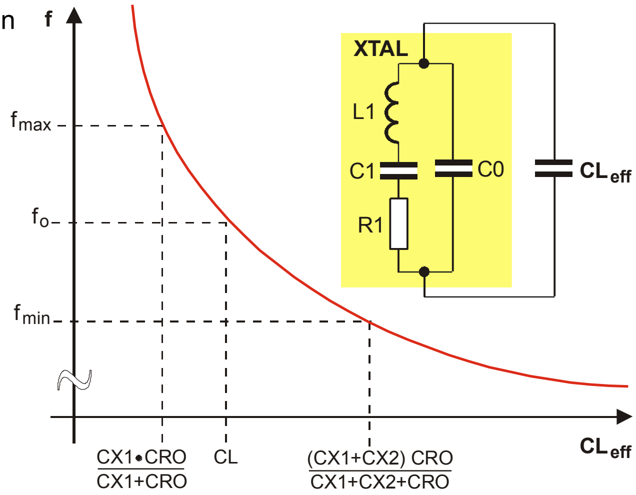


Fig. 11: Crystal Tuning Characteristic

4 Description of User Modes

4.1 Stand-alone User Mode Operation

After power up the transceiver is set to stand-alone user mode. In this mode, pins FS0/SDEN and FS1/LD must be connected to V_{EE} or V_{CC} to set the desired frequency of operation. The logic level at pin FS0/SDEN must not be changed after power up in order to remain in stand-alone user mode. The default settings of the control word bits in stand-alone user mode are described in the frequency selection table. Detailed information about the default settings can be found in the tables of section 5.

4.1.1 Frequency Selection

Channel frequency	433.92 MHz	868.3 MHz	315 MHz	915 MHz
FS0/SDEN	**1**	**0**	**1**	**0**
FS1/LD	**0**	**0**	**1**	**1**
Reference oscillator frequency	**7.1505 MHz**			
R counter ratio in RX mode (RR)	**32**	**16**	**18**	**32**
PFD frequency in RX mode	**223.45 kHz**	**446.91 kHz**	**397.25 kHz**	**223.45 kHz**
N counter ratio in RX mode (NR)	**1894**	**1919**	**766**	**4047**
VCO frequency in RX mode	**423.22 MHz**	**857.60 MHz**	**304.30 MHz**	**904.30 MHz**
RX frequency	**433.92 MHz**	**868.30 MHz**	**315.00 MHz**	**915.00 MHz**
R counter ratio in TX mode (RT)	**32**	**16**	**18**	**32**
PFD frequency in TX mode	**223.45 kHz**	**446.91 kHz**	**397.25 kHz**	**223.45 kHz**
N counter ratio in TX mode (NT)	**1942**	**1943**	**793**	**4095**
VCO frequency in TX mode	**433.92 MHz**	**868.30 MHz**	**315.00 MHz**	**915.00 MHz**
TX frequency	**433.92 MHz**	**868.30 MHz**	**315.00 MHz**	**915.00 MHz**
IF in RX mode	**10.7 MHz**	**10.7 MHz**	**10.7 MHz**	**10.7 MHz**

In stand-alone user mode, the transceiver can be set to Standby, Receive, Transmit or Idle mode (only PLL synthesizer active) via control pins RE/SCLK and TE/SDTA. The modulation scheme and the LNA gain are set by pins ASK/FSK and GAIN_LNA, respectively.

4.1.2 Operation Mode

Operation mode	Standby	Receive	Transmit	Idle
RE/SCLK	**0**	**1**	**0**	**1**
TE/SDTA	**0**	**0**	**1**	**1**

Note: Pins with internal pull-down

4.1.3 Modulation Type

Modulation type	ASK	FSK
ASK / FSK	**0**	**1**

4.1.4 LNA Gain Mode

LNA gain	high	low
GAIN_LNA	**0**	**1**

4.2 Programmable User Mode Operation

The transceiver can also be used in programmable user mode. After power-up the first logic change at pin FS0/SDEN enters into this mode. Now full programmability can be achieved via the Serial Control Interface (SCI).

4.2.1 Serial Control Interface Description

A 3-wire (SCLK, SDTA, SDEN) Serial Control Interface (SCI) is used to program the transceiver in programmable user mode. At each rising edge of the SCLK signal, the logic value on the SDTA pin is written into a 24-bit shift register. The data stored in the shift register are loaded into one of the 4 appropriate latches on the rising edge of SDEN. The control words are 24 bits lengths: 2 address bits and 22 data bits. The first two bits (bit 23 and 22) are latch address bits. As additional leading bits are ignored, only the least significant 24 bits are serial-clocked into the shift register. The first incoming bit is the most significant bit (MSB). To program the transceiver in multi-channel application, four 24-bit words may be sent: A-word, B-word, C-word and D-word. If individual bits within a word have to be changed, then it is sufficient to program only the appropriate 24-bit word. The serial data input timing and the structure of the control words are illustrated in Fig. 12 and 13.

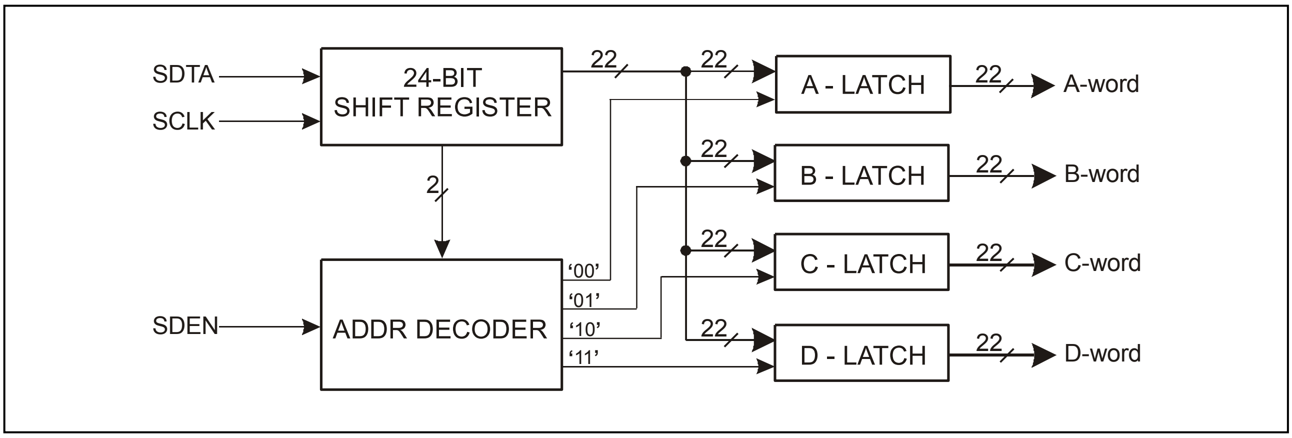


Fig. 12: SCI Block Diagram

Due to the static CMOS design, the SCI consumes virtually no current and it can be programmed in active as well as in standby mode.
If the transceiver is set from standby mode to any of the active modes (idle, receive, transmit), the SCI settings remain the same as previously set in one of the active modes, unless new settings are done on the SCI while entering into an active mode.

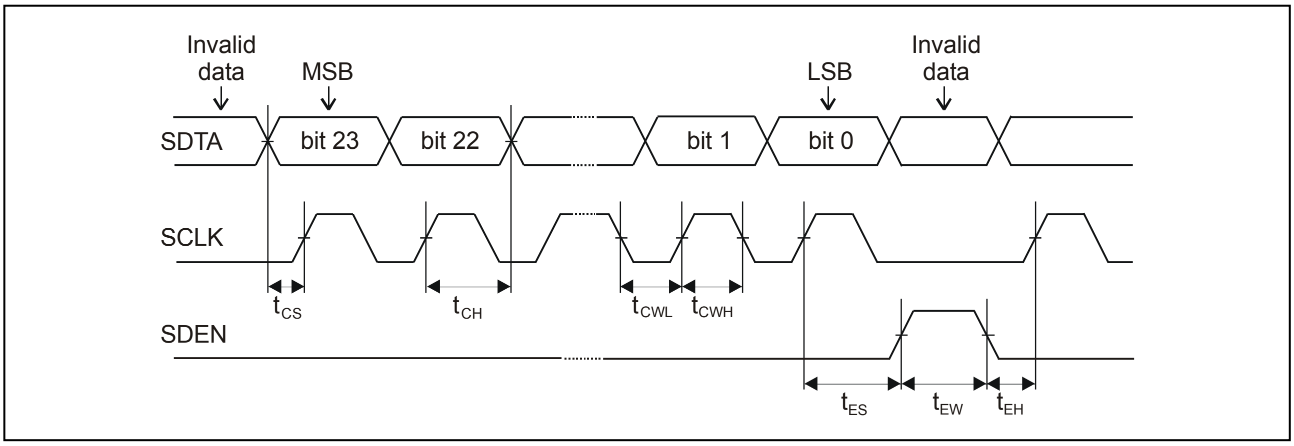


Fig. 13: Serial Data Input Timing

5 Register Description

As shown in the previous section there are four control words which stipulate the operation of the whole chip. In Stand-alone User Mode SUM the intrinsic default values with respect to the applied levels at pins FS0 and FS1 lay down the configuration of the transceiver. In Programmable User Mode (PUM) the register settings can be changed via 3-wire interface SCI. The default settings which vary with the desired operating frequency depend on the voltage levels at the frequency selection pins FS0 and FS1 before entering the PUM. Table 5.1.1 shows the default register settings of different frequency selections. It should be noted that the channel frequency listed below will be achieved with a crystal frequency of 7.1505 MHz. The following table depicts an overview of the register configuration of the TH71221.

5.1 Register Overview

WORD MSB		DATA																					LSB	
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**Bit No.**
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	Depends on FS0/FS1 voltage level after power up										**default**
A		**IDLE**	**DATAPOL**	**MODSEL**	**CPCUR**	**LOCKMODE**	**PACTRL**	**TXPOWER [1 :0]**		***Set to 1***	**LNAGAIN**	**OPMODE [1 : 0]**		**RR [9 : 0]**										
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**Bit No.**
0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**0**	**1**	**0**	Depends on FS0/FS1 voltage level after power up										**default**
B		**PKDET**	***Set to 1***	**DELPLL**	**LNAHYST**	**AFC**	**OA2**	**ROMAX [2 : 0]**			**ROMIN [2 : 0]**			**RT [9 : 0]**										
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**Bit No.**
1	**0**	**0**	**0**	Depends on FS0/FS1 voltage level after power up																				**default**
C		**LNACTRL**	**PFDPOL**	**VCOCUR [1 :0]**		**BAND**	**NR [16 : 0]**																	
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**Bit No.**
1	**1**	**0**	**0**	**1**	**0**	**0**	Depends on FS0/FS1 voltage level after power up																	**default**
D		**MODCTRL**	**LDTM [1 :0]**		**ERTM [1 :0]**		**NT [16 : 0]**																	

5.1.1 Default Register Settings for FS0, FS1

FS1	FS0	Channel frequency	BAND	VCOCUR [1 : 0]	RR [9 : 0]	NR [16 :0]	RT [9 :0]	NT [16 : 0]
0	0	**868.30 MHz**	1	11	16d	1919d	16d	1943d
0	1	**433.92 MHz**	0	01	32d	1894d	32d	1942d
1	0	**915.00 MHz**	1	11	32d	4047d	32d	4095d
1	1	**315.00 MHz**	0	00	18d	766d	18d	793d

Note: d – decimal code

A detailed description of the registers function and their configuration can be found in the following sections.

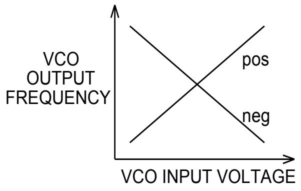
5.1.2 A – word

Name	Bits	Description
RR	[9:0]	Reference divider ratio in RX operation mode **4d .. 1023d**
OPMODE	[11:10]	Operation mode **00** **Standby mode** #default **01** **Receive mode** **10** **Transmit mode** **11** **Idle mode**
LNAGAIN	[12]	LNA gain **0** **low LNA gain** **1** **high LNA gain** #default This selection is valid if bit LNACTR (bit 21 in C-word) is set to internal LNA gain control.
not used	[13]	set to ‘1’ for correct function
TXPOWER	[15:14]	Output power steps **00** **P1** **01** **P2** **10** **P3** **11** **P4** #default
PACTRL	[16]	Set the PA-on condition **0** **PA is switched on if the PLL locks** **1** **PA is always on in TX mode** #default
LOCKMODE	[17]	Set the PLL locked state observation mode **0** **before lock only** #default Locked state condition will be ascertained only one time afterwards the LD signal remains in high state. **1** **before and after lock** locked state will be observed permanently
CPCUR	[18]	Charge Pump output current **0** **260 µA** #default **1** **1300 µA**
MODSEL	[19]	Modulation mode **0** **ASK** #default **1** **FSK** This selection is valid if bit MODCTRL (bit 21 in D-word) is set to internal modulation control.
DTAPOL	[20]	Input data polarity **0** **normal** #default ‘0’ for space at ASK or f_{min} at FSK, ‘1’ for mark at ASK or f_{max} at FSK **1** **inverse** ‘1’ for space at ASK or f_{min} at FSK, ‘0’ for mark at ASK or f_{max} at FSK
IDLESEL	[21]	Active blocks in IDLE mode **0** **only RO active** #default **1** **whole PLL active**

5.1.3 B – word

Name	Bits	Description
RT	[9:0]	Reference divider ratio in TX operation mode **4d .. 1023d**
ROMIN	[12:10]	Set the desired steady state current of the reference oscillator **000** **0 µA** **001** **75 µA** **010** **150 µA** #default **011** **225 µA** **100** **300 µA** **101** **375 µA** **110** **450 µA** **111** **525 µA** The control circuitry regulates the current of the oscillator core between the values ROMAX and ROMIN. As the regulation input signal the amplitude on pin RO is used. If the ROMIN value is sufficient to achieve an amplitude of about 400mV on pin RO the current of the reference oscillator core will be set to ROMIN. Otherwise the current will be permanently regulated between ROMAX and ROMIN. If ROMIN and ROMAX are equal no regulation of the oscillator current occurs. Please also note the block description of the reference oscillator in para. 3.1.1
ROMAX	[15:13]	Set the start-up current of the reference oscillator **000** **0 µA** **001** **75 µA** **010** **150 µA** **011** **225 µA** **100** **300 µA** **101** **375 µA** **110** **450 µA** **111** **525 µA** #default Set the start-up current of the reference oscillator core. Please also note the description of the ROMIN register and the block description of the reference oscillator which can be seen above.
OA2	[16]	OA2 operation **0** **disabled** #default **1** **enabled** OA2 can be enabled in FSK receive mode. OA2 is disabled in ASK mode receive.
AFC	[17]	Internal AFC feature **0** **disabled** #default **1** **enabled**
LNAHYST	[18]	Hysteresis on pin GAIN_LNA **0** **disabled** **1** **enabled** #default
DELPLL	[19]	Delayed start of the PLL **0** **undelayed start** PLL starts at the reference oscillator start-up **1** **starts after 8 valid RO-cycles** #default PLL starts after 8 valid RO-cycles before entering an active mode to ensure reliable oscillation of the reference oscillator.
not used	[20]	set to ‘1’ for correct function
PKDET	[21]	RSSI Peak Detector **0** **disabled** #default The RSSI output signal directly feeds the data slicer setup by means of OA1. **1** **enabled** In ASK receive mode the RSSI Peak Detector output is multiplexed to pin INT2/PDO.

5.1.4 C – word

Name	Bits	Description	
NR	[16:0]	Feedback divider ratio in RX operation mode	
		64d .. 131071d	
BAND	[17]	Set the desired frequency range	
		0	**recommended at f_{RF} < 500 MHz**
		1	**recommended at f_{RF} > 500MHz**
			Some tail current sources are linked to this bit in order to save current for low frequency operations.
VCOCUR	[19:18]	VCO active current	
		00	**low current (300 µA)**
		01	**standard current (500 µA)**
		10	**high1 current (700 µA)**
		11	**high2 current (900 µA)**
PFDPOL	[20]	Phase Detector polarity 	
		0	**negative** #default
		1	positive
LNACTRL	[21]	LNA gain control mode	
		0	**external LNA gain control** #default
			LNA gain will be set via pin GAIN_LNA.
		1	**internal LNA gain control**
			LNA gain will be set via bit LNAGAIN (bit 12 in A-word). Nevertheless pin GAIN_LNA must be connected to either VCC or VEE.

5.1.5 D – word

<table>
<tr><th>Name</th><th>Bits</th><th colspan="4">Description</th></tr>
<tr><td rowspan="2">NT</td><td rowspan="2">[16:0]</td><td colspan="4">Feedback divider ratio in TX operation mode</td></tr>
<tr><td colspan="4">64d .. 131071d</td></tr>
<tr><td rowspan="5">ERTM</td><td rowspan="5">[18:17]</td><td colspan="4">Set the unlock condition of the PLL</td></tr>
<tr><td>00</td><td>2 clocks</td><td>#default</td><td rowspan="4">Set the maximum allowed number of reference clocks (1/f_{RO}) during the phase detector output signals (UP & DOWN) can be in-consecutive.</td></tr>
<tr><td>01</td><td>4 clocks</td><td></td></tr>
<tr><td>10</td><td>8 clocks</td><td></td></tr>
<tr><td>11</td><td>16 clocks</td><td></td></tr>
<tr><td rowspan="5">LDTM</td><td rowspan="5">[20:19]</td><td colspan="4">Set the lock condition of the PLL</td></tr>
<tr><td>00</td><td>4 clocks</td><td></td><td rowspan="4">Set the minimum number of consecutive edges of phase detector output cycles, without appearance of any unlock condition.</td></tr>
<tr><td>01</td><td>16 clocks</td><td>#default</td></tr>
<tr><td>10</td><td>64 clocks</td><td></td></tr>
<tr><td>11</td><td>256 clocks</td><td></td></tr>
<tr><td rowspan="5">MODCTRL</td><td rowspan="5">[21]</td><td colspan="4">Set mode of modulation control:</td></tr>
<tr><td>0</td><td colspan="2">external modulation control</td><td>#default</td></tr>
<tr><td></td><td colspan="3">Modulation will be set via pin ASK/FSK.</td></tr>
<tr><td>1</td><td colspan="3">internal modulation control</td></tr>
<tr><td></td><td colspan="3">Modulation will be set via bit MODSEL (bit 19 in A-word). Nevertheless pin ASK/FSK must be connected to either VCC or VEE.</td></tr>
</table>

6 Technical Data

6.1 Absolute Maximum Ratings

Operation beyond absolute maximum ratings may cause permanent damage of the device.

Parameter	Symbol	Condition / Note	Min	Max	Unit
Supply voltage	V_{CC}		-0.3	6.0	V
Input voltage	V_{IN}		-0.3	V_{cc}+0.3	V
Input RF level	P_{iRF}	@ LNA input		10	dBm
Storage temperature	T_{STG}		-40	+125	°C
Junction temperature	T_J			+150	°C
Power dissipation	P_{diss}			0.25	W
Thermal Resistance	R_{thJA}			60	K/W
Electrostatic discharge	V_{ESD1}	human body model, 1)	-1.0	+1.0	kV
Electrostatic discharge	V_{ESD2}	human body model, 2)	-0.75	+0.75	kV

1) all pins, except LF, TNK_LO, VCC_PLL and FS1/LD

2) pins LF, TNK_LO, VCC_PLL and FS1/LD

6.2 Normal Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	V_{CC}		2.2	5.5	V
Operating temperature	T_A		-40	+85	ºC
Input low voltage (CMOS) pins IN_DTA, ASK/FSK, RE/SCLK, TE/SDTA, FS0/SDEN, FS1/LD	V_{IL}	$V_{IL\_FS1/LD}$ only in Stand-alone user mode		0.3*V_{CC}	V
Input high voltage (CMOS) pins IN_DTA, ASK/FSK, RE/SCLK, TE/SDTA, FS0/SDEN, FS1/LD	V_{IH}	$V_{IH\_FS1/LD}$ only in Stand-alone user mode	0.7*V_{CC}		V
Transmit frequency range	f_{TX}		300	930	MHz
Receive frequency range	f_{RX}		300	930	MHz
VCO frequency	f_{VCO}	Set by tank configuration	300	930	MHz
IF range	f_{IF}	$\| f_{RX} - f_{VCO} \|$	0.4	22	MHz
FSK demodulator operating range	f_{IF_FSK}		2	22	MHz
RO frequency	f_{RO}	Set by crystal	3	12	MHz
PFD comparison frequency	f_R	Set by crystal and R-counter	0.003	1	MHz
Frequency deviation	Δf	at FM or FSK	±2.5	±80	kHz
FSK data rate	R_{FSK}	w/ crystal pulling, NRZ		20	kbps
		w/ direct VCO mod., NRZ		115	kbps
ASK data rate	R_{ASK}	NRZ		40	kbps
FM bandwidth	f_m			10	kHz
VCO gain f_{RF}= 433.92MHz	K_{VCO}		14	23	MHz/V
f_{RF}= 868.3MHz			28	55	

6.3 DC Characteristics

all parameters under normal operating conditions, unless otherwise stated;
typical values at T_A = 23 °C and V_{CC} = 3 V

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Operating currents							
Standby current		I_{SBY}	Max at T_A = 25 °C		0.05	0.2	µA
			Max at T_A = 85 °C		0.05	1.0	
Idle current	Reg. BAND	I_{IDLE}	Idle mode (RO only), Reg. IDLESEL = 0		0.3	0.7	mA
	1 (> 500 MHz)		Idle mode, (whole PLL), Reg. IDLESEL = 1		3.5	4.8	mA
	1 (> 500 MHz)				6.3	8.0	
Receive supply current - **ASK**	0 (< 500 MHz)	I_{RXL_ASK}	ASK Receive mode, LNA @ low gain		6.1	8.2	mA
	1 (> 500 MHz)				8.9	13.0	
	0 (< 500 MHz)	I_{RXH_ASK}	ASK Receive mode, LNA @ high gain		7.4	10.1	mA
	1 (> 500 MHz)				10.2	14.9	
Receive supply current - **FSK**	0 (< 500 MHz)	I_{RXL_FSK}	FSK Receive mode, LNA @ low gain		6.7	9.2	mA
	1 (> 500 MHz)				9.5	13.8	
	0 (< 500 MHz)	I_{RXH_FSK}	FSK Receive mode, LNA @ high gain		8.0	11.1	mA
	1 (> 500 MHz)				10.8	15.7	
Transmit supply current @ P1	0 (< 500 MHz)	I_{P1}	Transmit mode, Reg. TXPOWER =00, V_{PS_PA} = 0.3V, continuous wave (CW) mode		13.2	16.4	mA
	1 (> 500 MHz)				17.1	20.8	
Transmit supply current @ P2	0 (< 500 MHz)	I_{P2}	Transmit mode, Reg. TXPOWER =01, V_{PS_PA} = 0.3V, CW mode		15.2	19.8	mA
	1 (> 500 MHz)				19.1	24.5	
Transmit supply current @ P3	0 (< 500 MHz)	I_{P3}	Transmit mode, Reg. TXPOWER =10, V_{PS_PA} = 0.3V, CW mode		18.6	25.8	mA
	1 (> 500 MHz)				22.5	31.1	
Transmit supply current @ P4	0 (< 500 MHz)	I_{P4}	Transmit mode, Reg. TXPOWER =11, V_{PS_PA} = 0.3V, CW mode		23.0	38.6	mA
	1 (> 500 MHz)				26.9	45.2	
Digital pin characteristics							
Input low voltage (CMOS) pins IN_DTA, ASK/FSK, RE/SCLK, TE/SDTA, FS0/SDEN, FS1/LD		V_{IL}	$V_{IL\_FS1/LD}$ only in Stand-alone user mode	-0.3		0.3*V_{CC}	V
Input high voltage (CMOS) pins IN_DTA, ASK/FSK, RE/SCLK, TE/SDTA, FS0/SDEN, FS1/LD		V_{IH}	$V_{IH\_FS1/LD}$ only in Stand-alone user mode	0.7*V_{CC}		Vcc+0.3	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Digital pin characteristics						
Pull-down Resistor pins IN_DTA , RE/SCLK, TE/SDTA	R_{PD}		70	120	220	kΩ
Low level input leakage current pins IN_DTA, ASK/FSK, RE/SCLK, TE/SDTA, FS0/SDEN, FS1/LD	I_{IL}	$I_{INL\_FS1/LD}$ only in Stand-alone user mode	-2			µA
High level input leakage current pins ASK/FSK, FS0/SDEN, FS1/LD	I_{IH}	$I_{INH\_FS1/LD}$ only in Stand-alone user mode			2	µA
Analog pin characteristics						
MOS switch On resistance FSK_SW pin	R_{ON}	Transmit mode, if Reg. DTAPOL = 0: IN_DTA = 0 if Reg. DTAPOL = 1: IN_DTA = 1		10	30	Ω
MOS switch Off resistance FSK_SW pin	R_{OFF}	Transmit mode, if Reg. DTAPOL = 0: IN_DTA = 1 if Reg. DTAPOL = 1: IN_DTA = 0	1			MΩ
Peak detector pull-up current INT2/PDO pin	I_{PU_PDO}	ASK Receive mode, Reg. PKDET = 1 $V_{OUT\_DEM} > V_{INT2/PDO}$	-1.1			mA
Peak detector leakage current INT2/PDO pin	I_{L_PDO}	ASK Receive mode, Reg. PKDET = 1 $V_{OUT\_DEM} =< V_{INT2/PDO}$	-2		2	µA
OA input offset voltage	V_{OS}	Receive mode	-25		25	mV
Voltage threshold for high to low LNA gain transition GAIN_LNA pin	V_{GAIN_HL}	Receive mode, Reg. LNACTRL = 0, Reg. LNAHYST = 1	1.0	1.3	1.6	V
Voltage threshold for low to high LNA gain transition GAIN_LNA pin	V_{GAIN_LH}	Receive mode, Reg. LNACTRL = 0, Reg. LNAHYST = 1	1.3	1.6	1.9	V
RSSI characteristics						
RSSI voltage at low IFA input level	V_{L_RSSI}	Receive mode, $V_{IN\_IFA} = 100\mu V$ (CW, 10.7MHz)		0.72		V
RSSI voltage at high IFA input level	V_{H_RSSI}	Receive mode, $V_{IN\_IFA} = 100mV$ (CW, 10.7MHz)		1.64		V

6.4 PLL Synthesizer Timings

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Channel switching time	wide band	t_{SW_WB}	B_{PLL} = 20kHz, I_{CP} = 260µA		200		µs
	narrow band	t_{SW_NB}	B_{PLL} = 2kHz, I_{CP} = 260µA		500		µs
TX – RX switching time		t_{TX_RX}	IF = 10.7MHz		1		ms

6.5 AC Characteristics of the Receiver Part

all parameters under normal operating conditions, unless otherwise stated;
typical values at T_a = 23 °C and V_{CC} = 3 V;
all parameters based on test circuits for FSK (Fig. 14 to 15) and ASK (Fig. 16 to 17), respectively;

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Input sensitivity **ASK**	f_{RF}= 433.92MHz	P_{minL_ASK}	B_{IF} = 180kHz, f_m = 2kHz BER $\leq 3 \cdot 10^{-3}$ LNA @ low gain		-96		dBm
	f_{RF}= 868.3MHz				-96		
	f_{RF}= 433.92MHz	P_{minH_ASK}	B_{IF} = 180kHz, f_m = 2kHz BER $\leq 3 \cdot 10^{-3}$ LNA @ high gain		-107		dBm
	f_{RF}= 868.3MHz				-107		
Input sensitivity **FSK**	f_{RF}= 433.92MHz	P_{minL_FSK}	B_{IF} = 180kHz, f_m = 2kHz $\Delta f = \pm$ 50 kHz BER $\leq 3 \cdot 10^{-3}$ LNA @ low gain		-87		dBm
	f_{RF}= 868.3MHz				-87		
	f_{RF}= 433.92MHz	P_{minH_FSK}	B_{IF} = 180kHz, f_m = 2kHz $\Delta f = \pm$ 50 kHz BER $\leq 3 \cdot 10^{-3}$ LNA @ high gain		-105		dBm
	f_{RF}= 868.3MHz				-105		
Maximum input signal **ASK**	f_{RF}= 433.92MHz	P_{maxL_ASK}	LNA @ low gain		-10		dBm
	f_{RF}= 868.3MHz				-10		
	f_{RF}= 433.92MHz	P_{maxH_ASK}	LNA @ high gain		-20		dBm
	f_{RF}= 868.3MHz				-20		
Maximum input signal **FSK**	f_{RF}= 433.92MHz	P_{maxL_FSK}	LNA @ low gain		-10		dBm
	f_{RF}= 868.3MHz				-10		
	f_{RF}= 433.92MHz	P_{maxH_FSK}	LNA @ high gain		-20		dBm
	f_{RF}= 868.3MHz				-20		
Start-up time - ASK		t_{on_ASK}	from standby to receive mode		1	1.5	ms
Start-up time - FSK		t_{on_FSK}	from standby to receive mode		1	1.5	ms
Spurious emission		P_{spur_RX}	referred to receiver input		-54		dBm

6.6 AC Characteristics of the Transmitter Part

all parameters under normal operating conditions, unless otherwise stated;
typical values at T_a = 23 °C and V_{CC} = 3 V;
all parameters based on test circuits for FSK (Fig. 14 to 15) and ASK (Fig. 16 to 17), respectively;

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Output power	f_{RF}= 433.92MHz	P1	mode = transmit, RPS = see para. 7.3 TXPOWER = 00		-7		dBm
	f_{RF}= 868.3MHz				-10		
Output power	f_{RF}= 433.92MHz	P2	mode = transmit, RPS = see para. 7.3 TXPOWER = 01		1		dBm
	f_{RF}= 868.3MHz				-2		
Output power	f_{RF}= 433.92MHz	P3	mode = transmit, RPS = see para. 7.3 TXPOWER = 10		6		dBm
	f_{RF}= 868.3MHz				3		
Output power	f_{RF}= 433.92MHz	P4	mode = transmit, RPS = see para. 7.3 TXPOWER = 11		10		dBm
	f_{RF}= 868.3MHz				9		
FSK deviation		Δf_{FSK}	depends on C_{x1}, C_{x2} and crystal parameters	±2.5	±25	±80	kHz
FM deviation		Δf_{FM}	please refer to the FM circuit in the cookbook		±6		kHz
Modulation frequency FM		f_{mod}				10	kHz
PLL reference spurious emission		P_{spur_PLL}				-40	dBm
Harmonic emission		P_{harm}				-36	dBm
Start-up time		t_{on_TX}	From standby to transmit mode		1	1.5	ms

6.7 Serial Control Interface

Parameter	Symbol	Condition	Min	Max	Unit
SDTA to SCLK set up time	t_{CS}		150		ns
SCLK to SDTA hold time	t_{CH}		50		ns
SCLK pulse width low	t_{CWL}		100		ns
SCLK pulse width high	t_{CWH}		100		ns
SCLK to SDEN set up time	t_{ES}		100		ns
SDEN pulse width	t_{EW}		100		ns
SDEN to SCLK hold time	t_{EH}		100		ns

6.8 Crystal Parameters

Parameter	Symbol	Condition	Min	Max	Unit
Crystal frequency	$f_{crystal}$	fundamental mode, AT	3	12	MHz
Load capacitance	C_{load}		10	15	pF
Static capacitance	C_0			5	pF
Equivalent series resistance	R_1			180	Ω
Spurious response	a_{spur}	only required for FSK		-10	dB

7 Application Circuit Examples

7.1 FSK Application Circuit Programmable User Mode (internal AFC option)

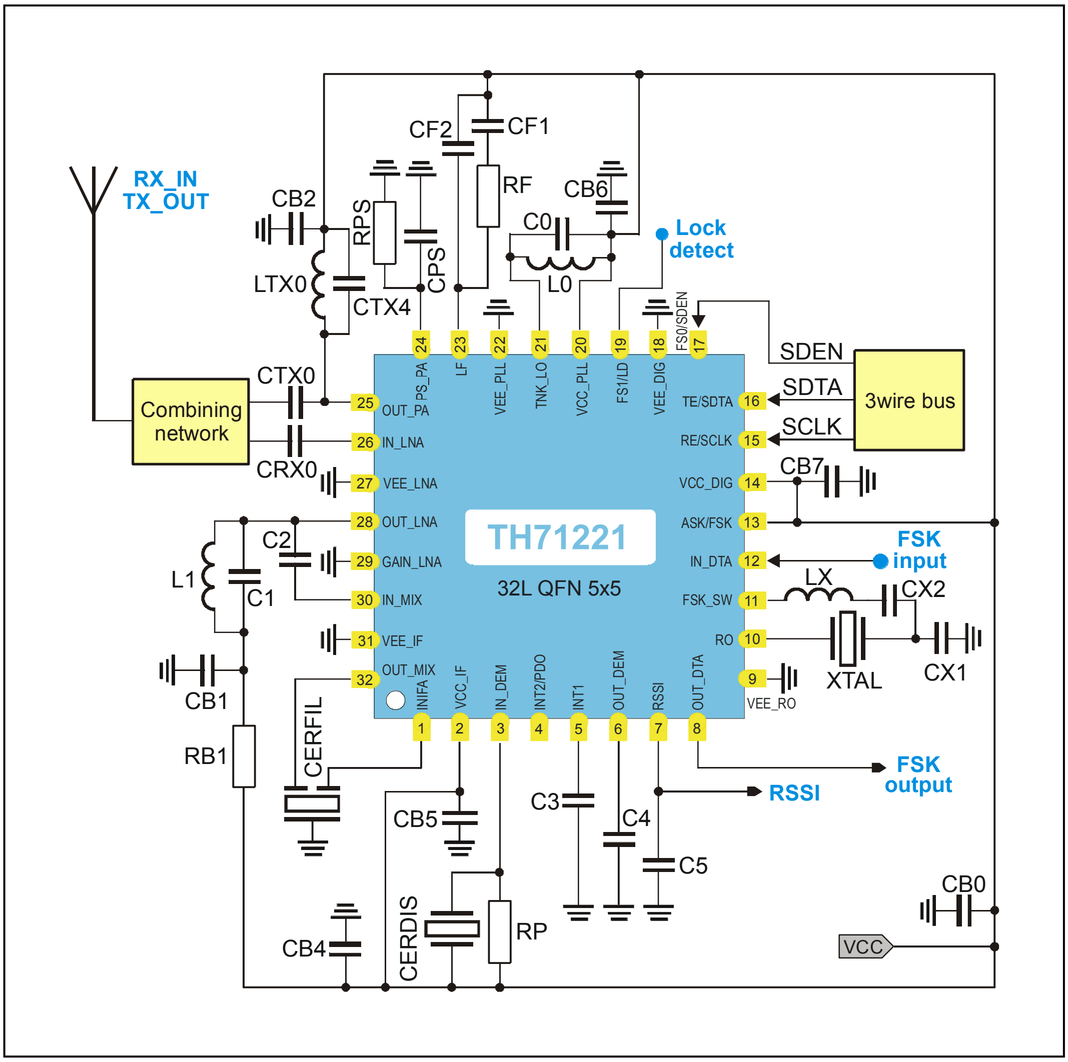


Fig. 14: Test circuit for FSK operation in Programmable User Mode (internal AFC option)

7.2 FSK Application Circuit Stand-alone User Mode

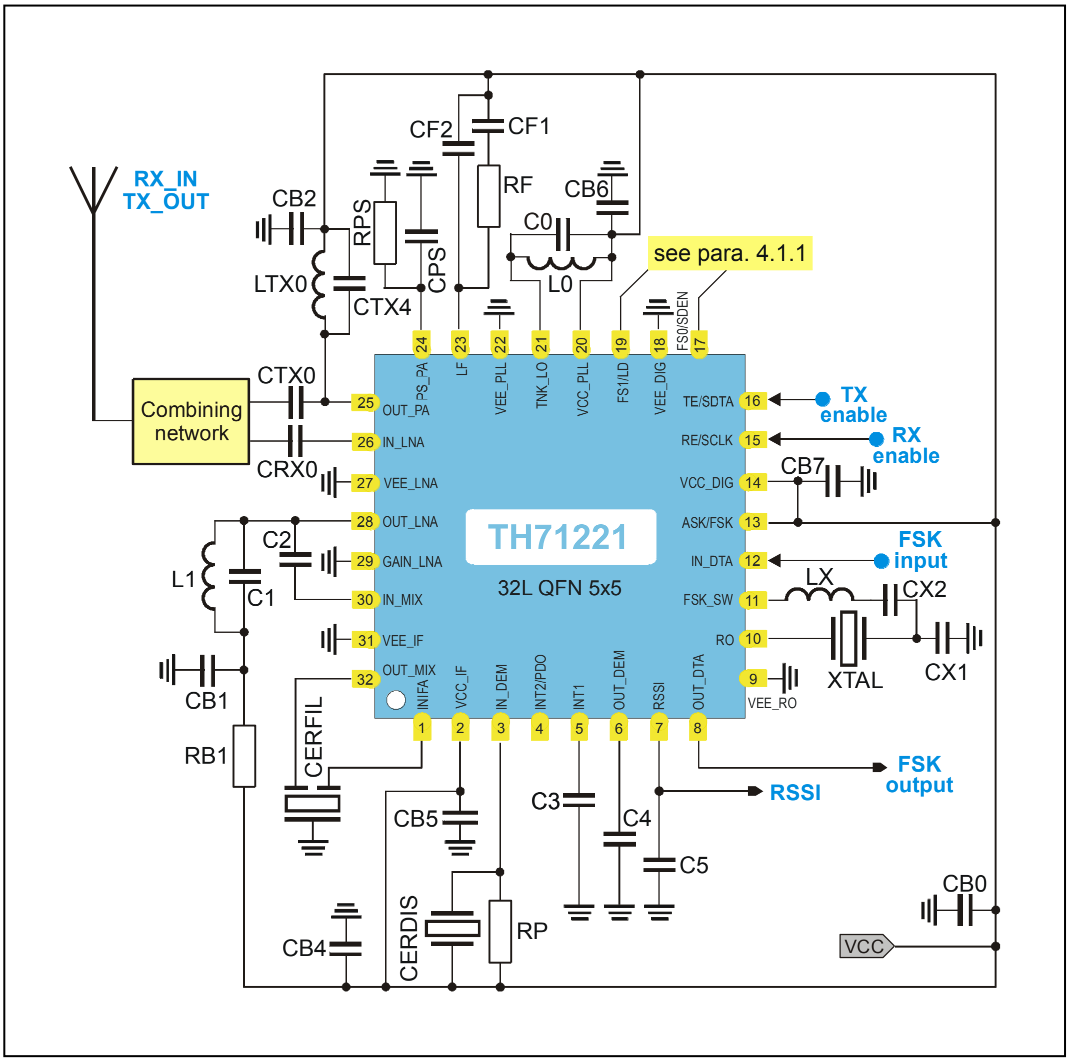


Fig. 15: Test circuit for FSK operation in Stand-alone User Mode

7.3 FSK Test Circuit Component List (Fig. 14 and Fig. 15)

Part	Size	Value @ 315 MHz	Value @ 433.92 MHz	Value @ 868.3 MHz	Value @ 915 MHz	Tol.	Description
C0	0603	1.2 pF	1.5 pF	1.8 pF	0.82 pF	±5%	VCO tank capacitor
C1	0603	3.9 pF	5.6 pF	2.2 pF	1.8 pF	±5%	LNA output tank capacitor
C2	0603	1.5 pF	1.5 pF	1.5 pF	1.5 pF	±5%	MIX input matching capacitor
C3	0603	10 nF	10 nF	10 nF	10 nF	±10%	data slicer capacitor
C4	0603	330 pF	330 pF	330 pF	330 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C5	0603	1.5 nF	1.5 nF	1.5 nF	1.5 nF	±10%	RSSI output low pass capacitor
CB0	1210	10 µF	10 µF	10 µF	10 µF	±20%	de-coupling capacitor
CB1	0603	10 nF	10 nF	10 nF	10 nF	±10%	de-coupling capacitor
CB2	0603	330 pF	330 pF	330 pF	330 pF	±10%	de-coupling capacitor
CB4	0603	10 nF	10 nF	10 nF	10 nF	±10%	de-coupling capacitor
CB5	0603	100 nF	100 nF	100 nF	100 nF	±10%	de-coupling capacitor
CB6	0603	100 pF	100 pF	100 pF	100 pF	±10%	de-coupling capacitor
CB7	0603	100 nF	100 nF	100 nF	100 nF	±10%	de-coupling capacitor
CF1	0603	1 nF	1 nF	1 nF	1 nF	±10%	loop filter capacitor
CF2	0603	68 pF	120 pF	150 pF	82 pF	±5%	loop filter capacitor
CPS	0603	10 nF	10 nF	10 nF	10 nF	±10%	power-select capacitor
CX1	0603	8.2 pF	10 pF	12 pF	12 pF	±5%	RO capacitor for FSK (Δf = ±20 kHz)
CX2	0603	150 pF	56 pF	18 pF	15 pF	±5%	RO capacitor for FSK (Δf = ±20 kHz)
CRX0	0603	100 pF	100 pF	100 pF	100 pF	±5%	RX coupling capacitor
CTX0	0603	10 pF	10 pF	10 pF	10 pF	±5%	TX coupling capacitor
CTX4	0603	12 pF	4.7 pF	2.2 pF	1.8 pF	±5%	TX impedance matching capacitor
RB1	0603	100 Ω	100 Ω	100 Ω	100 Ω	±5%	protection resistor
RF	0603	47 kΩ	47 kΩ	33 kΩ	33 kΩ	±5%	loop filter resistor
RP	0603	3.3 kΩ	3.3 kΩ	3.3 kΩ	3.3 kΩ	±5%	CERDIS loading resistor
RPS	0603	22 kΩ	33 kΩ	47 kΩ	47 kΩ	±5%	power-select resistor
L0	0603	47 nH	22 nH	3.9 nH	3.9 nH	±5%	VCO tank inductor from Würth-Elektronik (WE-KI series) or equivalent part
L1	0603	33 nH	15 nH	4.7 nH	4.7 nH	±5%	LNA output tank inductor from Würth-Elektronik (WE-KI series) or equivalent part
LTX0	0603	15 nH	15 nH	3.9 nH	3.9 nH	±5%	impedance matching inductor from Würth-Elektronik (WE-KI series) or equivalent part
LX	0603	0 Ω	0 Ω	10 nH	10 nH	±5%	RO inductor
XTAL	HC49 SMD 7x5	7.1505 MHz ±20ppm cal., ±20ppm temp.					fundamental-mode crystal, C_{load} = 10 pF to 15pF, $C_{0,\ max}$ = 7 pF, $R_{m,\ max}$ = 70 Ω
CERFIL	SMD 3.45x3.1	SFECF10M7HA00 B_{3dB} = 180 kHz					ceramic filter from Murata, or equivalent part
CERDIS	SMD 4.5x2	CDSCB10M7GA136					ceramic Discriminator from Murata, or equivalent part

Note: - Antenna matching network according to paragraph 9

7.4 ASK Application Circuit Programmable User Mode (normal data slicer option)

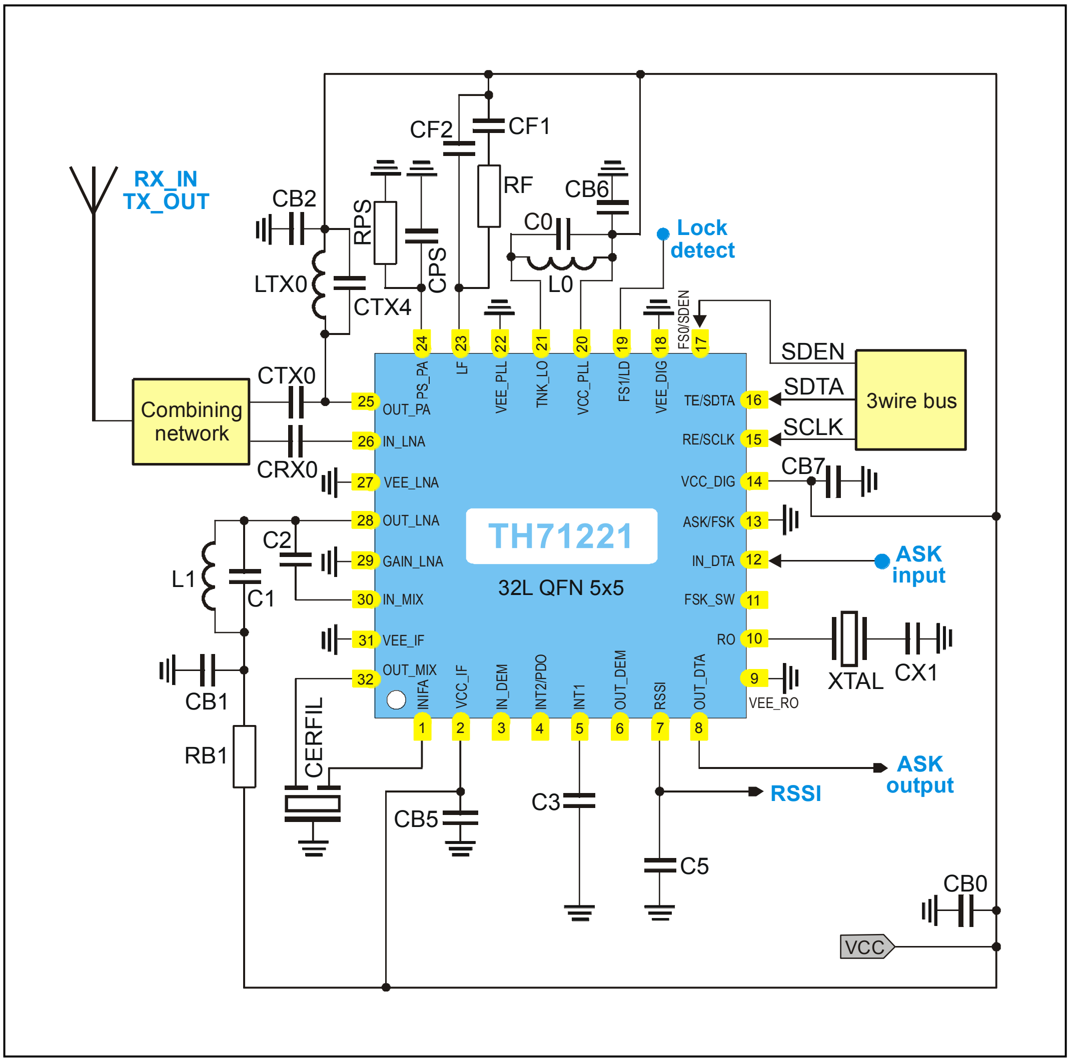


Fig. 16: Test circuit for ASK operation in Programmable User Mode (normal data slicer option)

Software Settings for ASK

Channel frequency	f_{RO} = 8.0000MHz				CPCUR		VCOCUR	
	RR	NR	RT	NT	RX	TX	RX	TX
315.00 MHz	80	3043	8	315	260µA	1300µA	300 µA	900µA
434.00 MHz	80	4233	8	434	260µA	1300µA	300 µA	900µA
915.00 MHz	80	9043	8	915	260µA	1300µA	300 µA	900µA

7.5 ASK Test Circuit Component List (Fig. 16)

Part	Size	Value @ 315 MHz	Value @ 434 MHz	Value @ 915 MHz	Tol.	Description
C0	0603	1.5 pF	1.8 pF	1 pF	±5%	VCO tank capacitor
C1	0603	3.9 pF	5.6 pF	1.8 pF	±5%	LNA output tank capacitor
C2	0603	1.5 pF	1.0 pF	1.5 pF	±5%	MIX input matching capacitor
C3	0603	10 nF	10 nF	10 nF	±10%	data slicer capacitor
C5	0603	1.5 nF	1.5 nF	1.5 nF	±10%	RSSI output low pass capacitor
CB0	1210	10 µF	10 µF	10 µF	±20%	de-coupling capacitor
CB1	0603	10 nF	10 nF	10 nF	±10%	de-coupling capacitor
CB2	0603	330 pF	330 pF	330 pF	±10%	de-coupling capacitor
CB5	0603	100 nF	100 nF	100 nF	±10%	de-coupling capacitor
CB6	0603	100 pF	100 pF	100 pF	±10%	de-coupling capacitor
CB7	0603	100 nF	100 nF	100 nF	±10%	de-coupling capacitor
CF1	0603	100 pF	100 pF	100 pF	±10%	loop filter capacitor
CF2	0603	39 pF	39 pF	39 pF	±5%	loop filter capacitor
CPS	0603	1 nF	1 nF	1 nF	±10%	power-select capacitor, depending on data rate
CX1	0805	18 pF	18 pF	18 pF	±5%	RO capacitor
CRX0	0603	100 pF	100 pF	10 pF	±5%	RX coupling capacitor
CTX0	0603	10 pF	10 pF	10 pF	±5%	TX coupling capacitor
CTX4	0603	12 pF	4.7 pF	1.8 pF	±5%	TX impedance matching capacitor
RB1	0603	100 Ω	100 Ω	100 Ω	±5%	protection resistor
RF	0603	33 kΩ	33 kΩ	33 kΩ	±5%	loop filter resistor
RPS	0603	18 kΩ	33 kΩ	43 kΩ	±5%	power-select resistor
L0	0603	47 nH	22 nH	3.9 nH	±5%	VCO tank inductor from Würth-Elektronik (WE-KI series) or equivalent part
L1	0603	33 nH	15 nH	4.7 nH	±5%	LNA output tank inductor from Würth-Elektronik (WE-KI series) or equivalent part
LTX0	0603	15 nH	15 nH	3.9 nH	±5%	impedance matching inductor from Würth-Elektronik (WE-KI series) or equivalent part
XTAL	HC49 SMD 7x5	8.0000 MHz ±20ppm cal., ±20ppm temp.				fundamental-mode crystal, C_{load} = 10 pF to 15pF, $C_{0,\ max}$ = 7 pF, $R_{m,\ max}$ = 70 Ω
CERFIL	SMD 3.45x3.1	SFECF10M7HA00 B_{3dB} = 180 kHz				ceramic filter from Murata, or equivalent part

Note: - Antenna matching network according to paragraph 9

7.6 ASK Application Circuit Programmable User Mode (peak detector option)

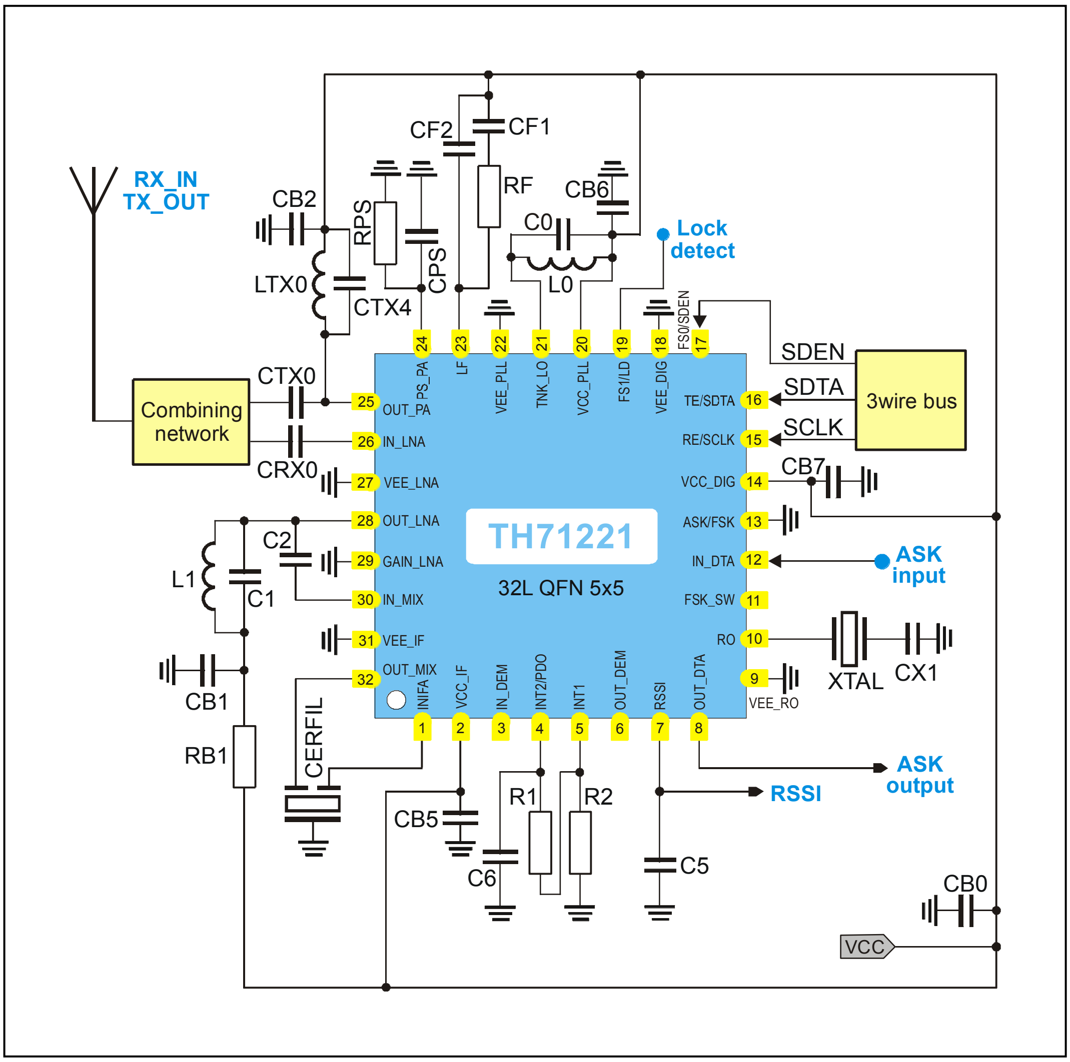


Fig. 17: Test circuit for ASK operation in Programmable User Mode (internal Peak Detector option)

Software Settings for ASK

Channel frequency	f_{RO} = 8.0000MHz				CPCUR		VCOCUR	
	RR	NR	RT	NT	RX	TX	RX	TX
315.00 MHz	80	3043	8	315	260µA	1300µA	300 µA	900µA
434.00 MHz	80	4233	8	434	260µA	1300µA	300 µA	900µA
915.00 MHz	80	9043	8	915	260µA	1300µA	300 µA	900µA

7.7 ASK Test Circuit Component List (Fig. 17)

Part	Size	Value @ 315 MHz	Value @ 434 MHz	Value @ 915 MHz	Tol.	Description
C0	0603	1.5 pF	1.8	1 pF	±5%	VCO tank capacitor
C1	0603	3.9 pF	5.6 pF	1.8F	±5%	LNA output tank capacitor
C2	0603	1.5 pF	1.0 pF	1.5 pF	±5%	MIX input matching capacitor
C5	0603	1.5 nF	1.5 nF	1.5 nF	±10%	RSSI output low pass capacitor
C6	0603	100 nF	100 nF	100 nF	±10%	PKDET capacitor
CB0	1210	10 µF	10 µF	10 µF	±20%	de-coupling capacitor
CB1	0603	10 nF	10 nF	10 nF	±10%	de-coupling capacitor
CB2	0603	330 pF	330 pF	330 pF	±10%	de-coupling capacitor
CB5	0603	100 nF	100 nF	100 nF	±10%	de-coupling capacitor
CB6	0603	100 pF	100 pF	100 pF	±10%	de-coupling capacitor
CB7	0603	100 nF	100 nF	100 nF	±10%	de-coupling capacitor
CF1	0603	100 pF	100 pF	100 pF	±10%	loop filter capacitor
CF2	0603	39 pF	39 pF	39 pF	±5%	loop filter capacitor
CPS	0603	1 nF	1 nF	1 nF	±10%	power-select capacitor, depending on data rate
CX1	0805	18 pF	18 pF	18 pF	±5%	RO capacitor
CRX0	0603	100 pF	100 pF	10 pF	±5%	RX coupling capacitor
CTX0	0603	10 pF	10 pF	10 pF	±5%	TX coupling capacitor
CTX4	0603	12 pF	4.7 pF	1.8 pF	±5%	TX impedance matching capacitor
R1	0603	100 kΩ	100 kΩ	100 kΩ	±5%	PKDET resistor
R2	0603	680 kΩ	680 kΩ	680 kΩ	±5%	PKDET resistor
RB1	0603	100 Ω	100 Ω	100 Ω	±5%	protection resistor
RF	0603	33 kΩ	33 kΩ	33 kΩ	±5%	loop filter resistor
RPS	0603	18 kΩ	33 kΩ	43 kΩ	±5%	power-select resistor
L0	0603	47 nH	22nH	3.9 nH	±5%	VCO tank inductor from Würth-Elektronik (WE-KI series) or equivalent part
L1	0603	33 nH	15 nH	4.7 nH	±5%	LNA output tank inductor from Würth-Elektronik (WE-KI series) or equivalent part
LTX0	0603	15 nH	15 nH	3.9 nH	±5%	impedance matching inductor from Würth-Elektronik (WE-KI series) or equivalent part
XTAL	HC49 SMD 7x5	8.0000 MHz ±20ppm cal., ±20ppm temp.				fundamental-mode crystal, C_{load} = 10 pF to 15pF, $C_{0, max}$ = 7 pF, $R_{m, max}$ = 70 Ω
CERFIL	SMD 3.45x3.1	SFECF10M7HA00 B_{3dB} = 180 kHz				ceramic filter from Murata, or equivalent part

Note: - Antenna matching network according to paragraph 9

8 Extended Frequency Range

The operating frequency range of 300 MHz to 930 MHz can be covered without the use of an additional VCO varactor diode. A frequency range extension down to 27 MHz can be realized by adding an external varactor diode to the VCO tank.

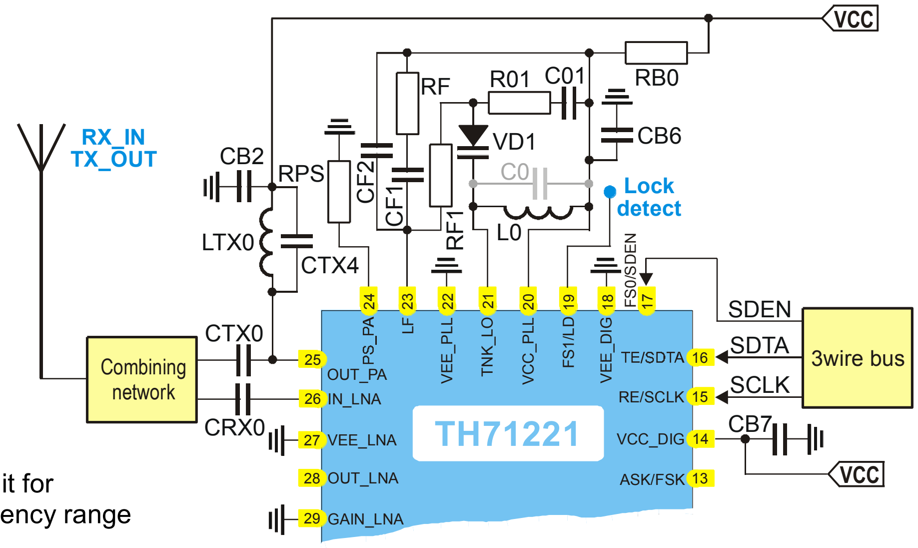


Fig. 18: VCO tank circuit for extended frequency range

8.1 Board Component List (Fig. 18)

Part	Size	Value @ 27 MHz	Value @ 40 MHz	Value @ 80 MHz	Value @ 144 MHz	Value @ 170 MHz	Description
C0	0805	NIP	NIP	NIP	NIP	NIP	VCO tank capacitor
C01	0805	1 nF	1 nF	68 pF	100pF	100 pF	VCO tank capacitor
CB2	0603	330 pF	330 pF	330 pF	330 pF	330 pF	de-coupling capacitor
VD1	SOD-323	BBY65	BBY65	BB639	BB833	BB535	varactor diode
CF1	0605	1 µF	1 µF	1µF	1µF	1µF	loop filter capacitor
CF2	0605	220 nF	100 nF	100nF	100 nF	100 nF	loop filter capacitor
CTX4	0605	NIP	33 pF	18pF	10 pF	8.2 pF	TX impedance matching capacitor
RB0	0605	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	protection resistor
R01	0805	22 Ω	22 Ω	0 Ω	0 Ω	0 Ω	VCO tank resistor
RF	0805	1.8 kΩ	1.8 kΩ	1.8 kΩ	2.7 kΩ	390 Ω	loop filter resistor
RF1	0805	10 kΩ	10 kΩ	10 kΩ	10 kΩ	10 kΩ	loop filter resistor
RPS	0805	15 kΩ	15 kΩ	15 kΩ	22 kΩ	33 kΩ	power-select resistor
CTX0	0805	10 nF	10 nF	10 nF	1 nF	220 pF	TX coupling capacitor
CRX0	0805	10 nF	10 nF	10 nF	1 nF	220 pF	RX coupling capacitor
L0	0805	1.2 µH	1.0 µH	220 nH	100 nH	47 nH	VCO tank inductor
LTX0	0805	2.2 µH	330 nH	220 nH	100 nH	100 nH	TX impedance matching inductor
CB6	0805	10 nF	10 nF	10 nF	1 nF	1 nF	de-coupling capacitor
CB7	0805	100 nF	100 nF	100 nF	100 nF	100 nF	de-coupling capacitor
f_R		25 kHz	25 kHz	25 kHz	25 kHz	100 kHz	**frequency resolution**
NT		1080	1600	3200	5760	1700	**NT counter**
NR		1508	2028	2772	5332	1807	**NR counter**
LO injection		high	high	low	low	high	

Note: The component values are optimized for the above listed settings of f_R, NR and NT. Direct VCO modulation as explained in section 3.3.5 must be applied.

9 TX/RX Combining Network

9.1 Board Component List (Fig. 19)

Part	Size	Value @ 315 MHz	Value @ 433.92 MHz	Value @ 868.3 MHz	Value @ 915 MHz
CRX0	0603	100 pF	100 pF	100 pF	100 pF
CTX0	0603	10 pF	10 pF	10 pF	10 pF
CTX1	0603	10 pF	6.8 pF	5.6 pF	4.7 pF
CTX2	0603	10 pF	6.8 pF	3.9 pF	3.9 pF
CTX4	0603	12 pF	4.7 pF	2.2 pF	1.8 pF
LRX2	0603	82 nH	56 nH	15 nH	15 nH
LTX0	0603	15 nH	15 nH	3.9 pF	3.9 nH
LTX1	0603	33 nH	33 nH	10 nH	10 nH
CB2	0603	330 pF	330 pF	330 pF	330 pF

- No TX/RX switch required
- Direct connection to $\lambda/4$ antenna possible

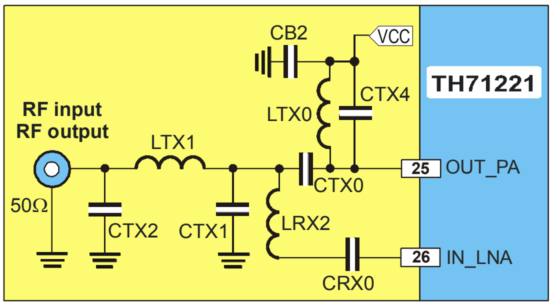


Fig. 19: Combining network schematic

9.2 Typical LNA S-Parameters in Receive Mode

Low Gain Mode

Frequency	Re[S_{11}]	Im[S_{11}]	Re[S_{12}]	Im[S_{12}]	Re[S_{21}]	Im[S_{21}]	Re[S_{22}]	Im[S_{22}]
27 MHZ	0.9138	-0.0145	6.06E-005	4.27E-004	-0.4172	0.0334	0.9986	-0.0095
40 MHz	0.9139	-0.0229	5.53E-005	6.73E-004	-0.4092	0.0400	0.9984	-0.0136
80 MHz	0.9126	-0.0481	5.36E-005	1.48E-004	-0.3989	0.0581	0.9979	-0.0265
170 MHz	0.9054	-0.1026	7.44E-004	3.25E-003	-0.3828	0.1056	0.9966	-0.0558
315 MHz	0.8836	-0.1814	2.16E-004	6.21-E003	-0.3300	0.1798	0.9926	-0.1033
433 MHz	0.8622	-0.2625	7.81E-004	6.34E-003	-0.3248	0.2168	0.9870	-0.1417
868 MHz	0.7161	-0.4577	2.35E-003	1.09E-003	-0.1265	0.3187	0.9543	-0.2829
915 MHz	0.6975	-0.4753	2.24E-003	1.10E-003	-0.1062	0.3206	0.9494	-0.2980

Note: input and output of the LNA are connected to 50 Ω ports without matching elements

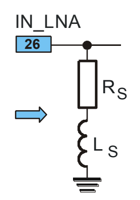
High Gain Mode

Frequency	Re[S_{11}]	Im[S_{11}]	Re[S_{12}]	Im[S_{12}]	Re[S_{21}]	Im[S_{21}]	Re[S_{22}]	Im[S_{22}]
27 MHZ	0.8417	-0.0151	1.36E-004	8.63E-005	-4.0840	0.1272	0.9994	-0.0092
40 MHz	0.8424	-0.0276	1.42E-004	1.07E-004	-4.0840	0.2055	0.9994	-0.0135
80 MHz	0.8403	-0.0621	1.52E-004	1.83E-004	-4.0630	0.4338	0.9991	-0.0269
170 MHz	0.8273	-0.1344	1.86E-004	3.72E-003	-3.9550	0.9279	0.9977	-0.0571
315 MHz	0.7884	-0.2328	4.02E-004	7.04E-003	-3.5100	1.6990	0.9846	-0.1072
433 MHz	0.7492	-0.3405	1.51E-004	6.18E-003	-3.4700	1.9920	0.9839	-0.1439
868 MHz	0.5007	-0.5322	2.36E-004	1.06E-003	-1.6710	3.2230	0.9501	-0.2847
915 MHz	0.4714	-0.5440	1.94E-004	1.06E-003	-1.4690	3.2700	0.9451	-0.2995

Note: input and output of the LNA are connected to 50 Ω ports without matching elements

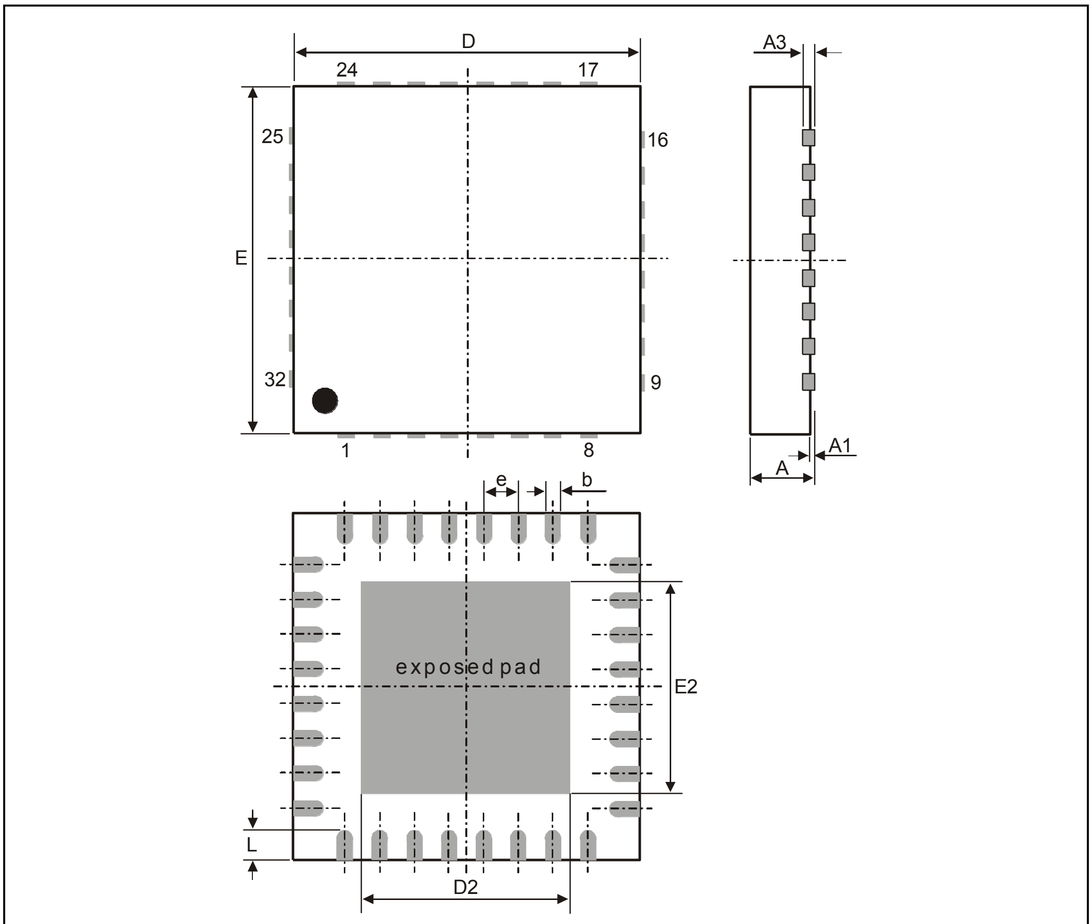
9.3 LNA Input Impedances in Transmit Mode

Mode	**LNA off, Pin LNA is shorted**				
Frequency	**R_S**	**L_S**	**Frequency**	**R_S**	**L_S**
27 MHz	33.6 Ω	1.9 nH	**315 MHz**	32.7 Ω	2.2 nH
40 MHz	33.6 Ω	2.1 nH	**433 MHz**	33.6 Ω	2.3 nH
80 MHz	33.6 Ω	2.4 nH	**868 MHz**	35.7 Ω	2.7 nH
170 MHz	34.3 Ω	2.2 nH	**915 MHz**	36.6 Ω	2.8 nH



10 Package Description

The device TH71221 is RoHS compliant.



The "exposed pad" is not connected to internal ground, it should not be connected to the PCB.

Fig 12: 32L QFN 5x5 Quad

all Dimension in mm										
	D	**E**	**D2**	**E2**	**A**	**A1**	**A3**	**L**	**e**	**b**
min max	4.75 5.25	4.75 5.25	3.00 3.25	3.00 3.25	0.80 1.00	0 0.05	0.20	0.3 0.5	0.50	0.18 0.30
all Dimension in inch										
min max	0.187 0.207	0.187 0.207	0.118 0.128	0.118 0.128	0.0315 0.0393	0 0.002	0.0079	0.0118 0.0197	0.0197	0.0071 0.0118

10.1 Soldering Information

- The device TH71221 is qualified for MSL3 with soldering peak temperature 260 deg C according to JEDEC J-STD-20

11 Manufacturability Information

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/quality.aspx

12 ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

Your Notes

13 Disclaimer

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