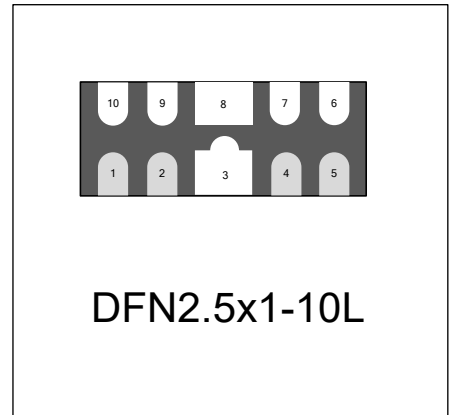


Features

- Solid-state silicon-avalanche technology
- Low operating and clamping voltage
- Up to four I/O Lines of Protection
- Ultra low capacitance: 0.35pF typical(I/O to I/O)
- Low Leakage
- Low operating voltage:5V
- Flow-Through design



IEC COMPATIBILITY (EN61000-4)

- IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact)
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- IEC 61000-4-5 (Lightning) 5A (8/20 μs)

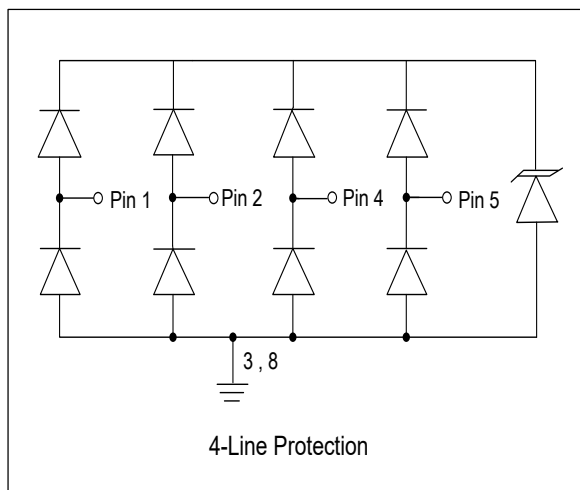
Mechanical Characteristics

- DFN-10L package (2.5×1.0×0.58mm)
- Molding compound flammability rating: UL 94V-0
- Marking: Marking Code
- Packaging: Tape and Reel
- RoHS/WEEE Compliant
- MSD Level: 2

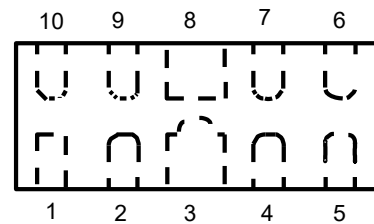
Applications

- Digital Visual Interface(DVI)
- MDDI Ports
- DisplayPort™ Interface
- PCI Express
- High Definition Multi-Media Interface(HDMI)
- eSATA Interfaces

Circuit Diagram



Schematic & PIN Configuration



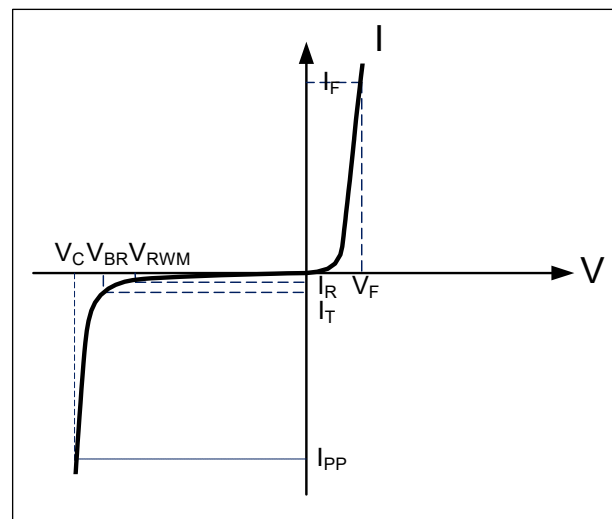
Pin	Identificaion
1,2,4,5	Input Lines
6,7,9,10	Output Lines (No Internal Connection)
3,8	Ground

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power ($t_p = 8/20\mu s$)	P_{PP}	150	Watts
Peak Pulse Current ($t_p = 8/20\mu s$)	I_{pp}	5	A
ESD per IEC 61000-4-2(Air)	V_{ESD}	+/-17	kV
ESD per IEC 61000-4-2(contact)		+/-12	
Operating Temperature	T_J	-55 to + 125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Parameters (T=25°C)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F

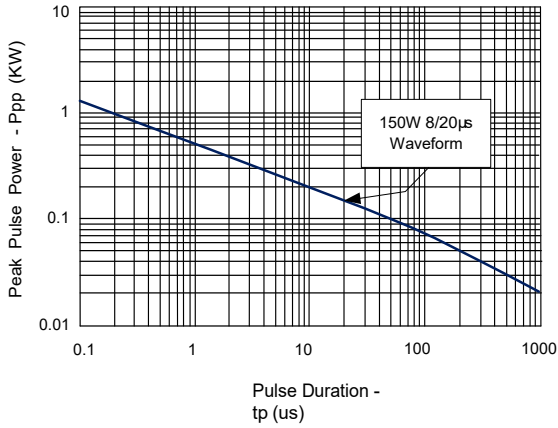


Electrical Characteristics

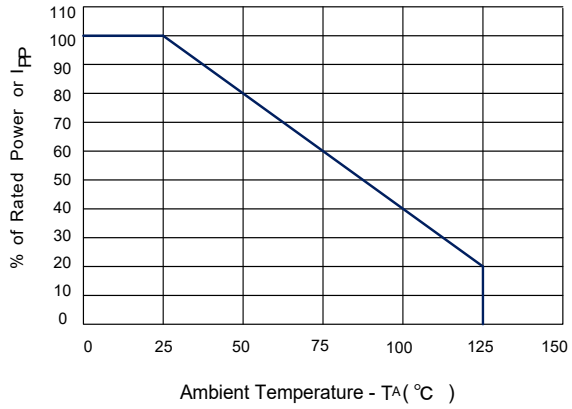
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}	Any I/O pin to ground			5.0	V
Reverse Breakdown Voltage	V_{BR}	$I_T = 1mA$ Any I/O pin to ground	6.0			V
Reverse Leakage Current	I_R	$V_{RWM} = 5V, T = 25^\circ C$ Any I/O pin to ground			1	μA
Clamping Voltage	V_C	$I_{pp} = 5A, t_p = 8/20\mu s$ Any I/O pin to ground			15	V
Junction Capacitance	C_j	$V_R = 0V, f = 1MHz$ I/O pin to GND			0.8	pF
		$V_R = 0V, f = 1MHz$ Between I/O pins		0.3	0.35	pF

Typical Characteristics

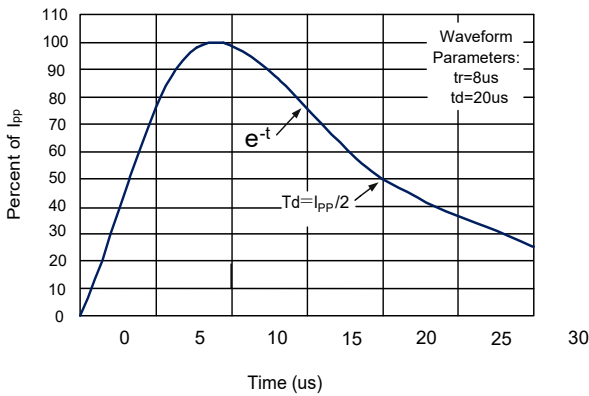
Non-Repetitive Peak Pulse Power vs. Pulse Time



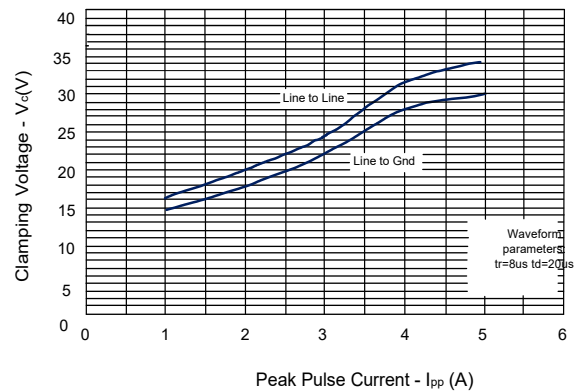
Power Derating curve



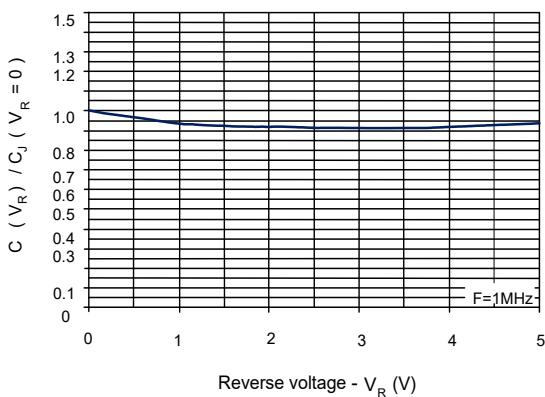
Pulse Waveform



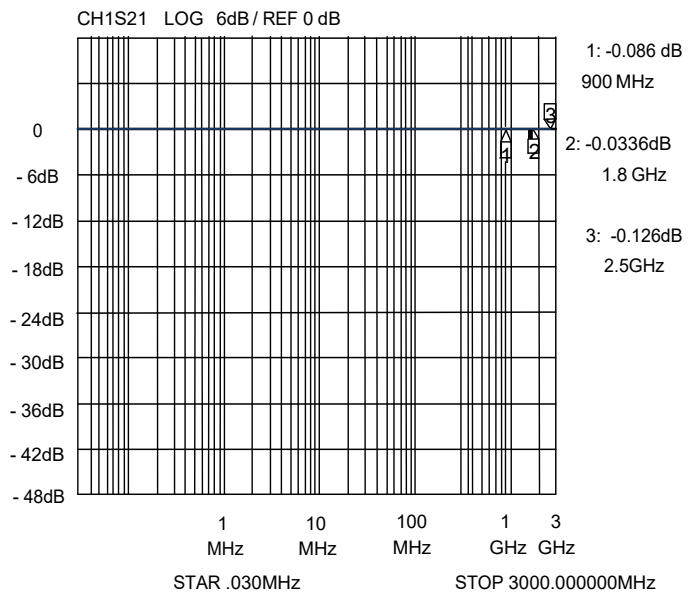
Clamping Voltage vs. Peak Pulse Current



Normalized Capacitance vs. Reverse Voltage



Insertion Loss S21 - I/O to GND



Design Recommendations for HDMI protection

Adding external ESD protection to HDMI ports can be challenging. First, ESD protection devices have an inherent junction capacitance. Furthermore, adding even a small amount of capacitance will cause the impedance of the differential pair to drop. Second, large packages and land pattern requirements cause discontinuities that adversely affect signal integrity. The MDFN10A54U are specifically designed for protection of high-speed interfaces such as HDMI.

They present <math><0.4\text{pF}</math> capacitance between the pairs while being rated to handle $\pm 8\text{kV}$ ESD contact discharges ($\pm 15\text{kV}$ air discharge) as outlined in IEC 61000-4-2. Each device is in a leadless SLP package that is less than 1.1mm wide. They are designed such that the traces flow straight through the device. The narrow package and flow-through design reduces discontinuities and minimizes impact on signal integrity. This becomes even more critical as signal speeds increase.

Pin Configuration

Figure 1 is an example of how to route the high speed differential traces through the MDFN10A054U. The solid line represents the PCB trace. The PCB traces are used to connect the pin pairs for each line (pin 1 to pin 10, pin 2 to pin 9, pin 4 to pin 7, pin 5 to pin 6). For example, line 1 enters at pin 1 and exits at Pin 10 and the PCB trace connects pin 1 and 10 together. This is true for lines connected at pins 2, 4, and 5 also. Ground is connected at pins 3 and 8. One large ground pad should be used in lieu of two separate pads. The same layout rules apply for the BDFN10A054U

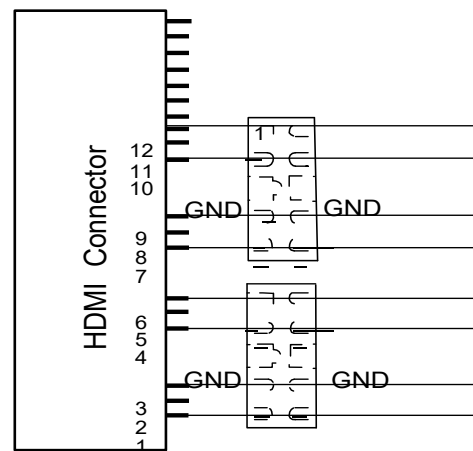
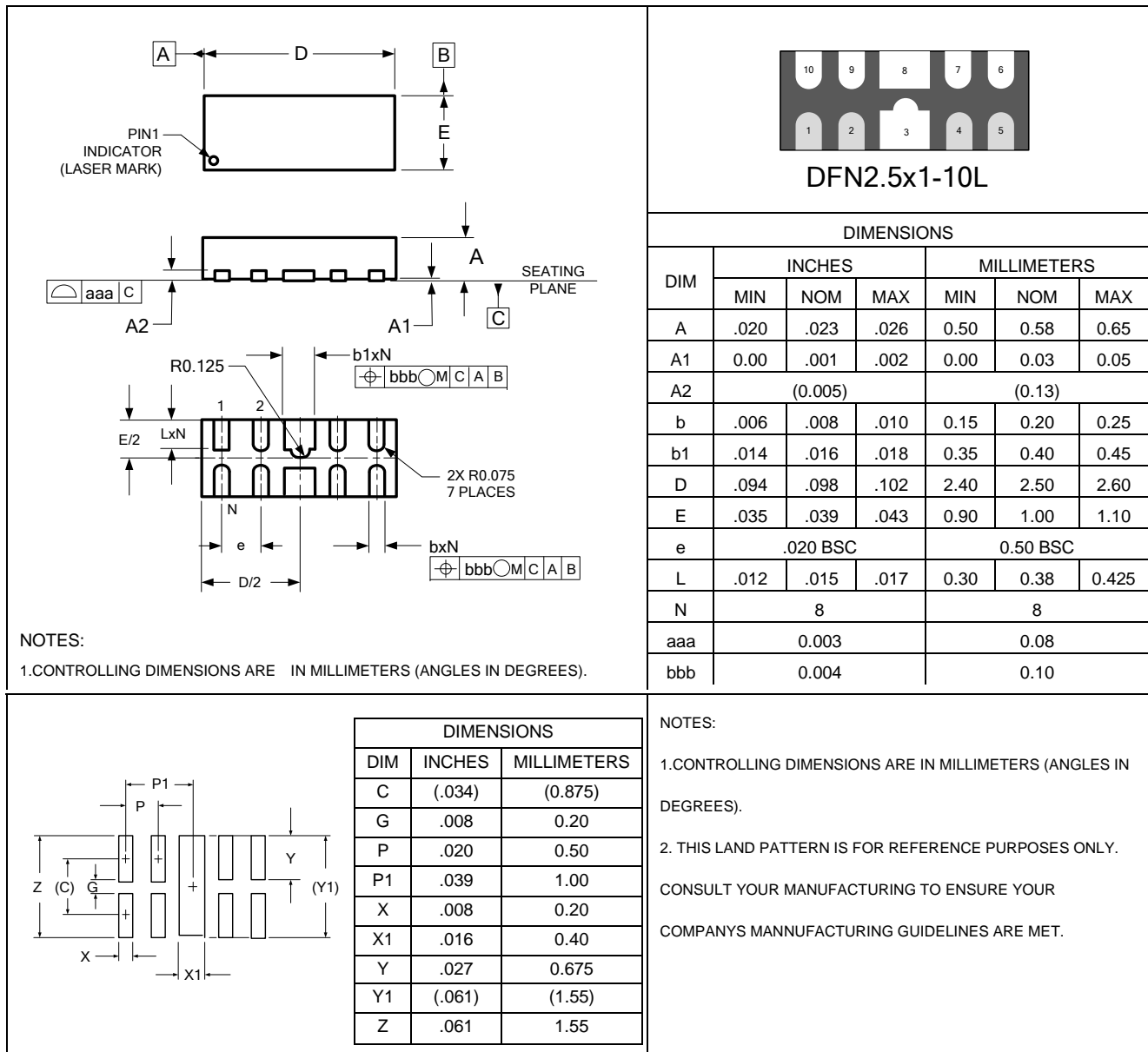


Figure 1. Flow through layout Using BDFN10A054U

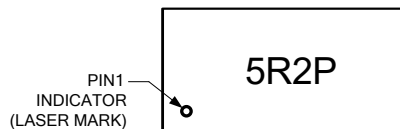
Design Recommendations for HDMI Protection

Good circuit board layout is critical not only for signal integrity, but also for effective suppression of ESD induced transients. For optimum ESD protection, the following guidelines are recommended:

- Place the device as close to the connector as possible. This practice restricts ESD coupling into adjacent traces and reduces parasitic inductance.
- The ESD transient return path to ground should be kept as short as possible. Whenever possible, use multiple micro vias connected directly from the device ground pad to the ground plane.
- Avoid running critical signals near board edges.

Outline Drawing – DFN-10L

Marking Codes

Part Number	MDFN10A054U
Marking Code	5R2P


Order Information

PN#	Type	Reel size	MOQ/interal box	MOQ/carton
MDFN10A054U	T/R	7 inch	20 reel= 60,000/box	4 box =240,000/carton

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[MPLAD30KP43CAE3](#) [SMAJ43A-TP](#) [D5V0F6U8LP33-7](#) [TVS5501V10MUT5G](#) [5.0SMLJ24CA-TP](#) [SMAJ110CA-TP](#) [MPLAD15KP75CAE3](#)
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