TRANSIENT VOLTAGE SUPPRESSOR (TVS) ARRAY A UT848ZA



iPU SEMI

UT848ZA

TVS ARRAY ▲ SMD type

Protects four I/O lines

AEC-Q101 qualified

4-CHANNEL A TVS ARRAY

ESD Protection for high-speed data lines

Ultra-low capacitance (I/O) to GND ▲ 0.28pF 2.5mm x 1.0mm x 0.5mm ▲ DFN2510-10L package

TRANK





SPECIFICATION

Item		Characteristics
Operating Junction Temperature Range	TJ	-55°C to +125°C
Storage Temperature Range	Ts	-55°C to +150°C
Peak Pulse Current (8/20µs)	I _{PP}	6A
ESD Rating (Per IEC 61000-4-2 ▲ Contact)	V _{ESD}	±14kV
ESD Rating (Per IEC 61000-4-2 ▲ Air)	V _{ESD}	±15kV

DESCRIPTION

The UT848ZA is a Transient Voltage Suppressor (TVS) array designed to protect sensitive high-speed data and transmission lines from high Electrostatic Discharge (ESD) and Cable Discharge Event (CDE).

This TVS array features ultra-low capacitance and low ESD clamping voltage using iPU's proprietary deep snapback technology.

The small flow-through style package enables simple PCB layout and facilitates necessary matched trace lengths to maintain consistent impedance between high-speed differential lines such USB 3.0/3.1, V-by-one and eSATA interfaces.

EMC STANDARDS

- ▲ IEC 61000-4-2 (ESD): ±14kV (Contact)
- ▲ IEC 61000-4-2 (ESD): ±15kV (Air)
- ▲ IEC 61000-4-4 (EFT): 40A (5/50ns)
- LEC 61000-4-5 (Lightning): 6A (8/20μs)

APPLICATIONS

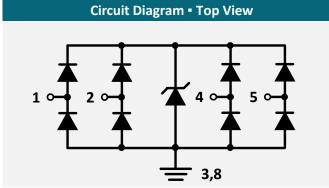
Automotive	Display Port	Data and I/O	SATA/eSATA	Thunderbolt	USB 2.0, 3.0
	Interface	Lines Protection	Interface	Interface	and 3.1
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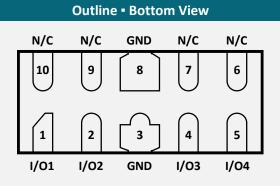
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PIN DESCRIPTION





ELECTRICAL CHARACTERISTICS A T_J = 25°C, unless otherwise noted

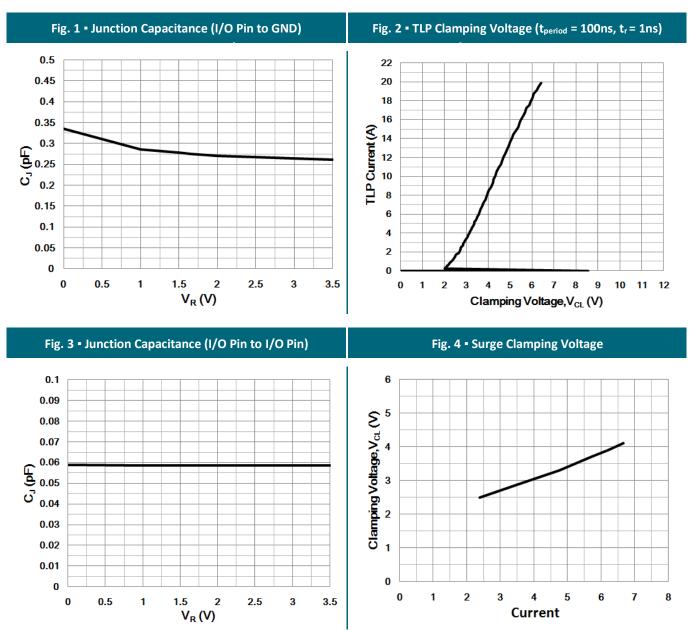
Item	Condition	Symbol	Min.	Тур.	Max.	Unit
Reverse Working Voltage	Any I/O Pin to GND	V _{RWM}			3.3	V
Breakdown Voltage	$I_{BR} = 1$ mA, any I/O Pin to GND	V_{BR}	6.5		16	V
Forward Voltage	I _F = 15mA, any I/O Pin to GND	VF		1		V
Reverse Leakage Current	V_{RWM} = 3.3V, any I/O Pin to GND	I _R			1	μA
Surge Clamping Voltage (8/20µs)	$I_{PP} = 5A$, any I/O Pin to GND	Vc		3.3		V
TLP Clamping Voltage Note1	I_{TLP} = 1A, any I/O Pin to GND	Vc		2.5		V
TLP Clamping Voltage Note1	I_{TLP} = 16A, any I/O Pin to GND	Vc		5.5		V
TLP Dynamic Resistance Note2	Any I/O Pin to GND	R _{DYN}		0.2		Ω
lunction Consoltance	V_R = 1.5V, f = 1MHz, any I/O Pin to GND	C		0.28	0.33	۳Ľ
Junction Capacitance	V_R = 1.5V, f = 1MHz, between I/O Pins	C		0.05	0.1	pF

Note

- 1: t_{period} = 100ns, t_r = 1ns
- 2: t_{period} = 100ns, t_r = 1ns



TYPICAL OPERATING CHARACTERISTICS

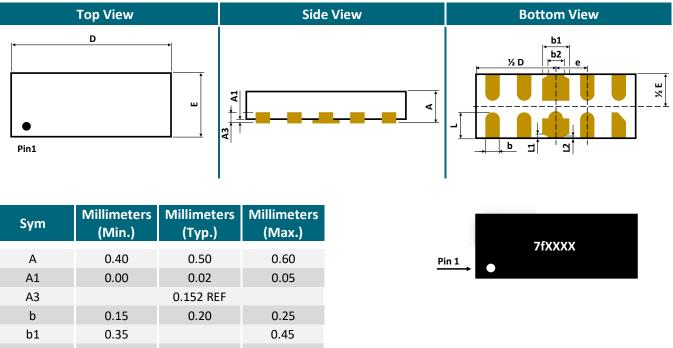


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PACKAGE OUTLINE AND PART MARKING



Sym	(Min.)	(Typ.)	(Max.)		
А	0.40	0.50	0.60		
A1	0.00	0.02	0.05		
A3		0.152 REF			
b	0.15	0.20	0.25		
b1	0.35		0.45		
b2	0.13		0.30		
D	2.40	2.50	2.60		
E	0.90	1.00	1.10		
е	0.50 BSC				
L1	0.075 REF				
L2	0.050 REF				
L	0.30	0.40	0.50		

Mark	ing:	
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11101 N.116.				
7f:	Product code			
	UT848ZA			
XXXX:	Date code			

Note

1:	Package Outline Unit Description:
	BSC: Basic. Represents theoretical exact dimension or dimension target.
	MIN: Minimum dimension specified
	MAX: Maximum dimension specified
	REF: Reference. Represents dimension for reference use only. This value is not a device specification.
	TYP: Typical. Provided as a general value. This value is not a device specification.
2:	Dimensions in Millimeters

- 3: Drawing not to scale
- 4: These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

ORDERING INFORMATION

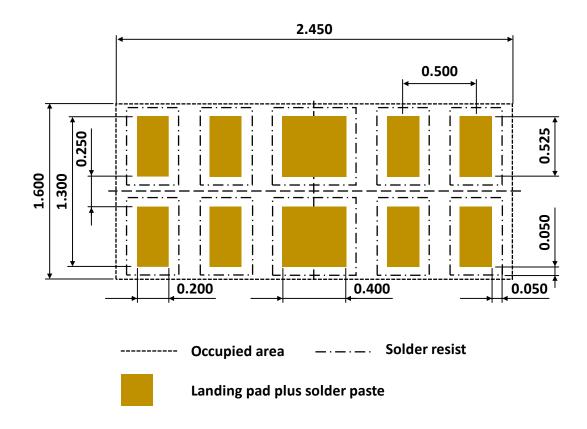
Part Number	Package Type	Package Code	Part Marking	Parameter
UT848ZAD5A	DFN2510-10L	D5A	7fXXXX	7f = Product Code XXXX = Date Code

Package Type	Vacuum Package					
DFN2510-10L	Packing	Reel 180mm (7")	Inner Box (3 Reels)	Carton (12 Boxes)		
DFN2510-10L	Tape and Reel	3 000pcs	9 000pcs	108 000pcs		

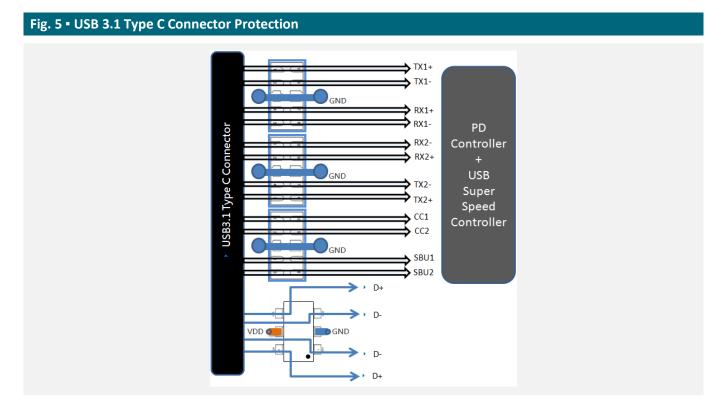


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RECOMMENDED PAD LAYOUT FOR DFN2510-10L All dimensions in mm



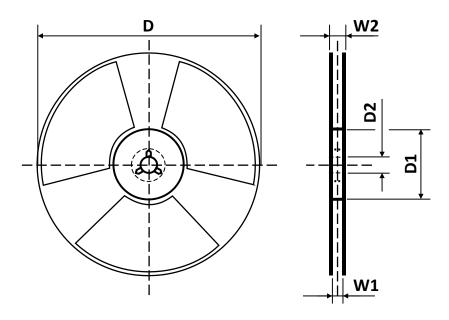
TYPICAL APPLICATION CIRCUIT





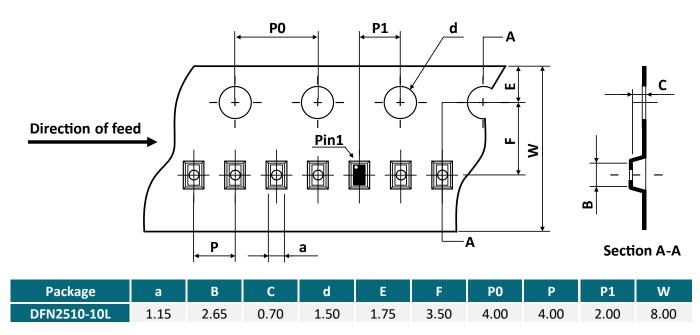
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REEL DIMENSIONS All dimensions in mm



Tape Size	Reel Size	D	D1	D2	W1	W2
8mm	7 inch	Ø178.00	54.40	13.00	9.50	12.30

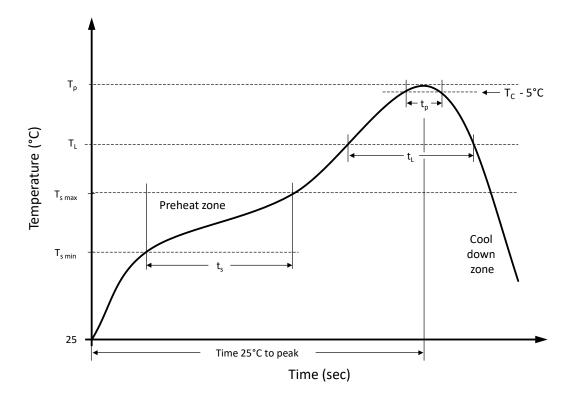
TAPE DIMENSIONS All dimensions in mm



Note: All dimensions meet EIA-481-D requirements.



RECOMMENDED REFLOW SOLDERING PROFILE



Recommended reflow soldering conditions ▲ **Refer to JEDEC J-STD-020E**

Profile Features		Sn-Pb Eutetic Assembly	Pb-Free Assembly
Preheat temperature min.	T_{smin}	100 °C	150 °C
Preheat temperature max.	$T_{s max}$	150 °C	200 °C
Preheat time t_s from $T_{s min}$ to $T_{s max}$	ts	120 seconds	120 seconds
Ramp-up rate (T _L to T _p)		max. 3 °C/second	max. 3 °C/second
Liquidous temperature	ΤL	183 °C	217 °C
Time t_L maintained above T_L	t∟	150 seconds max.	150 seconds max.
Peak package body temperature	Tp	235°C	260°C
Timeframe of within 5°C below and up to max actual peak body temperature	tp	20 seconds max.	30 seconds max.
Ramp-down rate (T_L to T_p)		max. 6 °C/second	max. 6 °C/second
Time 25°C to peak temperature		max. 6 minutes	max. 8 minutes



REVISION TABLE

Revision	Date	Status	Notes
001	01/10/2021	Initial release	Initial publication

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