# KSZ8721BL/SL

## 3.3V Single Power Supply 10/100 Base-TX/FX MII Physical Layer Transceiver

### Features

- Single Chip 100BASE-TX/100BASE-FX/ 10BASE-T Physical Layer Solution
- 2.5V CMOS Design; 2.5/3.3V Tolerance on I/O
- 3.3V Single Power Supply with Built-In Voltage Regulator; Power Consumption <340 mW (Including Output Driver Current)
- Fully Compliant to IEEE 802.3u Standard
- Supports MII and Reduced MII (RMII)
- Supports 10BASE-T, 100BASE-TX, and 100BASE-FX with Far-End Fault Detection
- Supports Power Down and Power Saving Modes
- Configurable Through MII Serial Management Ports or via External Control Pin
- Supports Auto-Negotiation and Manual Selection for 10/100 Mbps Speed and Full-Duplex/Half-Duplex Modes
- On-Chip, Built-In, Analog Front-End Filtering for Both 100BASE-TX and 10BASE-T
- LED Outputs for Link, Activity, Full-Duplex/Half-Duplex, Collision, and Speed
- Supports Back-to-Back, FX to TX for Media Converter Applications
- Supports MDI/MDI-X Auto-Crossover
- KSZ8721BL is a Drop-In Replacement for the KSZ8721BT in the Same Footprint
- KSZ8721SL is a Drop-In Replacement for the KSZ8721B in the Same Footprint
- Commercial Temperature Range: 0°C to +70°C
- Industrial Temperature Range: –40°C to +85°C
- Available in 48-pin SSOP and LQFP Packages

## TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

### Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

**http://www.microchip.com**

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

### Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include -literature number) you are using.

### Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

## Table of Contents

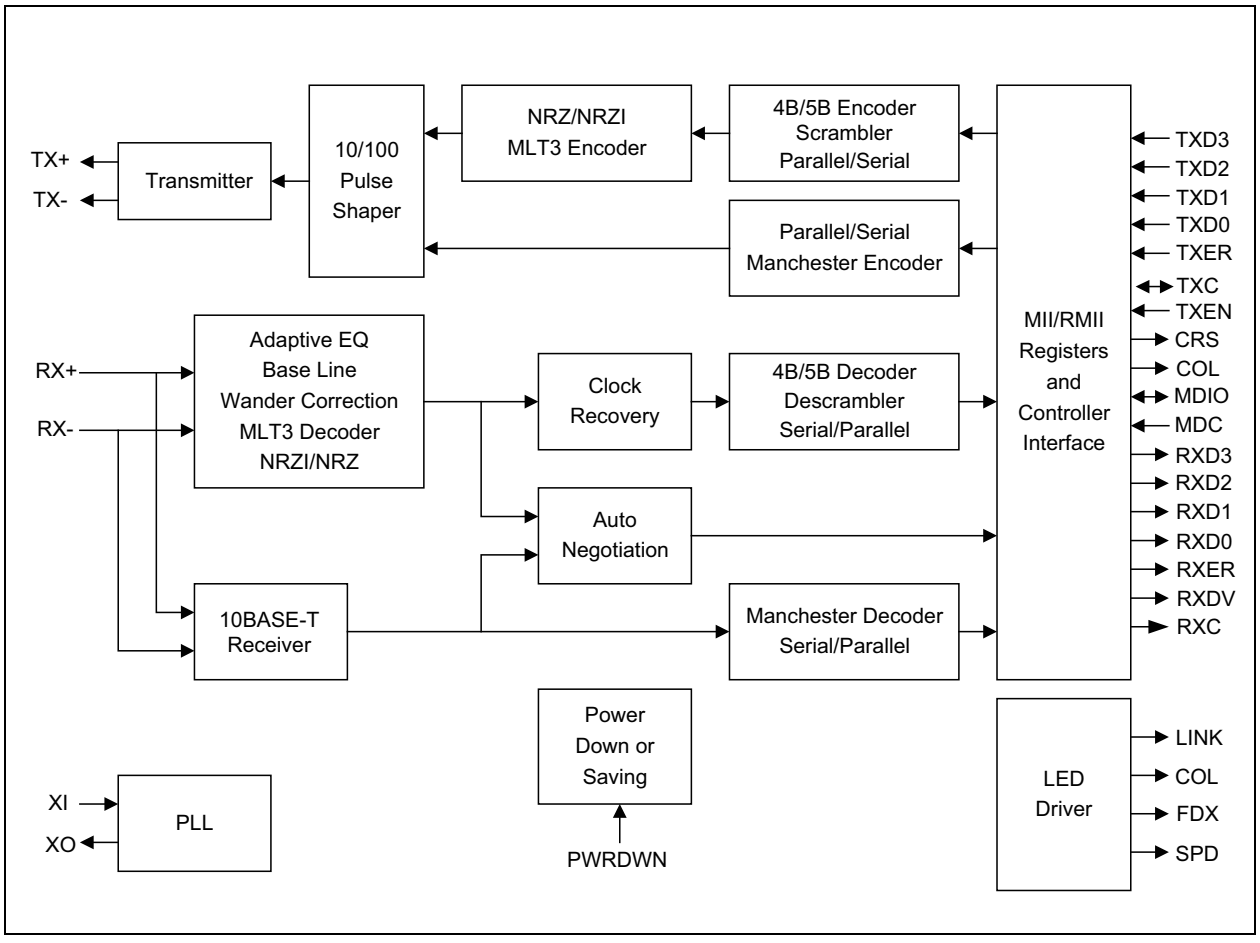
# 1.0 INTRODUCTION

## 1.1 General Description

Operating with a 2.5V core to meet low-voltage and low-power requirements, the KSZ8721BL and KSZ8721SL are 10BASE-T/100BASE-TX/FX Physical Layer Transceivers that use MII and RMII interfaces to transmit and receive data. They contain 10BASE-T Physical Medium Attachment (PMA), Physical Medium Dependent (PMD), and Physical Coding Sub-layer (PCS) functions. The KSZ8721BL/SL also have on-chip 10BASE-T output filtering. This eliminates the need for external filters and allows a single set of line magnetics to be used to meet requirements for both 100BASE-TX and 10BASE-T.

The KSZ8721BL/SL automatically configure themselves for 100 or 10Mbps and full-duplex or half-duplex operation, using an on-chip auto-negotiation algorithm. They are the ideal physical layer transceiver for 100BASE-TX/10BASE-T applications.

**FIGURE 1-1: KSZ8721BL/SL FUNCTIONAL DIAGRAM**



## 2.0 PIN DESCRIPTION AND CONFIGURATION

**FIGURE 2-1: 48-PIN SSOP (SM) AND 48-PIN LQFP (LQ) (TOP VIEW)**

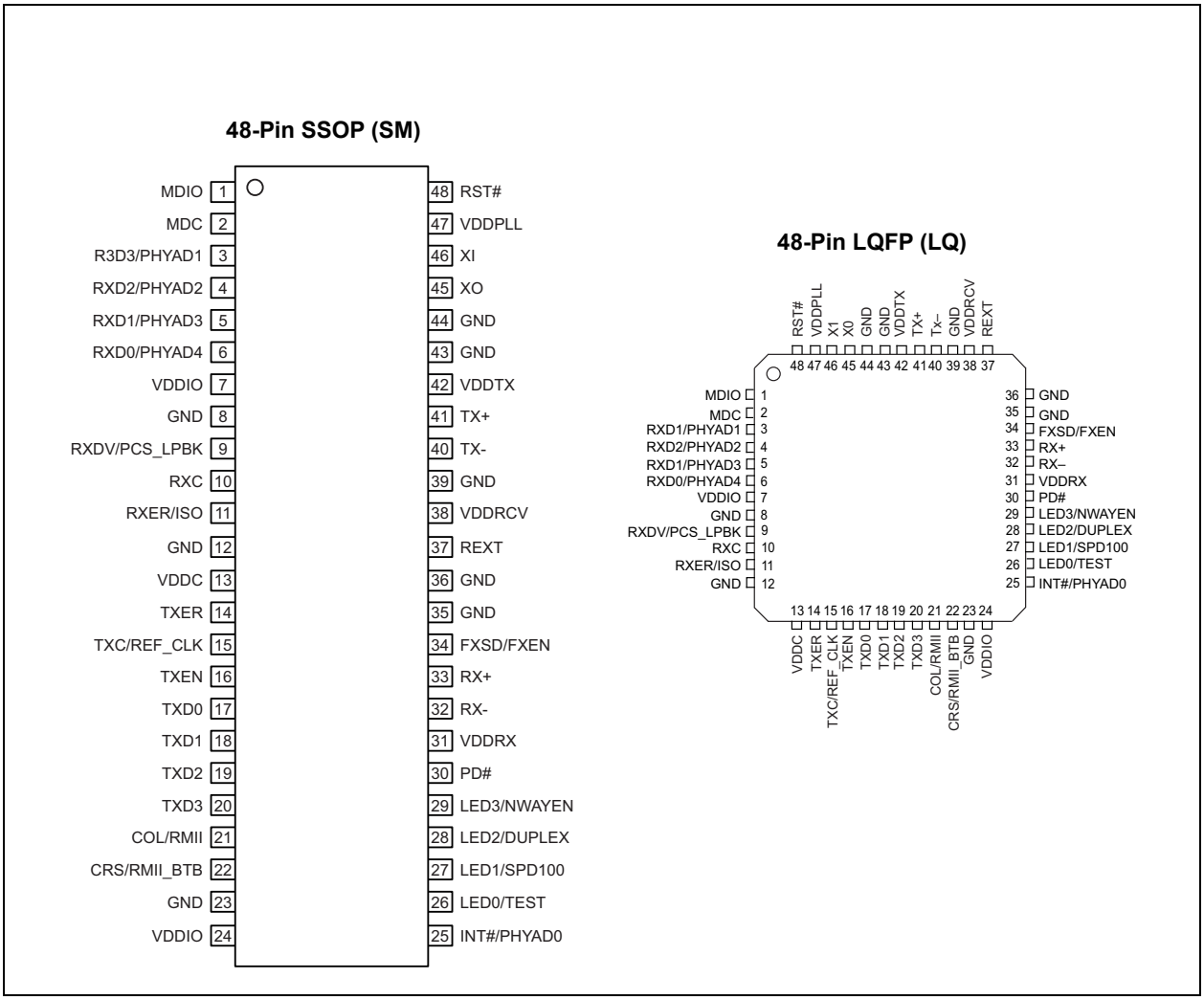


**TABLE 2-1: PIN DESCRIPTION**

| Pin Number | Pin Name | Type (Note 2-1) | Description |
|---|---|---|---|
| 1 | MDIO | I/O | Management Independent Interface (MII) Data I/O. This pin requires an external 4.7 kΩ pull-up resistor. |
| 2 | MDC | I | MII Clock Input. This pin is synchronous to the MDIO. |
| 3 | RXD3/PHYAD | IPD/O | MII Receive Data Output. RXD [3..0], these bits are synchronous with RXCLK. When RXDV is asserted, RXD [3..0] presents valid data to MAC through the MII. RXD [3..0] is invalid when RXDV is de-asserted.<br>During reset, the pull-up/pull-down value is latched as PHYADDR [1]. See Table 2-2 for details. |
| 4 | RXD2/PHYAD2 | IPD/O | MII Receive Data Output.<br>During reset, the pull-up/pull-down value is latched as PHY-ADDR[2]. See Table 2-2 for details. |
| 5 | RXD1/PHYAD1 | IPD/O | MII Receive Data Output.<br>During reset, the pull-up/pull-down value is latched as PHY-ADDR[3]. See Table 2-2 for details. |
| 6 | RXD0/PHYAD4 | IPD/O | MII Receive Data Output.<br>During reset, the pull-up/pull-down value is latched as PHY-ADDR[4]. See Table 2-2 for details. |
| 7 | VDDIO | P | Digital IO 2.5 /3.3V tolerant power supply. 3.3V power Input of voltage regulator. See **Section 3.23 "Circuit Design Reference for Power Supply"** for details. |
| 8 | GND | GND | Ground. |
| 9 | RXDV/CRSDV/ PCS_LPBK | IPD/O | MII Receive Data Valid Output.<br>During reset, the pull-up/pull-down value is latched as PCS_LPBK. See Table 2-2 for details. |
| 10 | RXC | O | MII Receive Clock Output. Operating at 25 MHz = 100 Mbps, 2.5 MHz = 10 Mbps. |
| 11 | RXER/ISO | IPD/O | MII Receive Error Output.<br>During reset, the pull-up/pull-down value is latched as ISOLATE during reset. See Table 2-2 for details. |
| 12 | GND | GND | Ground. |
| 13 | VDDC | P | Digital core 2.5V only power supply. See **Section 3.23 "Circuit Design Reference for Power Supply"** for details. |
| 14 | TXER | IPD | MII Transmit Error Input. |
| 15 | TXC/REFCLK | I/O | MII Transmit Clock Output.<br>Input for crystal or an external 50 MHz clock. When REFCLK pin is used for REF clock interface, pull up XI to VDDPLL 2.5V via 10 kΩ resistor and leave XO pin unconnected. |
| 16 | TXEN | IPD | MII Transmit Enable Input. |
| 17 | TXD0 | IPD | MII Transmit Data Input. |
| 18 | TXD1 | IPD | MII Transmit Data Input. |

**TABLE 2-1: PIN DESCRIPTION (CONTINUED)**

| Pin Number | Pin Name | Type (Note 2-1) | Description |
|---|---|---|---|
| 19 | TXD2 | IPD | MII Transmit Data Input. |
| 20 | TXD3 | IPD | MII Transmit Data Input. |
| 21 | COL/RMII | IPD/O | MII Collision Detect Output.<br>During reset, the pull-up/pull-down value is latched as RMII select. See Table 2-2 for details. |
| 22 | CRS/RMII_BTB | IPD/O | MII Carrier Sense Output.<br>During reset, the pull-up/pull-down value is latched as RMII back-to-back mode when RMII mode is selected. See Table 2-2 for details. |
| 23 | GND | GND | Ground. |
| 24 | VDDIO | P | Digital IO 2.5/3.3V tolerant power supply. 3.3V power input of voltage regulator. See Section 3.23, Circuit Design Reference for Power Supply for details. |
| 25 | INT#/PHYAD0 | IPU/O | Management Interface (MII) Interrupt Out. Interrupt level set by Register 1f, bit 9. During reset, latched as PHYAD[0]. See Table 2-2 for details. |
| 26 | LED0/TEST | IPU/O | Link/Activity LED Output. The external pull-down enable test mode and only used for the factory test. Active low.<br>**Link/Act** / **Pin State** / **LED Definition PHYAD0**<br>No Link / H / Off<br>Link / L / On<br>Act / — / Toggle |
| 27 | LED1/SPD100/ nFEF | IPU/O | Speed LED Output. Latched as SPEED (Register 0, bit 13) during power-up/ reset. See Table 2-2 for details. Active low.<br>**Speed** / **Pin State** / **LED Definition**<br>10BT / H / Off<br>100BT / L / On |
| 28 | LED2 | IPU/O | Full-duplex LED Output. Latched as DUPLEX (register 0h, bit 8) during power-up/ reset. See “Table 2-2 for details. Active low.<br>**Duplex** / **Pin State** / **LED Definition**<br>Half / H / Off<br>Full / L / On |
| 29 | LED3/NWAYEN | IPU/O | Collision LED Output. Latched as ANEG_EN (register 0h, bit 12) during power-up/ reset. See Table 2-2 for details.<br>**Collision** / **Pin State** / **LED Definition**<br>No Collision / H / Off<br>Collision / L / On |

**TABLE 2-1: PIN DESCRIPTION (CONTINUED)**

| Pin Number | Pin Name | Type (Note 2-1) | Description |
|---|---|---|---|
| 30 | PD# | IPU | Power Down. 1 = Normal operation, 0 = Power-down. Active low. |
| 31 | VDDRX | P | Analog 2.5V power supply. See **Section 3.23 "Circuit Design Reference for Power Supply"** section for details. |
| 32 | RX– | I | Receive Input. Differential receive input pins for 100FX, 100BASE-TX, or 10BASE-T. |
| 33 | RX+ | I | Receive Input: Differential receive input pin for 100FX, 100BASE-TX, or 10BASE-T. |
| 34 | FXSD/ FXEN | IPD/O | Fiber Mode Enable/Signal Detect in Fiber Mode. If FXEN = 0, FX mode is disable. The default is "0". See **Section 3.21 "100BT FX Mode"** for more details. |
| 35 | GND | GND | Ground. |
| 36 | GND | GND | Ground. |
| 37 | REXT | I | External resistor (6.49 kW) connects to REXT and GND. |
| 38 | VDDRCV | P | Analog 2.5V power supply. 2.5V power output of voltage regulator. See **Section 3.23 "Circuit Design Reference for Power Supply"** for details. |
| 39 | GND | GND | Ground. |
| 40 | TX– | O | Transmit Outputs: Differential transmit output for 100FX, 100BASE-TX, or 10BASE-T. |
| 41 | TX+ | O | Transmit Outputs: Differential transmit output for 100FX, 100BASE-TX, or 10BASE-T. |
| 42 | VDDTX | P | Transmitter 2.5V power supply. See **Section 3.23 "Circuit Design Reference for Power Supply"** for details. |
| 43 | GND | GND | Ground. |
| 44 | GND | GND | Ground. |
| 45 | XO | O | XTAL feedback: Used with XI for Xtal application. |
| 46 | XI | I | Crystal Oscillator Input: Input for a crystal or an external 25 MHz clock. If an oscillator is used, XI connects to a 3.3V tolerant oscillator, and X2 is a no-connect. |
| 47 | VDDPLL | P | Analog PLL 2.5V power supply. See **Section 3.23 "Circuit Design Reference for Power Supply"** for details. |
| 48 | RST# | IPU | Chip Reset. Active low, minimum of 50 µs pulse is required. |

**Note 2-1** P = Power supply;
GND = Ground;
I = Input; O = Output; I/O = Bi-directional;
IPU/O = Input with internal pull-up during power-up/reset; output pin otherwise.
IPU = Input with internal pull-up.
IPD = Input with internal pull-down.
IPD/O = Input with internal pull-down during reset; output pin otherwise.
IPU/O = Input with internal pull-up during reset; output pin otherwise.

**Note 2-2** **Speed**: Low (100BASE-TX), High (10BASE-T)
**Full-Duplex**: Low (full-duplex), High (half-duplex)
**Act**: Toggle (transmit / receive activity)
**Link**: Low (link), High (no link)

**TABLE 2-2: STRAPPING OPTIONS (Note 2-1)**

| Pin Number | Pin Name | Type (Note 2-2) | Pin Function |
|---|---|---|---|
| 6, 5, 4, 3 | PHYAD[4:1]/ RXD[0:3] | IPD/O | PHY Address latched at power-up/reset. The default PHY address is 00001. |
| 25 | PHYAD0/ INT# | IPU/O | Enables PCS_LPBK mode at power-up/reset. PD (default) = Disable, PU = Enable. |
| 9 (Note 2-3) | PCS_LPBK/ RXDV | IPD/O | Enables ISOLATE mode at power-up/reset. PD (default) = Disable, PU = Enable. |
| 11 (Note 2-3) | ISO/RXER | IPD/O | Enables RMII mode at power-up/reset. PD (default) = Disable, PU = Enable. |
| 21 (Note 2-3) | RMII/COL | IPD/O | Enable RMII back-to-back mode at power-up/reset. PD (default) = Disable, PU = Enable. |
| 22 (Note 2-3) | RMII_BTB CRS | IPD/O | Enable RMII back-to-back mode at power-up/reset. PD (default) = Disable, PU = Enable. |
| 27 | SPD100/ No FEF/ | IPU/O | Latched into Register 0h bit 13 during power-up/reset. PD = 10Mbps, PU (default) = 100Mbps. If SPD100 is asserted during power-up/reset, this pin is also latched as LED1 the Speed Support in register 4h. (If FXEN is pulled up, the latched value 0 means no Far_End _Fault.) |
| 28 | DUPLEX/ LED2 | IPU/O | Latched into Register 0h bit 8 during power-up/reset. PD = Half-duplex, PU (default) = Full-duplex. If Duplex is pulled up during reset, this pin is also latched as the Duplex support in register 4h. |
| 29 | NWAYEN/ LED3 | IPU/O | Nway (auto-negotiation) Enable. Latched into Register 0h bit 12 during power-up/reset. PD = Disable Auto-Negotiation, PU (default) = Enable Auto-Negotiation. |
| 30 | PD# | IPU | Power-Down Enable. PU (default) = Normal operation, PD = Power-Down mode. |

**Note 2-1** Strap-in is latched during power-up or reset.

**Note 2-2** IPU = Input with internal pull-up.
IPD/O = Input with internal pull-down during reset; output pin otherwise.
IPU/O = Input with internal pull-up during reset; output pin otherwise.
See “Reference Circuit” section for pull-up/pull-down and float information.

**Note 2-3** Some devices may drive MII pins that are designated as output (PHY) on power-up, resulting in incorrect strapping values latched at reset. It is recommended that an external pull-down via 1 kΩ resistor be used in these applications to augment the KSZ8721’s internal pull-down

# 3.0 FUNCTIONAL DESCRIPTION

## 3.1 100BASE-TX transmit

The 100BASE-TX transmit function performs parallel to serial conversion, NRZ-to-NRZI conversion, and MLT-3 encoding and transmission. The circuitry starts with a parallel to serial conversion that converts the 25 MHz, 4-bit nibbles into a 125 MHz serial bit stream. The incoming data is clocked in at the positive edge of the TXC signal. The serialized data is further converted from NRZ to NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 6.49 kΩ resistor for the 1:1 transformer ratio. Its typical rise/fall time of 4 ns complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output driver is also incorporated into the 100BASE-TX driver.

## 3.2 100BASE-TX Receive

The 100BASE-TX receive function performs adaptive equalization, DC restoration, MLT-3 to NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, and serial-to-parallel conversion. The receiving side starts with the equalization filter to compensate inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion are a function of the length of the cable, the equalizer has to adjust its characteristic to optimize performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and can self-adjust for environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effects of base line wander and improve dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. Finally, the NRZ serial data is converted to 4-bit parallel 4B nibbles. A synchronized 25 MHz RXC is generated so that the 4B nibbles are clocked out at the negative edge of RCK25 and is valid for the receiver at the positive edge. When no valid data is present, the clock recovery circuit is locked to the 25 MHz reference clock and both TXC and RXC clocks continue to run.

## 3.3 PLL Clock Synthesizer

The KSZ8721BL/SL generates 125 MHz, 25 MHz, and 20 MHz clocks for system timing. An internal crystal oscillator circuit provides the reference clock for the synthesizer.

## 3.4 Scrambler/De-scrambler (100BASE-TX Only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce electromagnetic interference (EMI) and baseline wander.

## 3.5 10BASE-T Transmit

When TXEN (transmit enable) goes high, data encoding and transmission begins. The KSZ8721BL/SL continues to encode and transmit data as long as TXEN remains high. The data transmission ends when TXEN goes low. The last transition occurs at the boundary of the bit cell if the last bit is zero, or at the center of the bit cell if the last bit is one. The output driver is incorporated into the 100BASE-T driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with typical 2.5V amplitude. The harmonic contents are at least 27dB below the fundamental when driven by all-ones, Manchester-encoded signal.

## 3.6 10BASE-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 300 mV or with short pulse widths in order to prevent noise at the RX+ or RX– input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8721BL/SL decodes a data frame. This activates the carrier sense (CRS) and RXDV signals and makes the receive data (RXD) available. The receive clock is maintained active during idle periods in between data reception.

## 3.7 SQE and Jabber Function (10BASE-T Only)

In 10BASE-T operation, a short pulse is put out on the COL pin after each packet is transmitted. This is required as a test of the 10BASE-T transmit/receive path and is called an SQE test. The 10BASE-T transmitter is disabled and COL goes high if TXEN is high for more than 20 ms (jabbering). If TXEN then goes low for more than 250 ms, the 10BASE-T transmitter is re-enabled and COL goes low.

## 3.8 Auto-Negotiation

The KSZ8721BL/SL performs auto-negotiation by hardware strapping option (pin 29) or software (Register 0.12). It automatically chooses its mode of operation by advertising its abilities and comparing them with those received from its link partner whenever auto-negotiation is enabled. It can also be configured to advertise 100BASE-TX or 10BASE-T in either full-duplex or half-duplex mode (please refer to ). Auto-negotiation is disabled in the FX mode.

During auto-negotiation, the contents of Register 4, coded in fast link pulse (FLP), are sent to its link partner under the conditions of power-on, link-loss, or restart. At the same time, the KSZ8721BL/SL monitors incoming data to determine its mode of operation. The parallel detection circuit is enabled as soon as either 10BASE-T normal link pulse (NLP) or 100BASE-TX idle is detected. The operation mode is configured based on the following priority:

- Priority 1: 100BASE-TX, full-duplex
- Priority 2: 100BASE-TX, full-duplex
- Priority 3: 100BASE-TX, full-duplex
- Priority 4: 10BASE-T, half-duplex

When the KSZ8721BL/SL receives a burst of FLP from its link partner with three identical link code words (ignoring acknowledge bit), it will store these code words in Register 5 and wait for the next three identical code words. Once the KSZ8721BL/SL detects the second code words, it then configures itself according to the above-mentioned priority. In addition, the KSZ8721BL/SL also checks for 100BASE-TX idle or 10BASE-T NLP symbols. If either is detected, the KSZ8721BL/SL automatically configures to match the detected operating speed.

- A physical connection including a data line (MDIO), a clock line (MDC), and an optional interrupt line (INTRPT).
- A specific protocol that runs across the above mentioned physical connection that allows one controller to communicate with multiple KSZ8721BL/SL devices. Each KSZ8721BL/SL is assigned an MII address between 0 and 31 by the PHYAD inputs.
- An internal addressable set of fourteen 16-bit MDIO registers. Registers [0:6] are required and their functions are specified by the IEEE 802.3 specifications. Additional registers are provided for expanded functionality.

The INTPRT pin functions as a management data interrupt in the MII. An active low or high in this pin indicates a status change on the KSZ8721BL/SL based on 1fh.9 level control. Register bits at 1bh[15:8] are the interrupt enable bits. Register bits at 1bh[7:0] are the interrupt condition bits. This interrupt is cleared by reading Register 1bh.

## 3.9 MII Data Interface

The data interface consists of separate channels for transmitting data from a 10/100 802.3-compliant Media Access Controller (MAC) to the KSZ8721BL/SL, and for receiving data from the line. Normal data transmission is implemented in 4B nibble mode (4-bit wide nibbles).

### 3.9.1 TRANSMIT CLOCK (TXC)

The transmit clock is normally generated by the KSZ8721BL/SL from an external 25 MHz reference source at the X1 input. The transmit data and control signals must always be synchronized to the TXC by the MAC. The KSZ8721BL/SL normally samples these signals on the rising edge of the TXC.

### 3.9.2 RECEIVE CLOCK (RXC)

For 100BASE-TX links, the receive clock is continuously recovered from the line. If the link goes down, and auto-negotiation is disabled, the receive clock operates off the master input clock (X1 or TXC). For 10BASE-T links, the receive clock is recovered from the line while carrier is active, and operates from the master input clock when the line is idle. The KSZ8721BL/SL synchronizes the receive data and control signals on the falling edge of RXC in order to stabilize the signals at the rising edge of the clock with 10 ns setup and hold times.

### 3.9.3 TRANSMIT ENABLE

The MAC must assert TXEN at the same time as the first nibble of the preamble, and deassert TXEN after the last bit of the packet.

### 3.9.4 RECEIVE DATA VALID

The KSZ8721BL/SL asserts RXDV when it receives a valid packet. Line operating speed and MII mode will determine timing changes in the following way:

- For 100BASE-TX links with the MII in 4B mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the data packet.
- For 10BASE-T links, the entire preamble is truncated. RXDV is asserted with the first nibble of the SFD “5D” and remains asserted until the end of the packet.

### 3.9.5 ERROR SIGNALS

Whenever the KSZ8721BL/SL receives an error symbol from the network, it asserts RXER and drives “1110” (4B) on the RXD pins. When the MAC asserts TXER, the KSZ8721BL/SL will drive “H” symbols (a Transmit Error defined in the IEEE 802.3 4B/5B code group) out on the line to force signaling errors.

### 3.9.6 CARRIER SENSE (CRS)

For 100BASE-TX links, a start-of-stream delimiter, or /J/K symbol pair causes assertion of Carrier Sense (CRS). An end-of-stream delimiter, or /T/R symbol pair, causes deassertion of CRS. The PMA layer will also de-assert CRS if IDLE symbols are received without /T/R, yet in this case RXER will be asserted for one clock cycle when CRS is deasserted. For 10BASE-T links, CRS assertion is based on reception of valid preamble, and deassertion on reception of an end-of-frame (EOF) marker.

### 3.9.7 COLLISION

Whenever the line state is half-duplex and the transmitter and receiver are active at the same time, the KSZ8721BL/SL asserts its collision signal, which is asynchronous to any clock.

## 3.10 RMII (Reduced MII) Data Interface

RMII interface specifies a low pin count, Reduced Media Independent Interface (RMII) intended for use between Ethernet PHYs and Switch or Repeater ASICs. It is fully compliant with IEEE 802.3u [2].

This interface has the following characteristics:

- It is capable of supporting 10 Mbps and 100 Mbps data rates.
- A single clock reference is sourced from the MAC to PHY (or from an external source).
- It provides independent 2-bit wide (di-bit) transmit and receive data paths.
- It uses TTL signal levels compatible with common digital CMOS ASIC processes.

**TABLE 3-1: RMII SIGNAL DEFINITION**

| Signal Name | Direction (w/respect to the PHY) | Direction (w/respect to the MAC) | Use |
|---|---|---|---|
| REF_CLK | Input | Input or Output | Synchronous clock reference for receive, transmit and control interface |
| CRS_DV | Output | Input | Carrier Sense/Receive Data Valid |
| RXD[1:0] | Output | Input | Receive Data |
| TX_EN | Input | Output | Transmit Enable |
| TXD[1:0] | Input | Output | Transmit Data |
| RX_ER | Output | Input | Receive Error |

## 3.11 Reference Clock (REF_CLK)

REF_CLK is a continuous 50 MHz clock that provides the timing reference for CRS_DV, RXD[1:0], TX_EN, TXD[1:0], and RX_E. REF_CLK is sourced by the MAC or an external source. Switch implementations may choose to provide REF_CLK as an input or an output depending on whether they provide a REF_CLK output or rely on an external clock distribution device. Each PHY device must have an input corresponding to this clock but may use a single clock input for multiple PHYs implemented on a single IC.

## 3.12 Carrier Sense/Receive Data Valid (CRS_DV)

CRS_DV is asserted asynchronously on detection of carrier due to the criteria relevant to the operating mode. That is, in 10BASE-T mode, when squelch is passed or in 100BASE-X mode when two noncontiguous zeroes in 10 bits are detected, the carrier is detected.

Loss-of-carrier results in the deassertion of CRS_DV synchronous to REF_CLK. As carrier criteria are met, CRS_DV remains continuously asserted from the first recovered di-bit of the frame through the final recovered di-bit and is negated prior to the first REF_CLK that follows the final di-bit.

The data on RXD[1:0] is considered valid once CRS_DV is asserted. However, because the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] remains as “00” until proper receive signal decoding takes place (see Section 3.13, Receive Data [1:0] (RXD[1:0])).

## 3.13 Receive Data [1:0] (RXD[1:0])

RXD[1:0] transitions synchronously to REF_CLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY. In some cases (e.g., before data recovery or during error conditions), a predetermined value for RXD[1:0] is transferred instead of recovered data. RXD[1:0] remains as “00” to indicate idle when CRS_DV is deasserted. Values of RXD[1:0] other than “00” when CRS_DV is deasserted are reserved for out-of-band signaling (to be defined). Values other than “00” on RXD[1:0] while CRS_DV is deasserted are ignored by the MAC/repeater. Upon assertion of CRS_DV, the PHY ensures that RXD[1:0]=00 until proper receive decoding takes place.

## 3.14 Transmit Enable (TX_EN)

Transmit Enable TX_EN indicates that the MAC is presenting di-bits on TXD[1:0] on the RMII for transmission. TX_EN is asserted synchronously with the first nibble of the preamble and remains asserted while all transmitted di-bits are presented to the RMII. TX_EN is negated prior to the first REF_CLK following the final di-bit of a frame. TX_EN transitions synchronously with respect to REF_CLK.

## 3.15 Transmit Data [1:0] (TXD[1:0])

Transmit Data TXD[1:0] transitions synchronously with respect to REF_CLK. When TX_EN is asserted, TXD[1:0] are accepted for transmission by the PHY. TXD[1:0] remains as “00” to indicate idle when TX_EN is deasserted. Values of TXD[1:0] other than “00” when TX_EN is deasserted are reserved for out-of-band signaling (to be defined). Values other than “00” on TXD[1:0] while TX_EN is deasserted are ignored by the PHY.

## 3.16 Collision Detection

Because the definition of CRS_DV and TX_EN both contain an accurate indication of the start of frame, the MAC reliably regenerates the COL signal of the MII by ANDing TX_EN and CRS_DV.

During the IPG time following the successful transmission of a frame, the COL signal is asserted by some transceivers as a self-test. The Signal Quality Error (SQE) function is not supported by the reduced MII due to the lack of the COL signal. Historically, SQE was present to indicate that a transceiver located physically remote from the MAC was functioning. Because the reduced MII only supports chip-to-chip connections on a PCB, SQE functionality is not required.

## 3.17 RX_ER

The PHY provides RX_ER as an output according to the rules specified in IEEE 802.3u [2] (see Clause 24, Figure 24-11– Receive State Diagram). RX_ER is asserted for one or more REF_CLK periods to indicate that an error (e.g., a coding error or any error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sublayer) is detected somewhere in the frame presently being transferred from the PHY. RX_ER transitions synchronously with respect to REF_CLK. While CRS_DV is deasserted, RX_ER has no effect on the MAC.

**TABLE 3-2: RMII AC CHARACTERISTICS**

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| — | REF_CLK Frequency | — | 50 | — | MHz |
| — | REF_CLK Duty Cycle | 35 | — | 65 | % |

**TABLE 3-2: RMII AC CHARACTERISTICS**

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{SU}$ | TXD[1:0], TX_EN, RXD[1:0], CRS_DV, RXER | 4 | — | — | ns |
| $t_H$ | TXD[1:0], TX_EN, RXD[1:0], CRS_DV, RXER Data Hold from REF_CLKRising Edge | 2 | — | — | ns |

## 3.18 Unused RMII Pins

Input Pins TXD[2:3] and TXER are pull-down to GND

Output Pins RXD[2:3] and RXC are no connect.

Note that the RMII pin needs to be pulled up to enable RMII mode.

## 3.19 Auto-Crossover (Auto-MDI/MDI-X)

Automatic MDI/MDI-X configuration is intended to eliminate the need for crossover cables between similar devices. The assignment of pinouts for a 10/100 BASE-T crossover function cable is shown below.

This feature eliminates the confusion in applications by allowing the use of both straight and crossover cables. This feature is controlled by register 1f:13. See Table 4-13 for details.

**FIGURE 3-1: STRAIGHT THROUGH CABLE**

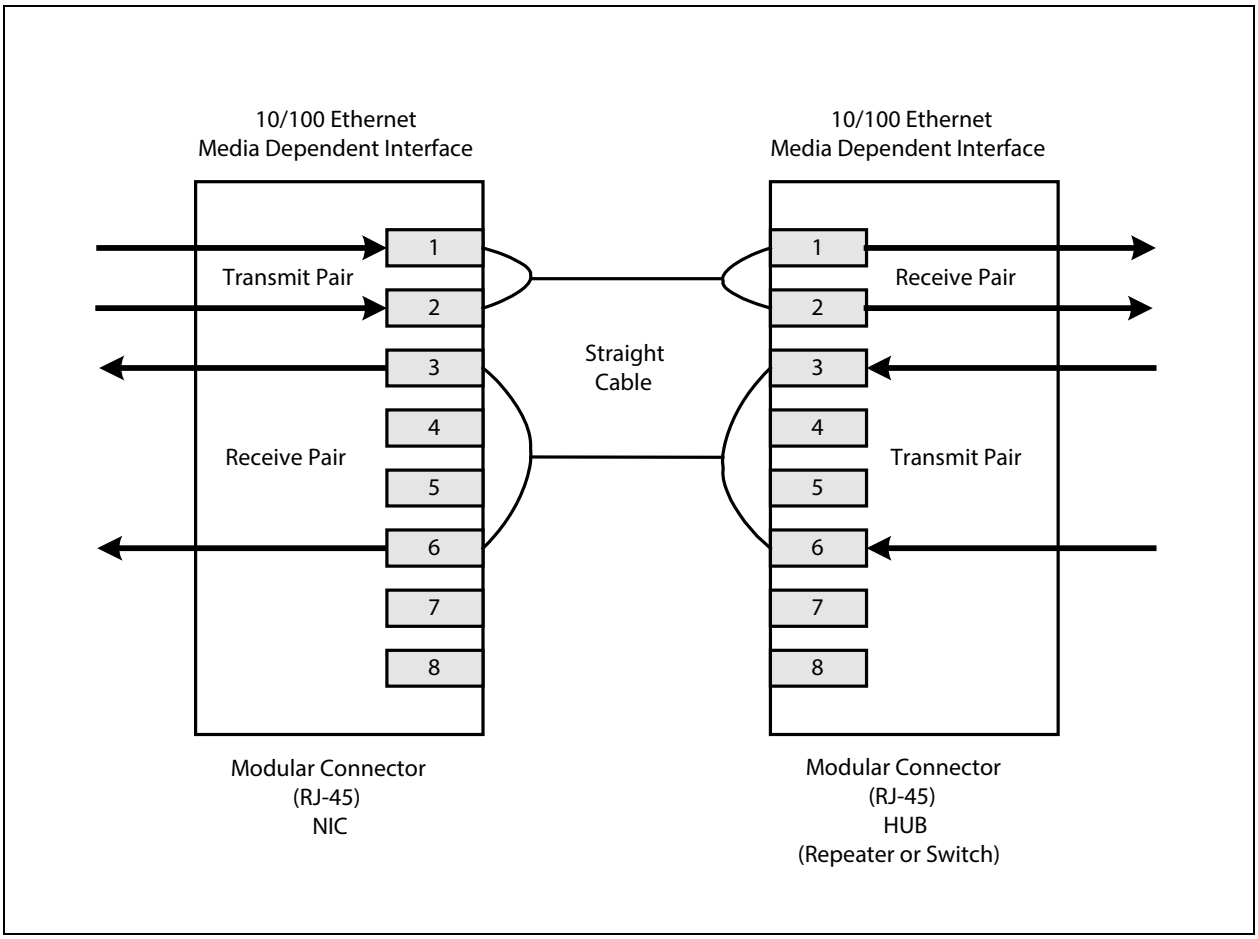
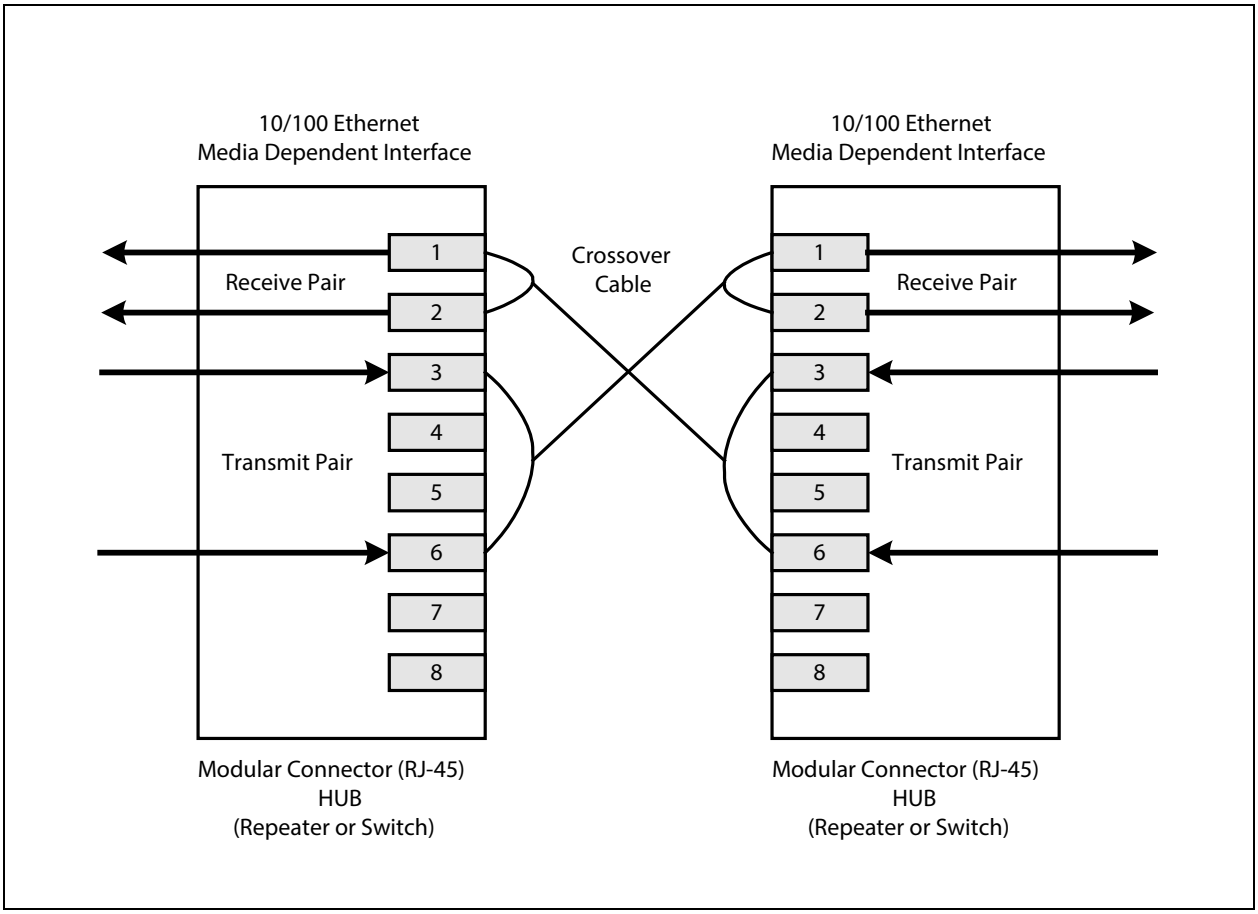


**FIGURE 3-2: CROSSOVER CABLE**




## 3.20 Power Management

The KSZ8721BL/SL offers the following modes for power management:

- Power-Down Mode: This mode can be achieved by writing to Register 0.11 or pulling pin 30 PD# low.
- Power-Saving Mode: This mode can be disabled by writing to Register 1fh.10. The KSZ8721BL/SL turns off everything except for the Energy Detect and PLL circuits when the cable is not installed. In other words, the KSZ8721BL/SL shuts down most of the internal circuits to save power if there is no link. Power-saving mode is in the most effective state when auto-negotiation mode is enabled.

## 3.21 100BT FX Mode

Please contact your local field application engineer (FAE) for a reference schematic on fiber connection.

100BT FX mode is activated when FXSD/FXEN is higher than 0.6V (this pin has a default pull down). Under this mode, the auto-negotiation and auto-MDI-X features are disabled.

In fiber operation, the FXSD pin should connect to the signal detect (SD) output of the fiber module. The internal threshold of FXSD is around 1/2 VDD ±50 mV (1.25V ±0.05V). Above this level, the fiber signal is considered detected.

The operation is summarized in Table 3-3:

**TABLE 3-3: 100BT FX MODE**

| FXSD/FXEN | Condition |
|---|---|
| Less than 0.6V | 100TX mode |
| Less than 1.25V,<br>but greater than 0.6V | FX mode<br>No signal detected<br>FEF generated |
| Greater than 1.25 | FX mode<br>Signal detected |

To ensure proper operation, the swing of fiber module SD should cover the threshold variation. A resistive voltage divider is recommended to adjust the SD voltage range.

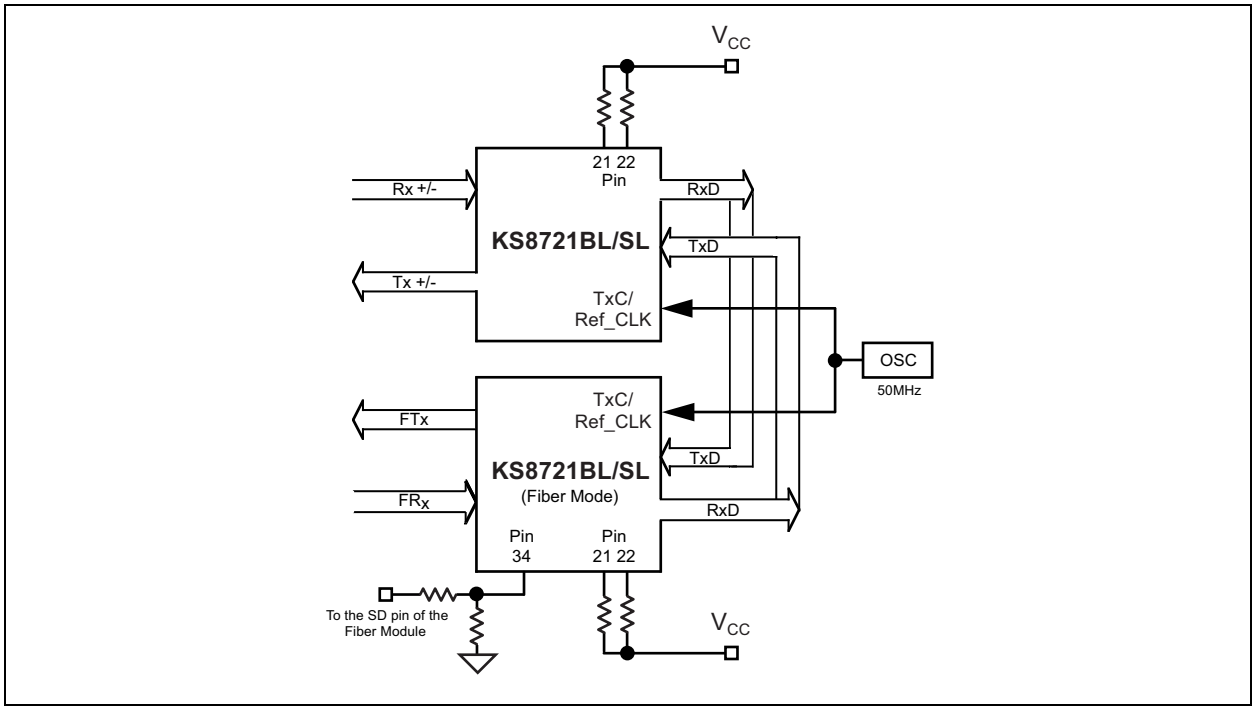
Far End Fault (FEF), repetition of a special pattern which consists of 84-one and 1-zero, is generated under “FX mode with no signal detected.” The purpose of FEF is to notify the sender of a faulty link. When receiving an FEF, the LINK will go down to indicate a fault, even with fiber signal detected. The transmitter is not affected by receiving an FEF and still sends out its normal transmit pattern from MAC. FEF can be disabled by strapping pin 27 low. Refer to Table 2-2.

## 3.22 Media Converter Operation

The KSZ8721BL/SL is capable of performing media conversion with two parts in a back-to-back RMII loop-back mode as indicated in the diagram. Both parts are in RMII mode and with RMII BTB asserted (pins 21 and 22 strapped high). One part is operating in TX mode and the other is operating in FX mode. Both parts can share a common 50 MHz oscillator.

Under this operation, auto-negotiation on the TX side prohibits 10BASE-T link-up. Additional options can be implemented under this operation. Disable the transmitter and set it at tri-state by controlling the high TXD2 pin. In order to do this, RXD2 and TXD2 pins need to be connected via inverter. When TXD2 pin is high in both the copper and fiber operation, it is disabled transmit. Meanwhile, the RXD2 pin on the copper side serves as the energy detect and can indicate if a line signal is detected. TXD3 should be tied low and RXD3 let float.

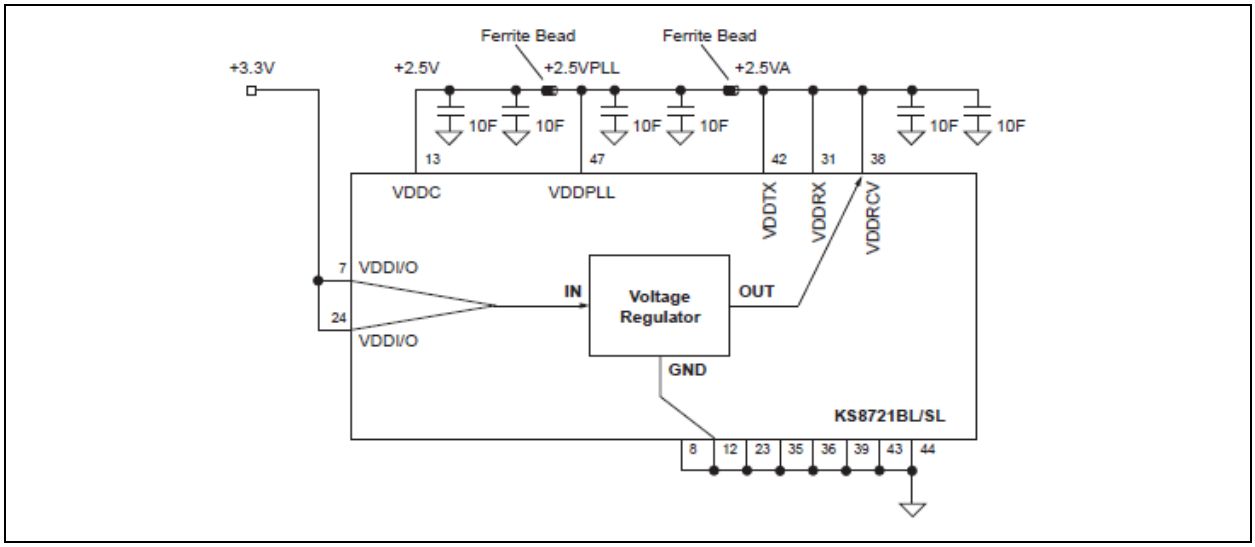
**FIGURE 3-3: FIBER MODULE**



## 3.23 Circuit Design Reference for Power Supply

Microchip's integrated built-in, voltage regulator technology and thoughtful implementation allows the user to save BOM cost on both existing and future designs with the use of the new KSZ8721BL/SL single supply, single port 10/100 Ethernet PHY.

**FIGURE 3-4: CIRCUIT DESIGN**




The circuit design in Figure 7-1 shows the power connections for the power supply: the 3.3V to VDDI/O is the only input power source and the 2.5V at VDDRCV, pin 38, is the output of the voltage regulator that needs to supply through the rest of the 2.5V VDD pins via the 2.5V power plane.

The 2.5V VDD pins make the drop-in replacement with the existing KSZ8721B/BT part. Table 3-4 shows the drop-in replacement from the existing KSZ8721B/BT to the KSZ8721SL/BL. Please contact your local Microchip FAE for Application Note AN-117, "Drop-in Replacement with KSZ8721BT."

**TABLE 3-4: DROP-IN REPLACEMENT**

| 2.5V/3.3V Supply | | 3.3V Supply with Built-in Regulator | |
|---|---|---|---|
| **Part Number** | **Package** | **Part Number** | **Package** |
| KSZ8721B | 48-SSOP | KSZ8721SL | 48-SSOP |
| KSZ8721BT | 48-TQFP | KSZ8721BL | 48-LQFP |
| KSZ8721BI | 48-SSOP | KSZ8721SLI | 48-SSOP |

**Notes:**

## 4.0 REGISTER MAP

**TABLE 4-1: REGISTER DESCRIPTION**

| Register Number | Description |
|---|---|
| 0h | Basic Control Register |
| 1h | Basic Status Register |
| 2h | PHY Identifier I |
| 3h | PHY Identifier II |
| 4h | Auto-Negotiation Advertisement Register |
| 5h | Auto-Negotiation Link Partner Ability Register |
| 6h | Auto-Negotiation Expansion Register |
| 7h | Auto-Negotiation Next Page Register |
| 8h | Link Partner Next Page Ability |
| 15h | RXER Counter Register |
| 1 bh | Interrupt Control/Status Register |
| 1 fh | 100BASE-TX PHY Control Register |

**TABLE 4-2: REGISTER 0H - BASIC CONTROL**

| Bit | Name | Description | Default | Reference |
|---|---|---|---|---|
| 0.15 | Reset | 1 = Software reset. Bit is self-clearing | RW/SC | 0 |
| 0.14 | Loop-Back | 1 = Loop-back mode<br>0 = Normal operation | RW | 0 |
| 0.13 | Speed Select (LSB) | 1 = 100 Mbps<br>0 = 10 Mbps<br>Ignored if Auto-Negotiation is enabled (0.12 = 1) | RW | Set by SPD100 |
| 0.12 | Auto-Negotiation Enable | 1 = Enable auto-negotiation process (override 0.13 and 0.8)<br>0 = Disable auto-negotiation process | RW | Set by NWAYEN |
| 0.11 | Power Down | 1 = Power-down mode<br>0 = Normal operation | RW | 0 |
| 0.10 | Isolate | 1 = Electrical isolation of PHY from MII and TX+/ TX–<br>0 = Normal operation | RW | Set by ISO |
| 0.9 | Restart Auto-Negotiation | 1 = Restart auto-negotiation process<br>0 = Normal operation. Bit is self-clearing | RW/SC | 0 |
| 0.8 | Duplex Mode | 1 = Full-duplex<br>0 = Half-duplex | RW | Set by DUPLEX |
| 0.7 | Collision Test | 1 = Enable COL test<br>0 = Disable COL test | RW | 0 |
| 0.6:1 | Reserved | — | RO | 0 |
| 0.0 | Disable Transmitter | 0 = Enable transmitter<br>1 = Disable transmitter | RW | 0 |

**TABLE 4-3: REGISTER 1H - BASIC STATUS**

| Bit | Name | Description | Default | Reference |
|---|---|---|---|---|
| 1.15 | 100BASE-T4 | 1 = T4 capable<br>0 = Not T4 capable | RO | 0 |
| 1.14 | 100BASE-TX Full-Duplex | 1 = Capable of 100BASE-X full-duplex<br>0 = Not capable of 100BASE-X full-duplex | RO | 1 |
| 1.13 | 100BASE-TX Half-Duplex | 1 = Capable of 100BASE-X half-duplex<br>0 = Not capable of 100BASE-X half-duplex | RO | 1 |
| 1.12 | 10BASE-T Full-Duplex | 1 = 10 Mbps with full-duplex<br>0 = No 10 Mbps with full-duplex capability | RO | 1 |
| 1.11 | 10BASE-T Half-Duplex | 1 = 10 Mbps with half-duplex<br>0 = No 10 Mbps with half-duplex capability | RO | 1 |
| 1.10:7 | Reserved | — | RO | 0 |
| 1.6 | No Preamble | 1 = Preamble suppression<br>0 = Normal preamble | RO | 1 |
| 1.5 | Auto-Negotiation Complete | 1 = Auto-negotiation process completed<br>0 = Auto-negotiation process not completed | RO | 0 |
| 1.4 | Remote Fault | 1 = Remote fault<br>0 = No remote fault | RO/LH | 0 |
| 1.3 | Auto-Negotiation Ability | 1 = Capable to perform auto-negotiation<br>0 = Unable to perform auto-negotiation | RO | 1 |
| 1.2 | Link Status | 1 = Link is up<br>0 = Link is down | RO/LL | 0 |
| 1.1 | Jabber Detect | 1 = Jabber detected<br>0 = Jabber not detected. Default is low | RO/LH | 0 |
| 1.0 | Extended Capability | 1 = Supports extended capabilities registers | RO | 1 |

**TABLE 4-4: REGISTER 2H - PHY IDENTIFIER 1**

| Bit | Name | Description | Default | Reference |
|---|---|---|---|---|
| 2.15:0 | PHY ID Number | Assigned to the 3rd through 18th bits of the organizationally unique identifier (OUI). Microchip's OUI is 0010A1 (hex). | RO | 0022h |

**TABLE 4-5: REGISTER 3H - PHY IDENTIFIER 2**

| Bit | Name | Description | Default | Reference |
|---|---|---|---|---|
| 3.15:0 | PHY ID Number | Assigned to the 19th through 24th bits of the organizationally unique identifier (OUI). Microchip's OUI is 0010A1 (hex). | RO | 000101 |
| 3.9:4 | Model Number | Six bit manufacturer's model number | RO | 100001 |
| 3.3:0 | Revision Number | Four bit manufacturer's model number | RO | 1001 |

**TABLE 4-6: REGISTER 4H - AUTO-NEGOTIATION ADVERTISEMENT**

| Bit | Name | Description | Default | Reference |
|---|---|---|---|---|
| 4.15 | Next page | 1 = Next page capable<br>0 = No next page capability | RW | 0 |
| 4.14 | Reserved | — | RO | 0 |
| 4.13 | Remote Fault | 1 = Remote fault supported<br>0 = No remote fault | RW | 0 |
| 4.12:11 | Reserved | — | RO | 0 |

**TABLE 4-6: REGISTER 4H - AUTO-NEGOTIATION ADVERTISEMENT (CONTINUED)**

| Bit | Name | Description | Default | Reference |
|---|---|---|---|---|
| 4.10 | Pause | 1 = Pause function supported<br>0 = No pause function | RW | 0 |
| 4.9 | 100BASE-T4 | 1 = T4 capable<br>0 = No T4 capability | RO | 0 |
| 4.8 | 100BASE-TX Full-Duplex | 1 = TX with full-duplex<br>0 = No TX full-duplex capability | RW | Set by SPD100 & DUPLEX |
| 4.7 | 100BASE-TX | 1 = TX capable<br>0 = No TX capability | RW | Set by SPD100 |
| 4.6 | 10BASE-T Full-Duplex | 1 = 10 Mbps with full-duplex<br>0 = No 10 Mbps full-duplex capability | RW | Set by DUPLEX |
| 4.5 | 10BASE-T | 1 = 10 Mbps capable<br>0 = No 10 Mbps capability | RW | 1 |
| 4.4:0 | Selector Field | 1 = 10 Mbps capable<br>0 = No 10 Mbps capability | RW | 00001 |

**TABLE 4-7: REGISTER 5H - AUTO-NEGOTIATION LINK PARTNER ABILITY**

| Bit | Name | Description | Default | Reference |
|---|---|---|---|---|
| 5.15 | Next page | 1 = Next page capable<br>0 = No next page capability | RO | 0 |
| 5.14 | Acknowledge | 1 = Link code word received from partner<br>0 = Link code word not yet received | RO | 0 |
| 5.13 | Remote Fault | 1 = Remote fault detected; 0 = no remote fault | RO | 0 |
| 5.12 | Reserved | — | RO | 0 |
| 5.11:10 | Pause | 5.10 5.11<br>0 0<br>No PAUSE<br>0 1<br>Asymmetric PAUSE (link partner)<br>1 0<br>Symmetric PAUSE<br>1 1<br>Symmetric & Asymmetric PAUSE (local device) | RO | 0 |
| 5.9 | 100 BASE-T4 | 1 = T4 capable<br>0 = No T4 capability | RO | 0 |
| 5.8 | 100BASE-TX Full-Duplex | 1 = TX with full-duplex<br>0 = No TX full-duplex capability | RO | 0 |
| 5.7 | 100BASE-TX | 1 = TX capable<br>0 = No TX capability | RO | 0 |
| 5.6 | 10BASE-T Full-Duplex | 1 = 10 Mbps with full-duplex<br>0 = No 10 Mbps full-duplex capability | RO | 0 |
| 5.5 | 10BASE-T | 1 = 10 Mbps capable<br>0 = No 10 Mbps capability | RO | 0 |
| 5.4:0 | Selector Field | [00001] = IEEE 802.3 | RO | 00001 |

**TABLE 4-8: REGISTER 6H - AUTO-NEGOTIATION EXPANSION**

| Bit | Name | Description | Default | Reference |
|---|---|---|---|---|
| 6.15:5 | Reserved | — | RO | 0 |
| 6.4 | Parallel Detection Fault | 1 = Fault detected by parallel detection<br>0 = No fault detected by parallel detection | RO/LH | 0 |
| 6.3 | Link Partner Next Page Able | 1 = Link partner has next page capability<br>0 = Link partner does not have next page capability | RO | 0 |
| 6.2 | Next Page Able | 1 = Local device has next page capability<br>0 = Local device does not have next page capability | RO | 1 |
| 6.1 | Page Received | 1 = New page received<br>0 = New page not yet received | RO/LH | 0 |
| 6.0 | Link Partner Auto-Negotiation Able | 1 = Link partner has auto-negotiation capability<br>0 = Link partner does not have auto-negotiation capability | RO | 0 |

**TABLE 4-9: REGISTER 7H - AUTO-NEGOTIATION NEXT PAGE**

| Bit | Name | Description | Default | Reference |
|---|---|---|---|---|
| 7.15 | Next Page | 1 = Additional next page(s) will follow<br>0 = Last page | RW | 0 |
| 7.14 | Reserved | — | RP | 0 |
| 7.13 | Message Page | 1 = Message page<br>0 = Unformatted page | RW | 1 |
| 7.12 | Acknowledge 2 | 1 = Will comply with message<br>0 = Cannot comply with message | RW | 0 |
| 7.11 | Toggle | 1 = Previous value of the transmitted link code word equaled logic One<br>0 = Logic Zero | RO | 0 |
| 7.10:0 | Message Field | 11-bit wide field to encode 2048 messages | RW | 001 |

**TABLE 4-10: REGISTER 8H - LINK PARTNER NEXT PAGE ABILITY**

| Bit | Name | Description | Default | Reference |
|---|---|---|---|---|
| 8.15 | Next Page | 1 = Additional next page(s) will follow<br>0 = Last page | RO | 0 |
| 8.14 | Acknowledge | 1 = Successful receipt of link word<br>0 = No successful receipt of link word | RO | 0 |
| 8.13 | Message Page | 1 = Message Page<br>0 = Unformatted page | RO | 0 |
| 8.12 | Acknowledge 2 | 1 = Able to act on the information<br>0 = Not able to act on the information | RO | 0 |
| 8.11 | Toggle | 1 = Previous value of transmitted link code word equal to logic zero<br>0 = Previous value of transmitted link code word equal to logic one | RO | 0 |
| 8.10:0 | Message Field | — | RO | 0 |

**TABLE 4-11: REGISTER 15H - RXER COUNTER**

| Bit | Name | Description | Default | Reference |
|---|---|---|---|---|
| 15.15:0 | RXER Counter | RX Error counter for the RX_ER in each package | RO | 000 |

**TABLE 4-12: REGISTER 1BH - INTERRUPT CONTROL/STATUS REGISTER**

| Bit | Name | Description | Default | Reference |
|---|---|---|---|---|
| 1b.15 | Jabber Interrupt Enable | 1 = Enable jabber interrupt<br>0 = Disable jabber interrupt | RW | 0 |
| 1b.14 | Receive Error Interrupt Enable | 1 = Enable receive error interrupt<br>0 = Disable receive error interrupt | RW | 0 |
| 1b.13 | Page Received Interrupt Enable | 1 = Enable page received interrupt<br>0 = Disable page received interrupt | RW | 0 |
| 1b.12 | Parallel Detect Fault Interrupt Enable | 1 = Enable parallel detect fault interrupt<br>0 = Disable parallel detect fault interrupt | RW | 0 |
| 1b.11 | Link Partner Acknowledge Interrupt Enable | 1 = Enable link partner acknowledge interrupt<br>0 = Disable link partner acknowledge interrupt | RW | 0 |
| 1b.10 | Link Down Interrupt Enable | 1 = Enable link down interrupt<br>0 = Disable link down interrupt | RW | 0 |
| 1b.9 | Remote Fault Interrupt Enable | 1 = Enable remote fault interrupt<br>0 = Disable remote fault interrupt | RW | 0 |
| 1b.8 | Link Up Interrupt Enable | 1 = Enable link up interrupt<br>0 = Disable link up interrupt | RW | 0 |
| 1b.7 | Jabber Interrupt | 1 = Jabber interrupt occurred<br>0 = Jabber interrupt has not occurred | RO/SC | 0 |
| 1b.6 | Receive Error Interrupt | 1 = Receive error occurred<br>0 = Receive error has not occurred | RO/SC | 0 |
| 1b.5 | Page Receive Interrupt | 1 = Page receive occurred<br>0 = Page receive has not occurred | RO/SC | 0 |
| 1b.4 | Parallel Detect Fault Interrupt | 1 = Parallel detect fault occurred<br>0 = Parallel detect fault has not occurred | RO/SC | 0 |
| 1b.3 | Link Partner Acknowledge Interrupt | 1 = Link partner acknowledge occurred<br>0 = Link partner acknowledge has not occurred | RO/SC | 0 |
| 1b.2 | Link Down Interrupt | 1 = Link down occurred<br>0 = Link down has not occurred | RO/SC | 0 |
| 1b.1 | Remote Fault Interrupt | 1 = Remote fault occurred<br>0 = Remote fault has not occurred | RO/SC | 0 |
| 1b.0 | Link Up Interrupt | 1 = Link up interrupt occurred<br>0 = Link up interrupt has not occurred | RO/SC | 0 |

**TABLE 4-13: REGISTER 1FH - 100BASE-TX PHY CONTROLLER**

| Bit | Name | Description | Default | Reference |
|---|---|---|---|---|
| 1f.15:14 | Reserved | — | RO | 0 |
| 1f.13 | Pairswap Disable | 1 = Disable MDI/MDI-X<br>0 = Enable MDI/MDI-X | RW | 0 |
| 1f.12 | Energy Detect | 1 = Presence of signal on RX+/RX– analog wire pair<br>0 = No signal detected on RX+/RX– | RO | 0 |
| 1f.11 | Force Link | 1 = Force link pass<br>0 = Normal link operation<br>This bit bypasses the control logic and allow transmitter to send pattern even if there is no link. | RW | 0 |
| 1f.10 | Power Saving | 1 = Enable power-saving<br>0 = Disable | RW | 1 |
| 1f.9 | Interrupt Level | 1 = Interrupt pin active high<br>0 = Active low | RW | 0 |
| 1f.8 | Enable Jabber | 1 = Enable jabber counter<br>0 = Disable | RW | 1 |
| 1f.7 | Auto-Negotiation Complete | 1 = Auto-negotiation complete<br>0 = Not complete | RW | 0 |
| 1f.6 | Enable Pause (Flow-Control Result) | 1 = Flow control capable<br>0 = No flow control | RO | 0 |
| 1f.5 | PHY Isolate | 1 = PHY in isolate mode<br>0 = Not isolated | RO | 0 |
| 1f.4:2 | Operation Mode Indication | [000] = Still in auto-negotiation<br>[001] = 10BASE-T half-duplex<br>[010] = 100BASE-TX half-duplex<br>[011] = Reserved<br>[101] = 10BASE-T full-duplex<br>[110] = 100BASE-TX full-duplex<br>[111] = PHY/MII isolate | RO | 0 |
| 1f.1 | Enable SQE Test | 1 = Enable SQE test<br>0 = Disable | RW | 0 |
| 1f.0 | Disable Data Scrambling | 1 = Disable scrambler<br>0 = Enable | RW | 0 |

**Note 4-1** RW = Read/Write
RO = Read Only
SC = Self Clear
LH = Latch High
LL = Latch Low
Some of the default values are set by strap-in. See Table 2-2.

# 5.0 OPERATIONAL CHARACTERISTICS

## 5.1 Absolute Maximum Ratings*

Storage Temperature ($T_S$) ..... –55°C to +150°C

Supply Referenced to GND ..... –0.5V to +4.0V

All Pins ..... –0.5V to +4.0V

*Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

## 5.2 Operating Ratings**

Supply Voltage

($V_{DD\_PLL}$, $V_{DD\_TX}$, $V_{DD\_RXC}$, $V_{DD\_RCV}$, $V_{DDC}$) ..... +2.5V

($V_{DDIO}$) ..... +3.3V

Ambient Temperature ($T_A$)

Commercial ..... 0°C to +70°C

Industrial ..... –40°C to +85°C

Package Thermal Resistance (Note 5-1)

LQFP ($\theta_{JA}$) No Airflow ..... +83.56°C/W

SSOP ($\theta_{JA}$) No Airflow ..... +75.19°C/W

**The device is not guaranteed to function outside its operating ratings. Unused inputs must always be tied to an appropriate logic voltage level (GROUND to $V_{DD\_IO}$).

**Note 5-1** No (HS) heat spreader in this package.

## 6.0 ELECTRICAL CHARACTERISTICS

**TABLE 6-1: ELECTRICAL CHARACTERISTICS (Note 6-1)**

| $V_{DD}$ = 3.3V ±10% | | | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **Total Supply Current (Including TX Output Driver Current) (Note 6-2)** | | | | | | |
| Normal 100BASE-TX | $I_{DD1}$ | — | 116 | — | mA | Including 43 mA output current |
| Normal 100BASE-TX (Independent of utilization) | $I_{DD2}$ | — | 151 | — | mA | Including 103 mA output current |
| Power Saving Mode 1 | $I_{DD3}$ | — | 47 | — | mA | Auto-negotiation is enable |
| Power Down Mode | $I_{DD5}$ | — | 4 | — | mA | — |
| **TTL Inputs** | | | | | | |
| Input High Voltage | $V_{IH}$ | $1/2V_{DD}$(I/O) +0.2 | — | — | V | — |
| Input Low Voltage | $V_{IL}$ | — | — | 0.8 | V | — |
| Input Current | $I_{IN}$ | –10 | — | 10 | µA | $V_{IN}$ = GND ~ $V_{DDIO}$ |
| **TTL Outputs** | | | | | | |
| Output High Voltage | $V_{OH}$ | $1/2V_{DD}$(I/O) +0.6 | — | — | V | $I_{OH}$ = –4mA |
| Output Low Voltage | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 4mA |
| Output Tri-state Leakage | $I_{OZ}$ | — | — | 10 | µA | — |
| **100Base-TX Receive** | | | | | | |
| RX+/RX– Differential Input Resistance | $R_{IN}$ | — | 8 | — | kΩ | — |
| Propagation Delay | | — | 50 | 110 | ns | From magnetics to RDTX |
| **10Base-TX Transmit (Measured Differentially After 1:1 Transformer)** | | | | | | |
| Peak Differential Output Voltage | $V_O$ | 0.95 | — | 1.05 | V | 50Ω from each output to $V_{DD}$ |
| Output Voltage Imbalance | $V_{IMB}$ | — | — | 2 | % | 50Ω from each output to $V_{DD}$ |
| Rise/Fall Time | $t_r$, $t_f$ | 3 | — | 5 | ns | — |
| Rise/Fall Time Imbalance | | 0 | — | 0.5 | ns | — |
| Duty Cycle Distortion | | — | — | ±0.5 | ns | — |
| Overshoot | | — | — | 5 | % | — |
| Reference Voltage of ISET | $V_{SET}$ | — | 0.75 | — | V | — |
| Propagation Delay | | — | 45 | 60 | ns | From TDTX to magentics |
| Jitters | | — | 0.7 | 1.4 | $ns_{(PP)}$ | — |
| **10Base-TX Receive** | | | | | | |
| RX+/RX– Differential Input Resistance | $R_{IN}$ | — | 8 | — | kW | — |
| Squelch Threshold | $V_{SQ}$ | — | 400 | — | mV | 5 MHz square wave |
| **100Base-TX Transmit (Measured Differentially After 1:1 Transformer)** | | | | | | |
| Peak Differential Output Voltage | $V_P$ | 2.2 | — | 2.8 | V | 50Ω from each output to $V_{DD}$ |
| Jitters Added | | — | — | ±3.5 | ns | 50Ω from each output to $V_{DD}$ |
| Rise/Fall Time | $t_r$, $t_f$ | — | 25 | — | ns | — |
| **Clock Outputs** | | | | | | |
| Crystal Oscillator | X1, X2 | — | 25 | — | MHz | — |
| Receive Clock, 100TX | $RXC_{100}$ | — | 25 | — | MHz | — |

**TABLE 6-1: ELECTRICAL CHARACTERISTICS (Note 6-1) (CONTINUED)**

| $V_{DD}$ = 3.3V ±10% | | | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| Receive Clock, 10T | $RXC_{10}$ | — | 2.5 | — | MHz | — |
| Receive Clock Jitters | | — | 3.0 | — | ns(pp) | — |
| Transmit Clock, 100TX | $TXC_{100}$ | — | 25 | — | MHz | — |
| Transmit Clock, 10T | $TXC_{10}$ | — | 2.5 | — | MHz | — |
| Transmit Clock Jitters | | — | 1.8 | — | ns(pp) | — |

**Note 6-1** $T_A$ = 25°C. Specification for packaged product only.

**Note 6-2** There is 100% data transmission in full-duplex mode and a minimum IPG with a 130 meter cable.

## 7.0 TIMING SPECIFICATIONS

### 7.1 10BASE-T MII Transmit Timing

**FIGURE 7-1: 10BASE-T MII TRANSMIT TIMING**

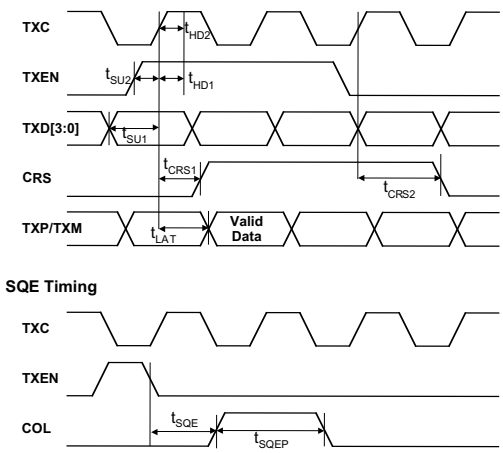



**TABLE 7-1: 10BASE-T MII TRANSMIT TIMING PARAMETERS**

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| TXD [3:0] Set-Up to TXC High | $t_{SU1}$ | 10 | — | — | ns |
| TXEN Set-Up to TXC High | $t_{SU2}$ | 10 | — | — | ns |
| TXD [3:0] Hold After TXC High | $t_{HD1}$ | 0 | — | — | ns |
| TXEN Hold After TXC High | $t_{HD2}$ | 0 | — | — | ns |
| TXEN High to CRS Asserted Latency | $t_{CRS1}$ | — | 4 | — | BT (Note 7-1) |
| TXEN Low to CRS De-Asserted Latency | $t_{CRS2}$ | — | 8 | — | BT |
| TXEN High to TXP/TXM Output (TX Latency) | $t_{LAT}$ | — | 4 | — | BT |
| COL (SQE) Delay After TXEN De-Asserted | $t_{SQE}$ | — | 2.5 | — | µs |
| COL (SQE) Pulse Duration | $t_{SQEP}$ | — | 1.0 | — | µs |

**Note 7-1** 1BT = 10 ns at 10BASE-TX.

## 7.2 100BASE-T MII Transmit Timing

**FIGURE 7-2: 100BASE-T MII TRANSMIT TIMING**

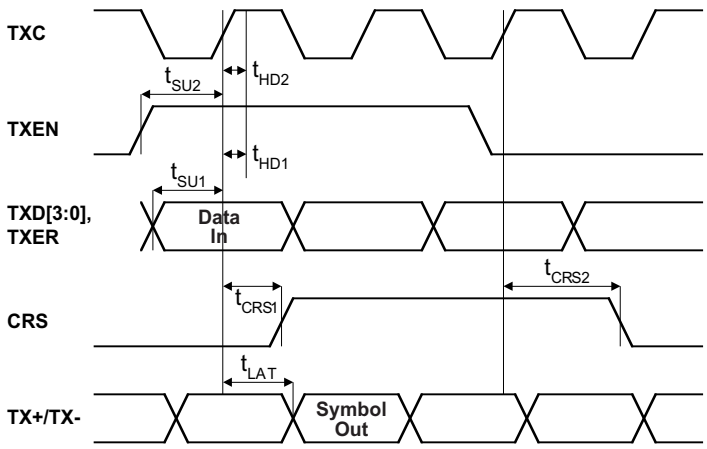



**TABLE 7-2: 100BASE-T MII TRANSMIT TIMING PARAMETERS**

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| TXD [3:0] Set-Up to TXC High | $t_{SU1}$ | 10 | — | — | ns |
| TXEN Set-Up to TXC High | $t_{SU2}$ | 10 | — | — | ns |
| TXD [3:0] Hold After TXC High | $t_{HD1}$ | 0 | — | — | ns |
| TXER Hold After TXC High | $t_{HD2}$ | 0 | — | — | ns |
| TXEN Hold After TXC High | $t_{HD3}$ | 0 | — | — | ns |
| TXEN High to CRS Asserted Latency | $t_{CRS1}$ | — | 4 | — | BT (Note 7-1) |
| TXEN Low to CRS De-Asserted Latency | $t_{CRS2}$ | — | 4 | — | BT |
| TXEN High to TXP/TXM Output (TX Latency) | $t_{LAT}$ | — | 9 | — | BT |

**Note 7-1** 1BT = 10 ns at 100BASE-TX

## 7.3 100BASE-T MII Receive Timing

**FIGURE 7-3: 100BASE-T MII RECEIVE TIMING**

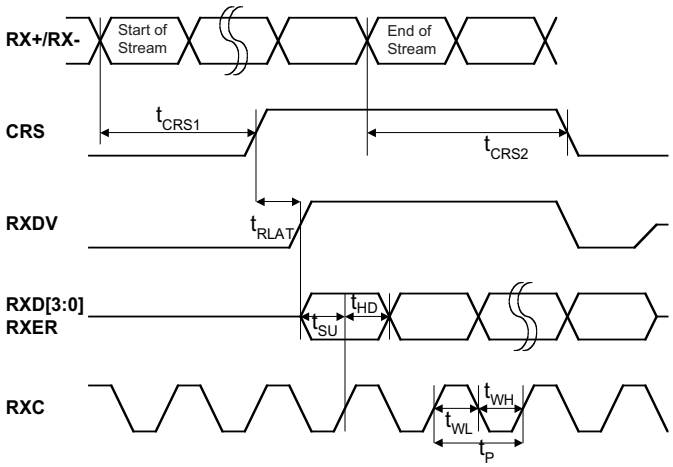



**TABLE 7-3: 100BASE-T MII RECEIVE TIMING PARAMETERS**

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| RXC Period | $t_P$ | — | 40 | — | ns |
| RXC Pulse Width | $t_{WL}$ | 20 | — | — | ns |
| RXC Pulse Width | $t_{WH}$ | 20 | — | — | ns |
| RXD [3:0], RXER, RXDV Set-Up to Rising Edge of RXC | $t_{SU}$ | — | 20 | — | ns |
| RXD [3:0], RXER, RXDV Hold from Rising Edge of RXC | $t_{HD}$ | — | 20 | — | ns |
| CRS to RXD Latency, 4B or 5B Aligned | $t_{RLAT}$ | — | 6 | — | BT |
| “Start of Stream” to CSR Asserted | $t_{CRS1}$ | 106 | — | 138 | ns |
| “End of Stream” to CSR De-Asserted | $t_{CRS2}$ | 154 | — | 186 | ns |

## 7.4 Auto-Negotiation

**FIGURE 7-4: AUTO-NEGOTIATION/FAST LINK PULSE TIMING**

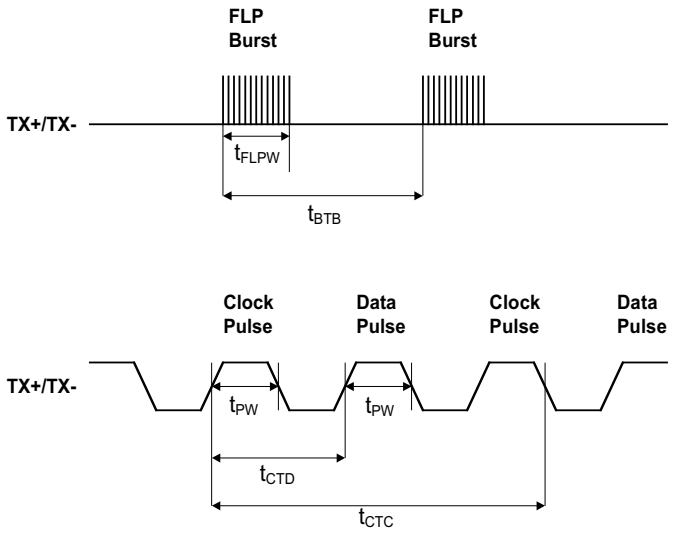



**TABLE 7-4: AUTO-NEGOTIATION/FAST LINK PULSE TIMING PARAMETERS**

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| FLP Burst to FLP Burst | $t_{BTB}$ | 8 | 16 | 24 | ms |
| FLP Burst Width | $t_{FLPW}$ | — | 2 | — | ms |
| Clock/Data Pulse Width | $t_{PW}$ | — | 100 | — | ns |
| Clock Pulse to Data Pulse | $t_{CTD}$ | — | 69 | — | µs |
| Clock Pulse to Clock Pulse | $t_{CTC}$ | — | 136 | — | µs |
| Number of Clock/Data Pulses per Burst | | 17 | — | 33 | |

## 7.5 SMI Timing

**FIGURE 7-5: SERIAL MANAGEMENT INTERFACE TIMING**

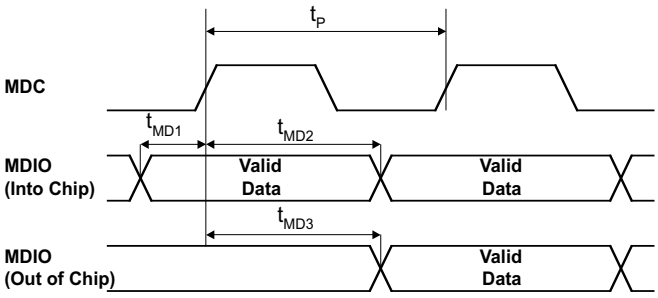



**TABLE 7-5: SERIAL MANAGEMENT INTERFACE TIMING PARAMETERS**

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| MDC Period | $t_P$ | — | 400 | — | ns |
| MDIO Set-Up to MDC (MDIO as Input) | $t_{MD1}$ | 10 | — | — | ns |
| MDIO Hold After MDC (MDIO as Input) | $t_{MD2}$ | 10 | — | — | ns |
| MDC to MDIO Valid (MDIO as Output) | $t_{MD3}$ | — | 222 | — | ns |

## 7.6 Reset Timing

**FIGURE 7-6: RESET TIMING**

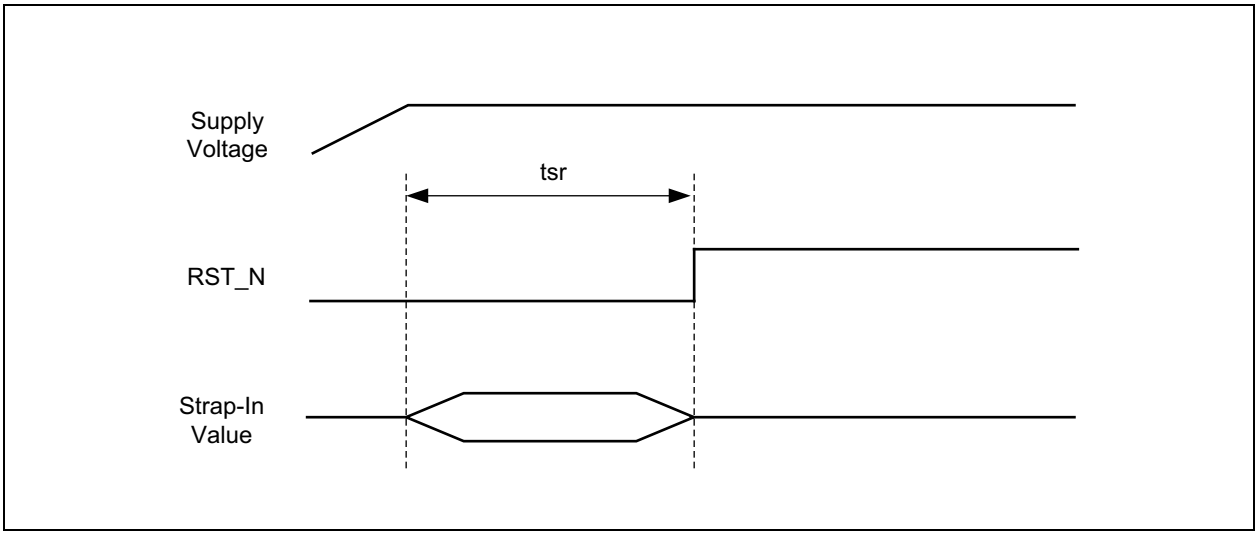



**TABLE 7-6: RESET TIMING PARAMETERS**

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Stable Supply Voltages to Reset High | $f_{SR}$ | 50 | — | — | µs |

### 7.6.1 RESET CIRCUIT DIAGRAM

The following discrete reset circuit as shown in Figure 7-7 is recommended when powering up the KSZ8721BL/SL device. For the application where the reset circuit signal comes from another device (e.g., CPU, FPGA, etc), please refer to the reset circuit as shown in Figure 8-8.

**FIGURE 7-7: RECOMMENDED RESET CIRCUIT**

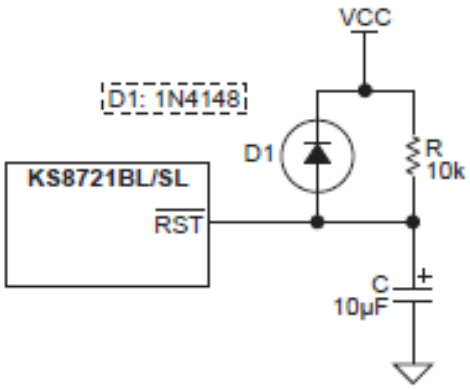
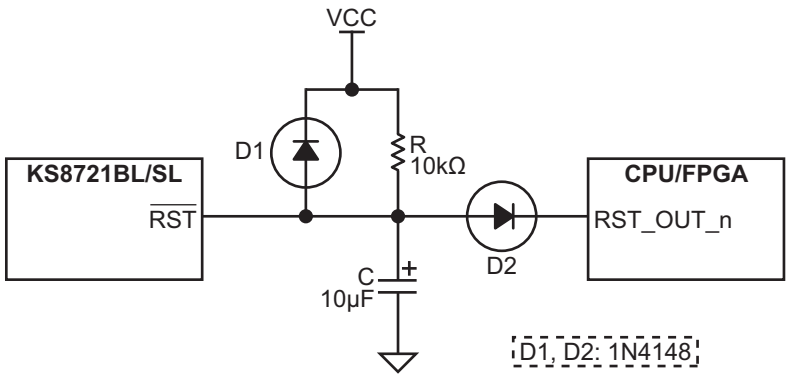


**FIGURE 7-8: RECOMMENDED CIRCUIT FOR INTERFACING WITH CPU/FPGA RESET**

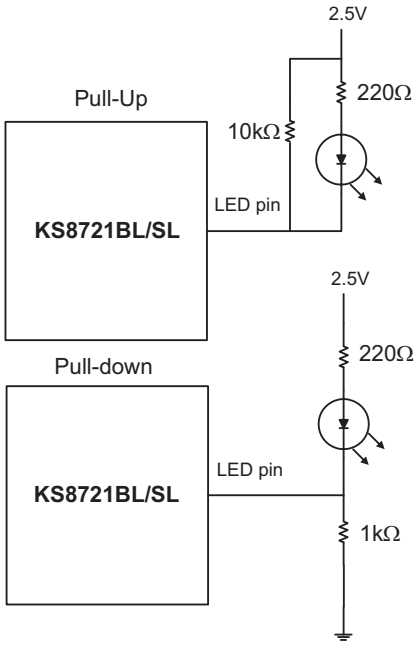



At power-on-reset, R, C, and D1 provide the necessary ramp rise time to reset the device. The reset out from CPU/FPGA provides warm reset after power up. It is also recommended to power up the $V_{DD}$ core voltage earlier than $V_{DDIO}$ voltage. At worst case, the both $V_{DD}$ core and $V_{DDIO}$ voltages should come up at the same time.

### 7.6.2 REFERENCE CIRCUIT FOR STRAPPING OPTION CONFIGURATION

Figure 7-9 shows the reference circuit for strapping option pins.

**FIGURE 7-9: REFERENCE CIRCUIT, STRAPPING OPTION PINS**




Reference circuits for unmanaged programming through LED ports.

## 7.7 Selection of Isolation Transformers

One simple 1:1 isolation transformer is needed at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements. The following table gives recommended transformer characteristics.

**TABLE 7-7: SELECTION OF ISOLATION TRANSFORMERS (Note 7-1)**

| Parameter | Value | Test Condition |
|---|---|---|
| Turns ratio | 1 CT : 1 CT | — |
| Open-circuit inductance (min) | 350 µH | 100 mV, 100 kHz, 8 mA |
| Leakage inductance (max) | 0.4 µH | 1 MHz (min) |
| Inter-winding capacitance (max) | 12 pF | — |
| D.C. resistance (max) | 0.9Ω | — |
| Insertion loss (max) | 1.0 dB | 0 MHz - 65 MHz |
| HIPOT (min) | $1500V_{rms}$ | — |

**Note 7-1** The IEEE 802.3u standard for 100BASE-TX assumes a transformer loss of 0.5dB. For the transmit line transformer, insertion loss of up to 1.3 dB can be compensated or by increasing the line drive current by means of reducing the $I_{SET}$ resistor value. Please select the transformer that supports auto-MDI/MDI-X.

## 7.8 Selection of Reference Crystal

An oscillator or crystal with the following typical characteristics is recommended.

**TABLE 7-8: SELECTION OF ISOLATION TRANSFORMERS**

| Characteristics | Value |
|---|---|
| Frequency | 25 MHz |
| Frequency tolerance (max) | ±100 ppm |
| Load capacitance (max) | 20 pF |
| Series resistance (max) | 40Ω |

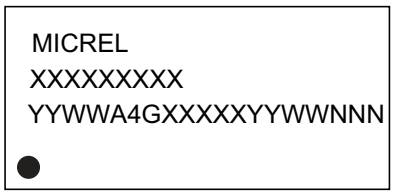
**TABLE 7-9: QUALIFIED SINGLE PORT TRANSFORMER LISTS**

| Single Port Magnetic Manufacturer | Part Number | Auto MDIX |
|---|---|---|
| Pulse | H1102 | Yes |
| Bel Fuse | S558-5999-U7 | Yes |
| YCL | PT163020 | Yes |
| Transpower | HB726 | Yes |
| Delta | LF8505 | Yes |
| LanKom | LF-H41S | Yes |
| **Integrated Transformers** | | |
| Pulse | J0011D21 | Yes |
| Pulse | J00-0061 | Yes |

## 8.0 PACKAGING INFORMATION

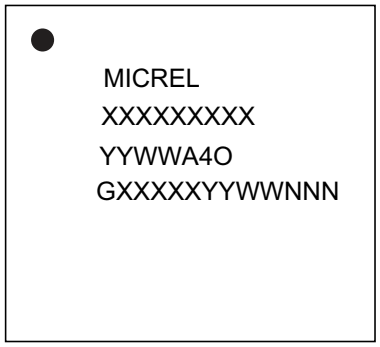
### 8.1 Package Marking Information

48-Lead SSOP*

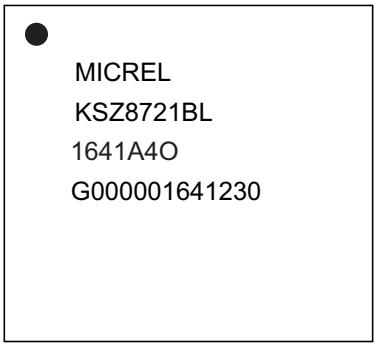



Example


48-Lead LQFP*




Example




| | | |
|---|---|---|
| **Legend:** | XX...X | Product code or customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |
| | ●, ▲, ▼ | Pin one index is identified by a dot, delta up, or delta down (triangle mark). |

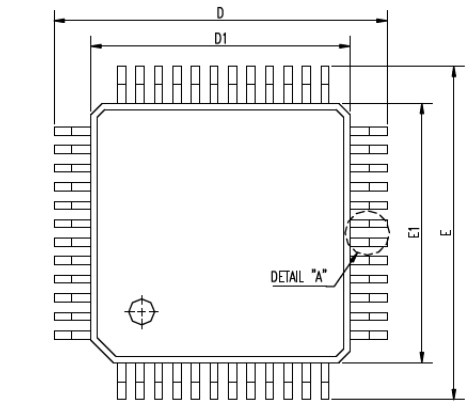
**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

**FIGURE 8-1: 48-LEAD LQFP 7 MM X 7 MM PACKAGE OUTLINE & RECOMMENDED LAND PATTERN**

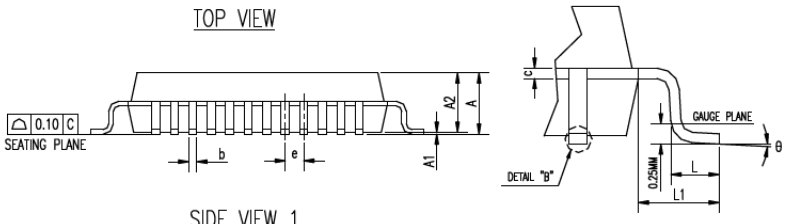
**TITLE**
48 LEAD LQFP 7x7mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

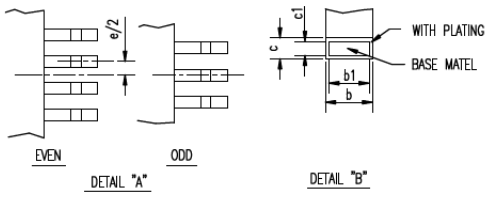
| DRAWING # | LQFP7x7-48LD-PL-1 | UNIT | MM [INCHES] |
|---|---|---|---|

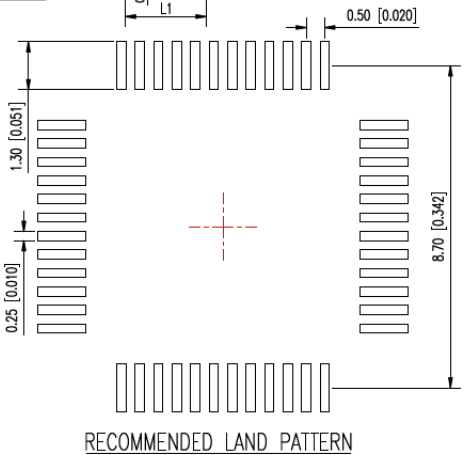



| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM | MAX. | MIN. | NOM | MAX. |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 8.90 | 9.00 | 9.10 | 0.350 | 0.354 | 0.358 |
| D1 | 6.90 | 7.00 | 7.10 | 0.272 | 0.276 | 0.280 |
| E | 8.90 | 9.00 | 9.10 | 0.350 | 0.354 | 0.358 |
| E1 | 6.90 | 7.00 | 7.10 | 0.272 | 0.276 | 0.280 |
| c | 0.178 TYP. | | | 0.007 TYP. | | |
| c1 | 0.127 TYP. | | | 0.005 TYP. | | |
| L | 0.50 | 0.60 | 0.70 | 0.020 | 0.024 | 0.028 |
| L1 | 1.00 REF. | | | 0.039 REF. | | |
| θ | 0 | 3.5 | 7 | 0 | 3.5 | 7 |
| JEDEC | | | | | | |

| | b (MM) | | | b1 (MM) | | | e (MM) | | | JEDEC |
|---|---|---|---|---|---|---|---|---|---|---|
| N | MIN. | NOM | MAX. | MIN. | NOM | MAX. | MIN. | NOM | MAX. | |
| 48L | 0.19 | 0.22 | 0.25 | 0.17 | 0.20 | 0.23 | 0.50 BSC. | | | |



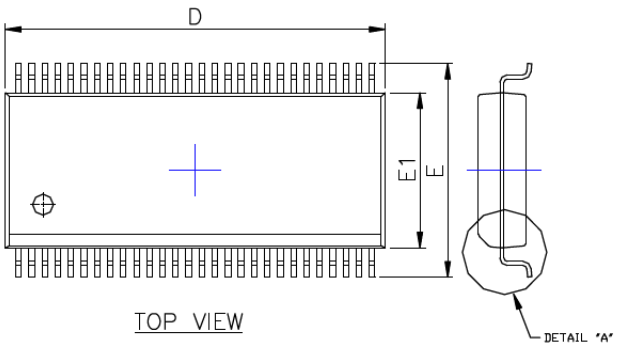

NOTES:
1. ALL DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION : MM.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

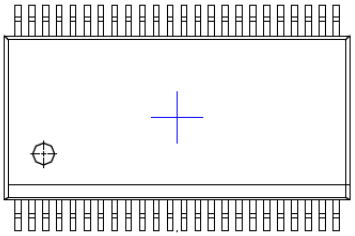
**FIGURE 8-2: 48-LEAD SSOP 7 MM X 7 MM PACKAGE OUTLINE & RECOMMENDED LAND PATTERN**

**TITLE**
48 LEAD SSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

| DRAWING # | SSOP-48LD-PL-1 | UNIT | MM |
|---|---|---|---|

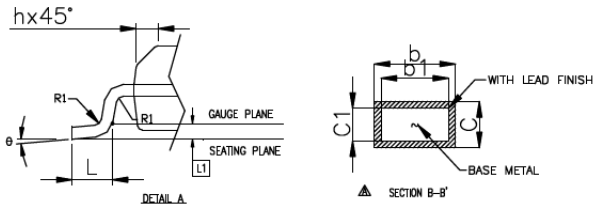



TOP VIEW

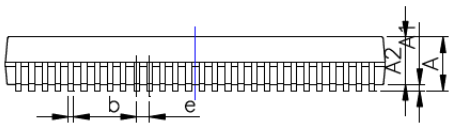


BOTTOM VIEW

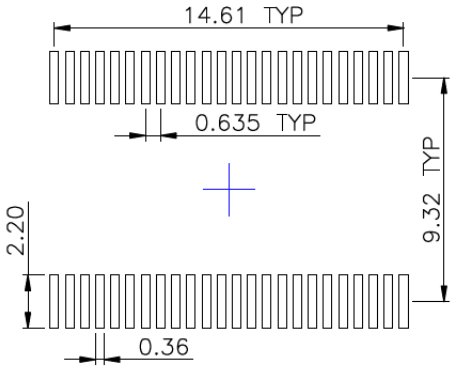
| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM | MAX. | MIN. | NOM | MAX. |
| A | 2.413 | 2.591 | 2.794 | 0.095 | 0.102 | 0.110 |
| A1 | 0.203 | 0.305 | 0.406 | 0.008 | 0.012 | 0.016 |
| b | 0.203 | | 0.343 | 0.008 | | 0.014 |
| b1 | 0.203 | 0.254 | 0.305 | 0.008 | 0.010 | 0.012 |
| c | 0.127 | | 0.254 | 0.005 | | 0.010 |
| c1 | 0.127 | | 0.216 | 0.005 | | 0.009 |
| E | 10.058 | 10.312 | 10.566 | 0.396 | 0.406 | 0.416 |
| E1 | 7.391 | 7.493 | 7.595 | 0.291 | 0.295 | 0.299 |
| e | 0.635 BASIC | | | 0.025 BASIC | | |
| h | 0.381 | | 0.635 | 0.015 | | 0.025 |
| L | 0.508 | | 1.016 | 0.020 | | 0.040 |
| L1 | 0.254 BASIC | | | 0.010 BASIC | | |
| R1 | | | | | | |
| θ | 0 | | 5 | 0 | | 5 |
| D | 15.748 | 15.875 | 16.002 | | | |




DETAILED VIEW




SIDE VIEW




RECOMMENDED LAND PATTERN

NOTES :
1. THE DIAGRAMS DO NOT REPRESNET THE ACTUAL PIN COUNT.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

## APPENDIX A: DATA SHEET REVISION HISTORY

**TABLE A-1: REVISION HISTORY**

| Revision | Section/Figure/Entry | Correction |
|---|---|---|
| DS00002813A (10-30-18) | — | Converted Micrel data sheet KSZ8721BL/SL to Microchip DS00002813A. Minor text changes throughout. |

## THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

## CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

## CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

**Technical support is available through the web site at: http://microchip.com/support**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | X | X | -XX |
|---|---|---|---|---|
| Device | Package | Supply Voltage | Temperature | Media Type |

| | |
|---|---|
| **Device:** | KSZ8721 |
| **Package:** | B = 48-Lead LQFP<br>S = 48-Lead SSOP |
| **Supply Voltage:** | L = Single 3.3V Supply |
| **Temperature:** | <blank> = 0°C to +70°C<br>I = –40°C to +85°C |
| **Media Type:** | <blank> = 30/Tube (SSOP Package Only)<br><blank> = 250/Tray (LQFP package Only)<br><TR> = 1000/Reel |

**Example:**

| | |
|---|---|
| a) KSZ8721-BL: | 10/100 Base-TX/FX MII Physical Layer Transceiver, 48-Lead LQFP, Single 3.3V Supply, 0°C to +70°C,250/Tray |
| b) KSZ8721-SL: | 10/100 Base-TX/FX MII Physical Layer Transceiver, 48-Lead SSOP, Single 3.3V Supply, 0°C to +70°C,30/Tube |
| c) KSZ8721-BLI: | 10/100 Base-TX/FX MII Physical Layer Transceiver, 48-Lead LQFP, Single 3.3V Supply, –40°C to +85°C,250/Tray |
| d) KSZ8721-SLI: | 10/100 Base-TX/FX MII Physical Layer Transceiver, 48-Lead SSOP, Single 3.3V Supply, –40°C to +85°C,30/Tube |
| e) KSZ8721-BL-TR: | 10/100 Base-TX/FX MII Physical Layer Transceiver, 48-Lead LQFP, Single 3.3V Supply, 0°C to +70°C,1000/Reel |
| f) KSZ8721-SL-TR: | 10/100 Base-TX/FX MII Physical Layer Transceiver, 48-Lead SSOP, Single 3.3V Supply, 0°C to +70°C, 1000/Tray |
| g) KSZ8721-BLI-TR: | 10/100 Base-TX/FX MII Physical Layer Transceiver, 48-Lead LQFP, Single 3.3V Supply, –40°C to +85°C,1000/Reel |
| d) KSZ8721-SLI-TR: | 10/100 Base-TX/FX MII Physical Layer Transceiver, 48-Lead SSOP, Single 3.3V Supply, –40°C to +85°C,1000/Reel |

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**NOTES:**

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.



ISBN: 978-1-5224-3789-5

**QUALITY MANAGEMENT SYSTEM**
**CERTIFIED BY DNV**
**═ ISO/TS 16949 ═**

*Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

# Worldwide Sales and Service


## AMERICAS

**Corporate Office**
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

**Atlanta**
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

**Austin, TX**
Tel: 512-257-3370

**Boston**
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

**Chicago**
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

**Dallas**
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

**Detroit**
Novi, MI
Tel: 248-848-4000

**Houston, TX**
Tel: 281-894-5983

**Indianapolis**
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

**Los Angeles**
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

**Raleigh, NC**
Tel: 919-844-7510

**New York, NY**
Tel: 631-435-6000

**San Jose, CA**
Tel: 408-735-9110
Tel: 408-436-4270

**Canada - Toronto**
Tel: 905-695-1980
Fax: 905-695-2078

## ASIA/PACIFIC

**Australia - Sydney**
Tel: 61-2-9868-6733

**China - Beijing**
Tel: 86-10-8569-7000

**China - Chengdu**
Tel: 86-28-8665-5511

**China - Chongqing**
Tel: 86-23-8980-9588

**China - Dongguan**
Tel: 86-769-8702-9880

**China - Guangzhou**
Tel: 86-20-8755-8029

**China - Hangzhou**
Tel: 86-571-8792-8115

**China - Hong Kong SAR**
Tel: 852-2943-5100

**China - Nanjing**
Tel: 86-25-8473-2460

**China - Qingdao**
Tel: 86-532-8502-7355

**China - Shanghai**
Tel: 86-21-3326-8000

**China - Shenyang**
Tel: 86-24-2334-2829

**China - Shenzhen**
Tel: 86-755-8864-2200

**China - Suzhou**
Tel: 86-186-6233-1526

**China - Wuhan**
Tel: 86-27-5980-5300

**China - Xian**
Tel: 86-29-8833-7252

**China - Xiamen**
Tel: 86-592-2388138

**China - Zhuhai**
Tel: 86-756-3210040

## ASIA/PACIFIC

**India - Bangalore**
Tel: 91-80-3090-4444

**India - New Delhi**
Tel: 91-11-4160-8631

**India - Pune**
Tel: 91-20-4121-0141

**Japan - Osaka**
Tel: 81-6-6152-7160

**Japan - Tokyo**
Tel: 81-3-6880- 3770

**Korea - Daegu**
Tel: 82-53-744-4301

**Korea - Seoul**
Tel: 82-2-554-7200

**Malaysia - Kuala Lumpur**
Tel: 60-3-7651-7906

**Malaysia - Penang**
Tel: 60-4-227-8870

**Philippines - Manila**
Tel: 63-2-634-9065

**Singapore**
Tel: 65-6334-8870

**Taiwan - Hsin Chu**
Tel: 886-3-577-8366

**Taiwan - Kaohsiung**
Tel: 886-7-213-7830

**Taiwan - Taipei**
Tel: 886-2-2508-8600

**Thailand - Bangkok**
Tel: 66-2-694-1351

**Vietnam - Ho Chi Minh**
Tel: 84-28-5448-2100

## EUROPE

**Austria - Wels**
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

**Denmark - Copenhagen**
Tel: 45-4450-2828
Fax: 45-4485-2829

**Finland - Espoo**
Tel: 358-9-4520-820

**France - Paris**
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

**Germany - Garching**
Tel: 49-8931-9700

**Germany - Haan**
Tel: 49-2129-3766400

**Germany - Heilbronn**
Tel: 49-7131-67-3636

**Germany - Karlsruhe**
Tel: 49-721-625370

**Germany - Munich**
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

**Germany - Rosenheim**
Tel: 49-8031-354-560

**Israel - Ra'anana**
Tel: 972-9-744-7705

**Italy - Milan**
Tel: 39-0331-742611
Fax: 39-0331-466781

**Italy - Padova**
Tel: 39-049-7625286

**Netherlands - Drunen**
Tel: 31-416-690399
Fax: 31-416-690340

**Norway - Trondheim**
Tel: 47-7288-4388

**Poland - Warsaw**
Tel: 48-22-3325737

**Romania - Bucharest**
Tel: 40-21-407-87-50

**Spain - Madrid**
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

**Sweden - Gothenberg**
Tel: 46-31-704-60-40

**Sweden - Stockholm**
Tel: 46-8-5090-4654

**UK - Wokingham**
Tel: 44-118-921-5800
Fax: 44-118-921-5820

# X-ON Electronics

Largest Supplier of Electrical and Electronic Components

***Click to view similar products for*** Ethernet Development Tools ***category:***

***Click to view products by*** Micrel ***manufacturer:***

Other Similar products are found below :

KSZ8863FLL-EVAL KSZ8873MLL-EVAL PD-IM-7648M PD-IM-7648T4 PD70101EVB15F-12 PD70101EVB6F PD70211EVB50FW-5 PD70211EVB72FW-12 EV44F42A WIZ550S2E-232-EVB DFR0272 A000024 DFR0125 UKIT-006GP UKIT-003FE UKIT-002GB UKIT-001FE EVB-KSZ9477 OM-E-ETH DP83867ERGZ-R-EVM UP-POE-A20-0001 2971 3785 ASX00006 ASX00021 ASX00026 XTIB-E ESP32-ETHERNET-KIT-VE EVB-KSZ9897-1 KSZ9031MNX-EVAL AC164121 AC164132 AC320004-5 AC320004-6 AC320004-7 DM320114 DM990004 EV02N47A EV44C93A EV57N07A EVB-KSZ8563 EVB-KSZ9477-1 EVB-KSZ9893 EVB-LAN7430 EVB-LAN7431-EDS EVB-LAN7800LC-1 EVB-LAN7850 EVB-LAN9252-3PORT EVB-LAN9252-ADD-ON EVB-LAN9252-DIGIO