KSZ8893FQL

Single-Chip 3-Port Switch with Fiber Support

Features

- **Integrated 3-Port 10/100 Ethernet Switch**
  - Three MACs and Two PHYs Fully Compliant with IEEE 802.3u Standard
  - Non-Blocking Switch Fabric Ensures Fast Packet Delivery by Utilizing an 1K MAC Address Lookup Table and a Store-and-Forward Architecture
  - Full-Duplex IEEE 802.3x Flow Control (PAUSE) with Force Mode Option
  - Half-Duplex Back Pressure Flow Control
  - HP Auto MDI-X for Reliable Detection of and Correction for Straight-Through and Crossover Cables with Disable and Enable Option
  - Microchip LINKMD® TDR-Based Cable Diagnostics Permit Identification of Faulty Copper Cabling
  - 100BASE-FX, 100BASE-SX, and 10BASE-FL Fiber Support on Port 1
  - MII Interface Supports Both MAC Mode and PHY Mode
  - RMII Interface Support with External 50 MHz System Clock
  - 7-Wire Serial Network Interface (SNI) Support for Legacy MAC
  - Comprehensive LED Indicator Support for Link, Activity, Full-/Half-Duplex and 10/100 Speed
- **Fiber Support**
  - Integrated LED Driver and Post Amplifier for 10BASE-FL and 100BASE-SX Optical Modules
- **TTC TS-1000 OAM**
  - Supports OAM Sub-Layer which Conforms to TS-1000 V2 Specification from Telecommunication Technology Committee (TTC)
  - Sends and Receives OAM Frames to Center or Terminal Side
  - Loopback Mode to Support Loopback Packet from Center Side to Terminal Side
  - Far-End Fault Detection with Disable and Enable
  - Link Transparency to Indicate Link Down from Link Partner
  - Unique User Defined Register (UDR) Feature Brings OAM to Low Cost/Complexity Nodes
- **Comprehensive Configuration Register Access**
  - SMI, SPI, and I^2C Management Interfaces to All 8-bit Internal Registers
  - MII Management (MIIM) Interface to PHY Registers
  - I/O Pins Strapping and EEPROM to Program Selective Registers in Unmanaged Switch Mode
  - Control Registers Configurable on the Fly (Port-Priority, 802.1p/d/q, AN…)
- **QoS/CoS Packet Prioritization Support**
  - Per Port, 802.1p, and DiffServ-Based
  - Re-Mapping of 802.1p Priority Field Per Port Basis
  - Four Priority Levels
- **Advanced Switch Features**
  - IEEE 802.1q VLAN Support for Up to 16 Groups (Full Range of VLAN IDs)
  - VLAN ID Tag/Untag Options, Per Port Basis
  - IEEE 802.1p/q Tag Insertion or Removal on a Per Port Basis (Egress)
  - Programmable Rate Limiting at the Ingress and Egress on a Per Port Basis
  - Broadcast Storm Protection with Percent Control (Global and Per Port Basis)
  - IEEE 802.1d Spanning Tree Protocol Support
  - Special Tagging Mode to Inform the Processor which Ingress Port Receives the Packet
  - IGMP Snooping (IPv4) and MLD Snooping (IPv6) Support for Multicast Packet Filtering
  - MAC Filtering Function to Forward Unknown Unicast Packets to Specified Port
  - Double-Tagging Support
- **Low Latency Support**
  - Repeater Mode
- **Switch Monitoring Features**
  - Port Mirroring/Monitoring/Sniffing: Ingress and/or Egress Traffic to Any Port or MII
  - MIB Counters for Fully Compliant Statistics Gathering, 34 MIB Counters Per Port
  - Loopback Modes for Remote Diagnostic of Failure
- **Low Power Dissipation**
  - Full-Chip Hardware Power-Down (Register Configuration Not Saved)
  - Per Port Based Software Power-Save on PHY (Idle Link Detection, Register Configuration Preserved)
  - Voltages: Core 1.2V, I/O and Transceiver 3.3V
- **Available in a 128-Pin PQFP, Lead-Free Package**

Applications

- Media Conversion Modules
  - 10BASE-FL to/from 10BASE-T
  - 100BASE-SX to/from 100BASE-TX
  - 100BASE-FX to/from 100BASE-TX
- FTTx Managed/Unmanaged Media Converters
- Fiber Broadband Gateways

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Table of Contents

1.0 INTRODUCTION

1.1 General Description

The KSZ8893FQL, a highly integrated single-chip 3-port Fast Ethernet switch is designed for applications with fiber support such as media converter. It provides two 10/100 transceivers with patented mixed-signal low-power technology, three media access control (MAC) units, a high-speed non-blocking switch fabric, a Layer-2 managed switch and TS-1000 OAM (Operations, Administration and Management) V2 in a compact solution. Backwards compatible to the TS-1000 (2002) specification, TS-1000 V2 is an OAM sub-layer that provides communication between CO (central office) and CPE (customer premises equipment).

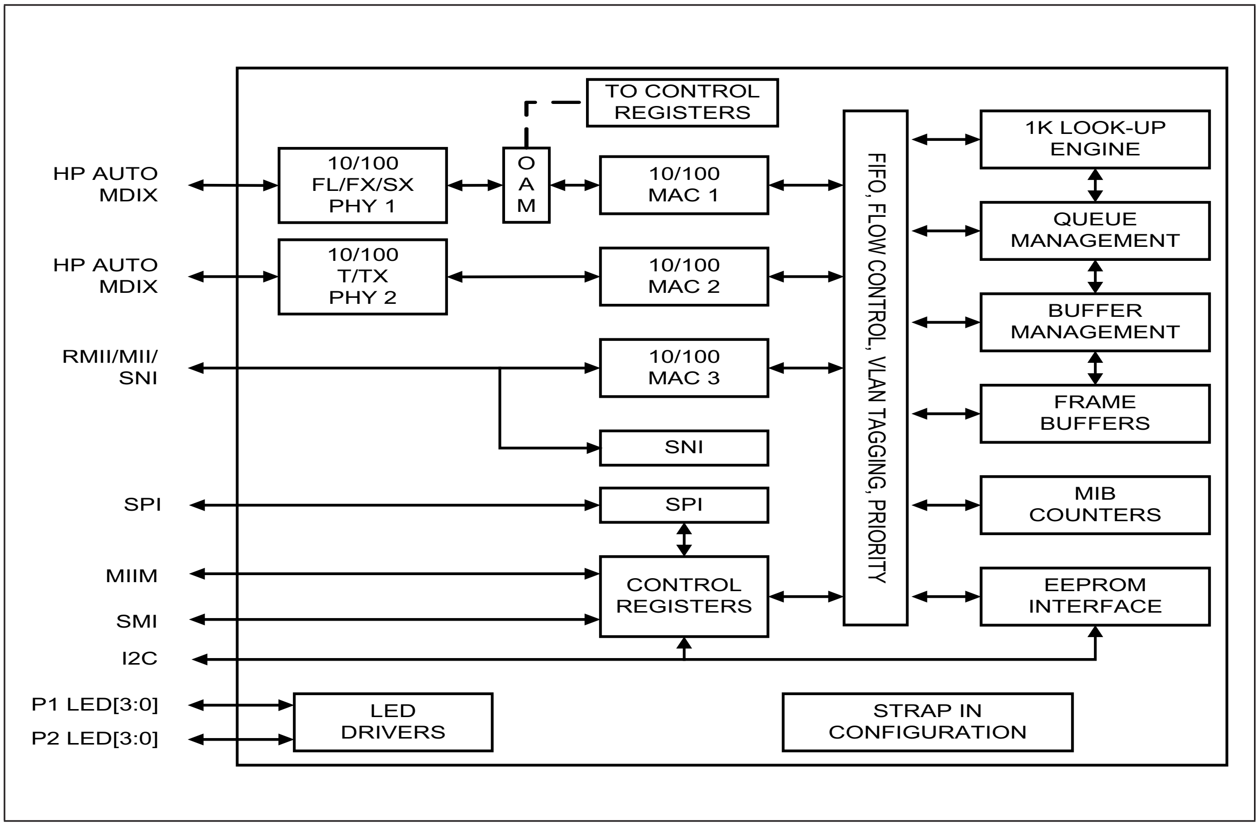
In fiber mode, one PHY unit can be configurable to 100BASE-FX, 100BASE-SX, or 10BASE-FL fiber for conversion to 10BASE-T and 100BASE-TX copper. A fiber LED driver and post amplifier are also included for 10BASE-FL and 100BASE-SX applications.

In copper mode, both PHY units support 10BASE-T and 100BASE-TX with HP Auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables, and LINKMD® TDR-based cable diagnostics for identification of faulty cabling.

The high-performance switching engine features an extensive feature set that includes programmable rate limiting, tag/port-based VLAN, 4 priority class, RMII/MII/SNI, and CPU control/data interfaces to effectively address both current and emerging Fast Ethernet applications.

The KSZ8893FQL comes in a lead-free package.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 128-PIN PQFP ASSIGNMENT, (TOP VIEW)

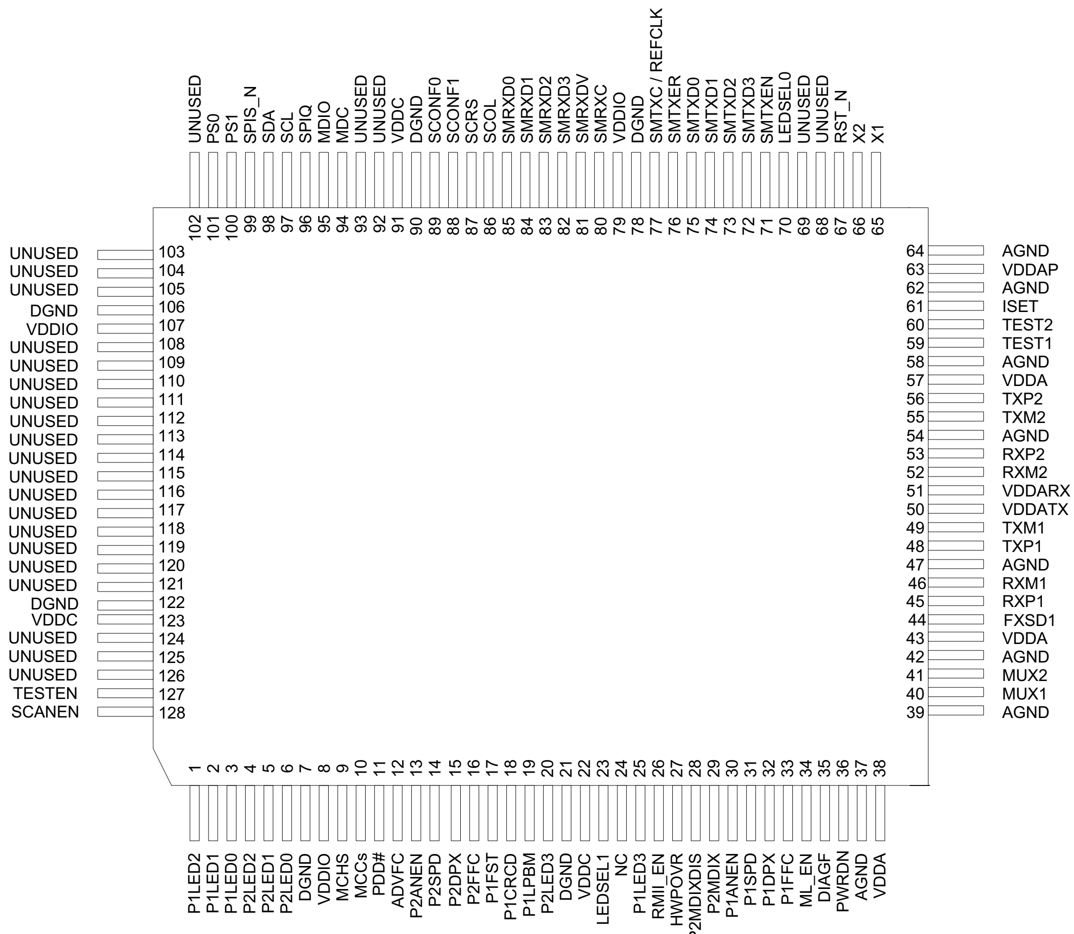


TABLE 2-1: SIGNALS

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th colspan="3">Description</th></tr>
<tr><td rowspan="7">1</td><td rowspan="7">P1LED2</td><td rowspan="7">IPU/O</td><td colspan="3">Port 1 LED indicators (active-low)
(applies to all modes of operation, except Repeater Mode)</td></tr>
<tr><td rowspan="2">—</td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td>[0,0] Default</td><td>[0,1]</td></tr>
<tr><td>P1LED3</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link/Activity</td><td>100Link/Activity</td></tr>
<tr><td>P1LED1</td><td>Full-Duplex/Col</td><td>10Link/Activity</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>Full-Duplex</td></tr>
<tr><td rowspan="8">2</td><td rowspan="8">P1LED1</td><td rowspan="8">IPU/O</td><td colspan="3">—</td></tr>
<tr><td rowspan="2">—</td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td>[1,0]</td><td>[1,1]</td></tr>
<tr><td>P1LED3</td><td>Activity</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1</td><td>Full-Duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>—</td></tr>
<tr><td colspan="3">Link/Act, 100Link/Activity, 10Link/Activity:
Low (link), High (no link), Toggle (transmit/receive activity)
Full-Duplex/Col:
Low (full-duplex), High (half-duplex), Toggles (collision)
Speed:
Low (100BASE-TX), High (10BASE-T)
Full-Duplex:
Low (full-duplex), High (half-duplex)
Activity:
Toggles (transmit/receive activity)
Link:
Low (link), High (no link)

Repeater Mode (only)</td></tr>
</table>

TABLE 2-1: SIGNALS (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th colspan="3">Description</th></tr>
<tr><td rowspan="7">3</td><td rowspan="7">P1LED0</td><td rowspan="7">IPU/O</td><td rowspan="2">—</td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td colspan="2">[0,0]</td></tr>
<tr><td>P1LED3</td><td colspan="2">RPT_COL</td></tr>
<tr><td>P1LED2</td><td colspan="2">RPT_LINK3/RX</td></tr>
<tr><td>P1LED1</td><td colspan="2">RPT_LINK2/RX</td></tr>
<tr><td>P1LED0</td><td colspan="2">RPT_LINK1/RX</td></tr>
<tr><td colspan="3">RPT_COL:
Low (collision)
RPT_LINK#/RX (# = port):
Low (link), High (no link), Toggles (receive activity)
Notes:
LEDSEL0 is external strap-in pin 70.
LEDSEL1 is external strap-in pin 23.
P1LED3 is pin 25.
During reset, P1LED[2:0] are inputs for internal testing.</td></tr>
<tr><td rowspan="7">4</td><td rowspan="7">P2LED2</td><td rowspan="7">IPU/O</td><td colspan="3">Port 2 LED indicators (active-low)
(applies to all modes of operation, except Repeater Mode)</td></tr>
<tr><td rowspan="2">—</td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td>[0,0] Default</td><td>[0,1]</td></tr>
<tr><td>P2LED3</td><td>—</td><td>—</td></tr>
<tr><td>P2LED2</td><td>Link/Activity</td><td>100Link/Activity</td></tr>
<tr><td>P2LED1</td><td>Full-Duplex/Col</td><td>10Link/Activity</td></tr>
<tr><td>P2LED0</td><td>Speed</td><td>Full-Duplex</td></tr>
</table>

TABLE 2-1: SIGNALS (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th colspan="3">Description</th></tr>
<tr><td rowspan="8">5</td><td rowspan="8">P2LED1</td><td rowspan="8">IPU/O</td><td colspan="3">—</td></tr>
<tr><td rowspan="2">—</td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td>[1,0]</td><td>[1,1]</td></tr>
<tr><td>P2LED3</td><td>Activity</td><td>—</td></tr>
<tr><td>P2LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P2LED1</td><td>Full-Duplex/Col</td><td>—</td></tr>
<tr><td>P2LED0</td><td>Speed</td><td>—</td></tr>
<tr><td colspan="3">Link/Act, 100Link/Activity, 10Link/Activity:
Low (link), High (no link), Toggle (transmit/receive activity)
Full-Duplex/Col:
Low (full-duplex), High (half-duplex), Toggles (collision)
Speed:
Low (100BASE-TX), High (10BASE-T)
Full-Duplex:
Low (full-duplex), High (half-duplex)
Activity:
Toggles (transmit/receive activity)
Link:
Low (link), High (no link)

Repeater Mode (only)</td></tr>
<tr><td rowspan="7">6</td><td rowspan="7">P2LED0</td><td rowspan="7">IPU/O</td><td rowspan="2">—</td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td colspan="2">[0,0]</td></tr>
<tr><td>P2LED3</td><td colspan="2">RPT_COL</td></tr>
<tr><td>P2LED2</td><td colspan="2">RPT_LINK3/RX</td></tr>
<tr><td>P2LED1</td><td colspan="2">RPT_LINK2/RX</td></tr>
<tr><td>P2LED0</td><td colspan="2">RPT_LINK1/RX</td></tr>
<tr><td colspan="3">RPT_COL:
Low (collision)
RPT_LINK#/RX (# = port):
Low (link), High (no link), Toggles (receive activity)
Notes:
LEDSEL0 is external strap-in pin 70.
LEDSEL1 is external strap-in pin 23.
P2LED3 is pin 25.
During reset, P2LED[2:0] are inputs for internal testing.</td></tr>
<tr><td>7</td><td>DGND</td><td>GND</td><td colspan="3">Digital ground.</td></tr>
<tr><td>8</td><td>VDDIO</td><td>P</td><td colspan="3">3.3V digital V_{DD}</td></tr>
</table>

TABLE 2-1: SIGNALS (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th colspan="2">Description</th></tr>
<tr><td rowspan="3">9</td><td rowspan="3">MCHS</td><td rowspan="3">IPD</td><td colspan="2">KSZ8893FQL operating modes (defined below):</td></tr>
<tr><td>(MCHS, MCCS)</td><td>Description</td></tr>
<tr><td>(0, 0)</td><td>Normal 3 port switch mode (3 MAC + 2 PHY)
MC mode is disabled.
Port 1 is either Fiber or UTP.
Port 2 is UTP.
Port 3 (MII) is enabled.</td></tr>
<tr><td rowspan="3">10</td><td rowspan="3">MCCS</td><td rowspan="3">IPD</td><td>(0, 1)</td><td>Center MC mode (3 MAC + 2 PHY)
MC mode is enabled.
Port 1 is Fiber and has Center MC enabled.
Port 2 is UTP.
Port 3 (MII) is enabled.</td></tr>
<tr><td>(1, 0)</td><td>Terminal MC mode (2 MAC + 2 PHY)
MC mode is enabled.
Port 1 is Fiber and has Terminal MC enabled.
Port 2 is UTP.
Port 3 (MII) is disabled.</td></tr>
<tr><td>(1, 1)</td><td>Terminal MC mode (3 MAC + 2 PHY)
MC mode is enabled.
Port 1 Fiber and has Terminal MC enabled.
Port 2 is UTP.
Port 3 (MII) is enabled.</td></tr>
<tr><td>11</td><td>PDD#</td><td>IPU</td><td colspan="2">Power Down Detect
1 = Normal operation.
0 = Power down detected.

In Terminal MC mode (pin MCHS is ‘1’), a high to low transition to this pin will cause port 1 (fiber) to generate and send out an “Indicate Terminal MC Condition” OAM frame with the S0 status bit set to ‘1’.</td></tr>
<tr><td>12</td><td>ADVFC</td><td>IPU</td><td colspan="2">1 = Advertise the switch’s flow control capability via auto-negotiation.
0 = Will not advertise the switch’s flow control capability via auto-negotiation.</td></tr>
<tr><td>13</td><td>P2ANEN</td><td>IPU</td><td colspan="2">1 = Enable auto-negotiation on port 2.
0 = Disable auto-negotiation on port 2.</td></tr>
<tr><td>14</td><td>P2SPD</td><td>IPD</td><td colspan="2">1 = Force port 2 to 100BT if P2ANEN = 0.
0 = Force port 2 to 10BT if P2ANEN = 0.</td></tr>
<tr><td>15</td><td>P2DPX</td><td>IPD</td><td colspan="2">1 = Port 2 default to full duplex mode if P2ANEN = 1 and auto-negotiation fails. Force port 2 in full duplex mode if P2ANEN = 0.
0 = Port 2 default to half duplex mode if P2ANEN = 1 and auto-negotiation fails. Force port 2 in half duplex mode if P2ANEN = 0.</td></tr>
<tr><td>16</td><td>P2FFC</td><td>IPD</td><td colspan="2">1 = Always enable (force) port 2 flow control feature.
0 = Port 2 flow control feature enable is determine by the auto-negotiation result.</td></tr>
<tr><td>17</td><td>P1FST</td><td>OPU</td><td colspan="2">1 = Normal function.
0 = MC in loopback mode or MC abnormal conditions occur.</td></tr>
</table>

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
18	P1LCRCD	IPD	In MC loopback mode, 1 = Drop OAM frames and Ethernet frames with the following errors – CRS, undersize, oversize. Loopback Ethernet frames with only good CRC and valid length. 0 = Drop OAM frames only. Loopback all Ethernet frames including those with errors.
19	P1LPBM	IPD	1 = Perform MC loopback at PHY of port 1. 0 = Perform MC loopback at MAC of port 2
20	P2LED3	OPD	Port 2 LED indicator Note: An external 1 kΩ pull-down is needed on this pin if it is connected to an LED. The 1 kΩ resistor will not turn ON the LED. See description in pin 4.
21	DGND	GND	Digital ground.
22	VDDC/ VOUT_1V2	P	1.2V digital V_{DD} Provides V_{OUT_1V2} to KSZ8893FQL's input power pins: VDDAP (pin 63), VDDC (pins 91 and 123), and VDDA (pins 38, 43, and 57). It is recommended the pin should be connected to 3.3V power rail by a 100Ω resistor for the internal LDO application.
23	LEDSEL1	IPD	LED display mode select. See description in pins 1 and 4.
24	NC	O	No connect
25	P1LED3	OPD	Port 1 LED indicator Note: An external 1 kΩ pull-down is needed on this pin if it is connected to an LED. The 1 kΩ resistor will not turn ON the LED. See description in pin 1.
26	RMII_EN	OPD	Strap pin for RMII Mode 1 = Enable 0 = Disable After reset, this pin has no meaning and is a no connect.
27	HWPOVR	IPD	Hardware pin overwrite 1 = Enable: All strap-in pin configurations are overwritten by the EEPROM configuration data, except for P2ANEN (pin 13), P2SPD (pin 14), P2DPX (pin 15) and ML_EN (pin 34). After reset, the pin state for P2ANEN, P2SPD and P2DPX is polled by the KSZ8893FQL. 0 = Disable: All strap-in pin configurations are overwritten by the EEPROM configuration data.
28	P2MDIXDIS	IPD	Port 2 Auto MDI/MDI-X PD (default) = enable PU = disable
29	P2MDIX	IPD	Port 2 MDI/MDI-X setting when auto MDI/MDI-X is disabled. PD (default) = MDI-X (transmit on TXP2/TXM2 pins) PU = MDI, (transmit on RXP2/RXM2 pins)
30	P1ANEN	IPU	1 = Enable auto-negotiation on port 1 0 = Disable auto-negotiation on port 1

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
31	P1SPD	IPD	1 = Force port 1 to 100BT if P1ANEN = 0 0 = Force port 1 to 10BT if P1ANEN = 0
32	P1DPX	IPD	1 = Port 1 default to full-duplex mode if P1ANEN = 1 and auto-negotiation fails. Force port 1 in full-duplex mode if P1ANEN = 0. 0 = Port 1 default to half-duplex mode if P1ANEN = 1 and auto-negotiation fails. Force port 1 in half-duplex mode if P1ANEN = 0.
33	P1FFC	IPD	1 = Always enable (force) port 1 flow control feature 0 = Port 1 flow control feature enable is determined by auto-negotiation result.
34	ML_EN	IPD	1 = Enable missing link 0 = Disable missing link
35	DIAGF	IPD	1 = Diagnostic fail 0 = Diagnostic normal
36	PWRDN	IPU	Chip power down input (active-low) 1 = Normal operation 0 = The chip is powered down
37	AGND	GND	Analog ground
38	VDDA	P	1.2V analog V_{DD}
39	AGND	GND	Analog ground
40	MUX1	I	No connect
41	MUX2	I	10BASE-FL/100BASE-SX Enable. Active-low.
42	AGND	GND	Analog ground
43	VDDA	P	1.2V analog V_{DD}
44	FXSD1	I	Fiber signal detect/factory test pin
45	RXP1	I/O	Physical receive or transmit signal (+ differential)
46	RXM1	I/O	Physical receive or transmit signal (– differential)
47	AGND	GND	Analog ground
48	TXP1	I/O	Physical transmit or receive signal (+ differential)
49	TXM1	I/O	Physical transmit or receive signal (– differential)
50	VDDATX	P	3.3V analog V_{DD}
51	VDDARX	P	3.3V analog V_{DD}
52	RXM2	I/O	Physical receive or transmit signal (– differential)
53	RXP2	I/O	Physical receive or transmit signal (+ differential)
54	AGND	GND	Analog ground
55	TXM2	I/O	Physical transmit or receive signal (– differential)
56	TXP2	I/O	Physical transmit or receive signal (+ differential)

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
57	VDDA	P	1.2 analog V_{DD}
58	AGND	GND	Analog ground
59	TEST1	I	Factory test pin – float for normal operation
60	TEST2	I	Factory test pin – float for normal operation
61	ISET	O	Set physical transmit output current Pull-down this pin with a 3.01 kΩ 1% resistor to ground.
62	AGND	GND	Analog ground
63	VDDAP	P	1.2V analog V_{DD} for PLL
64	AGND	GND	Analog ground
65	X1	I	25 MHz crystal/oscillator clock connections Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is no connected. Note: Clock is ±50 ppm for both crystal and oscillator.
66	X2	O	
67	RST_N	IPU	Hardware Reset (active-low)
68	UNUSED	I	Unused pin – externally pull down for normal operation
69	UNUSED	I	Unused pin – externally pull down for normal operation
70	LEDSEL0	I	LED display mode select See description in pins 1 and 4.
71	SMTXEN	I	Switch MII transmit enable
72	SMTXD3	I	Switch MII transmit data bit 3
73	SMTXD2	I	Switch MII transmit data bit 2
74	SMTXD1	I	Switch MII transmit data bit 1
75	SMTXD0	I	Switch MII transmit data bit 0
76	SMTXER	I	Switch MII transmit error
77	SMTXC/ REFCLK	I/O	Switch MII transmit clock (MII and SNI modes only) Output in PHY MII mode and SNI mode Input in MAC MII mode Reference Clock (RMII mode only) Input for 50 MHz ±50 ppm system clock Note: In RMII mode, pin X1 is pulled up to VDDIO supply with a 10 kΩ resistor and pin X2 is a no connect.
78	DGND	GND	Digital ground
79	VDDIO	P	3.3V digital V_{DD}
80	SMRXC	I/O	Switch MII receive clock. Output in PHY MII mode Input in MAC MII mode

TABLE 2-1: SIGNALS (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th colspan="2">Description</th></tr>
<tr><td>81</td><td>SMRXDV</td><td>O</td><td colspan="2">Switch MII receive data valid I/O</td></tr>
<tr><td>82</td><td>SMRXD3</td><td>IPD/O</td><td colspan="2">Switch MII receive data bit 3
Strap option: switch MII full-duplex flow control
PD (default) = disable
PU = enable</td></tr>
<tr><td>83</td><td>SMRXD2</td><td>IPD/O</td><td colspan="2">Switch MII receive data bit 2
Strap option: switch MII is in
PD (default) = full-duplex mode
PU = half-duplex mode</td></tr>
<tr><td>84</td><td>SMRXD1</td><td>IPD/O</td><td colspan="2">Switch MII receive data bit 1
Strap option: Switch MII is in
PD (default) = 100 Mbps mode
PU = 10 Mbps mode</td></tr>
<tr><td>85</td><td>SMRXD0</td><td>I/O</td><td colspan="2">Switch MII receive data bit 0
Strap option: switch will accept packet size up to
PD = 1536 bytes (inclusive)
PU = 1522 bytes (tagged), 1518 bytes (untagged)</td></tr>
<tr><td>86</td><td>SCOL</td><td>I/O</td><td colspan="2">Switch MII collision detect</td></tr>
<tr><td>87</td><td>SCRS</td><td>I/O</td><td colspan="2">Switch MII carrier sense</td></tr>
<tr><td rowspan="3">88</td><td rowspan="3">SCONF1</td><td rowspan="6">I</td><td colspan="2">Switch MII interface configuration</td></tr>
<tr><td>(SCONF1, SCONF0)</td><td>Description</td></tr>
<tr><td>(0,0)</td><td>Disable, outputs tri-stated</td></tr>
<tr><td rowspan="3">89</td><td rowspan="3">SCONF0</td><td>(0,1)</td><td>PHY mode MII</td></tr>
<tr><td>(1,0)</td><td>MAC mode MII</td></tr>
<tr><td>(1,1)</td><td>PHY mode SNI</td></tr>
<tr><td>90</td><td>DGND</td><td>GND</td><td colspan="2">Digital core ground</td></tr>
<tr><td>91</td><td>VDDC</td><td>P</td><td colspan="2">1.2V digital V_{DD}</td></tr>
<tr><td>92</td><td>UNUSED</td><td>I</td><td colspan="2">Unused pin - externally pull down for normal operation</td></tr>
<tr><td>93</td><td>UNUSED</td><td>I</td><td colspan="2">Unused pin - externally pull down for normal operation</td></tr>
<tr><td>94</td><td>MDC</td><td>I</td><td colspan="2">MII management interface: clock input</td></tr>
<tr><td>95</td><td>MDIO</td><td>I/O</td><td colspan="2">MII management interface: data input/output
Note: an external pull-up is needed on this pin when it is in use</td></tr>
<tr><td>96</td><td>SPIQ</td><td>O</td><td colspan="2">SPI slave mode: serial data output
See description in pins 100 and 101
Note: an external pull-up is needed on this pin when it is in use</td></tr>
<tr><td>97</td><td>SCL</td><td>I/O</td><td colspan="2">SPI slave mode/ I^2C slave mode: clock input
I^2C master/slave mode: clock output
See description in pins 100 and 101</td></tr>
</table>

TABLE 2-1: SIGNALS (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th colspan="3">Description</th></tr>
<tr><td>98</td><td>SDA</td><td>I/O</td><td colspan="3">SPI slave mode: serial data input
I2C master/slave mode: serial data input/output
See description in pins 100 and 101
Note: an external pull-up is needed on this pin when it is in use</td></tr>
<tr><td>99</td><td>SPIS_N</td><td>I</td><td colspan="3">SPI slave mode: chip select (active low)
When SPIS _N is high, the KSZ8893FQL is deselected and SPIQ is held in high impedance state
A high-to-low transition is used to initiate SPI data transfer
See description in pins 100 and 101
Note: an external pull-up is needed on this pin when it is in use</td></tr>
<tr><td rowspan="10">100</td><td rowspan="10">PS1</td><td rowspan="10">I</td><td colspan="3">Serial bus configuration pins to select mode of access to KSZ8893FQL internal registers.
[PS1, PS0] = [0, 0] — I^2C master (EEPROM) mode
(If EEPROM is not detected, the KSZ8893FQL will be configured with the default values of its internal registers and the values of its strap-in pins.)</td></tr>
<tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr>
<tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr>
<tr><td>SCL</td><td>O</td><td>I^2C clock</td></tr>
<tr><td>SDA</td><td>I/O</td><td>I^2C data I/O</td></tr>
<tr><td>SPIS_N</td><td>I</td><td>Not used</td></tr>
<tr><td colspan="3">**[PS1, PS0] = [0, 1] — I^2C slave mode**
The external I^2C master will drive the SCL clock.
The KSZ8893FQL device addresses are:
1011_1111 <read>
1011_1110 <write></td></tr>
<tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr>
<tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr>
</table>

TABLE 2-1: SIGNALS (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th colspan="3">Description</th></tr>
<tr><td rowspan="12">101</td><td rowspan="12">PS0</td><td rowspan="12">I</td><td>SCL</td><td>I</td><td>I^2C clock</td></tr>
<tr><td>SDA</td><td>I/O</td><td>I^2C data I/O</td></tr>
<tr><td>SPIS_N</td><td>I</td><td>Not used</td></tr>
<tr><td colspan="3">[PS1, PS0] = [1, 0] — SPI slave mode</td></tr>
<tr><td>Interface Signals</td><td>Type</td><td>Description</td></tr>
<tr><td>SPIQ</td><td>O</td><td>SPI data out</td></tr>
<tr><td>SCL</td><td>I</td><td>SPI clock</td></tr>
<tr><td>SDA</td><td>I</td><td>SPI data in</td></tr>
<tr><td>SPIS_N</td><td>I</td><td>SPI chip select</td></tr>
<tr><td colspan="3">[PS1, PS0] = [1, 1] – SMI-mode
In this mode, the KSZ8893FQL provides access to all its internal 8-bit registers through its MDC and MDIO pins.
Note:
When (PS1, PS0) does not equal (1,1), the KSZ8893FQL provides access to its 16-bit MIIM registers through its MDC and MDIO pins.</td></tr>
<tr style="display:none"><td colspan="3"></td></tr>
<tr style="display:none"><td colspan="3"></td></tr>
<tr><td>102</td><td>UNUSED</td><td>I</td><td colspan="3">Unused pin – externally pull up for normal operation</td></tr>
<tr><td>103</td><td>UNUSED</td><td>I</td><td colspan="3">Unused pin – externally pull up for normal operation</td></tr>
<tr><td>104</td><td>UNUSED</td><td>I</td><td colspan="3">Unused pin – externally pull up for normal operation</td></tr>
<tr><td>105</td><td>UNUSED</td><td>I</td><td colspan="3">Unused pin – externally pull up for normal operation</td></tr>
<tr><td>106</td><td>DGND</td><td>GND</td><td colspan="3">Digital ground</td></tr>
<tr><td>107</td><td>VDDIO</td><td>P</td><td colspan="3">3.3V digital V_{DD}</td></tr>
<tr><td>108</td><td>UNUSED</td><td>I</td><td colspan="3">Unused pin – externally pull up for normal operation</td></tr>
<tr><td>109</td><td>UNUSED</td><td>I</td><td colspan="3">Unused pin – externally pull up for normal operation</td></tr>
<tr><td>110</td><td>UNUSED</td><td>I</td><td colspan="3">Unused pin – externally pull down for normal operation</td></tr>
<tr><td>111</td><td>UNUSED</td><td>I</td><td colspan="3">Unused pin – externally pull down for normal operation</td></tr>
<tr><td>112</td><td>UNUSED</td><td>I</td><td colspan="3">Unused pin – externally pull down for normal operation</td></tr>
<tr><td>113</td><td>UNUSED</td><td>I</td><td colspan="3">Unused pin – externally pull down for normal operation</td></tr>
<tr><td>114</td><td>UNUSED</td><td>I</td><td colspan="3">Unused pin – externally pull down for normal operation</td></tr>
<tr><td>115</td><td>UNUSED</td><td>I</td><td colspan="3">Unused pin – externally pull down for normal operation</td></tr>
<tr><td>116</td><td>UNUSED</td><td>I</td><td colspan="3">Unused pin – externally pull down for normal operation</td></tr>
<tr><td>117</td><td>UNUSED</td><td>I</td><td colspan="3">Unused pin – externally pull down for normal operation</td></tr>
<tr><td>118</td><td>UNUSED</td><td>I</td><td colspan="3">Unused pin – externally pull down for normal operation</td></tr>
<tr><td>119</td><td>UNUSED</td><td>I</td><td colspan="3">Unused pin – externally pull down for normal operation</td></tr>
</table>

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
120	UNUSED	I	Unused pin – externally pull down for normal operation
121	UNUSED	I	Unused pin – externally pull up for normal operation
122	DGND	GND	Digital ground
123	VDDC	P	1.2V digital V_{DD}
124	UNUSED	I	Unused pin – externally pull down for normal operation
125	UNUSED	I	Unused pin – externally pull down for normal operation
126	UNUSED	I	Unused pin – externally pull down for normal operation
127	TESTEN	IPD	Scan Test Enable For normal operation, pull down this pin to ground.
128	SCANEN	IPD	Scan Test Scan Mux Enable For normal operation, pull down this pin to ground.

Note 2-1 P = power supply; GND = ground; I = input; O = output
I/O = bi-directional
Ipu/O = Input with internal pull-up during reset; output pin otherwise.
Ipu = Input with internal pull-up.
Ipd = Input with internal pull-down.
Opu = Output with internal pull-up.
Opd = Output with internal pull-down.
Speed: Low (100BASE-TX), High (10BASE-T)
Full-Duplex: Low (full-duplex), High (half-duplex)
Activity: Toggle (transmit/receive activity)
Link: Low (link), High (no link)

3.0 FUNCTIONAL DESCRIPTION

The KSZ8893FQL is a single-chip Fast Ethernet media converter. It contains two 10/100 physical layer transceivers and three Media Access Control (MAC) units with an integrated Layer 2 managed switch.

On the media side, the KSZ8893FQL supports IEEE 802.3 10BASE-T and 100BASE-TX on both PHY ports. In Media Converter (MC) applications, PHY port 1 is the fiber port and supports 100BASE-FX, 100BASE-SX, and 10BASE-FL.

The KSZ8893FQL has the flexibility to reside in either a managed or unmanaged design. In a managed design, the host processor has complete control of the KSZ8893FQL via the SMI interface, MIIM interface, SPI bus, or I^2C bus. An unmanaged design is achieved through I/O strapping and/or EEPROM programming at system reset time.

Physical signal transmission and reception are enhanced through the use of patented analog circuitries that make the design more efficient and allow for lower power consumption and smaller chip die size.

3.1 Media Conversion

3.1.1 TS-1000 OAM OPERATION

The KSZ8893FQL implements Japan’s TTC (Telecommunication Technology Committee) TS-1000 version 2, OAM sub-layer, which resides between RS and PCS layer in the IEEE 802.3 Standard. The OAM sub-layer is provided in 100BASE-FX mode and is used by the KSZ8893FQL to send and receive OAM frames. These special frames are used for the transmission of OAM (Operations, Administration, Management) information between center MC and terminal MC. Key TS-1000 OAM features include:

- Private point-to-point communication between two TS-1000 compliant devices
- 96 bits (12 bytes) frames for the transmission of OAM information between center MC and terminal MC
- Transmission of MC status between center MC and terminal MC
- Automatic generation of OAM frame to inform MC link partner of local MC’s status change
- Transmission of vendor code and model number information between center MC and terminal MC for device identification
- Inquisition of terminal MC status by center MC
- Remote loop back for diagnostic by center MC

3.1.1.1 OAM Frame Format

The TS-1000 OAM (Operations, Administration, and Management) Frame Format is shown in Table 3-1.

TABLE 3-1: TS-1000 OAM FRAME FORMAT

Bit	Command	Description
F0 - F7	Preamble	1010 1010
C0	Conservation Delimiter	0
C1	Direction Delimiter	0 = Upstream (from terminal MC to center MC) 1 = Downstream (from center MC to terminal MC)
C2 - C3	Configuration Delimiter	10 = Request 11 = Response 01 = Indication 00 = Reserved
C4 - C7	Version	0000
C8 - C15	Control Signal	1000 0000 = Start loopback test 0000 0000 = Stop loopback test 0100 0000 = Notify status

TABLE 3-1: TS-1000 OAM FRAME FORMAT (CONTINUED)

Bit		Command	Description
S0	Status	Power	0 = Normal operation 1 = Power down
S1		Optical	0 = Normal 1 = Abnormal
S2		UTP Link	0 = Link up 1 = Link down
S3		MC	0 = Normal 1 = Brake
S4		Way for Information	0 = Use conservation frame 1 = Use FEFI
S5		Loop Mode	0 = Normal operation 1 = In loop mode
S6		Terminal MC Link Option	0 = Center side MC have to set always “0” 1 = Terminal side MC have to set always “1”
S7		Terminal MC Link Speed 1	This bit must be set “0”
S8		Terminal MC Link Speed 2	0 = 10 Mbps 1 = 100 Mbps These bits have to be set “0”, if S2 is “1” (Center side MC have to set always “0”)
S9		Terminal MC Link Duplex	0 = Half-Duplex 1 = Full-Duplex This bit have to be set “0”, if S2 is “1” (Center side MC have to set always “0”)
S10		Terminal MC Auto-Negotiation Capability	0 = Not Support Auto-Negotiation 1 = Support Auto-Negotiation (Center side MC have to set always “0”)
S11		Multiple Link Partner	0 = One link partner on UTP side 1 = Multiple link partner on UTP side
S12 - S15		Reserved	All bits must be set “0”
M0 - M23		Vendor Code	—
M24 - M47		Model Number	—
E0 - E7		FCS	Create FCS at this sub-layer (C0 - M47)

3.1.1.2 Media Converter Modes

TS-1000 Media Converter (MC) modes are selected and configured using hardware pins: MCHS and MCCS. The MC modes are summarized in Table 3-2 and are also shown in the Pin Description and Configuration section.

TABLE 3-2: TS-1000 MEDIA CONVERTER MODE SELECTION

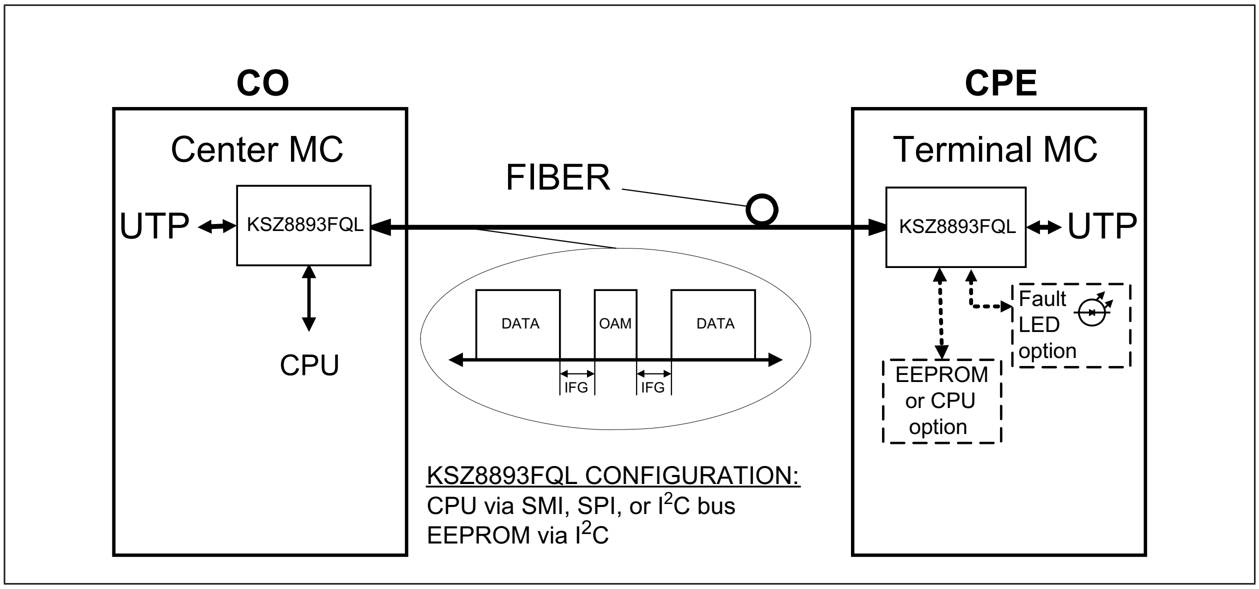
(MCHS, MCCS)	Description
(0, 0)	Normal 3 port switch mode (3 MAC + 2 PHY) MC mode is disabled. Port 1 is either Fiber or UTP. Port 2 is UTP. Port 3 (MII) is enabled.
(0, 1)	Center MC mode (3 MAC + 2 PHY) MC mode is enabled. Port 1 is Fiber & has Center MC enabled. Port 2 is UTP. Port 3 (MII) is enabled.

TABLE 3-2: TS-1000 MEDIA CONVERTER MODE SELECTION (CONTINUED)

(MCHS, MCCS)	Description
(1, 0)	Terminal MC mode (2 MAC + 2 PHY) MC mode is enabled. Port 1 is Fiber & has Terminal MC enabled. Port 2 is UTP. Port 3 (MII) is disabled.
(1, 1)	Terminal MC mode (3 MAC + 2 PHY) MC mode is enabled. Port 1 is Fiber & has Terminal MC enabled. Port 2 is UTP. Port 3 (MII) is enabled.

Figure 3-1 shows two KSZ8893FQLs connected in a typical center MC to terminal MC application.

FIGURE 3-1: TYPICAL TS-1000 MEDIA CONVERTER APPLICATION



3.1.1.3 MC Loopback Operation

TS-1000 MC loopback operation is initiated and enabled by the center MC. The terminal MC provides the loopback path to return the loopback packet back to the center MC. The KSZ8893FQL in terminal MC mode provides three loopback path options:

Port 1 OPT

- Receive loopback packet from center MC at RXP1/RXM1 input pins of port 1 (fiber).
- Turn around loopback packet at PMD/PMA of port 1 (fiber).
- Transmit loopback packet back to center MC from TXP1/TXM1 output pins of port 1 (fiber).

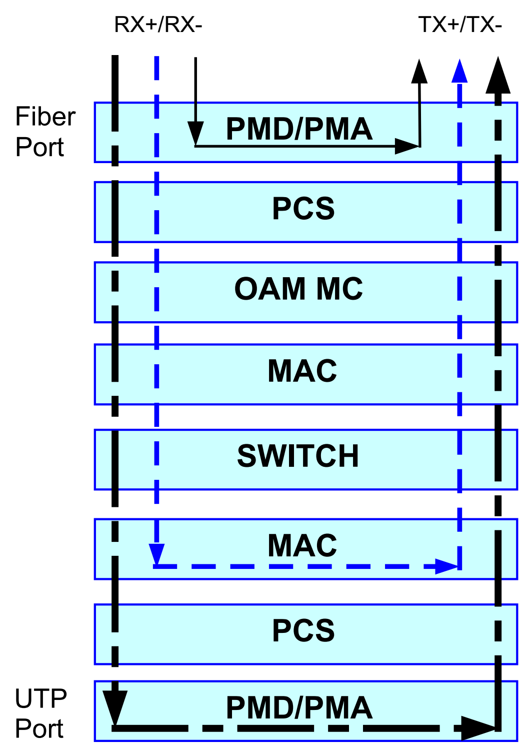
Port 2 MAC

- Receive loopback packet from center MC at RXP1/RXM1 input pins of port 1 (fiber).
- Turn around loopback packet at MAC of port 2 (copper).
- Transmit loopback packet back to center MC from TXP1/TXM1 output pins of port 1 (fiber).

Port 2 UTP

- Receive loopback packet from center MC at RXP1/RXM1 input pins of port 1 (fiber).
- Turn around loopback packet at PMD/PMA of port 2 (copper).
- Transmit loopback packet back to center MC from TXP1/TXM1 output pins of port 1 (fiber).

FIGURE 3-2: KSZ8893FQL MC LOOPBACK PATHS



3.1.1.4 Dedicated TS-1000 Registers and Pins

The KSZ8893FQL provides 32 dedicated registers to support TS-1000 OAM communication in center MC and terminal MC modes. The TS-1000 MC registers are located at 64 to 95 (0x40 to 0x5F), and provide the following functions:

- PHY address configuration
- Center MC and Terminal MC configuration
- OAM frame selection and execution
- MC loopback setup
- MC loopback counters for CRC error, timeout, good packet
- Remote command access
- Counters for valid MC packet transmitted and received
- MC (local) - status, vendor code, and model number
- Link Partner (remote) - status, vendor code, and model number

Table 3-3 lists the dedicated KSZ8893FQL pins used in center MC and terminal MC modes.

TABLE 3-3: DEDICATED TS-1000 PINS

Pin	Signal Name	Type	Description
9	MCHS	IPD	Selects center MC and terminal MC modes. See “Media Converter Modes” section for details.
10	MCCS	IPD	

TABLE 3-3: DEDICATED TS-1000 PINS (CONTINUED)

Pin	Signal Name	Type	Description
11	PDD#	IPU	Power-Down Detect: Used by terminal MC to detect a power-down condition or indicate a failure has occurred. 1 = Normal operation 0 = Power down detected After detecting a high-to-low transition on this pin, the KSZ8893FQL then sends out an “Indicate Terminal MC Condition” OAM frame with the S0 status bit set to ‘1’ to inform the center MC that a power down condition or failure has occurred on the terminal MC side. If this pin is implemented, PWRDN (pin 36) needs to be deasserted (pulled up).
17	P1FST	OPU	Drives low to indicate fault conditions (far-end fault detected, link partner’s fiber or UTP port down), or MC loopback mode. This pin has 8 mA drive and can directly drive a LED.
18	P1CRCD	IPD	Used by terminal MC for MC loopback – strap-in pin to select: 1 = Drop OAM frames and Ethernet frames with the following errors: CRC, undersize, oversize. Loopback Ethernet frames with only good CRC and valid length. 0 = Drop OAM frames only. Loopback all Ethernet frames including those with errors.
19	P1LPBM	IPD	Used by terminal MC for MC loopback – strap-in pin to select: 1 = Perform MC loopback at PHY of port 1 0 = Perform MC loopback at MAC of port 2 See also register 11 (0x0B) bits[3:2].
34	ML_EN	IPD	Used by terminal MC for Missing Link Indication – strap-in pin to select: 1 = Enable Missing Link feature 0 = Disable Missing Link feature
35	DIAGF	IPD	Used by terminal MC for Diagnostic status: 1 = Diagnostic fail 0 = Diagnostic normal After detecting a change of state on this pin, the KSZ8893FQL sends out an “Indicate Terminal MC Condition” OAM frame with the S3 status bit set to the state of this pin to inform the center MC that a diagnostic status change has occurred on the terminal MC side.

3.1.2 10BASE-FL OPERATION

10BASE-FL operation is supported on port 1 of the KSZ8893FQL. It conforms to clause 15 and 18 of the IEEE802.3 Standard for 10BASe-FL fiber operation. Refer to the Standard for details.

In a typical application, the KSZ8893FQL provides media conversion from 10BASE-FL fiber on port 1 to 10BASE-T copper on port 2. Alternatively, port 2 can be substituted with port 3 to directly connect to an external MAC.

3.1.2.1 Physical Interface

For 10BASE-FL operation, port 1 interfaces with an external fiber module to drive 850 nm fiber optic links. The interface connections between the KSZ8893FQL and fiber module are single-ended (common mode). 10BASE-FL signal transmission and reception are done on TXM1 (pin 49) and RXM1 (pin 46), respectively. Refer to Microchip’s reference schematic for recommended interface circuit and termination.

3.1.2.2 Enabling 10BASE-FL Mode

To enable 10BASE-FL mode, tie FXSD1 (pin 44) high to +3.3V and MUX2 (pin 41) low-to-ground. Port 1 should also be configured with auto-negotiation disabled, forced to 10 Mbps for the speed, and set to either half- or full-duplex. Optionally, flow control can be enabled to send out PAUSE frames in full-duplex mode.

The 10BASE-FL settings use the same strapping pins, MIIM registers and port registers as 10BASE-T copper. These settings are summarized in Table 3-4.

TABLE 3-4: 10BASE-FL CONFIGURATION

10BASE-FL Setting	Strapping Pin	MIIM Register	Port Register
Auto-Negotiation (disable only)	P1ANEN (30)	Reg. 0, Bit[12]	Reg. 28, Bit[7]
Speed (10 Mbps only)	P1SPD (31)	Reg. 0, Bit[13]	Reg. 28, Bit[6]
Duplex (half or full)	P1DPX (32)	Reg. 0, Bit[8]	Reg. 28, Bit[5]
Forced Flow Control (option)	P1FFC (33)	—	Reg. 18, Bit[4]

3.1.3 100BASE-SX OPERATION

100BASE-SX operation is supported on port 1 of the KSZ8893FQL. It conforms to the TIA/EIA-785 Standard for 100BASE-SX fiber operation. Refer to the Standard for details.

In a typical application, the KSZ8893FQL provides media conversion from 100BASE-SX fiber on port 1 to 100BASE-TX copper on port 2. Alternatively, port 2 can be substituted with port 3 to directly connect to an external MAC.

3.1.3.1 Physical Interface

For 100BASE-SX operation, port 1 interfaces with an external fiber module to drive 850 nm fiber optic links. The interface connections between the KSZ8893FQL and fiber module are single-ended (common mode). 100BASE-SX signal transmission and reception are done on TXM1 (pin 49) and RXM1 (pin 46), respectively. Refer to Microchip's reference schematic for recommended interface circuit and termination.

3.1.3.2 Enabling 100BASE-SX Mode

To enable 100BASE-SX mode, tie FXSD1 (pin 44) high to +3.3V and MUX2 (pin 41) low-to-ground. Port 1 should also be configured with auto-negotiation disabled, forced to 100 Mbps for the speed, and set to either half- or full-duplex. Optionally, flow control can be enabled to send out PAUSE frames in full-duplex mode.

The 100BASE-SX settings use the same strapping pins, MIIM registers and port registers as 100BASE-TX copper. These settings are summarized in Table 3-5.

TABLE 3-5: 100BASE-SX CONFIGURATION

100BASE-SX Settings	Strapping Pin	MIIM Register	Port Register
Auto-Negotiation (disable only)	P1ANEN (30)	Reg. 0, Bit[12]	Reg. 28, Bit[7]
Speed (100 Mbps only)	P1SPD (31)	Reg. 0, Bit[13]	Reg. 28, Bit[6]
Duplex (half or full)	P1DPX (32)	Reg. 0, Bit[8]	Reg. 28, Bit[5]
Forced Flow Control (option)	P1FFC (33)	—	Reg. 18, Bit[4]

3.2 Physical Layer Transceiver

3.2.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 3.01 kΩ resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

3.2.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

3.2.3 PLL CLOCK SYNTHESIZER

The KSZ8893FQL generates 125 MHz, 31.25 MHz, 25 MHz, and 10 MHz clocks for system timing. Internal clocks are generated from an external 25 MHz crystal or oscillator. In RMII mode, these internal clocks are generated from an external 50 MHz oscillator or system clock.

3.2.4 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, and the receiver then de-scrambles the incoming data stream using the same sequence as at the transmitter.

3.2.5 100BASE-FX OPERATION

100BASE-FX operation is similar to 100BASE-TX operation with the differences being that the scrambler/de-scrambler and MLT3 encoder/decoder are bypassed on transmission and reception. In addition, auto-negotiation is bypassed and auto MDI/MDI-X is disabled.

3.2.6 100BASE-FX SIGNAL DETECTION

In 100BASE-FX operation, FXSD1 (fiber signal detect), input pin 44, is usually connected to the fiber transceiver SD (signal detect) output pin. 100BASE-FX mode is activated when the FXSD1 input pin is greater than 1V. When FXSD1 is between 1V and 1.8V, no fiber signal is detected and a far-end fault (FEF) is generated. When FXSD1 is over 2.2V, the fiber signal is detected.

Alternatively, the designer may choose not to implement the FEF feature. In this case, the FXSD1 input pin is tied high to force 100BASE-FX mode.

100BASE-FX signal detection is summarized in Table 3-6.

TABLE 3-6: FX AND TX MODE SELECTION

FXSD1 Input Voltage	Mode
Less than 0.2V	TX mode
Greater than 1V, but less than 1.8V	FX mode No signal detected Far-end fault generated
Greater than 2.2V	FX mode Signal detected

To ensure proper operation, a resistive voltage divider is recommended to adjust the fiber transceiver SD output voltage swing to match the FXSD1 pin's input voltage threshold.

3.2.7 100BASE-FX FAR-END FAULT

A far-end fault (FEF) occurs when the signal detection is logically false on the receive side of the fiber transceiver. The KSZ8893FQL detects a FEF when its FXSD1 input is between 1V and 1.8V. When a FEF is detected, the KSZ8893FQL signals its fiber link partner that a FEF has occurred by sending 84 1's followed by a zero in the idle period between frames.

By default, FEF is enabled. FEF can be disabled through register setting.

3.2.8 10BASE-T TRANSMIT

The 10BASE-T driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude. The harmonic contents are at least 27 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

3.2.9 10BASE-T RECEIVE

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths to prevent noise at the RXP-or-RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8893FQL decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

3.2.10 FIBER LED DRIVER

The device provides a current mode fiber LED driver. The edge enhanced current mode does not require any output wave shaping. The drive current of the fiber LED driver is programmable through register 138 (0x8A) bit[7:6]. The programmable current values are as follows:

TABLE 3-7: PROGRAMMABLE CURRENT VALUES FOR FIBER LED DRIVER

Reg. 138 (0x8A) bit[7:6]	Current Value
00	60 mA
01	80 mA
10	90 mA
11	40 mA

3.2.11 POST AMPLIFIER

The KSZ8893FQL also includes a post amplifier. The post amplifier is intended for interfacing the output of the pre-amplifier of the PIN diode module. The minimum sensitivity of the post amplifier is 2.5 mV_{RMS}.

3.2.12 POWER MANAGEMENT

The KSZ8893FQL features a per-port power down mode. To save power, a PHY port that is not in use can be powered down via port control register or via MIIM PHY register.

In addition, there is a full chip power down mode. When activated, the entire chip is powered down.

3.2.13 MDI/MDI-X AUTO CROSSOVER

To eliminate the need for crossover cables between similar devices, the KSZ8893FQL offers HP Auto MDI/MDI-X and Microchip Auto MDI/MDI-X crossover. HP Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns transmit and receive pairs for the KSZ8893FQL device. This feature is extremely useful when end users are unaware of cable types, and also, saves on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers, or MIIM PHY registers.

The IEEE 802.3u standard MDI and MDI-X definitions are illustrated in Table 3-8.

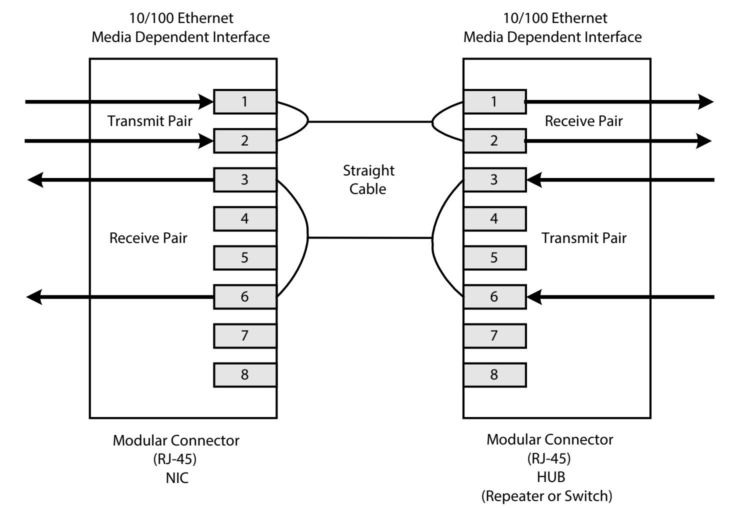
TABLE 3-8: MDI/MDI-X PIN DEFINITIONS

MDI		MDI-X	
RJ-45 Pins	Signals	RJ-45 Pins	Signals
1	TD+	1	RD+
2	TD–	2	RD–
3	RD+	3	TD+
6	RD–	6	TD–

3.2.13.1 Straight Cable

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 3-3 depicts a typical straight cable connection between a NIC card (MDI) and a switch or hub (MDI-X).

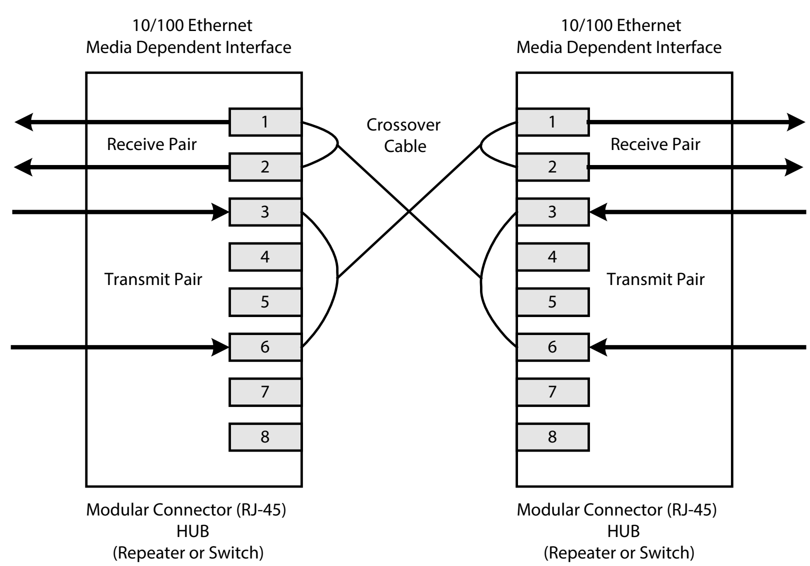
FIGURE 3-3: TYPICAL STRAIGHT CABLE CONNECTION



3.2.13.2 Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 3-4 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

FIGURE 3-4: TYPICAL CROSSOVER CABLE CONNECTION



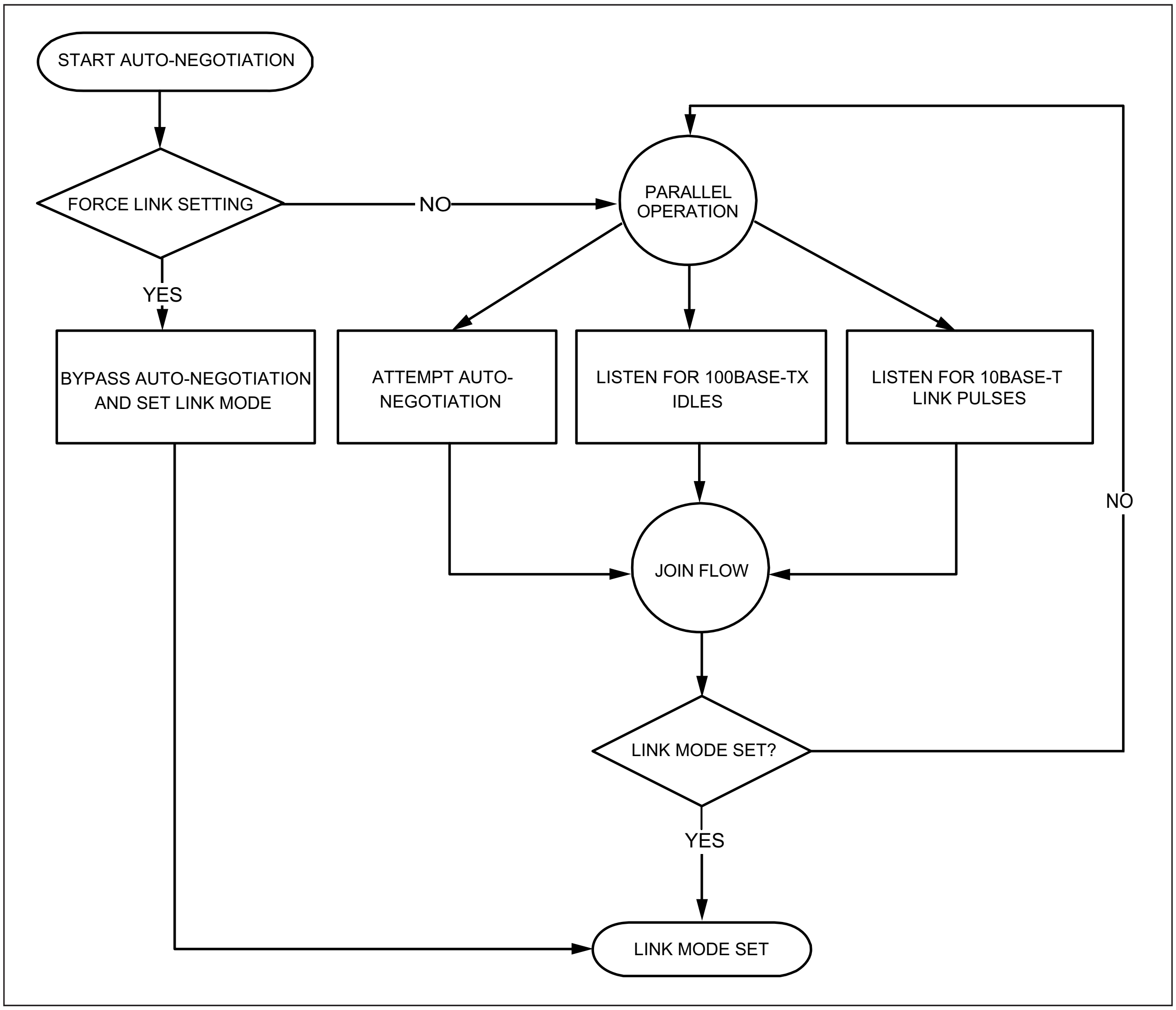
3.2.14 AUTO-NEGOTIATION

The KSZ8893FQL conforms to the auto-negotiation protocol, as defined in Clause 28 of the IEEE 802.3u specification.

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto-negotiation, link partners advertise their capabilities across the link to each other. If auto-negotiation is not supported or the KSZ8893FQL link partner is forced to bypass auto-negotiation, then the KSZ8893FQL sets its operating mode by observing the signal at its receiver. This is known as parallel detection and allows the KSZ8893FQL to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol.

The link up process is shown in Figure 3-5.

FIGURE 3-5: AUTO-NEGOTIATION AND PARALLEL OPERATION



3.2.15 LINKMD® CABLE DIAGNOSTICS

The LINKMD® feature utilizes time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits, and impedance mismatches.

LINKMD works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with maximum distance of 200m and accuracy of ±2m. Internal circuitry displays the TDR information in a user-readable digital format.

Note that cable diagnostics are only valid for copper connections and do not support fiber optic operation.

3.2.15.1 Access

LINKMD is initiated by accessing registers {26,27} and {42,43}, the LINKMD Control/Status registers, for ports 1 and 2, respectively; and in conjunction with registers 29 and 45, Port Control Register 13, for ports 1 and 2, respectively.

Alternatively, the MIIM PHY registers 0 and 29 can be used for LINKMD access.

3.2.15.2 Usage

The following is a sample procedure for using LINKMD with registers {26,27,29} on port 1.

1. Disable auto MDI/MDI-X by writing a ‘1’ to register 29, bit [2] to enable manual control over the differential pair used to transmit the LINKMD pulse.
2. Start cable diagnostic test by writing a ‘1’ to register 26, bit [4]. This enable bit is self-clearing.
3. Wait (poll) for register 26, bit [4] to return a ‘0’, indicating cable diagnostic test is complete.
4. Read cable diagnostic test results in register 26, bits [6:5]. The results are as follows:

    00 = normal condition (valid test)

    01 = open condition detected in cable (valid test)

    10 = short condition detected in cable (valid test)

    11 = cable diagnostic test failed (invalid test)

The ‘11’ case, invalid test, occurs when the KSZ8893FQL is unable to shut down the link partner. In this instance, the test is not run, because it would be impossible for the KSZ8893FQL to determine if the detected signal is a reflection of the signal generated or a signal from another source.

5. Get distance to fault by concatenating register 26, bit [0] and register 27, bits [7:0]; and multiplying the result by a constant of 0.4. The distance to the cable fault can be determined by the following formula:

EQUATION 3-1:

$$D(Distance\ \text{to cable fault in meters}) = 0.4 \times (Register\ \text{26 Bit [0], Register 27 Bits [7:0]})$$

Concatenated values of registers 26 and 27 are converted to decimal before multiplying by 0.4.

The constant (0.4) may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

For port 2 and for the MIIM PHY registers, LINKMD usage is similar.

3.3 MAC and Switch

3.3.1 ADDRESS LOOKUP

The internal lookup table stores MAC addresses and their associated information. It contains a 1K unicast address table plus switching information.

The KSZ8893FQL is guaranteed to learn 1K addresses and distinguishes itself from hash-based look-up tables, which depending upon the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

3.3.2 LEARNING

The internal lookup engine updates its table with a new entry if the following conditions are met:

- The received packet's source address (SA) does not exist in the lookup table.
- The received packet is good; the packet has no receiving errors and is of legal length.

The lookup engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, the last entry of the table is deleted to make room for the new entry.

3.3.3 MIGRATION

The internal lookup engine also monitors whether a station has moved. If a station has moved, it will update the table accordingly. Migration happens when the following conditions are met:

- The received packet's SA is in the table, but the associated source port information is different.
- The received packet is good; the packet has no receiving errors and is of legal length.

The lookup engine will update the existing record in the table with the new source port information.

3.3.4 AGING

The lookup engine updates the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the lookup engine removes the record from the table. The lookup engine constantly performs the aging process and will continuously remove aging records. The aging period is about 200 seconds. This feature can be enabled or disabled through register 3 (0x03) bit [2].

3.3.5 FORWARDING

The KSZ8893FQL forwards packets using the algorithm that is depicted in the following flowcharts. Figure 3-6 shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with "port to forward 1" (PTF1). PTF1 is then further modified by spanning tree, IGMP snooping, port mirroring, and port VLAN processes to come up with "port to forward 2" (PTF2), as shown in Figure 3-7. The packet is sent to PTF2.

FIGURE 3-6: DESTINATION ADDRESS LOOKUP FLOW CHART, STAGE 1

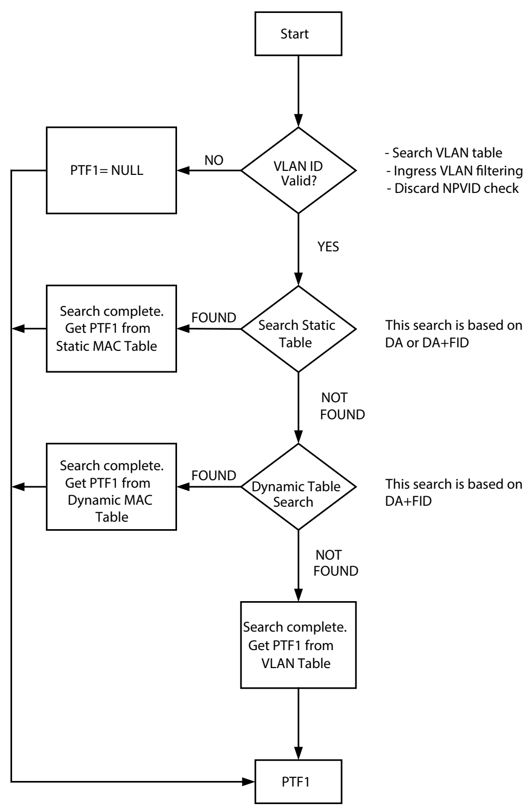
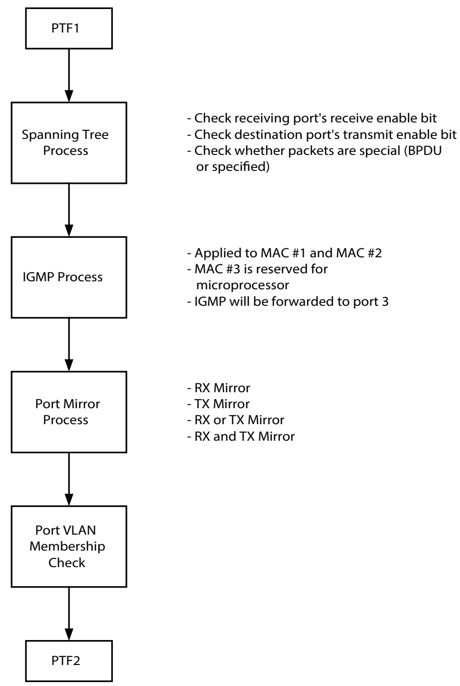


FIGURE 3-7: DESTINATION ADDRESS RESOLUTION FLOW CHART, STAGE 2



The KSZ8893FQL will not forward the following packets:

1. Error packets: These include framing errors, Frame Check Sequence (FCS) errors, alignment errors, and illegal size packet errors.
2. IEEE802.3x PAUSE frames: KSZ8893FQL intercepts these packets and performs full-duplex flow control accordingly.
3. "Local" packets: Based on destination address (DA) lookup. If the destination port from the lookup table matches the port from which the packet originated, the packet is defined as local.

3.3.6 SWITCHING ENGINE

The KSZ8893FQL features a high-performance switching engine to move data to and from the MAC’s packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency.

The switching engine has a 32 kB internal frame buffer. This buffer pool is shared between all three ports. There are a total of 256 buffers available. Each buffer is sized at 128 bytes.

3.3.7 MAC OPERATION

The KSZ8893FQL strictly abides by IEEE 802.3 standards to maximize compatibility.

3.3.7.1 Inter Packet Gap (IPG)

If a frame is successfully transmitted, the 96 bits time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96 bits time IPG is measured from MCRS and the next MTXEN.

3.3.7.2 Back-Off Algorithm

The KSZ8893FQL implements the IEEE 802.3 standard for the binary exponential back-off algorithm, and optional "aggressive mode" back-off. After 16 collisions, the packet is optionally dropped depending on the switch configuration for register 4 (0x04) bit [3].

3.3.7.3 Late Collision

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet is dropped.

3.3.7.4 Illegal Frames

The KSZ8893FQL discards frames less than 64 bytes and can be programmed to accept frames up to 1518 bytes, 1536 bytes, or 1916 bytes. These maximum frame size settings are programmed in register 4 (0x04). Because the KSZ8893FQL supports VLAN tags, the maximum sizing is adjusted when these tags are present.

3.3.7.5 Full-Duplex Flow Control

The KSZ8893FQL supports standard IEEE 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KSZ8893FQL receives a pause control frame, the KSZ8893FQL will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (while it is flow controlled), only flow control packets from the KSZ8893FQL are transmitted.

On the transmit side, the KSZ8893FQL has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues, and available receive queues.

The KSZ8893FQL will flow control a port that has just received a packet if the destination port resource is busy. The KSZ8893FQL issues a flow control frame (XOFF), containing the maximum pause time defined by the IEEE 802.3x standard. Once the resource is freed up, the KSZ8893FQL sends out the other flow control frame (XON) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being constantly activated and deactivated.

The KSZ8893FQL flow controls all ports if the receive queue becomes full.

3.3.7.6 Half-Duplex Backpressure

A half-duplex backpressure option (not in IEEE 802.3 standards) is also provided. The activation and deactivation conditions are the same as full-duplex flow control. If backpressure is required, the KSZ8893FQL sends preambles to defer the other stations' transmission (carrier sense deference).

To avoid jabber and excessive deference (as defined in the 802.3 standard), after a certain time, the KSZ8893FQL discontinues the carrier sense and then raises it again quickly. This short silent time (no carrier sense) prevents other stations from sending out packets thus keeping other stations in a carrier sense deferred state. If the port has packets to send during a backpressure situation, the carrier sense type backpressure is interrupted and those packets are transmitted instead. If there are no additional packets to send, carrier sense type backpressure is reactivated again until switch resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, thus reducing the chance of further collisions and carrier sense is maintained to prevent packet reception.

To ensure no packet loss in 10BASE-T or 100BASE-TX half-duplex modes, the user must enable the following:

- Aggressive back-off (register 3 (0x03), bit [0])
- No excessive collision drop (register 4 (0x04), bit [3])

Note that these bits are not set as defaults because this is not the IEEE standard.

3.3.7.7 Broadcast Storm Protection

The KSZ8893FQL has an intelligent option to protect the switch system from receiving too many broadcast packets. As the broadcast packets are forwarded to all ports except the source port, an excessive number of switch resources (bandwidth and available space in transmit queues) may be utilized. The KSZ8893FQL has the option to include “multicast packets” for storm control. The broadcast storm rate parameters are programmed globally, and can be enabled or disabled on a per port basis. The rate is based on a 67 ms interval for 100BT and a 500 ms interval for 10BT. At the beginning of each interval, the counter is cleared to zero, and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in register 6 (0x06) and 7 (0x07). The default setting is 0x63 (99 decimal). This is equal to a rate of 1%, calculated as follows:

148,800 frames/sec × 67 ms/interval × 1% = 99 frames/interval (approx.) = 0x63

Note: 148,800 frames/sec is based on 64-byte block of packets in 100BASE-TX with 12 bytes of IPG and 8 bytes of preamble between two packets.

3.3.8 MII INTERFACE OPERATION

The Media Independent Interface (MII) is specified in Clause 22 of the IEEE 802.3u Standard. It provides a common interface between physical layer and MAC layer devices. The MII provided by the KSZ8893FQL is connected to device's third MAC. The interface contains two distinct groups of signals: one for transmission and the other for reception. Table 3-9 describes the signals used by the MII bus.

TABLE 3-9: MII SIGNALS

PHY Mode Connections		Pin Description	MAC Mode Connections	
External MAC Controller Signals	KSZ8893FQL PHY Signals		External PHY Signals	KSZ8893FQL MAC Signals
MTXEN	SMTXEN	Transmit Enable	MTXEN	SMRXDV
MTXER	SMTXER	Transmit Error	MTXER	(NOT USED)
MTXD3	SMTXD[3]	Transmit Data Bit 3	MTXD3	SMRXD[3]
MTXD2	SMTXD[2]	Transmit Data Bit 2	MTXD2	SMRXD[2]
MTXD1	SMTXD[1]	Transmit Data Bit 1	MTXD1	SMRXD[1]
MTXD0	SMTXD[0]	Transmit Data Bit 0	MTXD0	SMRXD[0]
MTXC	SMTXC	Transmit Clock	MTXC	SMRXC
MCOL	SCOL	Collision Detection	MCOL	SCOL
MCRS	SCRS	Carrier Sense	MCRS	SCRS
MRXDV	SMRXDV	Receive Data Valid	MRXDV	SMTXEN
MRXER	(NOT USED)	Receive Error	MRXER	SMTXER
MRXD3	SMRXD[3]	Receive Data Bit 3	MRXD3	SMTXD[3]
MRXD2	SMRXD[2]	Receive Data Bit 2	MRXD2	SMTXD[2]
MRXD1	SMRXD[1]	Receive Data Bit 1	MRXD1	SMTXD[1]
MRXD0	SMRXD[0]	Receive Data Bit 0	MRXD0	SMTXD[0]
MRXC	SMRXC	Receive Clock	MRXC	SMTXC

The MII operates in either PHY mode or MAC mode. The data interface is a nibble wide and runs at one-quarter the network bit rate (not encoded). Additional signals on the transmit side indicate when data is valid or when an error has occurred during transmission. Similarly, the receive side has signals that convey when the data is valid and without physical layer errors. For half-duplex operation, the SCOL signal indicates if a collision has occurred during transmission.

The KSZ8893FQL does not provide the MRXER signal for PHY mode operation and the MTXER signal for MAC mode operation. Normally, MRXER indicates a receive error coming from the physical layer device and MTXER indicates a transmit error from the MAC device. Because the switch filters error frames, these MII error signals are not used by the KSZ8893FQL. So, for PHY mode operation, if the device interfacing with the KSZ8893FQL has an MRXER input pin, it needs to be tied low. And, for MAC mode operation, if the device interfacing with the KSZ8893FQL has an MTXER input pin, it also needs to be tied low.

3.3.9 RMII INTERFACE OPERATION

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). RMII provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports 10 Mbps and 100 Mbps data rates.
- Uses a single 50 MHz clock reference (provided externally).
- Provides independent 2-bit wide (di-bit) transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception

The RMII provided by the KSZ8893FQL is connected to the device's third MAC. It complies with the RMII Specification. The following table describes the signals used by the RMII bus. Refer to RMII Specification for full detail on the signal description.

TABLE 3-10: RMII SIGNAL DESCRIPTION

RMII Signal Name	Direction with Respect to PHY	Direction with Respect to MAC	RMII Signal Description	Device RMII Signal Direction
REF_CLK	Input	Input or Output	Synchronous 50 MHz clock reference for receive, transmit, and control interface	REFCLK (input)
CRS_DV	Output	Input	Carrier sense/Receive data valid	SMRXDV (output)
RXD1	Output	Input	Receive data bit 1	SMRXD[1] (output)
RXD0	Output	Input	Receive data bit 0	SMRXD[0] (output)
TX_EN	Input	Output	Transmit enable	SMTXEN (input)
TXD1	Input	Output	Transmit data bit 1	SMTXD[1] (input)
TXD0	Input	Output	Transmit data bit 0	SMTXD[0] (input)
RX_ER	Output	Input (not req'd)	Receive error	(Not used)
—	—	—	—	SMTXER* (input) * Connects to RX_ER signal of RMII PHY device

The KSZ8893FQL filters error frames, and thus does not implement the RX_ER output signal. To detect error frames from RMII PHY devices, the SMTXER input signal of the KSZ8893FQL is connected to the RXER output signal of the RMII PHY device.

Collision detection is implemented in accordance with the RMII Specification.

In RMII mode, tie MII signals, SMTXD[3:2] and SMTXER, to ground if they are not used.

The KSZ8893FQL RMII can interface with RMII PHY and RMII MAC devices. The latter allows two KSZ8893FQL devices to be connected back-to-back. The following table shows the KSZ8893FQL RMII pin connections with an external RMII PHY and an external RMII MAC, such as another KSZ8893FQL device.

TABLE 3-11: RMII SIGNAL CONNECTIONS

PHY-to-MAC Connections		Pin Descriptions	MAC-to-MAC Connections	
External PHY Signals	KSZ8893FQL MAC Signals		KSZ8893FQL MAC Signals	External MAC Signals
REF_CLK	REFCLK	Reference Clock	REFCLK	REF_CLK
CRS_DV	SMRXDV	Carrier Sense/ Receive Data Valid	SMRXDV	CRS_DV
RXD1	SMRXD[1]	Receive Data Bit 1	SMRXD[1]	RXD1
RXD0	SMRXD[0]	Receive Data Bit 0	SMRXD[0]	RXD0
TX_EN	SMTXEN	Transmit Enable	SMTXEN	TX_EN
TXD1	SMTXD[1]	Transmit Data Bit 1	SMTXD[1]	TXD1
TXD0	SMTXD[0]	Transmit Data Bit 0	SMTXD[0]	TXD0
RX_ER	SMTXER	Receive Error	(Not used)	(Not used)

3.3.10 SNI (7-WIRE) OPERATION

The serial network interface (SNI), or 7-wire, is compatible with some controllers used for network layer protocol processing. In SNI mode, the KSZ8893FQL acts like a PHY and the external controller functions as the MAC. The KSZ8893FQL can interface directly with external controllers using the 7-wire interface. These signals are divided into two groups, one for transmission and the other for reception. The signals involved are described in the following table.

TABLE 3-12: SNI SIGNALS

Pin Description	External MAC Controller Signal	KSZ8893FQL PHY Signal
Transmit enable	TXEN	SMTXEN
Serial transmit data	TXD	SMTXD[0]
Transmit clock	TXC	SMTXC
Collision detection	COL	SCOL
Carrier sense	CRS	SMRXDV
Serial receive data	RXD	SMRXD[0]
Receive clock	RXC	SMRXC

The SNI interface is a bit wide data interface and, therefore, runs at the network bit rate (not encoded). An additional signal on the transmit side indicates when data is valid. Similarly, the receive side has an indicator that conveys when the data is valid.

For half-duplex operation, the SCOL signal is used to indicate that a collision has occurred during transmission.

3.3.11 MII MANAGEMENT (MIIM) INTERFACE

The KSZ8893FQL supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the states of the KSZ8893FQL. An external device with MDC/MDIO capability is used to read the PHY status or configure the PHY settings. Further details on the MIIM interface can be found in Clause 22.2.4.5 of the IEEE 802.3u Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the data line (MDIO) and the clock line (MDC).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with the KSZ8893FQL device.
- Access to a set of eight 16-bit registers, consisting of six standard MIIM registers [0:5] and two custom MIIM registers [29, 31].

The MIIM Interface can operate up to a maximum clock speed of 5 MHz.

Table 3-13 depicts the MII Management Interface frame format.

TABLE 3-13: MII MANAGEMENT INTERFACE FRAME FORMAT

	Preamble	Start of Frame	Read/ Write OP Code	PHY Address Bits[4:0]	REG Address Bits[4:0]	TA	Data Bits[15:0]	Idle
Read	32 1's	01	10	AAAAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	AAAAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

3.3.12 SERIAL MANAGEMENT INTERFACE (SMI)

The SMI is the KSZ8893FQL non-standard MIIM interface that provides access to all KSZ8893FQL configuration registers. This interface allows an external device to completely monitor and control the states of the KSZ8893FQL.

The SMI interface consists of the following:

- A physical connection that incorporates the data line (MDIO) and the clock line (MDC).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with the KSZ8893FQL device.
- Access to all KSZ8893FQL configuration registers. Register access includes the Global, Port, and Advanced Control Registers 0-141 (0x00 – 0x8D), and indirect access to the standard MIIM registers [0:5] and custom MIIM registers [29, 31].

Table 3-14 depicts the SMI frame format.

TABLE 3-14: SERIAL MANAGEMENT INTERFACE (SMI) FRAME FORMAT

	Preamble	Start of Frame	Read/ Write OP Code	PHY Address Bits[4:0]	REG Address Bits[4:0]	TA	Data Bits[15:0]	Idle
Read	32 1's	01	00	1xRRR	RRRRR	Z0	0000_0000_DDDD_DDDD	Z
Write	32 1's	01	00	0xRRR	RRRRR	10	xxxx_xxxx_DDDD_DDDD	Z

SMI register read access is selected when OP Code is set to "00" and bit 4 of the PHY address is set to '1'. SMI register write access is selected when OP Code is set to "00" and bit 4 of the PHY address is set to '0'. PHY address bit[3] is undefined for SMI register access, and hence can be set to either '0' or '1' in read/write operations.

To access the KSZ8893FQL registers 0-141 (0x00 – 0x8D), the following applies:

- PHYAD[2:0] and REGAD[4:0] are concatenated to form the 8-bit address; that is, {PHYAD[2:0], REGAD[4:0]} = bits [7:0] of the 8-bit address.
- Registers are 8 data bits wide.
  - For read operation, data bits [15:8] are read back as 0's.
  - For write operation, data bits [15:8] are not defined, and hence can be set to either '0' or '1'.

SMI register access is the same as the MIIM register access, except for the register access requirements presented in this section.

3.3.13 REPEATER MODE

The KSZ8893FQL supports repeater mode in 100BASE-TX half-duplex mode. In repeater mode, all ingress packets are broadcast to the other two ports. MAC address checking and learning are disabled.

Repeater mode is enabled by setting register 6 bit[7] to '1'. Prior to setting this bit, all three ports need to be configured to 100BASE-TX half-duplex mode. Additionally, both PHY ports need to have auto-negotiation disabled.

The latency between the two PHY ports is 270 ns (minimum) and 310 ns (maximum). The 40 ns difference is one clock skew (one 25 MHz clock period) between reception and transmission. Latency is defined as the time from the first bit of the Destination Address (DA) entering the ingress port to the first bit of the DA exiting the egress port.

3.4 Advanced Switch Functions

3.4.1 SPANNING TREE SUPPORT

To support spanning tree, port 3 is designated as the processor port.

The other ports (port 1 and port 2) can be configured in one of the five spanning tree states via "transmit enable", "receive enable", and "learning disable" register settings in registers 18 and 34 for ports 1 and 2, respectively. Table 3-15 shows the port setting and software actions taken for each of the five spanning tree states.

TABLE 3-15: SPANNING TREE STATES

Disable State	**Port Setting**	**Software Action**
The port should not forward or receive any packets. Learning is disabled.	"transmit enable = 0, receive enable = 0, learning disable =1"	The processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the "Static MAC table" with "overriding bit" set) and the processor should discard those packets. Address learning is disabled on the port in this state.
Blocking State	**Port Setting**	**Software Action**
Only packets to the processor are forwarded. Learning is disabled.	"transmit enable = 0, receive enable = 0, learning disable =1"	The processor should not send any packets to the port(s) in this state. The processor should program the "Static MAC table" with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit should also be set so that the switch will forward those specific packets to the processor. Address learning is disabled on the port in this state.

TABLE 3-15: SPANNING TREE STATES (CONTINUED)

Listening State	Port Setting	Software Action
Only packets to and from the processor are forwarded. Learning is disabled.	“transmit enable = 0, receive enable = 0, learning disable =1”	The processor should program the “Static MAC table” with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. See Special Tagging Mode for details. Address learning is disabled on the port in this state.
Learning State	**Port Setting**	**Software Action**
Only packets to and from the processor are forwarded. Learning is enabled.	“transmit enable = 0, receive enable = 0, learning disable = 0”	The processor should program the “Static MAC table” with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. See Special Tagging Mode for details. Address learning is enabled on the port in this state.
Forwarding State	**Port Setting**	**Software Action**
Packets are forwarded and received normally. Learning is enabled.	“transmit enable = 1, receive enable = 1, learning disable = 0”	The processor programs the “Static MAC table” with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit is set so that the switch forwards those specific packets to the processor. The processor can send packets to the port(s) in this state. See Special Tagging Mode for details. Address learning is enabled on the port in this state.

3.4.2 SPECIAL TAGGING MODE

Special Tagging Mode is designed for spanning tree protocol IGMP snooping and is flexible for use in other applications. Special Tagging, similar to 802.1Q Tagging, requires software to change network drivers to insert/modify/strip/interpret the special tag. This mode is enabled by setting both register 11 bit [0] and register 48 bit [2] to ‘1’.

TABLE 3-16: SPECIAL TAGGING MODE FORMAT

802.1Q Tag Format	Special Tag Format
TPID (tag protocol identifier, 0x8100) + TCI	STPID (special tag identifier, 0x810 + 4 bit for “port mask”) + TCI

The STPID is only seen and used by the port 3 interface, which should be connected to a processor. Packets from the processor to the switch’s port 3 should be tagged with the STPID and the port mask, defined as follows:

- “0001”, forward packet to port 1 only
- “0010”, forward packet to port 2 only
- “0011”, broadcast packet to port 1 and port 2

Packets with normal tags (“0000” port masks) will use KSZ8893FQL internal MAC table look-up to determine the forwarding port(s). Also, if packets from the processor are not tagged, the KSZ8893FQL will treat them as normal packets and use internal MAC table lookup to determine the forwarding port(s).

The KSZ8893FQL uses a non-zero “port mask” to bypass the internal MAC table lookup result, and override any port setting, regardless of port states (disable, blocking, listening, and learning). Table 3-17 below shows the processor to switch egress rules when dealing with STPID.

TABLE 3-17: STPID EGRESS RULES (PROCESSOR TO SWITCH PORT 3)

Ingress Tag Field	TX Port “Tag Insertion”	TX Port “Tag Removal”	Egress Action to Tag Field
(0x810 + port mask)	0	0	- Modify tag field to 0x8100 - Recalculate CRC - No change to TCI if not null VID - Replace VID with ingress (port 3) port VID if null VID
(0x810 + port mask)	0	1	- (STPID + TCI) will be removed - Padding to 64 bytes if necessary - Recalculate CRC

TABLE 3-17: STPID EGRESS RULES (PROCESSOR TO SWITCH PORT 3) (CONTINUED)

Ingress Tag Field	TX Port "Tag Insertion"	TX Port "Tag Removal"	Egress Action to Tag Field
(0x810 + port mask)	1	0	- Modify tag field to 0x8100 - Recalculate CRC - No change to TCI if not null VID - Replace VID with ingress (port 3) port VID if null VID
(0x810 + port mask)	1	1	- Modify tag field to 0x8100 - Recalculate CRC - No change to TCI if not null VID - Replace VID with ingress (port 3) port VID if null VID
Not Tagged	Don't Care	Don't Care	- Determined by the Dynamic MAC Address Table

For packets from regular ports (port 1 & port 2) to port 3, the port mask is used to tell the processor which port the packets were received on, defined as follows:

- "0001", packet from port 1
- "0010", packet from port 2

No port mask values, other than the previous two defined ones, should be received in this direction in Special Tagging Mode. The switch to processor egress rules are defined as follows:

TABLE 3-18: STPID EGRESS RULES (SWITCH PORT 3 TO PROCESSOR)

Ingress Packets	Egress Action to Tag Field
Tagged with 0x8100 + TCI	- Modify TPID to 0x810 + "port mask", which indicates source port - No change to TCI if VID is not null - Replace null VID with ingress port VID - Recalculate CRC
Not tagged	- Insert TPID to 0x810 + "port mask", which indicates source port - Insert TCI with ingress port VID - Recalculate CRC

3.4.3 IGMP SUPPORT

For Internet Group Management Protocol (IGMP) support in layer 2, the KSZ8893FQL provides two components:

3.4.3.1 IGMP Snooping

The KSZ8893FQL traps IGMP packets and forwards them only to the processor (port 3). The IGMP packets are identified as IP packets (either Ethernet IP packets, or IEEE 802.3 SNAP IP packets) with IP version = 0x4 and protocol version number = 0x2.

3.4.3.2 Multicast Address Insertion in the Static MAC Table

Once the multicast address is programmed in the Static MAC Table, the multicast session is trimmed to the subscribed ports, instead of broadcasting to all ports.

To enable IGMP support, set register 5 bit [6] to '1'. Also, Special Tagging Mode needs to be enabled, so that the processor knows which port the IGMP packet was received on. This is achieved by setting both register 11 bit [0] and register 48 bit [2] to '1'.

3.4.4 IPV6 MLD SNOOPING

The KSZ8893FQL traps IPv6 Multicast Listener Discovery (MLD) packets and forwards them only to processor (port 3). MLD snooping is controlled by register 5 bit 5 (MLD snooping enable) and register 5 bit 4 (MLD option).

With MLD snooping enabled, the KSZ8893FQL traps packets that meet all of the following conditions:

- IPv6 multicast packets
- Hop count limit = 1
- IPv6 next header = 1 or 58 (or = 0 with hop-by-hop next header = 1 or 58)

If the MLD option bit is set to "1", the KSZ8893FQL traps packets with the following additional condition:

- IPv6 next header = 43, 44, 50, 51, or 60 (or = 0 with hop-by-hop next header = 43, 44, 50, 51, or 60)

For MLD snooping, Special Tagging Mode also needs to be enabled, so that the processor knows which port the MLD packet was received on. This is achieved by setting both register 11 bit [0] and register 48 bit [2] to ‘1’.

3.4.5 PORT MIRRORING SUPPORT

KSZ8893FQL supports port mirroring comprehensively as:

- **“Receive Only” mirror on a port:** All the packets received on the port are mirrored on the sniffer port. For example, port 1 is programmed to be “receive sniff” and port 3 is programmed to be the “sniffer port”. A packet received on port 1 is destined to port 2 after the internal lookup. The KSZ8893FQL forwards the packet to both port 2 and port 3. The KSZ8893FQL can optionally even forward “bad” received packets to the “sniffer port”.
- **“Transmit Only” mirror on a port:** All the packets transmitted on the port are mirrored on the sniffer port. For example, port 1 is programmed to be “transmit sniff” and port 3 is programmed to be the “sniffer port”. A packet received on port 2 is destined to port 1 after the internal lookup. The KSZ8893FQL forwards the packet to both port 1 and port 3.
- **“Receive and Transmit” mirror on two ports:** All the packets received on port A and transmitted on port B are mirrored on the sniffer port. To turn on the “AND” feature, set register 5 bit [0] to ‘1’. For example, port 1 is programmed to be “receive sniff”, port 2 is programmed to be “transmit sniff”, and port 3 is programmed to be the “sniffer port”. A packet received on port 1 is destined to port 2 after the internal lookup. The KSZ8893FQL forwards the packet to both port 2 and port 3.

Multiple ports can be selected as “receive sniff” or “transmit sniff”. In addition, any port can be selected as the “sniffer port”. All these per port features can be selected through registers 17, 33 and 49 for ports 1, 2 and 3, respectively.

3.4.6 IEEE 802.1Q VLAN SUPPORT

The KSZ8893FQL supports 16 active VLANs out of the 4096 possible VLANs specified in the IEEE 802.1Q specification. KSZ8893FQL provides a 16-entry VLAN Table, which converts the 12-bits VLAN ID (VID) to the 4-bits Filter ID (FID) for address lookup. If a non-tagged or null-VID-tagged packet is received, the ingress port default VID is used for lookup. In VLAN mode, the look-up process starts with VLAN Table lookup to determine whether the VID is valid. If the VID is not valid, the packet is dropped and its address is not learned. If the VID is valid, the FID is retrieved for further lookup. The FID + Destination Address (FID+DA) are used to determine the destination port. The FID + Source Address (FID+SA) are used for address learning.

TABLE 3-19: FID+DA LOOKUP IN VLAN MODE

DA Found in Static MAC Table?	Use FID Flag?	FID Match?	FID+DA Found in Dynamic MAC Table?	Action
No	Don’t care	Don’t care	No	Broadcast to the membership ports defined in the VLAN Table bits [18:16]
No	Don’t care	Don’t care	Yes	Send to the destination port defined in the Dynamic MAC Address Table bits [53:52]
Yes	0	Don’t care	Don’t care	Send to the destination port(s) defined in the Static MAC Address Table bits [50:48]
Yes	1	No	No	Broadcast to the membership ports defined in the VLAN Table bits [18:16]
Yes	1	No	Yes	Send to the destination port defined in the Dynamic MAC Address Table bits [53:52]
Yes	1	Yes	Don’t care	Send to the destination port(s) defined in the Static MAC Address Table bits [50:48]

TABLE 3-20: FID+SA LOOKUP IN VLAN MODE

FID+SA Found in Dynamic MAC Table?	Action
No	Learn and add FID+SA to the Dynamic MAC Address Table
Yes	Update time stamp

Advanced VLAN features, such as “Ingress VLAN filtering” and “Discard Non PVID packets” are also supported by the KSZ8893FQL. These features can be set on a per port basis, and are defined in register 18, 34, and 50 for ports 1, 2, and 3, respectively.

3.4.7 QOS PRIORITY SUPPORT

The KSZ8893FQL provides Quality of Service (QoS) for applications such as VoIP and video conferencing. Offering four priority queues per port, the per-port transmit queue can be split into four priority queues: Queue 3 is the highest priority queue and Queue 0 is the lowest priority queue. Bit [0] of registers 16, 32, and 48 is used to enable split transmit queues for ports 1, 2, and 3, respectively. If a port's transmit queue is not split, high priority and low priority packets have equal priority in the transmit queue.

There is an additional option to either always deliver high priority packets first or use weighted fair queuing for the four priority queues. This global option is set and explained in bit [3] of register 5.

3.4.8 PORT-BASED PRIORITY

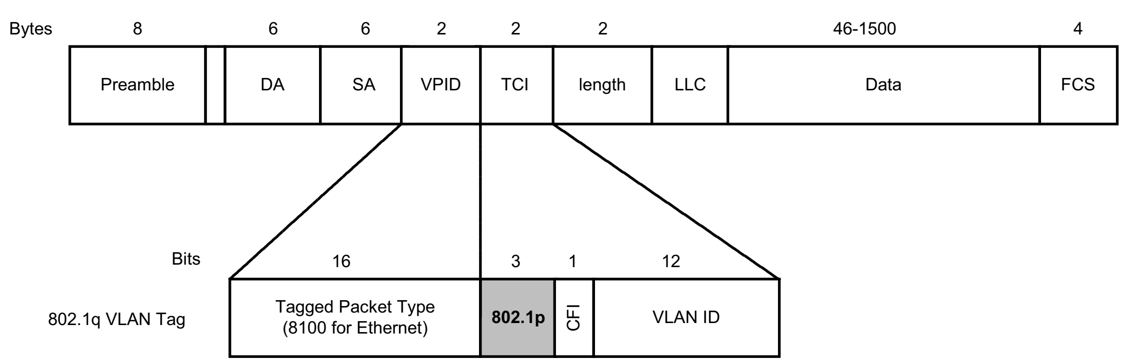
With port-based priority, each ingress port is individually classified as a high priority receiving port. All packets received at the high priority receiving port are marked as high priority and are sent to the high-priority transmit queue if the corresponding transmit queue is split. Bits [4:3] of registers 16, 32, and 48 are used to enable port-based priority for ports 1, 2, and 3, respectively.

3.4.9 802.1P-BASED PRIORITY

For 802.1p-based priority, the KSZ8893FQL examines the ingress (incoming) packets to determine whether they are tagged. If tagged, the 3-bit priority field in the VLAN tag is retrieved and compared against the “priority mapping” value, as specified by the registers 12 and 13. The “priority mapping” value is programmable.

Figure 3-8 illustrates how the 802.1p priority field is embedded in the 802.1Q VLAN tag.

FIGURE 3-8: 802.1P PRIORITY FIELD FORMAT



802.1p-based priority is enabled by bit [5] of registers 16, 32, and 48 for ports 1, 2, and 3, respectively.

The KSZ8893FQL provides the option to insert or remove the priority tagged frame's header at each individual egress port. This header, consisting of the 2 bytes VLAN Protocol ID (VPID) and the 2-byte Tag Control Information field (TCI), is also referred to as the IEEE 802.1Q VLAN tag.

Tag Insertion is enabled by bit [2] of the port registers control 0 and the register 194 to select which source port (ingress port) PVID can be inserted on the egress port for ports 1, 2, and 3, respectively. At the egress port, untagged packets are tagged with the ingress port's default tag. The default tags are programmed in register sets {19,20}, {35,36}, and {51,52} for ports 1, 2, and 3, respectively, and the source port VID has to be inserted at selected egress ports by bit[5:0] of register 194. The KSZ8893FQL will not add tags to already tagged packets.

Tag Removal is enabled by bit [1] of registers 16, 32, and 48 for ports 1, 2, and 3, respectively. At the egress port, tagged packets will have their 802.1Q VLAN Tags removed. The KSZ8893FQL will not modify untagged packets.

The CRC is recalculated for both tag insertion and tag removal.

802.1p Priority Field Re-mapping is a QoS feature that allows the KSZ8893FQL to set the "User Priority Ceiling" at any ingress port. If the ingress packet's priority field has a higher priority value than the default tag's priority field of the ingress port, the packet's priority field is replaced with the default tag's priority field. The "User Priority Ceiling" is enabled by bit [3] of registers 17, 33, and 49 for ports 1, 2, and 3, respectively.

3.4.10 DIFFSERV-BASED PRIORITY

DiffServ-based priority uses the ToS registers (registers 96 to 111) in the Advanced Control Registers section. The ToS priority control registers implement a fully decoded, 64-bit Differentiated Services Code Point (DSCP) register to determine packet priority from the 6-bit ToS field in the IP header. When the most significant 6 bits of the ToS field are fully decoded, the resultant of the 64 possibilities is compared with the corresponding bits in the DSCP register to determine priority.

3.4.11 RATE LIMITING SUPPORT

The KSZ8893FQL supports hardware rate limiting from 64 kbps to 88 Mbps, independently on the "receive side" and on the "transmit side" on a per port basis. For 10BASE-T, a rate setting above 10 Mbps means the rate is not limited. On the receive side, the data receive rate for each priority at each port can be limited by setting up Ingress Rate Control Registers. On the transmit side, the data transmit rate for each priority queue at each port can be limited by setting up Egress Rate Control Registers. The size of each frame has options to include minimum IFG (Inter Frame Gap) or Preamble byte, in addition to the data field (from packet DA to FCS).

For ingress rate limiting, KSZ8893FQL provides options to selectively choose frames from all types, multicast, broadcast, and flooded unicast frames. The KSZ8893FQL counts the data rate from those selected type of frames. Packets are dropped at the ingress port when the data rate exceeds the specified rate limit.

For egress rate limiting, the Leaky Bucket algorithm is applied to each output priority queue for shaping output traffic. Inter frame gap is stretched on a per frame base to generate smooth, non-burst egress traffic. The throughput of each output priority queue is limited by the egress rate specified.

If any egress queue receives more traffic than the specified egress rate throughput, packets may be accumulated in the output queue and packet memory. After the memory of the queue or the port is used up, packet dropping or flow control will be triggered. As a result of congestion, the actual egress rate may be dominated by flow control/dropping at the ingress end, and may be therefore, slightly less than the specified egress rate.

To reduce congestion, it is a good practice to make sure the egress bandwidth exceeds the ingress bandwidth.

3.5 Unicast MAC Address Filtering

The unicast MAC address filtering function works in conjunction with the static MAC address table. First, the static MAC address table is used to assign a dedicated MAC address to a specific port. If a unicast MAC address is not recorded in the static table, it is also not learned in the dynamic MAC table. The KSZ8893FQL is then configured with the option to either filter or forward unicast packets for an unknown MAC address. This option is enabled and configured in register 14.

This function is useful in preventing the broadcast of unicast packets that could degrade the quality of the port in applications such as voice over Internet Protocol (VoIP).

3.6 Configuration Interface

The KSZ8893FQL can operate as both a managed switch and an unmanaged switch.

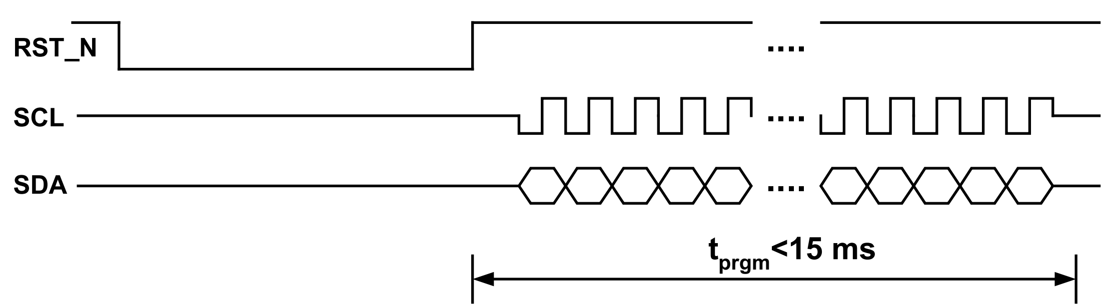
In unmanaged mode, the KSZ8893FQL is typically programmed using an EEPROM. If no EEPROM is present, the KSZ8893FQL is configured using its default register settings. Some default settings are configured via strap-in pin options. The strap-in pins are indicated in Table 2-1.

3.6.1 I^{2}C MASTER SERIAL BUS CONFIGURATION

With an additional I^{2}C (“2-wire”) EEPROM, the KSZ8893FQL can perform more advanced switch features like “broadcast storm protection” and “rate control” without the need of an external processor.

For KSZ8893FQL I^{2}C Master configuration, the EEPROM stores the configuration data for register 0 to register 120 (as defined in the KSZ8893FQL register map) with the exception of the “Read Only” status registers. After the de-assertion of reset, the KSZ8893FQL sequentially reads in the configuration data for all 121 registers, starting from register 0. The configuration access time (t_{prgm}) is less than 15 ms, as depicted in Figure 3-9.

FIGURE 3-9: EEPROM CONFIGURATION TIMING DIAGRAM



The following is a sample procedure for programming the KSZ8893FQL with a pre-configured EEPROM:

1. Connect the KSZ8893FQL to the EEPROM by joining the SCL and SDA signals of the respective devices. For the KSZ8893FQL, SCL is pin 97 and SDA is pin 98.
2. Enable I^{2}C master mode by setting the KSZ8893FQL strap-in pins, PS[1:0] (pins 100 and 101, respectively) to “00”.
3. Check to ensure that the KSZ8893FQL reset signal input, RST_N (pin 67), is properly connected to the external reset source at the board level.
4. Program the desired configuration data into the EEPROM.
5. Place the EEPROM on the board and power up the board.
6. Assert an active-low reset to the RSTN pin of the KSZ8893FQL. After reset is de-asserted, the KSZ8893FQL begins reading the configuration data from the EEPROM. The KSZ8893FQL checks that the first byte read from the EEPROM is “88”. If this value is correct, EEPROM configuration continues. If not, EEPROM configuration access is denied and all other data sent from the EEPROM is ignored by the KSZ8893FQL. The configuration access time (t_{prgm}) is less than 15 ms.

For proper operation, ensure that the KSZ8893FQL PWRDN input signal (pin 36) is not asserted during the reset operation. The PWRDN input is active-low.

3.6.2 I^{2}C SLAVE SERIAL BUS CONFIGURATION

In managed mode, the KSZ8893FQL can be configured as an I^{2}C slave device. In this mode, an I^{2}C master device (external controller/CPU) has complete programming access to the KSZ8893FQL’s 142 registers. Programming access includes the Global Registers, Port Registers, Advanced Control Registers, and indirect access to the “Static MAC Table”, “VLAN Table”, “Dynamic MAC Table,” and “MIB Counters.” The tables and counters are indirectly accessed via registers 121 to 131.

In I^{2}C slave mode, the KSZ8893FQL operates like other I^{2}C slave devices. Addressing the KSZ8893FQL’s 8-bit registers is similar to addressing the Microchip AT24C02 EEPROM’s memory locations. Details of I^{2}C read/write operations and related timing information can be found in the AT24C02 data sheet.

Two fixed 8-bit device addresses are used to address the KSZ8893FQL in I^{2}C slave mode. One is for read; the other is for write. The addresses are as follows:

- 1011_1111 <read>

- 1011_1110 <write>

The following is a sample procedure for programming the KSZ8893FQL using the I2C slave serial bus:

1. Enable I2C slave mode by setting the KSZ8893FQL strap-in pins PS[1:0] (pins 100 and 101, respectively) to “01”.
2. Power up the board and assert reset to the KSZ8893FQL. After reset, the “Start Switch” bit (register 1 bit [0]) is set to ‘0’.
3. Configure the desired register settings in the KSZ8893FQL using the I2C write operation.
4. Read back and verify the register settings in the KSZ8893FQL using the I2C read operation.
5. Write a ‘1’ to the “Start Switch” bit to start the KSZ8893FQL with the programmed settings.

The “Start Switch” bit cannot be set to ‘0’ to stop the switch after a ‘1’ is written to this bit. Thus, it is recommended that all switch configuration settings are programmed before the “Start Switch” bit is set to ‘1’.

Some of the configuration settings, such as “Aging Enable”, “Auto Negotiation Enable”, “Force Speed”, and “Power down” can be programmed after the switch has been started.

3.6.3 SPI SLAVE SERIAL BUS CONFIGURATION

In managed mode, the KSZ8893FQL can be configured as a SPI slave device. In this mode, a SPI master device (external controller/CPU) has complete programming access to the KSZ8893FQL’s 142 registers. Programming access includes the Global Registers, Port Registers, Advanced Control Registers and indirect access to the “Static MAC Table”, “VLAN Table”, “Dynamic MAC Table” and “MIB Counters”. The tables and counters are indirectly accessed via registers 121 to 131.

The KSZ8893FQL supports two standard SPI commands: ‘0000_0011’ for data read and ‘0000_0010’ for data write. SPI multiple read and multiple write are also supported by the KSZ8893FQL to expedite register read back and register configuration, respectively.

SPI multiple read is initiated when the master device continues to drive the KSZ8893FQL SPIS_N input pin (SPI Slave Select signal) low after a byte (a register) is read. After the read, the KSZ8893FQL internal address counter increments automatically to the next byte (next register) after the read. The next byte at the next register address is shifted out onto the KSZ8893FQL SPIQ output pin. SPI multiple read continues until the SPI master device terminates it by deasserting the SPIS_N signal to the KSZ8893FQL.

Similarly, SPI multiple write is initiated when the master device continues to drive the KSZ8893FQL SPIS_N input pin low after a byte (a register) is written. The KSZ8893FQL internal address counter increments automatically to the next byte (next register) after the write. The next byte that is sent from the master device to the KSZ8893FQL SDA input pin is written to the next register address. SPI multiple write continues until the SPI master device terminates it by deasserting the SPIS_N signal to the KSZ8893FQL.

For both SPI multiple read and multiple write, the KSZ8893FQL internal address counter wraps back to register address zero once the highest register address is reached. This feature allows all 142 KSZ8893FQL registers to be read or written with a single SPI command from any initial register address.

The KSZ8893FQL is capable of supporting a 5 MHz SPI bus.

The following is a sample procedure for programming the KSZ8893FQL using the SPI bus:

1. At the board level, connect the KSZ8893FQL pins as follows:

TABLE 3-21: SPI CONNECTIONS

Pin Number	Signal Name	External Processor Signal Description
99	SPIS N	SPI Slave Select
97	SCL (SPIC)	SPI Clock
98	SDA (SPID)	SPI Data (Master output; Slave input)
96	SPIQ	SPI Data (Master input; Slave output)

2. Enable SPI slave mode by setting the KSZ8893FQL strap-in pins PS[1:0] (pins 100 and 101, respectively) to “10”.
3. Power up the board and assert reset to the KSZ8893FQL. After reset, the “Start Switch” bit (register 1 bit [0]) is set to ‘0’.
4. Configure the desired register settings in the KSZ8893FQL using the SPI write or multiple write command.

5. Read back and verify the register settings in the KSZ8893FQL using the SPI read or multiple read command.
6. Write a ‘1’ to the “Start Switch” bit to start the KSZ8893FQL with the programmed settings.

The “Start Switch” bit cannot be set to ‘0’ to stop the switch after a ‘1’ is written to this bit. Thus, it is recommended that all switch configuration settings are programmed before the “Start Switch” bit is set to ‘1’.

Some of the configuration settings, such as “Aging Enable,” “Auto Negotiation Enable,” “Force Speed,” and “Power Down” can be programmed after the switch has been started.

The following four figures illustrate the SPI data cycles for “Write,” “Read,” “Multiple Write,” and “Multiple Read.” The read data is registered out of SPIQ on the falling edge of SPIC, and the data input on SPID is registered on the rising edge of SPIC.

FIGURE 3-10: SPI WRITE DATA CYCLE

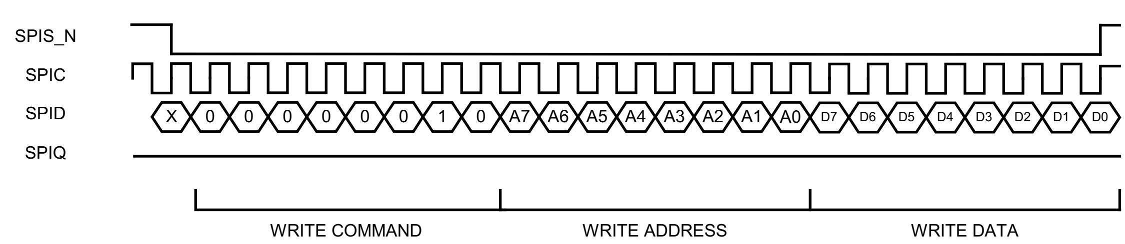


FIGURE 3-11: SPI READ DATA CYCLE

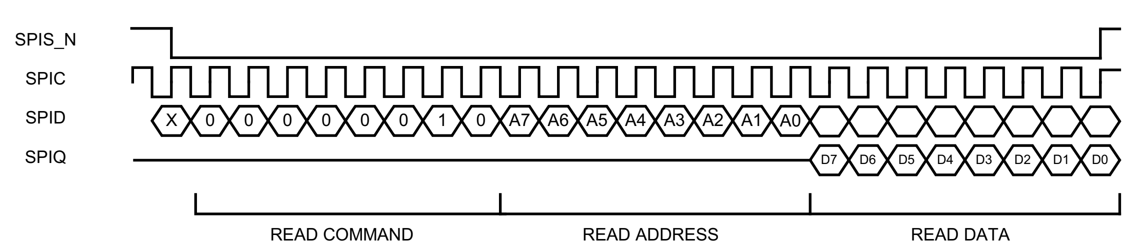


FIGURE 3-12: SPI MULTIPLE WRITE

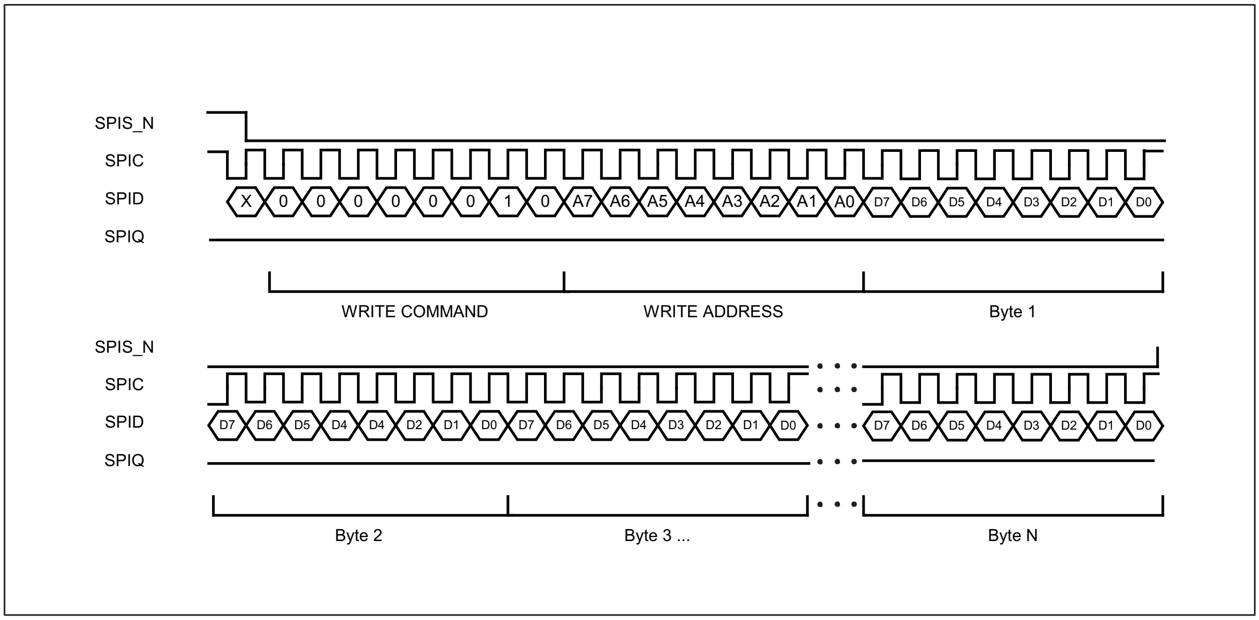
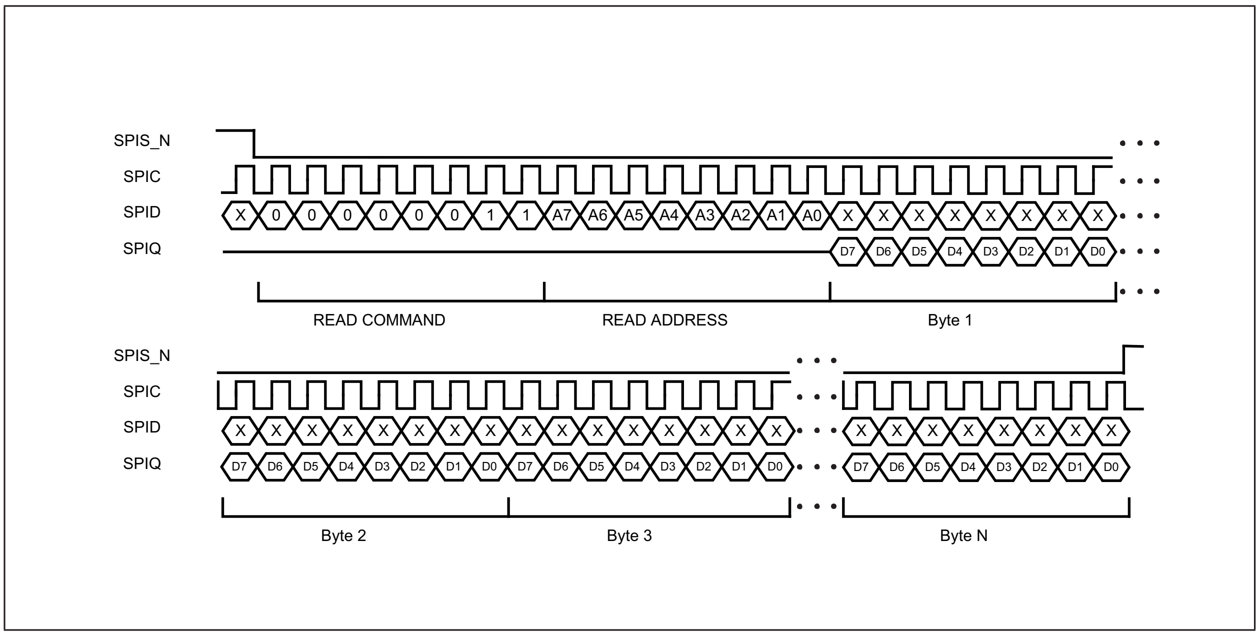


FIGURE 3-13: SPI MULTIPLE READ



3.7 Loopback Support

The KSZ8893FQL provides loopback support for remote diagnostic of failure. In loopback mode, the speed at both PHY ports needs to be set to 100BASE-TX. Two types of loopback are supported: Far-end Loopback and Near-end (Remote) Loopback.

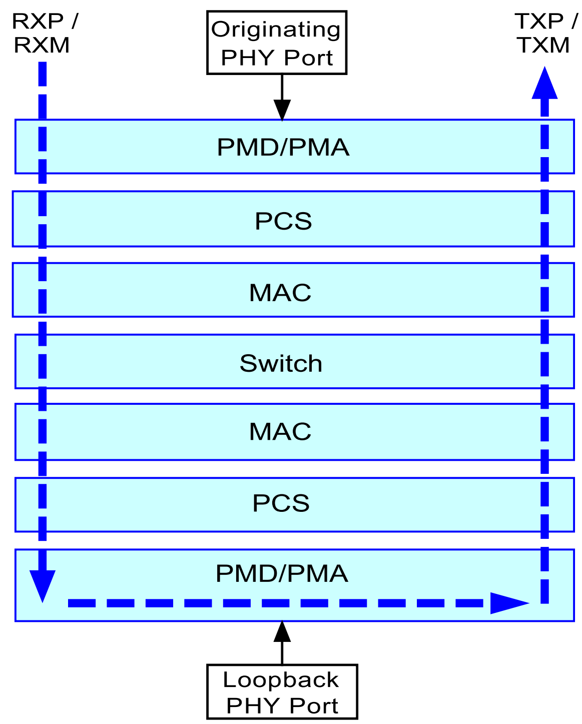
3.7.1 FAR-END LOOPBACK

Far-end loopback is conducted between the KSZ8893FQL's two PHY ports. The loopback path starts at the "Originating." PHY port's receive inputs (RXP/RXM), wraps around at the "loopback" PHY port's PMD/PMA, and ends at the "Originating" PHY port's transmit outputs (TXP/TXM).

Bit [0] of registers 29 and 45 is used to enable far-end loopback for ports 1 and 2, respectively. Alternatively, the MII Management register 0, bit [14] can be used to enable far-end loopback.

The far-end loopback path is illustrated in the following figure.

FIGURE 3-14: FAR-END LOOPBACK PATH



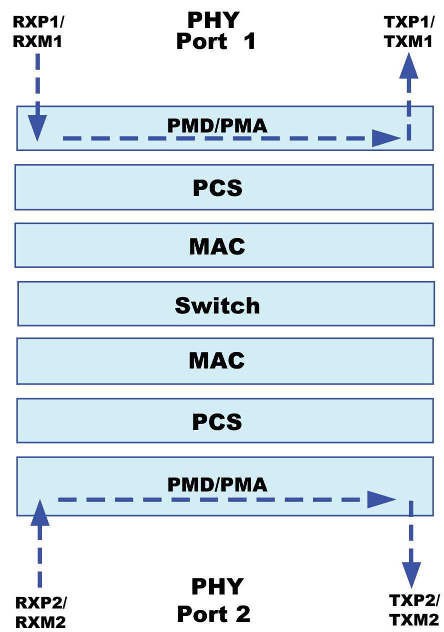
3.7.2 NEAR-END (REMOTE) LOOPBACK

Near-end (Remote) loopback is conducted at either PHY port 1 or PHY port 2 of the KSZ8893FQL. The loopback path starts at the PHY port's receive inputs (RXPx/RXMx), wraps around at the same PHY port's PMD/PMA, and ends at the PHY port's transmit outputs (TXPx/TXMx).

Bit [1] of registers 26 and 42 is used to enable near-end loopback for ports 1 and 2, respectively. Alternatively, the MII Management register 31, bit [1] can be used to enable near-end loopback.

The near-end loopback paths are illustrated in Figure 3-15.

FIGURE 3-15: NEAR-END (REMOTE) LOOPBACK PATH



4.0 REGISTER DESCRIPTIONS

4.1 MII Management (MIIM) Registers

The MIIM interface is used to access the MII PHY registers defined in this section. The SPI, I^2C, and SMI interfaces can also be used to access some of these registers. The latter three interfaces use a different mapping mechanism than the MIIM interface.

The “PHYADs” by defaults are assigned “0x1” for PHY1 (port 1) and “0x2” for PHY2 (port 2). Additionally, these “PHY-ADs” can be programmed to the PHY addresses specified in bits[7:3] of Register 15 (0x0F): Global Control 13.

The “REGAD” supported are 0x0-0x5, 0x1D, and 0x1F.

TABLE 4-1: MIIM REGISTERS FOR KSZ8893FQL

Register Number	Description
PHYAD = 0x1, REGAD = 0x0	PHY1 Basic Control Register
PHYAD = 0x1, REGAD = 0x1	PHY1 Basic Status Register
PHYAD = 0x1, REGAD = 0x2	PHY1 Physical Identifier I
PHYAD = 0x1, REGAD = 0x3	PHY1 Physical Identifier II
PHYAD = 0x1, REGAD = 0x4	PHY1 Auto-Negotiation Advertisement Register
PHYAD = 0x1, REGAD = 0x5	PHY1 Auto-Negotiation Link Partner Ability Register
PHYAD = 0x1, 0x6 – 0x1C	PHY1 Not supported
PHYAD = 0x1, 0x1D	PHY1 LinkMD Control/Status
PHYAD = 0x1, 0x1E	PHY1 Not supported
PHYAD = 0x1, 0x1F	PHY1 Special Control/Status
PHYAD = 0x2, REGAD = 0x0	PHY2 Basic Control Register
PHYAD = 0x2, REGAD = 0x1	PHY2 Basic Status Register
PHYAD = 0x2, REGAD = 0x2	PHY2 Physical Identifier I
PHYAD = 0x2, REGAD = 0x3	PHY2 Physical Identifier II
PHYAD = 0x2, REGAD = 0x4	PHY2 Auto-Negotiation Advertisement Register
PHYAD = 0x2, REGAD = 0x5	PHY2 Auto-Negotiation Link Partner Ability Register
PHYAD = 0x2, 0x6 – 0x1C	PHY2 Not supported
PHYAD = 0x2, 0x1D	PHY2 LinkMD Control/Status
PHYAD = 0x2, 0x1E	PHY2 Not supported
PHYAD = 0x2, 0x1F	PHY2 Special Control/Status

4.2 Register Descriptions

TABLE 4-2: REGISTER DESCRIPTIONS

Bit	Name	R/W	Description	Default	Reference
PHY1 Register 0 (PHYAD = 0x1, REGAD = 0x0): MII Basic Control PHY2 Register 0 (PHYAD = 0x2, REGAD = 0x0): MII Basic Control					
15	Soft Reset	RO	Not Supported	0	—
14	Loopback	R/W	1 = Perform loopback, as indicated: Port 1 Loopback (reg. 29, bit 0 = ‘1’) Start: RXP2/RXM2 (port 2) Loopback: PMD/PMA of port 1’s PHY End: TXP2/TXM2 (port 2) Port 2 Loopback (reg. 45, bit 0 = ‘1’) Start: RXP1/RXM1 (port 1) Loopback: PMD/PMA of port 2’s PHY End: TXP1/TXM1 (port 1) 0 = Normal operation	0	Reg. 29, bit 0 Reg. 45, bit 0
13	Force 100	R/W	1 = 100 Mbps 0 = 10 Mbps	0	Reg. 28, bit 6 Reg. 44, bit 6
12	AN Enable	R/W	1 = Auto-negotiation enabled 0 = Auto-negotiation disabled	1	Reg. 28, bit 7 Reg. 44, bit 7
11	Power Down	R/W	1 = Power down 0 = Normal operation	0	Reg. 29, bit 3 Reg. 45, bit 3
10	Isolate	RO	Not Supported	0	—
9	Restart AN	R/W	1 = Restart auto-negotiation 0 = Normal operation	0	Reg. 29, bit 5 Reg. 45, bit 5
8	Force Full-Duplex	R/W	1 = Full-duplex 0 = Half-duplex	0	Reg. 28, bit 5 Reg. 44, bit 5
7	Collision Test	RO	Not Supported	0	—
6	Reserved	RO	—	0	—
5	Hp_mdix	R/W	1 = HP Auto MDI/MDI-X mode 0 = Microchip Auto MDI/MDI-X mode	1	Reg. 31, bit 7 Reg. 47, bit 7
4	Force MDI	R/W	1 = Force MDI (transmit on RXP/RXM pins) 0 = Normal operation (transmit on TXP/TXM pins)	0	Reg. 29, bit 1 Reg. 45, bit 1
3	Disable MDIX	R/W	1 = Disable auto MDI-X 0 = Enable auto MDI-X	0	Reg. 29, bit 2 Reg. 45, bit 2
2	Disable Far-End Fault	R/W	1 = Disable far-end fault detection 0 = Normal operation	0	Reg. 29, bit 4
1	Disable Transmit	R/W	1 = Disable transmit 0 = Normal operation	0	Reg. 29, bit 6 Reg. 45, bit 6
0	Disable LED	R/W	1 = Disable LED 0 = Normal operation	0	Reg. 29, bit 7 Reg. 45, bit 7
PHY1 Register 1 (PHYAD = 0x1, REGAD = 0x1): MII Basic Status PHY2 Register 1 (PHYAD = 0x2, REGAD = 0x1): MII Basic Status					
15	T4 Capable	RO	0 = Not 100BASE-T4 capable	0	—
14	100 Full Capable	RO	1 = 100BASE-TX full-duplex capable 0 = Not capable of 100BASE-TX full-duplex	1	Always 1
13	100 Half Capable	RO	1 = 100BASE-TX half-duplex capable 0 = Not 100BASE-TX half-duplex capable	1	Always 1
12	10 Full Capable	RO	1 = 10BASE-T full-duplex capable 0 = Not 10BASE-T full-duplex capable	1	Always 1

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Bit	Name	R/W	Description	Default	Reference
11	10 Half Capable	RO	1 = 10BASE-T half-duplex capable 0 = Not 10BASE-T half-duplex capable	1	Always 1
10-7	Reserved	RO	—	0000	—
6	Preamble Suppressed	RO	Not Supported	0	—
5	AN Complete	RO	1 = Auto-negotiation complete 0 = Auto-negotiation not completed	0	Reg. 30, bit 6 Reg. 46, bit 6
4	Far-End Fault	RO	1 = Far-end fault detected 0 = No far-end fault detected	0	Reg. 31, bit 0
3	AN Capable	RO	1 = Auto-negotiation capable 0 = Not auto-negotiation capable	1	Reg. 28, bit 7 Reg. 44, bit 7
2	Link Status	RO	1 = Link is up 0 = Link is down	0	Reg. 30, bit 5 Reg. 46, bit 5
1	Jabber Test	RO	Not Supported	0	—
0	Extended Capable	RO	0 = Not extended register capable	0	—
PHY1 Register 2 (PHYAD = 0x1, REGAD = 0x2): PHYID High PHY2 Register 2 (PHYAD = 0x2, REGAD = 0x2): PHYID High					
15-0	PHYID High	RO	High order PHYID bits	0x0022	—
PHY1 Register 3 (PHYAD = 0x1, REGAD = 0x3): PHYID Low PHY2 Register 3 (PHYAD = 0x2, REGAD = 0x3): PHYID Low					
15-0	PHYID Low	RO	Low order PHYID bits	0x1430	—
PHY1 Register 4 (PHYAD = 0x1, REGAD = 0x4): Auto-Negotiation Advertisement Ability PHY2 Register 4 (PHYAD = 0x2, REGAD = 0x4): Auto-Negotiation Advertisement Ability					
15	Next Page	RO	Not Supported	0	—
14	Reserved	RO	—	0	—
13	Remote Fault	RO	Not Supported	0	—
12-11	Reserved	RO	—	00	—
10	Pause	R/W	1 = Advertise pause ability 0 = Do not advertise pause ability	1	Reg. 28, bit 4 Reg. 44, bit 4
9	Reserved	R/W	—	0	—
8	Adv 100 Full	R/W	1 = Advertise 100 full-duplex ability 0 = Do not advertise 100 full-duplex ability	1	Reg. 28, bit 3 Reg. 44, bit 3
7	Adv 100 Half	R/W	1 = Advertise 100 half-duplex ability 0 = Do not advertise 100 half-duplex ability	1	Reg. 28, bit 2 Reg. 44, bit 2
6	Adv 10 Full	R/W	1 = Advertise 10 full-duplex ability 0 = Do not advertise 10 full-duplex ability	1	Reg. 28, bit 1 Reg. 44, bit 1
5	Adv 10 Half	R/W	1 = Advertise 10 half-duplex ability 0 = Do not advertise 10 half-duplex ability	1	Reg. 28, bit 0 Reg. 44, bit 0
4-0	Selector Field	RO	802.3	00001	—
PHY1 Register 5 (PHYAD = 0x1, REGAD = 0x5): Auto-Negotiation Link Partner Ability PHY2 Register 5 (PHYAD = 0x2, REGAD = 0x5): Auto-Negotiation Link Partner Ability					
15	Next Page	RO	Not Supported	0	—
14	LP ACK	RO	Not Supported	0	—
13	Remote Fault	RO	Not Supported	0	—
12-11	Reserved	RO	—	00	—

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Bit	Name	R/W	Description	Default	Reference
10	Pause	RO	Link partner pause capability	0	Reg. 30, bit 4 Reg. 46, bit 4
9	Reserved	RO	—	0	—
8	Adv 100 Full	RO	Link partner 100 full-duplex capability	0	Reg. 30, bit 3 Reg. 46, bit 3
7	Adv 100 Half	RO	Link partner 100 half-duplex capability	0	Reg. 30, bit 2 Reg. 46, bit 2
6	Adv 10 Full	RO	Link partner 10 full-duplex capability	0	Reg. 30, bit 1 Reg. 46, bit 1
5	Adv 10 Half	RO	Link partner 10 half-duplex capability	0	Reg. 30, bit 0 Reg. 46, bit 0
4-0	Reserved	RO	—	00000	—
PHY1 Register 29 (PHYAD = 0x1, REGAD = 0x1D): LINKMD Control/Status **PHY2 Register 29 (PHYAD = 0x2, REGAD = 0x1D): LINKMD Control/Status**					
15	Vct_enable	R/W (SC)	1 = Enable cable diagnostic. After VCT test has completed, this bit will be self-cleared. 0 = Indicate cable diagnostic test (if enabled) has completed and the status information is valid for read.	0	Reg. 26, bit 4 Reg. 42, bit 4
14-13	Vct_result	RO	00 = Normal condition 01 = Open condition detected in cable 10 = Short condition detected in cable 11 = Cable diagnostic test has failed	00	Reg 26, bit[6:5] Reg 42, bit[6:5]
12	Vct 10M Short	RO	1 = Less than 10 meter short	0	Reg. 26, bit 7 Reg. 42, bit 7
11-9	Reserved	RO	Reserved	000	—
8-0	Vct_-fault_count	RO	Distance to the fault. It's approximately 0.4m*vct_fault_count[8:0]	{0, (0x00)}	{(Reg. 26, bit 0), (Reg. 27, bit[7:0])} {(Reg. 42, bit 0), (Reg. 43, bit[7:0])}
PHY1 Register 31 (PHYAD = 0x1, REGAD = 0x1F): PHY Special Control/Status **PHY2 Register 31 (PHYAD = 0x2, REGAD = 0x1F): PHY Special Control/Status**					
15-6	Reserved	RO	Reserved	{(0x00),00}	—
5	Polrvs	RO	1 = Polarity is reversed 0 = Polarity is not reversed	0	Reg. 31, bit 5 Reg. 47, bit 5
4	MDI-X status	RO	1 = MDI 0 = MDI-X	0	Reg. 30, bit 7 Reg. 46, bit 7
3	Force_lnk	R/W	1 = Force link pass 0 = Normal Operation	0	Reg. 26, bit 3 Reg. 42, bit 3
2	Pwrsave	R/W	0 = Enable power saving 1 = Disable power saving	1	Reg. 26, bit 2 Reg. 42, bit 2
1	Remote Loopback	R/W	1 = Perform Remote loopback, as follows: Port 1 (reg. 26, bit 1 = '1') Start: RXP1/RXM1 (port 1) Loopback: PMD/PMA of port 1's PHY End: TXP1/TXM1 (port 1) Port 2 (reg. 42, bit 1 = '1') Start: RXP2/RXM2 (port 2) Loopback: PMD/PMA of port 2's PHY End: TXP2/TXM2 (port 2) 0 = Normal Operation	0	Reg. 26, bit 1 Reg. 42, bit 1

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Bit	Name	R/W	Description	Default	Reference
0	Reserved	R/W	Reserved Do not change the default value.	0	—

4.3 Register Map: Switch, PHY, TS-1000 Media Converter (8-bit registers)

TABLE 4-3: GLOBAL REGISTERS

Register (Decimal)	Register (Hex)	Description
0-1	0x00-0x01	Chip ID Register
2-15	0x02-0x0F	Global Control Register

TABLE 4-4: PORT REGISTERS

Register (Decimal)	Register (Hex)	Description
16-29	0x10-0x1D	Port 1 Control Registers, including MII PHY Registers
30-31	0x1E-0x1F	Port 1 Status Registers, including MII PHY Registers
32-45	0x20-0x2D	Port 2 Control Registers, including MII PHY Registers
46-47	0x2E-0x2F	Port 2 Status Registers, including MII PHY Registers
48-57	0x30-0x39	Port 3 Control Registers
58-62	0x3A-0x3E	Reserved
63	0x3F	Port 3 Status Register

TABLE 4-5: TS-1000 MEDIA CONVERTER REGISTERS

Register (Decimal)	Register (Hex)	Description
64	0x40	PHY Address
65	0x41	Center Side Status
66	0x42	Center Side Command
67	0x43	PHY-SW Initialize
68	0x44	Loopback Setup1
69	0x45	Loopback Setup2
70	0x46	Loopback Result Counter for CRC Error
71	0x47	Loopback Result Counter for Timeout
72	0x48	Loopback Result Counter for Good Packet
73	0x48	Additional Status
74	0x4A	Remote Command1
75	0x4B	Remote Command2
76	0x4C	Remote Command3
77	0x4D	Valid MC Packet Transmitted Counter
78	0x4E	Valid MC Packet Received Counter
79	0x4F	Shadow of Register 0x58h
80	0x50	My Status 1
81	0x51	My Status 2
82	0x52	My Vendor Info (1)
83	0x53	My Vendor Info (2)
84	0x54	My Vendor Info (3)
85	0x55	My Model Info (1)

TABLE 4-5: TS-1000 MEDIA CONVERTER REGISTERS (CONTINUED)

Register (Decimal)	Register (Hex)	Description
86	0x56	My Model Info (2)
87	0x57	My Model Info (3)
88	0x58	LNK Partner Status (1)
89	0x59	LNK Partner Status (2)
90	0x5A	LNK Partner Vendor Info (1)
91	0x5B	LNK Partner Vendor Info (2)
92	0x5C	LNK Partner Vendor Info (3)
93	0x5D	LNK Partner Model Info (1)
94	0x5E	LNK Partner Model Info (2)
95	0x5F	LNK Partner Model Info (3)

TABLE 4-6: ADVANCED CONTROL REGISTERS

Register (Decimal)	Register (Hex)	Description
96-111	0x60-0x6F	TOS Priority Control Registers
112-117	0x70-0x75	Switch Engine's MAC Address Registers
118-120	0x76-0x78	User Defined Registers
121-122	0x79-0x7A	Indirect Access Control Registers
123-131	0x7B-0x83	Indirect Data Registers
132	0x84	Digital Testing Status Register
133	0x85	Digital Testing Control Register
134-137	0x86-0x89	Analog Testing Control Registers
138	0x8A	Analog Testing Status Register
139	0x8B	Analog Testing Control Register
140-141	0x8C-0x8D	QM Debug Registers

4.4 Register Descriptions

TABLE 4-7: GLOBAL REGISTERS (0-15)

Bit	Name	R/W	Description	Default
Register 0 (0x00): Chip ID0				
7-0	Family ID	RO	Chip family	0x88
Register 1 (0x01): Chip ID1/Start Switch				
7-4	Chip ID	RO	Chip ID	0xA
3-1	Revision ID	RO	Revision ID	—

TABLE 4-7: GLOBAL REGISTERS (0-15) (CONTINUED)

Bit	Name	R/W	Description	Default
0	Start Switch	R/W	1 = Start the chip when external pins (PS1, PS0) = (0,1) or (1,0) or (1,1). **Note:** In (PS1, PS0) = (0, 0) mode, the chip will start automatically after trying to read the external EEPROM. If EEPROM does not exist, the chip will use pin strapping and default values for all internal registers. If EEPROM is present, the contents in the EEPROM will be checked. The switch will check: (1) Register 0 = 0x88, (2) Register 1 bits [7:4] = 0xA. If this check is OK, the contents in the EEPROM will override chip registers' default values. 0 = Chip will not start when external pins (PS1, PS0) = (0,1) or (1,0) or (1,1).	1
Register 2 (0x02): Global Control 0				
7	New Back-Off Enable	R/W	New back-off algorithm designed for UNH 1 = Enable 0 = Disable	0
6-4	Reserved	RO	Reserved, Do not change the default value	100
3	Pass Flow Control Packet	R/W	1 = Switch will pass 802.1x flow control packets 0 = Switch will drop 802.1x flow control packets	0
2	Reserved	R/W	Reserved Do not change the default value.	1
1	Reserved	R/W	Reserved Do not change the default value.	0
0	Link Change Age	R/W	Link change from "link" to "no link" will cause fast aging (<800 µs) to age address table faster. After an age cycle is complete, the age logic will return to normal aging (about 200 sec). 1 = Enable 0 = Disable Note: If any port is unplugged, all addresses will be automatically aged out.	0
Register 3 (0x03): Global Control 1				
7	Pass All Frames	R/W	1 = Switch all packets including bad ones. Used solely for debugging purposes. Works in conjunction with sniffer mode only.	0
6	Reserved	R/W	Reserved Do not change the default value.	0
5	IEEE 802.3x Transmit Direction Flow Control Enable	R/W	1 = Will enable transmit direction flow control feature. 0 = Will not enable transmit direction flow control feature. Switch will not generate any flow control (PAUSE) frame.	1
4	IEEE 802.3x Receive Direction Flow Control Enable	R/W	1 = Will enable receive direction flow control feature. 0 = Will not enable receive direction flow control feature. Switch will not react to any flow control (PAUSE) frame it receives.	1
3	Frame Length Field Check	R/W	1 = Will check frame length field in the IEEE packets. If the actual length does not match, the packet will be dropped (for Length/Type field < 1500). 0 = Will not check	0

TABLE 4-7: GLOBAL REGISTERS (0-15) (CONTINUED)

Bit	Name	R/W	Description	Default
2	Aging Enable	R/W	1 = Enable age function in the chip 0 = Disable age function in the chip	Invert of P2LED3 (pin 20) value during reset Note: P2LED3 has internal pull-down.
1	Fast Age Enable	R/W	1 = Turn on fast age (800 µs)	0
0	Aggressive Back-Off Enable	R/W	1 = Enable more aggressive back off algorithm in half-duplex mode to enhance performance. This is not an IEEE standard.	0
Register 4 (0x04): Global Control 2				
7	Unicast Port-VLAN Mismatch Discard	R/W	This feature is used with port-VLAN (described in reg. 17, reg. 33, etc.) 1 = All packets cannot cross VLAN boundary 0 = Unicast packets (excluding unknown/multicast/broadcast) can cross VLAN boundary Note: Port mirroring is not supported if this bit is set to “0”.	1
6	Multicast Storm Protection Disable	R/W	1 = Broadcast Storm Protection does not include multicast packets. Only DA = FF-FF-FF-FF-FF-FF packets will be regulated. 0 = Broadcast Storm Protection includes DA = FF-FF-FF-FF-FF-FF and DA[40] = 1 packets.	1
5	Back Pressure Mode	R/W	1 = Carrier sense based back pressure is selected 0 = Collision based back pressure is selected	1
4	Flow Control and Back Pressure Fair Mode	R/W	1 = Fair mode is selected. In this mode, if a flow control port and a non-flow control port talk to the same destination port, packets from the non-flow control port may be dropped. This is to prevent the flow control port from being flow controlled for an extended period of time. 0 = In this mode, if a flow control port and a non-flow control port talk to the same destination port, the flow control port will be flow controlled. This may not be “fair” to the flow control port.	1
3	No Excessive Collision Drop	R/W	1 = The switch will not drop packets when 16 or more collisions occur. 0 = The switch will drop packets when 16 or more collisions occur.	0
2	Huge Packet Support	R/W	1 = Will accept packet sizes up to 1916 bytes (inclusive). This bit setting will override setting from bit 1 of this register. 0 = The max packet size will be determined by bit 1 of this register.	0
1	Legal Maximum Packet Size Check Enable	R/W	0 = Will accept packet sizes up to 1536 bytes (inclusive). 1 = 1522 bytes for tagged packets, 1518 bytes for untagged packets. Any packets larger than the specified value will be dropped.	SMRXD0 (pin 85) value during reset

TABLE 4-7: GLOBAL REGISTERS (0-15) (CONTINUED)

Bit	Name	R/W	Description	Default
0	Priority Buffer Reserve	R/W	1 = Each port is pre-allocated 48 buffers for high priority (q3, q2, and q1) packets. This selection is effective only when the multiple queue feature is turned on. It is recommended to enable this bit for multiple queue. 0 = No reserved buffers for high priority packets. Each port is pre-allocated 48 buffers for all priority packets (q3, q2,q1, and q0).	1
Register 5 (0x05): Global Control 3				
7	802.1Q VLAN Enable	R/W	1 = 802.1Q VLAN mode is turned on. VLAN table needs to set up before the operation. 0 = 802.1Q VLAN is disabled.	0
6	IGMP Snoop Enable on Switch MII Interface	R/W	1 = IGMP snoop is enabled. All IGMP packets will be forwarded to the Switch MII port. 0 = IGMP snoop is disabled.	0
5	IPv6 MLD Snooping Enable	R/W	IPv6 MLD snooping 1 = Enable 0 = Disable	0
4	IPv6 MLD Snooping Option	R/W	IPv6 MLD snooping option 1 = Enable 0 = Disable	0
3	Weighted Fair Queue Enable	R/W	0 = Always transmit higher priority packets first 1 = Weighted Fair Queuing enabled. When all four queues have packets waiting to transmit, the bandwidth allocation is q3:q2:q1:q0 = 8:4:2:1. If any queues are empty, the highest non-empty queue gets one more weighting. For example, if q2 is empty, q3:q2:q1:q0 becomes (8+1):0:2:1.	0
2-1	Reserved	R/W	Reserved Do not change the default values.	00
0	Sniff Mode Select	R/W	1 = Will do RX AND TX sniff (both source port and destination port need to match) 0 = Will do RX OR TX sniff (either source port or destination port needs to match). This is the mode used to implement RX only sniff.	0
Register 6 (0x06): Global Control 4				
7	Repeater Mode	R/W	1 = Enable repeater mode 0 = Disable repeater mode Note: For repeater mode, all ports need to be set to 100BASE-TX and half duplex mode. PHY ports need to have auto-negotiation disabled.	0
6	Switch MII Half-Duplex Mode	R/W	1 = Enable MII interface half-duplex mode. 0 = Enable MII interface full-duplex mode.	Pin SMRXD2 strap option. Pull-down(0): Full-duplex mode Pull-up(1): Half-duplex mode Note: SMRXD2 has internal pull-down.

TABLE 4-7: GLOBAL REGISTERS (0-15) (CONTINUED)

Bit	Name	R/W	Description	Default
5	Switch MII Flow Control Enable	R/W	1 = Enable full-duplex flow control on Switch MII interface. 0 = Disable full-duplex flow control on Switch MII interface.	Pin SMRXD3 strap option. Pull-down(0): Disable flow control Pull-up(1): Enable flow control Note: SMRXD3 has internal pull-down.
4	Switch MII 10BT	R/W	1 = The Port 3 MII switch interface is in 10 Mbps mode 0 = The Port 3 MII switch interface is in 100 Mbps mode	Pin SMRXD1 strap option. Pull-down(0): Enable 100 Mbps Pull-up(1): Enable 10 Mbps Note: SMRXD1 has internal pull-down.
3	Null VID Replacement	R/W	1 = Will replace NULL VID with port VID (12 bits) 0 = No replacement for NULL VID	0
2-0	Broadcast Storm Protection Rate Bit [10:8]	R/W	This register along with the next register determines how many “64 byte blocks” of packet data are allowed on an input port in a preset period. The period is 67 ms for 100BT or 500 ms for 10BT. The default is 1%.	000
Register 7 (0x07): Global Control 5				
7-0	Broadcast Storm Protection Rate Bit [7:0]	R/W	This register along with the previous register determines how many “64 byte blocks” of packet data are allowed on an input port in a preset period. The period is 67 ms for 100BT or 500 ms for 10BT. The default is 1%. Note: 100BT Rate: 148,800 frames/sec * 67 ms/interval * 1% = 99 frames/interval (approx.) = 0x63	0x63
Register 8 (0x08): Global Control 6				
7-0	Factory Testing	R/W	Reserved Do not change the default values.	0x00
Register 9 (0x09): Global Control 7				
7-0	Factory Testing	R/W	Reserved Do not change the default values.	0x24
Register 10 (0x0A): Global Control 8				
7-0	Factory Testing	R/W	Reserved Do not change the default values.	0x35
Register 11 (0x0B): Global Control 9				
7	LEDSEL1	R/W	LED mode select See description in bit 1 of this register.	LEDSEL1 (pin 23) value during reset
6	Reserved	R/W	Reserved Do not change the default values.	0

TABLE 4-7: GLOBAL REGISTERS (0-15) (CONTINUED)

Bit	Name	R/W	Description	Default
5	CRC Drop	R/W	In TS-1000 MC loopback mode, 1 = Drop OAM frames and Ethernet frames with the following errors: CRC, undersize, oversize. Loop back Ethernet frames with only good CRC and valid length. 0 = Drop OAM frames only. Loop back all Ethernet frames including those with errors.	P1LCRCD (pin 18) value during reset
4	Reserved	R/W	Testing mode. Set to '0' for normal operation.	0
3	MCLBM1	R/W	MCLBM1 MCLBM0 Loopback position 0 0 at Port 2 UTP 1 0 at Port 2 MAC (default) x 1 at Port 1 OPT Note: If MCLBM0 is set to '1', MCLBM1 is a "Don't care".	1
2	MCLBM0			P1LPBM (pin 19) value during reset
1	LEDSEL0	R/W	LED mode select This bit and bit 7 of this register select the LED mode. For LED definitions, see pins 1, 2, 3, 4, 5, and 6 of Pin Description and I/O Assignment listing. Notes: LEDSEL1 is also external strap-in pin 23. LEDSEL0 is also external strap-in pin 70.	LEDSEL0 (pin 70) value during reset
0	Special TPID Mode	R/W	Used for direct mode forwarding from port 3. See description in spanning tree functional description. 0 = Disable 1 = Enable	0
Register 12 (0x0C): Global Control 10				
7-6	Tag_0x3	R/W	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x3.	01
5-4	Tag_0x2	R/W	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x2.	01
3-2	Tag_0x1	R/W	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x1.	00
1-0	Tag_0x0	R/W	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x0.	00
Register 13 (0x0D): Global Control 11				
7-6	Tag_0x7	R/W	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x7.	11
5-4	Tag_0x6	R/W	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x6.	11
3-2	Tag_0x5	R/W	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x5.	10
1-0	Tag_0x4	R/W	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x4.	10

TABLE 4-7: GLOBAL REGISTERS (0-15) (CONTINUED)

Bit	Name	R/W	Description	Default
Register 14 (0x0E): Global Control 12				
7	Unknown Packet Default Port Enable	R/W	Send packets with unknown destination MAC addresses to specified port(s) in bits [2:0] of this register. 0 = Disable 1 = Enable	0
6-3	Reserved	R/W	Reserved Do not change the default values.	0x0
2-0	Unknown Packet Default Port	R/W	Specify which port(s) to send packets with unknown destination MAC addresses. This feature is enabled by bit [7] of this register. Bit 2 stands for port 3. Bit 1 stands for port 2. Bit 0 stands for port 1. A ‘1’ includes a port. A ‘0’ excludes a port.	111
Register 15 (0x0F): Global Control 13				
7-3	PHY Address	R/W	00000: N/A 00001: Port 1 PHY address is 0x1 00010: Port 1 PHY address is 0x2 … 11101: Port 1 PHY address is 0x29 11110: N/A 11111: N/A Note: Port 2 PHY address = (Port 1 PHY address) + 1	00001
2-0	Reserved	RO	Reserved Do not change the default values.	000

The following registers are used to enable features that are assigned on a per port basis. The register bit assignments are the same for all ports, but the address for each port is different, as indicated.

TABLE 4-8: PORT REGISTERS (REGISTERS 16 - 95)

Bit	Name	R/W	Description	Default
Register 16 (0x10): Port 1 Control 0 **Register 32 (0x20): Port 2 Control 0** **Register 48 (0x30): Port 3 Control 0**				
7	Broadcast Storm Protection Enable	R/W	1 = Enable broadcast storm protection for ingress packets on port 0 = Disable broadcast storm protection	0
6	DiffServ Priority Classification Enable	R/W	1 = Enable DiffServ priority classification for ingress packets (IPv4 and IPv6) on port 0 = Disable DiffServ function	0
5	802.1p Priority Clas-sification Enable	R/W	1 = Enable 802.1p priority classification for ingress packets on port 0 = Disable 802.1p	0
4-3	Port-based Priority Classification	R/W	00 = Ingress packets on port will be classified as priority 0 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. 01 = Ingress packets on port will be classified as priority 1 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. 10 = Ingress packets on port will be classified as priority 2 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. 11 = Ingress packets on port will be classified as priority 3 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. Note: “DiffServ,” “802.1p,” and port priority can be enabled at the same time. The OR’ed result of 802.1p and DSCP overwrites the port priority.	00
2	Tag Insertion	R/W	1 = When packets are output on the port, the switch will add 802.1p/q tags to packets without 802.1p/q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port’s “port VID”. 0 = Disable tag insertion	0
1	Tag Removal	R/W	1 = When packets are output on the port, the switch will remove 802.1p/q tags from packets with 802.1p/q tags when received. The switch will not modify pack-ets received without tags. 0 = Disable tag removal	0
0	TX Multiple Queues Select Enable	R/W	1 = The port output queue is split into four priority queues. 0 = Single output queue on the port. There is no prior-ity differentiation even though packets are classified into high or low priority.	0
Register 17 (0x11): Port 1 Control 1 **Register 33 (0x21): Port 2 Control 1** **Register 49 (0x31): Port 3 Control 1**				
7	Sniffer Port	R/W	1 = Port is designated as sniffer port and will transmit packets that are monitored. 0 = Port is a normal port	0

TABLE 4-8: PORT REGISTERS (REGISTERS 16 - 95) (CONTINUED)

Bit	Name	R/W	Description	Default
6	Receive Sniff	R/W	1 = All packets received on the port will be marked as “monitored packets” and forwarded to the designated “sniffer port” 0 = No receive monitoring	0
5	Transmit Sniff	R/W	1 = All packets transmitted on the port will be marked as “monitored packets” and forwarded to the designated “sniffer port” 0 = No transmit monitoring	0
4	Double Tag	R/W	1 = All packets will be tagged with port default tag of ingress port regardless of the original packets are tagged or not 0 = Do not double tagged on all packets	0
3	User Priority Ceiling	R/W	1 = If the packet’s “user priority field” is greater than the “user priority field” in the port default tag register, replace the packet’s “user priority field” with the “user priority field” in the port default tag register. 0 = Do not compare and replace the packet’s ‘user priority field”	0
2-0	Port VLAN Membership	R/W	Define the port’s egress port VLAN membership. The port can only communicate within the membership. Bit 2 stands for port 3, bit 1 stands for port 2, bit 0 stands for port 1. A ‘1’ includes a port in the membership. A ‘0’ excludes a port from membership.	111
Register 18 (0x12): Port 1 Control 2 **Register 34 (0x22): Port 2 Control 2** **Register 50 (0x32): Port 3 Control 2**				
7	Reserved	R/W	Reserved Do not change the default values.	0
6	Ingress VLAN Filtering	R/W	1 = The switch will discard packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port. 0 = No ingress VLAN filtering.	0
5	Discard non-PVID Packets	R/W	1 = The switch will discard packets whose VID does not match ingress port default VID. 0 = No packets will be discarded	0
4	Force Flow Control	R/W	1 = Will always enable full-duplex flow control on the port, regardless of AN result. 0 = Full-duplex flow control is enabled based on AN result.	Pin value during reset: For port 1, P1FFC pin For port 2, P2FFC pin For port 3, this bit has no meaning. Flow control is set by Reg. 6, bit 5.
3	Back Pressure Enable	R/W	1 = Enable port’s half-duplex back pressure 0 = Disable port’s half-duplex back pressure	0
2	Transmit Enable	R/W	1 = Enable packet transmission on the port 0 = Disable packet transmission on the port Note: This bit is used for spanning tree support.	1

TABLE 4-8: PORT REGISTERS (REGISTERS 16 - 95) (CONTINUED)

Bit	Name	R/W	Description	Default
1	Receive Enable	R/W	1 = Enable packet reception on the port 0 = Disable packet reception on the port Note: This bit is used for spanning tree support.	1
0	Learning Disable	R/W	1 = Disable switch address learning capability 0 = Enable switch address learning Note: This bit is used for spanning tree support.	0
Register 19 (0x13): Port 1 Control 3 **Register 35 (0x23): Port 2 Control 3** **Register 51 (0x33): Port 3 Control 3**				
7-0	Default Tag [15:8]	R/W	Port’s default tag, containing 7-5 = User priority bits 4 = CFI bit 3-0 = VID[11:8]	0x00
Register 20 (0x14): Port 1 Control 4 **Register 36 (0x24): Port 2 Control 4** **Register 52 (0x34): Port 3 Control 4**				
7-0	Default Tag [7:0]	R/W	Port’s default tag, containing 7-0: VID[7:0]	0x01
Note: Registers 19 and 20 (and those corresponding to other ports) serve two purposes: Associated with the ingress untagged packets, and used for egress tagging. Default VID for the ingress untagged or null-VID-tagged packets, and used for address lookup.				
Register 21 (0x15): Port 1 Control 5 **Register 37 (0x25): Port 2 Control 5** **Register 53 (0x35): Port 3 Control 5**				
7-4	Reserved	R/W	Reserved Do not change the default values.	0x0
3-2	Limit Mode	R/W	Ingress Limit Mode These bits determine what kinds of frames are limited and counted against ingress rate limiting. 00 = Limit and count all frames 01 = Limit and count Broadcast, Multicast, and flooded unicast frames 10 = Limit and count Broadcast and Multicast frames only 11 = Limit and count Broadcast frames only	00
1	Count IFG	R/W	Count IFG bytes 1 = Each frame’s minimum inter frame gap (IFG) bytes (12 per frame) are included in Ingress and Egress rate limiting calculations. 0 = IFG bytes are not counted.	0
0	Count Pre	R/W	Count Preamble bytes 1 = Each frame’s preamble bytes (8 per frame) are included in Ingress and Egress rate limiting calculations. 0 = Preamble bytes are not counted.	0

TABLE 4-8: PORT REGISTERS (REGISTERS 16 - 95) (CONTINUED)

Bit	Name	R/W	Description	Default
Register 22 [6:0] (0x16): Port 1 Control 6 **Register 38 [6:0] (0x26): Port 2 Control 6** **Register 54 [6:0] (0x36): Port 3 Control 6**				
7-4	Ingress Pri1 Rate	R/W	Ingress data rate limit for priority 1 frames Ingress traffic from this priority queue is shaped according to the ingress rate selected below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (Not limited).	0x0
3-0	Ingress Pri0 Rate	R/W	Ingress data rate limit for priority 0 frames Ingress traffic from this priority queue is shaped according to the ingress rate selected below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (Not limited).	0x0

TABLE 4-8: PORT REGISTERS (REGISTERS 16 - 95) (CONTINUED)

Bit	Name	R/W	Description	Default
Register 23 [6:0] (0x17): Port 1 Control 7 **Register 39 [6:0] (0x27): Port 2 Control 7** **Register 55 [6:0] (0x37): Port 3 Control 7**				
7-4	Ingress Pri3 Rate	R/W	Ingress data rate limit for priority 3 frames Ingress traffic from this priority queue is shaped according to the ingress rate selected below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (Not limited).	0x0
3-0	Ingress Pri2 Rate	R/W	Ingress data rate limit for priority 2 frames Ingress traffic from this priority queue is shaped according to the ingress rate selected below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (Not limited).	0x0

TABLE 4-8: PORT REGISTERS (REGISTERS 16 - 95) (CONTINUED)

Bit	Name	R/W	Description	Default
Register 24 [6:0] (0x18): Port 1 Control 8 Register 40 [6:0] (0x28): Port 2 Control 8 Register 56 [6:0] (0x38): Port 3 Control 8				
7-4	Egress Pri1 Rate	R/W	Egress data rate limit for priority 1 frames Egress traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (Not limited). When TX multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.	0x0
3-0	Egress Pri0 Rate	R/W	Egress data rate limit for priority 0 frames. Egress traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (Not limited). When TX multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.	0x0

TABLE 4-8: PORT REGISTERS (REGISTERS 16 - 95) (CONTINUED)

Bit	Name	R/W	Description	Default
Register 25 [6:0] (0x19): Port 1 Control 9 **Register 41 [6:0] (0x29): Port 2 Control 9** **Register 57 [6:0] (0x39): Port 3 Control 9**				
7-4	Egress Pri3 Rate	R/W	Egress data rate limit for priority 3 frames Egress traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (Not limited). When TX multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.	0x0
3-0	Egress Pri2 Rate	R/W	Egress data rate limit for priority 2 frames Egress traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (Not limited). When TX multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.	0x0
Note: Most of the contents in registers 26-31 and registers 42-47 for ports 1 and 2, respectively, can also be accessed with the MIIM PHY registers.				

TABLE 4-8: PORT REGISTERS (REGISTERS 16 - 95) (CONTINUED)

Bit	Name	R/W	Description	Default
Register 26 (0x1A): Port 1 PHY Special Control/Status **Register 42 (0x2A): Port 2 PHY Special Control/Status** **Register 58 (0x3A): Reserved, Not Applicable to Port 3**				
7	Vct 10M Short	RO	1 = Less than 10 meter short	0
6-5	Vct_result	RO	00 = Normal condition 01 = Open condition detected in cable 10 = Short condition detected in cable 11 = Cable diagnostic test has failed	00
4	Vct_en	R/W (SC)	1 = Enable cable diagnostic test. After VCT test has completed, this bit will be self-cleared. 0 = Indicate cable diagnostic test (if enabled) has completed and the status information is valid for read.	0
3	Force_lnk	R/W	1 = Force link pass 0 = Normal Operation	0
2	Pwrsave	R/W	0 = Enable power saving 1 = Disable power saving	1
1	Remote Loopback	R/W	1 = Perform Remote loopback, as follows: Port 1 (reg. 26, bit 1 = ‘1’) Start: RXP1/RXM1 (port 1) Loopback: PMD/PMA of port 1’s PHY End: TXP1/TXM1 (port 1) Port 2 (reg. 42, bit 1 = ‘1’) Start: RXP2/RXM2 (port 2) Loopback: PMD/PMA of port 2’s PHY End: TXP2/TXM2 (port 2) 0 = Normal Operation	0
0	Vct_fault_count[8]	RO	Bit[8] of VCT fault count Distance to the fault. It’s approximately 0.4m*vct_fault_count[8:0]	0
Register 27 (0x1B): Port 1 LINKMD Result **Register 43 (0x2B): Port 2 LINKMD Result** **Register 59 (0x3B): Reserved, Not Applicable to Port 3**				
7-0	Vct_fault_count[7:0]	RO	Bits[7:0] of VCT fault count Distance to the fault. It’s approximately 0.4m*Vct_fault_count[8:0]	0x00
Register 28 (0x1C): Port 1 Control 12 **Register 44 (0x2C): Port 2 Control 12** **Register 60 (0x3C): Reserved, Not Applicable to Port 3**				
7	Auto Negotiation Enable	R/W	1 = Auto negotiation is on 0 = Disable auto negotiation; speed and duplex are determined by bits 6 and 5 of this register.	For port 1, P1ANEN pin value during reset. For port 2, P2ANEN pin value during reset

TABLE 4-8: PORT REGISTERS (REGISTERS 16 - 95) (CONTINUED)

Bit	Name	R/W	Description	Default
6	Force Speed	R/W	1 = Forced 100BT if AN is disabled (bit 7) 0 = Forced 10BT if AN is disabled (bit 7)	For port 1, P1SPD pin value during reset. For port 2, P2SPD pin value during reset.
5	Force Duplex	R/W	1 = Forced full-duplex if (1) AN is disabled or (2) AN is enabled but failed. 0 = Forced half-duplex if (1) AN is disabled or (2) AN is enabled but failed.	For port 1, P1DPX pin value during reset. For port 2, P2DPX pin value during reset.
4	Advertise Flow Control Capability	R/W	1 = Advertise flow control (pause) capability 0 = Suppress flow control (pause) capability from transmission to link partner	ADVFC pin value during reset.
3	Advertise 100BT Full-Duplex Capability	R/W	1 = Advertise 100BT full-duplex capability 0 = Suppress 100BT full-duplex capability from transmission to link partner	1
2	Advertise 100BT Half-Duplex Capability	R/W	1 = Advertise 100BT half-duplex capability 0 = Suppress 100BT half-duplex capability from transmission to link partner	1
1	Advertise 10BT Full-Duplex Capability	R/W	1 = Advertise 10BT full-duplex capability 0 = Suppress 10BT full-duplex capability from transmission to link partner	1
0	Advertise 10BT Half-Duplex Capability	R/W	1 = Advertise 10BT half-duplex capability 0 = Suppress 10BT half-duplex capability from transmission to link partner	1
Register 29 (0x1D): Port 1 Control 13 **Register 45 (0x2D): Port 2 Control 13** **Register 61 (0x3D): Reserved, Not Applicable to Port 3**				
7	LED Off	R/W	1 = Turn off all port's LEDs (LEDx_3, LEDx_2, LEDx_1, LEDx_0, where "x" is the port number). These pins will be driven high if this bit is set to one. 0 = Normal operation	0
6	Txdis	R/W	1 = Disable the port's transmitter 0 = Normal operation	0
5	Restart AN	R/W	1 = Restart auto-negotiation 0 = Normal operation	0
4	Disable Far-End Fault	R/W	1 = Disable far-end fault detection and pattern transmission. 0 = Enable far-end fault detection and pattern transmission	0 Note: Only port 1 supports fiber. This bit is applicable to port 1 only.
3	Power Down	R/W	1 = Power down 0 = Normal operation	0

TABLE 4-8: PORT REGISTERS (REGISTERS 16 - 95) (CONTINUED)

Bit	Name	R/W	Description	Default
2	Disable Auto MDI/ MDI-X	R/W	1 = Disable auto MDI/MDI-X function 0 = Enable auto MDI/MDI-X function	0 For port 2, P2MDIXDIS pin value during reset.
1	Force MDI	R/W	If auto MDI/MDI-X is disabled, 1 = Force PHY into MDI mode (transmit on RXP/RXM pins) 0 = Force PHY into MDI-X mode (transmit on TXP/ TXM pins)	0 For port 2, P2MDIX pin value during reset.
0	Loopback	R/W	1 = Perform loopback, as indicated: Port 1 Loopback (reg. 29, bit 0 = ‘1’) Start: RXP2/RXM2 (port 2) Loopback: PMD/PMA of port 1’s PHY End: TXP2/TXM2 (port 2) Port 2 Loopback (reg. 45, bit 0 = ‘1’) Start: RXP1/RXM1 (port 1) Loopback: PMD/PMA of port 2’s PHY End: TXP1/TXM1 (port 1) 0 = Normal operation	0
Register 30 (0x1E): Port 1 Status 0 **Register 46 (0x2E): Port 2 Status 0** **Register 62 (0x3E): Reserved, Not Applicable to Port 3**				
7	MDI-X Status	RO	1 = MDI 0 = MDI-X	0
6	AN Done	RO	1 = Auto-negotiation completed 0 = Auto-negotiation not completed	0
5	Link Good	RO	1 = Link good 0 = Link not good	0
4	Partner Flow Con-trol Capability	RO	1 = Link partner flow control (pause) capable 0 = Link partner not flow control (pause) capable	0
3	Partner 100BT Full-Duplex Capability	RO	1 = Link partner 100BT full-duplex capable 0 = Link partner not 100BT full-duplex capable	0
2	Partner 100BT Half-Duplex Capability	RO	1 = Link partner 100BT half-duplex capable 0 = Link partner not 100BT half-duplex capable	0
1	Partner 10BT Full-Duplex Capability	RO	1 = Link partner 10BT full-duplex capable 0 = Link partner not 10BT full-duplex capable	0
0	Partner 10BT Half-Duplex Capability	RO	1 = Link partner 10BT half-duplex capable 0 = Link partner not 10BT half-duplex capable	0
Register 31 (0x1F): Port 1 Status 1 **Register 47 (0x2F): Port 2 Status 1** **Register 63 (0x3F): Port 3 Status 1**				
7	Hp_mdix	R/W	1 = HP Auto MDI/MDI-X mode 0 = Microchip Auto MDI/MDI-X mode	1 Note: Only ports 1 and 2 are PHY ports. This bit is not applicable to port 3 (MII).
6	Reserved	RO	Reserved Do not change the default value.	0

TABLE 4-8: PORT REGISTERS (REGISTERS 16 - 95) (CONTINUED)

Bit	Name	R/W	Description	Default
5	Polrvs	RO	1 = Polarity is reversed 0 = Polarity is not reversed	0 Note: Only ports 1 and 2 are PHY ports. This bit is not applicable to port 3 (MII).
4	Transmit Flow Control Enable	RO	1 = Transmit flow control feature is active 0 = Transmit flow control feature is inactive	0
3	Receive Flow Control Enable	RO	1 = Receive flow control feature is active 0 = Receive flow control feature is inactive	0
2	Operation Speed	RO	1 = Link speed is 100 Mbps 0 = Link speed is 10 Mbps	0
1	Operation Duplex	RO	1 = Link duplex is full 0 = Link duplex is half	0
0	Far-End Fault	RO	1 = Far-end fault status detected 0 = No far-end fault status detected	0 Note: Only port 1 supports fiber. This bit is applicable to port 1 only.

TABLE 4-9: TS-1000 MEDIA CONVERTER REGISTERS

Bit	Name	R/W	Description	Default
Register 64 (0x40): PHY Address				
7-5	Number of Indication OAM frame(s)	R/W	Set the number of Indication OAM frame(s) to be transmitted for a single OAM status change. This setting is applicable to only the following three OAM frames: Indicate Center MC Condition, Indicate Terminal MC Condition, and Loop Mode Stop Indication. 000 : send 1 OAM frame 001 : send 2 OAM frames 010 : send 3 OAM frames 011 : send 4 OAM frames 100 : send 5 OAM frames 101 : N/A 110 : N/A 111 : N/A	000
4	Addr4	R/W	These 5-bits set the PHY addresses for port 1 and port 2. 00000 : N/A 00001 : Port 1 PHY address is 0x1 00010 : Port 1 PHY address is 0x2 … 11101 : Port 1 PHY address is 0x29 11110 : N/A 11111 : N/A Port 2 PHY address = (Port 1 PHY address) + 1 Note: In Center side MC mode (pins MCHS,MCCS] = [0,1]), a write to these bits with port 1’s PHY address is required to enable port 1 and start the Center side MC.	0
3	Addr3	R/W		0
2	Addr2	R/W		0
1	Addr1	R/W		0
0	Addr0	R/W		1
Register 65 (0x41): Center Side Status				
7	BUSY	RO	1 = Indicate MC loop back mode in progress, or receive reply frame/timeout is pending 0 = Exclude the above situations	0
6	Vendor mode	R/W	1 = Non special vendor mode 0 = Special vendor mode (compare My & LNK Partner Vendor Info = 0x009099h)	0
5-3	Reserved	RO	Reserved Do not change the default values.	000
2	Option b	R/W	1 = Clear status bits S6 to S10 to zero on Terminal MC side 0 = Normal operation – supporting option b	0
1	Option a	R/W	1 = Disable “Indicate Center MC Condition” frame 0 = Enable “Indicate Center MC condition” frame	0
0	Request	RO	1 = indicate change of status/value in registers # 0x50h, 0x51h, 0x58h, 0x59h, 0x5Dh, 0x5Eh, 0x5Fh. This bit is self-cleared after a read. 0 = exclude the above situations	0
Note: Register 65 is managed by the Center side.				

TABLE 4-9: TS-1000 MEDIA CONVERTER REGISTERS (CONTINUED)

Bit	Name	R/W	Description	Default
Register 66 (0x42): Center Side Command				
7-5	Timer Delay	R/W	000 = Reserved (Do Not Use) 001 = 32 µs (default) 010 = 128 µs 011 = 256 µs 100 = 512 µs 101 = 1 ms 110 = 2 ms 111 = 4 ms	001
4	Com4	R/W	To send a maintenance frame, an external controller writes to these command bits via the SMI, SPI, or I^2C interface. 0 0000 : No request 0 0001 : Send “Condition Inform Request” frame 0 0010 : Send “Loop Mode Start Request” frame 0 0100 : Send “Loop Mode Stop Request” frame 0 1000 : Send “Remote Command”. Here, the Maintenance frame will be made up of the “Condition Inform Request/Reply” frame, but the My Model Info bits MM24-MM47 will be mapped to Registers 4Ah-4Ch, instead of Registers 55h-57h. 1 0000 : Send “Indicate Center/Terminal MC Condition” frame. Usually, “Indicate Center/Terminal MC Condition” frame will be sent automatically. But this OAM frame can be sent manually using this command. Other values : N/A Note: Except for the “Indicate Center/Terminal MC Condition” frame, all maintenance frames here are sent by the Center side MC only.	0
3	Com3	R/W		0
2	Com2	R/W		0
1	Com1	R/W		0
0	Com0	R/W		0
Register 67 (0x43): PHY-SW Initialize				
7	P2 SPEED	R/W	1 = 100 Mbps 0 = 10 Mbps This bit share the same physical register as Reg. 2Ch bit 6.	P2SPD pin value during reset
6	P2 DUPLEX	R/W	1 = Full-duplex 0 = Half-duplex This bit share the same physical register as Reg. 2Ch bit 5.	P2DPX pin value during reset
5	P2 Auto Negotiation	R/W	1 = AN enable 0 = AN disable This bit share the same physical register as Reg. 2Ch bit 7.	P2ANEN pin value during reset
4	SW Reset	R/W	1 = Reset MC sub-layer, MACs of both PHY ports and switch fabric to their default states. This bit is self-cleared after a ‘1’ is written to it. 0 = Normal operation	0
3	Remote Command Enable	R/W	1 = Enable “Remote Command” access at Center side and Terminal side 0 = Disable “Remote Command” access at Center side and Terminal side	0

TABLE 4-9: TS-1000 MEDIA CONVERTER REGISTERS (CONTINUED)

Bit	Name	R/W	Description	Default
2	Enhanced ML_EN	R/W	1 = Defined as follows: In Terminal side MC mode, if a link down is detected on the fiber or the Center side UTP, the Terminal side will disable the TX on its UTP and turn off the LEDs to its UTP. In Center side MC mode, this bit has no meaning. 0 = Normal operation	ML_EN pin value during reset
1	P1 TX_DIS	R/W	1 = Disable (tri-state) transmit to Fiber PHY (port 1) 0 = Normal operation	0
0	PHY Reset	R/W	1 = Reset the PHY of both PHY ports to their default states. This bit is self-cleared after a ‘1’ is written to it. 0 = Normal operation Note: MC (maintenance) sub-layer registers are not reset by this bit.	1 (Powered on value in Center side MC mode. After reg. 0x40h is programmed, this bit will be cleared.) -------------------- 0 (Default value for non Center side MC mode)
Register 68 (0x44): Loopback Setup 1				
7	T7	R/W	**Center and Terminal sides** 0000_0000 = Clear valid transmit and valid receive counters in registers 4Dh and 4Eh. Also for center side, clear loopback counters in registers 46h, 47h and 48h. **Center side only** 0000_0001 = Send 1 MC loopback packet 0000_0010 = Send 2 MC loopback packets : 0000_0111 = Send 7 MC loopback packets (default) : 0110_0100 = Send 100 MC loopback packets other values (0x65h to 0xFFh) : N/A	0
6	T6	R/W		0
5	T5	R/W		0
4	T4	R/W		0
3	T3	R/W		0
2	T2	R/W		1
1	T1	R/W		1
0	T0	R/W		1

TABLE 4-9: TS-1000 MEDIA CONVERTER REGISTERS (CONTINUED)

Bit	Name	R/W	Description	Default
Register 69 (0x45): Loopback Setup 2				
7	P7	R/W	**Center side only** Use to select pattern for MC loopback packet 0000_0000 = 64 bytes DA; Unicast Data: 55AA 0000_0001 = 1518 bytes DA; UnicastData: 55AA 0000_0010 = 64 bytes DA; Broadcast Data: 55AA 0000_0100 = 1518 bytes DA; Broadcast Data: 55AA 0000_1000 = 64 bytes DA; Unicast Data: 0F0F 0001_0000 = 1518 bytes DA; Unicast Data: 0F0F 0010_0000 = 64 bytes DA; Broadcast Data: 0F0F 0100_0000 = 1518 bytes DA; Broadcast Data: 0F0F 1000_0000 = 1518 bytes DA; Broadcast Data: FF00 Other values = N/A Where the packet's... **DA** is [Register #52h]:[Register #53h]:[Register #54h]:[Register #55h]:[Register #56h]: ([Register #57h] + 1). And the last byte ([Register #57h] + 1) increments repeatedly by 1 for the next loopback packet. **SA** is [Register #52h]:[Register #53h]:[Register #54h]:[Register #55h]:[Register #56h]: [Register #57h] **Type/length** is 0x0800h	0
6	P6	R/W		0
5	P5	R/W		0
4	P4	R/W		0
3	P3	R/W		0
2	P2	R/W		0
1	P1	R/W		0
0	P0	R/W		0
Register 70 (0x46): Loopback Result Counter for CRC Error				
7	CRC7	RO	**Center side only** This counter is incremented when the loopback packet has a CRC error. 0000_0000 = No CRC error received 0000_0001 = 1 CRC error received : 1111_1111 = 255 CRC errors received This counter is cleared when 0x00h is written to reg. 0x44h.	0
6	CRC6	RO		0
5	CRC5	RO		0
4	CRC4	RO		0
3	CRC3	RO		0
2	CRC2	RO		0
1	CRC1	RO		0
0	CRC0	RO		0
Register 71 (0x47): Loopback Result Counter for Timeout				
7	TO7	RO	**Center side only** This counter is incremented when loopback packet has timeout. 0000_0000 = No timeout occurred 0000_0001 = 1 timeout occurred : 1111_1111 = 255 timeouts occurred This counter is cleared when 0x00h is written to reg. 0x44h.	0
6	TO6	RO		0
5	TO5	RO		0
4	TO4	RO		0
3	TO3	RO		0
2	TO2	RO		0
1	TO1	RO		0
0	TO0	RO		0

TABLE 4-9: TS-1000 MEDIA CONVERTER REGISTERS (CONTINUED)

Bit	Name	R/W	Description	Default
Register 72 (0x48): Loopback Result Counter for Good Packet				
7	GO7	RO	**Center side only** This counter is incremented when loopback packet is returned good. 0000_0000 = No good packet 0000_0001 = 1 good packet : 1111_1111 = 255 good packets This counter is cleared when 0x00h is written to reg. 0x44h.	0
6	GO6	RO		0
5	GO5	RO		0
4	GO4	RO		0
3	GO3	RO		0
2	GO2	RO		0
1	GO1	RO		0
0	GO0	RO		0
Register 73 (0x49): Additional Status (Center and Terminal side)				
7	Hard Version 1	RO	Hard Version (bits [7:6])	0
6	Hard Version 0	RO		1
5	Model Version 1	R/W	Model Version (bits [5:4]): 00 = 15 km model 01 = 40 km model Others = Reserved	0
4	Model Version 0	R/W		0
3	HMC Loopback Timeout	RO	1 = Center side receives “Loop Mode Stop Indication” frame from the Terminal side. This bit is self-cleared after it is read. 0 = Normal operation	0
2	CMC Loopback Timeout	RO	1 = Center side is in Loopback mode too long and the T1 timer has timeout. This bit is self-cleared after it is read. 0 = Normal operation	0
1	Timeout	RO	1 = Center side does not receive reply frame from the Terminal side and the TE timer has timeout. This bit is self-cleared after it is read. 0 = Normal operation	0
0	P1 LNK Down	RO	1 = Link is down on port 1 0 = Link is up on port 1	0
Note: Remote Command Registers 74, 75, and 76 are accessed by the Center side only. **Register 74 (0x4A): Remote Command 1**				
7	AMM31	R/W	Reserved (This bit must be set to ‘0’ for normal operation)	0
6	AMM30	R/W	Read Acknowledge. This bit combines with bits [3:2] = ‘01’ in this register to select between read request and read acknowledge. reg. 74 bits [6,3,2] = ‘001’ = Read request reg. 74 bits [6,3,2] = ‘101’ = Read acknowledge	0
5	AMM29	RO	Indicate support capability for “A-vendor” only. If Operating Mode (bits [1:0] of this register) is set to “10”, these two bits are used by “A-vendor” to indicate support for “extended mode”. 10 = Support “extended mode” Others = Reserved	1
4	AMM28	RO		0

TABLE 4-9: TS-1000 MEDIA CONVERTER REGISTERS (CONTINUED)

Bit	Name	R/W	Description	Default
3	AMM27	R/W	**Operating Code** If Operating Mode (bits [1:0] of this register) is set to "10", these two bits are used to select one of the following Operating Codes: 00 = Read reply 01 = Read request 10 = Write reply 11 = Write request	0
2	AMM26	R/W		0
1	AMM25	R/W	**Operating Mode** Select between "normal mode" and "extended mode", defined as follows: 00 = Normal mode, MM24-MM47 (registers 0x55h to 0x57h) are used for My Model Info. 10 = Extended mode, MM24-MM47 (registers 0x55h to 0x57h) are mapped to Remote Command (registers 0x4Ah to 0x4Ch) 01 = Reserved 11 = Reserved	1
0	AMM24	R/W		0
Register 75 (0x4B): Remote Command 2				
7	AMM39	R/W	If Center MC sends the "Remote Command" in register 0x42h, this register value will be used for M39-M32 of the Maintenance frame, instead of register 0x56h. [AMM39:AMM32] = bits[7:0] of the KSZ8893FQL address byte if the Operating Mode in register 0x4Ah bits[1:0] is set to "10"	0
6	AMM38	R/W		0
5	AMM37	R/W		0
4	AMM36	R/W		0
3	AMM35	R/W		0
2	AMM34	R/W		0
1	AMM33	R/W		0
0	AMM32	R/W		0
Register 76 (0x4C): Remote Command 3				
7	AMM47	R/W	If Center MC sends the "Remote Command" in register 0x42h, this register value will be used for M47-M40 of the Maintenance frame, instead of register 0x57h. [AMM47:AMM40] = bits[7:0] of the KSZ8893FQL data byte if the Operating Mode in register 0x4Ah bits[1:0] is set to "10"	0
6	AMM46	R/W		0
5	AMM45	R/W		0
4	AMM44	R/W		0
3	AMM43	R/W		0
2	AMM42	R/W		0
1	AMM41	R/W		0
0	AMM40	R/W		0
Register 77 (0x4D): Valid MC Packet Transmitted Counter				
7	VMTX7	RO	At both the Center and Terminal sides, this counter is incremented when a valid maintenance packet is transmitted. 0000_0000 = No valid maintenance packet transmitted 0000_0001 = 1 valid maintenance packet transmitted : 1111_1111 = 255 valid maintenance packets transmitted This counter is cleared when 0x00h is written to reg. 0x44h.	0
6	VMTX6	RO		0
5	VMTX5	RO		0
4	VMTX4	RO		0
3	VMTX3	RO		0
2	VMTX2	RO		0
1	VMTX1	RO		0
0	VMTX0	RO		0

TABLE 4-9: TS-1000 MEDIA CONVERTER REGISTERS (CONTINUED)

Bit	Name	R/W	Description	Default
Register 78 (0x4E): Valid MC Packet Received Counter				
7	VMRX7	RO	At both the Center and Terminal sides, this counter is incremented when a valid maintenance packet (good CRC, valid OP code, valid direction) is received. 0000_0000 = No valid maintenance packet received 0000_0001 = 1 valid maintenance packet received : 1111_1111 = 255 valid maintenance packets received This counter is cleared when 0x00h is written to reg. 0x44h.	0
6	VMRX6	RO		0
5	VMRX5	RO		0
4	VMRX4	RO		0
3	VMRX3	RO		0
2	VMRX2	RO		0
1	VMRX1	RO		0
0	VMRX0	RO		0
Register 79 (0x4F): Shadow of 0x58h Register				
7-0	SHA7-0	RO	For **Terminal MC** mode, this register is always a shadow of register 0x58h when the OPT link is up. For **Center MC** mode, this register is a shadow of register 0x58h on the initial power on reset when the OPT link is up. After power up, if a warm reset or chip power down is asserted, this register will retain the value of register 0x58 prior to either of the aforementioned conditions. This is so that the link partner's OAM status prior to warm reset or chip power down can be reported when the OPT link is initially re-established. Thereafter, this register is a shadow of register 0x58h when the OPT link is up.	0x07 (Terminal side) -------------------- 0x47 (Center side)
Register 80 (0x50): My Status 1 (Terminal and Center side)				
7	S7	RO	H-MC Link Speed 1	0
6	S6	RO	H-MC Link Option 1 = Terminal MC mode 0 = Center MC mode	1 (Terminal side) 0 (Center side)
5	S5	RO	Loopback mode indication 1 = In loopback state (CST1, CST2, UST1) 0 = Normal	0
4	S4	R/W	Loss of optical signal notification 1 = Use FEFI 0 = Use maintenance frame (Center side - CPU will update this bit. Terminal side - Hardware will update this bit based on external pin value.)	0
3	S3	R/W	DIAG result 1 = Diagnostic Fail 0 = Normal operation (Center side - CPU will update this bit. Terminal side - This bit will be updated through DIAGF pin.)	DIAGF pin value DIAGF (IPD)
2	S2	R/W	UTP Link Down 1 = Link down 0 = Link up (Center side - CPU will update this bit. Terminal side - This bit is read only and updated by hardware.)	1

TABLE 4-9: TS-1000 MEDIA CONVERTER REGISTERS (CONTINUED)

Bit	Name	R/W	Description	Default
1	S1	RO	SD disable 1 = Abnormal (no optical signal detected) 0 = Normal (optical signal detected)	FXSD1 pin value is polled.
0	S0	RO	Power down 1 = Power down 0 = Normal operation	Inverse of PDD# pin value PDD# (IPU)
Register 81 (0x51): My Status 2				
7-4	S15-S12	RO	Reserved Do not change the default values.	0x0
3	S11	R/W	For **Terminal MC** mode, this bit must always be “0”. For **Center MC** mode, this bit indicates the number of physical interface(s) making up the UTP link 0 = One 1 = Greater than one	0
2	S10	RO	For **Terminal MC** mode, this bit indicates the auto negotiation capability, and is the same value as bit [5] of register 67. 1 = Auto-negotiation is supported 0 = Auto-negotiation is not supported For **Center MC** mode, this bit must always be “0”.	P2ANEN pin value (Terminal MC) -------------------- 0 (Center MC)
1	S9	RO	For **Terminal MC** mode, this bit indicates the UTP port’s DUPLEX status. 1 = Full-Duplex 0 = Half-Duplex, or Register 0x50h bit[2] is “1” (UTP link is down) For **Center MC** mode, this bit is always “0”.	0
0	S8	RO	For **Terminal MC** mode, this bit indicates the UTP port’s SPEED status. 1 = 100 Mbps 0 = 10 Mbps, or Register 0x50h bit[2] is “1” (UTP link is down) For **Center MC** mode, this bit is always “0”.	0
Register 82 (0x52): My Vendor Info (1)				
7-0	MM7-MM0	R/W	—	0x00
Register 83 (0x53): My Vendor Info (2)				
7-0	MM15-MM8	R/W	—	0x00
Register 84 (0x54): My Vendor Info (3)				
7-0	MM23-MM16	R/W	—	0x00
Register 85 (0x55): My Model Info (1)				
7-0	MM31-MM24	R/W	Note: If Remote Command feature is used, this register value cannot be set to 0x22, 0x26, 0x2A, 0x2E, and 0x66. All other values are valid.	0x00
Register 86 (0x56): My Model Info (2)				
7-0	MM39-MM32	R/W	—	0x00
Register 87 (0x57): My Model Info (3)				
7-0	MM47-MM40	R/W	—	0x00

TABLE 4-9: TS-1000 MEDIA CONVERTER REGISTERS (CONTINUED)

Bit	Name	R/W	Description	Default
Register 88 (0x58): LNK Partner Status (1)				
7-0	LS7-LS0	RO	This register has the same bits descriptions as register 80 (0x50).	0x47 (Center side) -------------------- 0x07 (Terminal side)
Register 89 (0x59): LNK Partner Status (2)				
7-0	LS15-LS8	RO	This register has the same bits descriptions as register 81 (0x51).	0x00
Register 90 (0x5A): LNK Partner Vendor Info (1)				
7-0	LM7-LM0	RO	—	0x00
Register 91 (0x5B): LNK Partner Vendor Info (2)				
7-0	LM15-LM8	RO	—	0x00
Register 92 (0x5C): LNK Partner Vendor Info (3)				
7-0	LM23-LM16	RO	—	0x00
Register 93 (0x5D): LNK Partner Model Info (1)				
7-0	LM31-LM24	RO	—	0x00
Register 94 (0x5E): LNK Partner Model Info (2)				
7-0	LM39-LM32	RO	—	0x00
Register 95 (0x5F): LNK Partner Model Info (3)				
7-0	LM47-LM40	RO	—	0x00

4.5 Advanced Control Registers (Registers 96-141)

The IPv4/IPv6 Type of Service (TOS) Priority Control Registers implement a fully decoded, 128-bit Differentiated Services Code Point (DSCP) register set that is used to determine priority from the TOS field in the IP header. The most significant 6 bits of the TOS field are fully decoded into 64 possibilities, and the singular code that results is compared against the corresponding bits in the DSCP register to determine the priority.

TABLE 4-10: ADVANCED CONTROL REGISTERS (REGISTERS 96-141)

Bit	Name	R/W	Description	Default
Register 96 (0x60): TOS Priority Control Register 0				
7-6	DSCP[7:6]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x0C.	00
5-4	DSCP[5:4]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x08.	00
3-2	DSCP[3:2]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x04.	00
1-0	DSCP[1:0]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x00.	00
Register 97 (0x61): TOS Priority Control Register 1				
7-6	DSCP[15:14]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x1C.	00
5-4	DSCP[13:12]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x18.	00
3-2	DSCP[11:10]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x14.	00
1-0	DSCP[9:8]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x10.	00
Register 98 (0x62): TOS Priority Control Register 2				
7-6	DSCP[23:22]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x2C.	00
5-4	DSCP[21:20]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x28.	00
3-2	DSCP[19:18]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x24.	00
1-0	DSCP[17:16]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x20.	00
Register 99 (0x63): TOS Priority Control Register 3				
7-6	DSCP[31:30]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x3C.	00

TABLE 4-10: ADVANCED CONTROL REGISTERS (REGISTERS 96-141) (CONTINUED)

Bit	Name	R/W	Description	Default
5-4	DSCP[29:28]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x38.	00
3-2	DSCP[27:26]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x34.	00
1-0	DSCP[25:24]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x30.	00
Register 100 (0x64): TOS Priority Control Register 4				
7-6	DSCP[39:38]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x4C.	00
5-4	DSCP[37:36]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x48.	00
3-2	DSCP[35:34]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x44.	00
1-0	DSCP[33:32]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x40.	00
Register 101 (0x65): TOS Priority Control Register 5				
7-6	DSCP[47:46]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x5C.	00
5-4	DSCP[45:44]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x58.	00
3-2	DSCP[43:42]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x54.	00
1-0	DSCP[41:40]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x50.	00
Register 102 (0x66): TOS Priority Control Register 6				
7-6	DSCP[55:54]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x6C.	00
5-4	DSCP[53:52]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x68.	00
3-2	DSCP[51:50]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x64.	00
1-0	DSCP[49:48]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x60.	00

TABLE 4-10: ADVANCED CONTROL REGISTERS (REGISTERS 96-141) (CONTINUED)

Bit	Name	R/W	Description	Default
Register 103 (0x67): TOS Priority Control Register 7				
7-6	DSCP[63:62]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x7C.	00
5-4	DSCP[61:60]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x78.	00
3-2	DSCP[59:58]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x74.	00
1-0	DSCP[57:56]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x70.	00
Register 104 (0x68): TOS Priority Control Register 8				
7-6	DSCP[71:70]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x8C.	00
5-4	DSCP[69:68]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x88.	00
3-2	DSCP[67:66]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x84.	00
1-0	DSCP[65:64]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x80.	00
Register 105 (0x69): TOS Priority Control Register 9				
7-6	DSCP[79:78]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x9C.	00
5-4	DSCP[77:76]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x98.	00
3-2	DSCP[75:74]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x94.	00
1-0	DSCP[73:72]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x90.	00
Register 106 (0x6A): TOS Priority Control Register 10				
7-6	DSCP[87:86]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xAC.	00
5-4	DSCP[85:84]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xA8.	00
3-2	DSCP[83:82]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xA4.	00

TABLE 4-10: ADVANCED CONTROL REGISTERS (REGISTERS 96-141) (CONTINUED)

Bit	Name	R/W	Description	Default
1-0	DSCP[81:80]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xA0.	00
Register 107 (0x6B): TOS Priority Control Register 11				
7-6	DSCP[95:94]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xBC.	00
5-4	DSCP[93:92]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xB8.	00
3-2	DSCP[91:90]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xB4.	00
1-0	DSCP[89:88]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xB0.	00
Register 108 (0x6C): TOS Priority Control Register 12				
7-6	DSCP[103:102]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xCC.	00
5-4	DSCP[101:100]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xC8.	00
3-2	DSCP[99:98]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xC4.	00
1-0	DSCP[97:96]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xC0.	00
Register 109 (0x6D): TOS Priority Control Register 13				
7-6	DSCP[111:110]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xDC.	00
5-4	DSCP[109:108]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xD8.	00
3-2	DSCP[107:106]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xD4.	00
1-0	DSCP[105:104]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xD0.	00
Register 110 (0x6E): TOS Priority Control Register 14				
7-6	DSCP[119:118]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xEC.	00
5-4	DSCP[117:116]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xE8.	00

TABLE 4-10: ADVANCED CONTROL REGISTERS (REGISTERS 96-141) (CONTINUED)

Bit	Name	R/W	Description	Default
3-2	DSCP[115:114]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xE4.	00
1-0	DSCP[113:112]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xE0.	00
Register 111 (0x6F): TOS Priority Control Register 15				
7-6	DSCP[127:126]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xFC.	00
5-4	DSCP[125:124]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xF8.	00
3-2	DSCP[123:122]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xF4.	00
1-0	DSCP[121:120]	R/W	The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0xF0.	00
Registers 112 to 117 contain the switch engine's MAC address. This 48-bit address is used as the Source Address for the MAC's full-duplex flow control (PAUSE) frame.				
Register 112 (0x70): MAC Address Register 0				
7-0	MACA[47:40]	R/W	—	0x00
Register 113 (0x71): MAC Address Register 1				
7-0	MACA[39:32]	R/W	—	0x10
Register 114 (0x72): MAC Address Register 2				
7-0	MACA[31:24]	R/W	—	0xA1
Register 115 (0x73): MAC Address Register 3				
7-0	MACA[23:16]	R/W	—	0xFF
Register 116 (0x74): MAC Address Register 4				
7-0	MACA[15:8]	R/W	—	0xFF
Register 117 (0x75): MAC Address Register 5				
7-0	MACA[7:0]	R/W	—	0xFF
Registers 118 to 120 are User Defined Registers (UDRs). These are general purpose read/write registers that can be used to pass user defined control and status information between the KSZ8893FQL and the external processor.				
Register 118 (0x76): User Defined Register 1				
7-0	UDR1	R/W	—	0x00
Register 119 (0x77): User Defined Register 2				
7-0	UDR2	R/W	—	0x00
Register 120 (0x78): User Defined Register 3				
7-0	UDR3	R/W	—	0x00
Registers 121 to 131 provide read and write access to the static MAC address table, VLAN table, dynamic MAC address table, and MIB counters.				
Register 121 (0x79): Indirect Access Control 0				
7-5	Reserved	R/W	Reserved Do not change the default values.	000
4	Read High/Write Low	R/W	1 = Read cycle 0 = Write cycle	0

TABLE 4-10: ADVANCED CONTROL REGISTERS (REGISTERS 96-141) (CONTINUED)

Bit	Name	R/W	Description	Default
3-2	Table Select	R/W	00 = Static MAC address table selected 01 = VLAN table selected 10 = Dynamic MAC address table selected 11 = MIB counter selected	00
1-0	Indirect Address High	R/W	Bits [9:8] of indirect address	00
Register 122 (0x7A): Indirect Access Control 1				
7-0	Indirect Address Low	R/W	Bits [7:0] of indirect address. Note: A write to register 122 triggers the read/write command. Read or write access is determined by register 121 bit 4.	0000_0000
Register 123 (0x7B): Indirect Data Register 8				
7	CPU Read Status	RO	This bit is applicable only for dynamic MAC address table and MIB counter reads. 1 = Read is still in progress 0 = Read has completed	0
6-3	Reserved	RO	Reserved	0000
2-0	Indirect Data [66:64]	RO	Bits [66:64] of indirect data	000
Register 124 (0x7C): Indirect Data Register 7				
7-0	Indirect Data [63:56]	R/W	Bits [63:56] of indirect data	0000_0000
Register 125 (0x7D): Indirect Data Register 6				
7-0	Indirect Data [55:48]	R/W	Bits [55:48] of indirect data	0000_0000
Register 126 (0x7E): Indirect Data Register 5				
7-0	Indirect Data [47:40]	R/W	Bits [47:40] of indirect data	0000_0000
Register 127 (0x7F): Indirect Data Register 4				
7-0	Indirect Data [39:32]	R/W	Bits [39:32] of indirect data	0000_0000
Register 128 (0x80): Indirect Data Register 3				
7-0	Indirect Data [31:24]	R/W	Bits [31:24] of indirect data	0000_0000
Register 129 (0x81): Indirect Data Register 2				
7-0	Indirect Data [23:16]	R/W	Bits [23:16] of indirect data	0000_0000
Register 130 (0x82): Indirect Data Register 1				
7-0	Indirect Data [15:8]	R/W	Bits [15:8] of indirect data	0000_0000
Register 131 (0x83): Indirect Data Register 0				
7-0	Indirect Data [7:0]	R/W	Bits [7:0] of indirect data	0000_0000
Reserved registers 132 to 141 are used by Microchip for internal testing only. Do not change the values of these registers. **Register 132 (0x84): Digital Testing Status 0**				
7-3	Reserved	RO	Factory testing	00000
2-0	Om_split Status	RO	Factory testing	000
Register 133 (0x85): Digital Testing Control 0				
7-0	Reserved	R/W	Factory testing Dbg[7:0]	0x3F
Register 134 (0x86): Analog Testing Control 0				
7-0	Reserved	R/W	Factory testing (dgt_actl0)	0x00
Register 135 (0x87): Analog Testing Control 1				
7-0	Reserved	R/W	Factory testing (dgt_actl1)	0x00

TABLE 4-10: ADVANCED CONTROL REGISTERS (REGISTERS 96-141) (CONTINUED)

Bit	Name	R/W	Description	Default
Register 136 (0x88): Analog Testing Control 2				
7-0	Reserved	R/W	Factory testing (dgt_actl2)	0x00
Register 137 (0x89): Analog Testing Control 3				
7-0	Reserved	R/W	Factory testing (dgt_actl3)	0x00
Register 138 (0x8A): Analog Testing Status				
7-6	LED Driver Current Set	R/W	00 = 60 mA 01 = 80 mA 10 = 90 mA 11 = 40 mA	00
5-0	Reserved	RO	Factory Testing	00_0000
Register 139 (0x8B): Analog Testing Control 4				
7-0	Reserved	R/W	Factory testing (dgt_actl4)	0x40
Register 140 (0x8C): QM Debug 1				
7-0	Reserved	RO	Factory testing QM_Debug bit[7:0]	0x00
Register 141 (0x8D): QM Debug 2				
7-1	Reserved	RO	Reserved	0000_000
0	Reserved	RO	Factory testing QM_Debug bit[8]	0

4.6 Static MAC Address Table

The KSZ8893FQL supports both a static and a dynamic MAC address table. In response to a Destination Address (DA) look-up, the KSZ8893FQL searches both tables to make a packet forwarding decision. In response to a Source Address (SA) look-up, only the dynamic table is searched for aging, migration, and learning purposes.

The static DA look up result takes precedence over the dynamic DA look-up result. If there is a DA match in both tables, then the result from the static table is used. The entries in the static table will not be aged out by the KSZ8893FQL.

The static table is accessed by an external processor via the SMI, SPI, or I^2C interfaces. The external processor performs all addition, modification, and deletion of static MAC table entries.

TABLE 4-11: FORMAT OF STATIC MAC TABLE (8 ENTRIES)

Bit	Name	R/W	Description	Default
57-54	FID	R/W	Filter VLAN ID – identifies one of the 16 active VLANs	0000
53	Use FID	R/W	1 = Use (FID+MAC) for static table look ups 0 = Use MAC only for static table look ups	0
52	Override	R/W	1 = Override port setting “transmit enable=0” or “receive enable=0” setting 0 = No override	0
51	Valid	R/W	1 = This entry is valid, the lookup result will be used 0 = This entry is not valid	0
50-48	Forwarding Ports	R/W	These 3 bits control the forwarding port(s): 001 = Forward to port 1 010 = Forward to port 2 100 = Forward to port 3 011 = Forward to port 1 and port 2 110 = Forward to port 2 and port 3 101 = Forward to port 1 and port 3 111 = Broadcasting (excluding the ingress port)	000

TABLE 4-11: FORMAT OF STATIC MAC TABLE (8 ENTRIES) (CONTINUED)

Bit	Name	R/W	Description	Default
47-0	MAC Address	R/W	48-bit MAC Address	0x0000_0000 _0000

Examples:

1. Static Address Table Read (Read the 2nd Entry)

Write to reg. 121 (0x79) with 0x10 // Read static table selected

Write to reg. 122 (0x7A) with 0x01 // Trigger the read operation

Then,

Read reg. 124 (0x7C), static table bits [57:56]

Read reg. 125 (0x7D), static table bits [55:48]

Read reg. 126 (0x7E), static table bits [47:40]

Read reg. 127 (0x7F), static table bits [39:32]

Read reg. 128 (0x80), static table bits [31:24]

Read reg. 129 (0x81), static table bits [23:16]

Read reg. 130 (0x82), static table bits [15:8]

Read reg. 131 (0x83), static table bits [7:0]

2. Static Address Table Write (Write the 8th Entry)

Write to reg. 124 (0x7C), static table bits [57:56]

Write to reg. 125 (0x7D), static table bits [55:48]

Write to reg. 126 (0x7E), static table bits [47:40]

Write to reg. 127 (0x7F), static table bits [39:32]

Write to reg. 128 (0x80), static table bits [31:24]

Write to reg. 129 (0x81), static table bits [23:16]

Write to reg. 130 (0x82), static table bits [15:8]

Write to reg. 131 (0x83), static table bits [7:0]

Write to reg. 121 (0x79) with 0x00 // Write static table selected

Write to reg. 122 (0x7A) with 0x07 // Trigger the write operation

4.7 VLAN Table

The KSZ8893FQL uses the VLAN table to perform look-ups. If 802.1Q VLAN mode is enabled (register 5, bit 7 = 1), this table will be used to retrieve the VLAN information that is associated with the ingress packet. This information includes FID (filter ID), VID (VLAN ID), and VLAN membership as described in Table 4-12.

TABLE 4-12: FORMAT OF STATIC VLAN TABLE (16 ENTRIES)

Bit	Name	R/W	Description	Default
19	Valid	R/W	1 = Entry is valid 0 = Entry is invalid	1
18-16	Membership	R/W	Specify which ports are members of the VLAN. If a DA lookup fails (no match in both static and dynamic tables), the packet associated with this VLAN will be forwarded to ports specified in this field. For example, 101 means port 3 and 1 are in this VLAN.	111
15-12	FID	R/W	Filter ID. KSZ8893FQL supports 16 active VLANs represented by these four bit fields. FID is the mapped ID. If 802.1Q VLAN is enabled, the look up will be based on FID+DA and FID+SA.	0x0

TABLE 4-12: FORMAT OF STATIC VLAN TABLE (16 ENTRIES) (CONTINUED)

Bit	Name	R/W	Description	Default
11-0	VID	R/W	IEEE 802.1Q 12 bits VLAN ID	0x001

If 802.1Q VLAN mode is enabled, KSZ8893FQL will assign a VID to every ingress packet. If the packet is untagged or tagged with a null VID, the packet is assigned with the default port VID of the ingress port. If the packet is tagged with non-null VID, the VID in the tag will be used. The look up process will start from the VLAN table look up. If the VID is not valid, the packet will be dropped and no address learning will take place. If the VID is valid, the FID is retrieved. The FID+DA and FID+SA lookups are performed. The FID+DA look up determines the forwarding ports. If FID+DA fails, the packet will be broadcast to all the members (excluding the ingress port) of the VLAN. If FID+SA fails, the FID+SA will be learned.

Examples:

1. VLAN Table Read (read the 3rd entry)

Write to reg. 121 (0x79) with 0x14 // Read VLAN table selected

Write to reg. 122 (0x7A) with 0x02 // Trigger the read operation

Then,

Read reg. 129 (0x81), VLAN table bits [19:16]

Read reg. 130 (0x82), VLAN table bits [15:8]

Read reg. 131 (0x83), VLAN table bits [7:0]

2. VLAN Table Write (write the 7th entry)

Write to reg. 129 (0x81), VLAN table bits [19:16]

Write to reg. 130 (0x82), VLAN table bits [15:8]

Write to reg. 131 (0x83), VLAN table bits [7:0]

Write to reg. 121 (0x79) with 0x04 // Write VLAN table selected

Write to reg. 122 (0x7A) with 0x06 // Trigger the write operation

4.8 Dynamic MAC Address Table

The KSZ8893FQL maintains the dynamic MAC address table. Only read access is allowed.

TABLE 4-13: FORMAT OF DYNAMIC MAC ADDRESS TABLE (1K ENTRIES)

Bit	Name	R/W	Description	Default
71	Data Not Ready	RO	1 = Entry is not ready, continue retrying until this bit is set to 0 0 = Entry is ready	—
70-67	Reserved	RO	Reserved	—
66	MAC Empty	RO	1 = There is no valid entry in the table 0 = There are valid entries in the table	1
65-56	Number of Valid Entries	RO	Indicates how many valid entries in the table 0x3FF means 1k entries 0x001 means 2 entries 0x000 and bit 66 = 0 means 1 entry 0x000 and bit 66 = 1 means 0 entry	00_0000_0000
55-54	Time Stamp	RO	2 bits counter for internal aging	—
53-52	Source Port	RO	The source port where FID+MAC is learned 00 = Port 1 01 = Port 2 10 = Port 3	00
51-48	FID	RO	Filter ID	0x0
47-0	MAC Address	RO	48-bit MAC Address	0x0000_0000_0000

Example:

Dynamic MAC Address Table Read (read the 1st entry and retrieve the MAC table size)

Write to reg. 121 (0x79) with 0x18 // Read dynamic table selected

Write to reg. 122 (0x7A) with 0x00 // Trigger the read operation

Then,

Read reg. 123 (0x7B), bit [7]   // if bit 7 = 1, restart (reread) from this register dynamic table bits [66:64]

Read reg. 124 (0x7C), dynamic table bits [63:56]

Read reg. 125 (0x7D), dynamic table bits [55:48]

Read reg. 126 (0x7E), dynamic table bits [47:40]

Read reg. 127 (0x7F), dynamic table bits [39:32]

Read reg. 128 (0x80), dynamic table bits [31:24]

Read reg. 129 (0x81), dynamic table bits [23:16]

Read reg. 130 (0x82), dynamic table bits [15:8]

Read reg. 131 (0x83), dynamic table bits [7:0]

4.9 Management Information Base (MIB) Counters

The KSZ8893FQL provides 34 MIB counters per port. These counters are used to monitor the port activity for network management. The MIB counters have two format groups: “Per Port” and “All Port Dropped Packet.”

TABLE 4-14: FORMAT OF “PER PORT” MIB COUNTERS

Bit	Name	R/W	Description	Default
31	Overflow	RO	1 = Counter overflow 0 = No counter overflow	0
30	Count Valid	RO	1 = Counter value is valid 0 = Counter value is not valid	0
29-0	Counter Values	RO	Counter value	0

“Per Port” MIB counters are read using indirect memory access. The base address offsets and address ranges for all three ports are:

- Port 1, base is 0x00 and range is (0x00-0x1F)
- Port 2, base is 0x20 and range is (0x20-0x3F)
- Port 3, base is 0x40 and range is (0x40-0x5F)

Port 1 MIB counters are read using the indirect memory offsets in Table 4-15.

TABLE 4-15: PORT 1’S “PER PORT” MIB COUNTERS INDIRECT MEMORY OFFSETS

Offset	Counter Name	Description
0x0	RxLoPriorityByte	Rx lo-priority (default) octet count including bad packets
0x1	RxHiPriorityByte	Rx hi-priority octet count including bad packets
0x2	RxUndersizePkt	Rx undersize packets w/ good CRC
0x3	RxFragments	Rx fragment packets w/ bad CRC, symbol errors or alignment errors
0x4	RxOversize	Rx oversize packets w/ good CRC (max: 1536 or 1522 bytes)
0x5	RxJabbers	Rx packets longer than 1522 bytes w/ either CRC errors, alignment errors, or symbol errors (depends on max packet size setting)
0x6	RxSymbolError	Rx packets w/ invalid data symbol and legal packet size.
0x7	RxCRCError	Rx packets within (64,1522) bytes w/ an integral number of bytes and a bad CRC (upper limit depends on max packet size setting)
0x8	RxAlignmentError	Rx packets within (64,1522) bytes w/ a non-integral number of bytes and a bad CRC (upper limit depends on max packet size setting)

TABLE 4-15: PORT 1'S "PER PORT" MIB COUNTERS INDIRECT MEMORY OFFSETS

Offset	Counter Name	Description
0x9	RxControl8808Pkts	Number of MAC control frames received by a port with 88-08h in Ether-Type field
0xA	RxPausePkts	Number of PAUSE frames received by a port. PAUSE frame is qualified with EtherType (88-08h), DA, control opcode (00-01), data length (64B min), and a valid CRC
0xB	RxBroadcast	Rx good broadcast packets (not including error broadcast packets or valid multicast packets)
0xC	RxMulticast	Rx good multicast packets (not including MAC control frames, error multicast packets or valid broadcast packets)
0xD	RxUnicast	Rx good unicast packets
0xE	Rx64Octets	Total Rx packets (bad packets included) that were 64 octets in length
0xF	Rx65to127Octets	Total Rx packets (bad packets included) that are between 65 and 127 octets in length
0x10	Rx128to255Octets	Total Rx packets (bad packets included) that are between 128 and 255 octets in length
0x11	Rx256to511Octets	Total Rx packets (bad packets included) that are between 256 and 511 octets in length
0x12	Rx512to1023Octets	Total Rx packets (bad packets included) that are between 512 and 1023 octets in length
0x13	Rx1024to1522Octets	Total Rx packets (bad packets included) that are between 1024 and 1522 octets in length (upper limit depends on max packet size setting)
0x14	TxLoPriorityByte	Tx lo-priority good octet count, including PAUSE packets
0x15	TxHiPriorityByte	Tx hi-priority good octet count, including PAUSE packets
0x16	TxLateCollision	The number of times a collision is detected later than 512 bit-times into the Tx of a packet
0x17	TxPausePkts	Number of PAUSE frames transmitted by a port
0x18	TxBroadcastPkts	Tx good broadcast packets (not including error broadcast or valid multi-cast packets)
0x19	TxMulticastPkts	Tx good multicast packets (not including error multicast packets or valid broadcast packets)
0x1A	TxUnicastPkts	Tx good unicast packets
0x1B	TxDeferred	Tx packets by a port for which the 1st Tx attempt is delayed due to the busy medium
0x1C	TxTotalCollision	Tx total collision, half duplex only
0x1D	TxExcessiveCollision	A count of frames for which Tx fails due to excessive collisions
0x1E	TxSingleCollision	Successfully Tx frames on a port for which Tx is inhibited by exactly one collision
0x1F	TxMultipleCollision	Successfully Tx frames on a port for which Tx is inhibited by more than one collision

TABLE 4-16: FORMAT OF "ALL PORT DROPPED PACKET" MIB COUNTERS

Bit	Name	R/W	Description	Default
30-16	Reserved	N/A	Reserved	N/A
15-0	Counter Value	RO	Counter Value	0

"All Port Dropped Packet" MIB counters are read using indirect memory access. The address offsets for these counters are shown in Table 4-17.

TABLE 4-17: "ALL PORT DROPPED PACKET" MIB COUNTERS INDIRECT MEMORY OFFSETS

Offset	Counter Name	Description
0x100	Port 1 TX Drop Packets	TX packets dropped due to lack of resources
0x101	Port 2 TX Drop Packets	TX packets dropped due to lack of resources
0x102	Port 3 TX Drop Packets	TX packets dropped due to lack of resources
0x103	Port 1 RX Drop Packets	RX packets dropped due to lack of resources
0x104	Port 2 RX Drop Packets	RX packets dropped due to lack of resources
0x105	Port 3 RX Drop Packets	RX packets dropped due to lack of resources

Examples:

1. MIB Counter Read (Read port 1 "Rx64Octets" Counter)

Write to reg. 121 (0x79) with 0x1c // Read MIB counters selected

Write to reg. 122 (0x7A) with 0x0e // Trigger the read operation

Then

Read reg. 128 (0x80), overflow bit [31] // If bit 31 = 1, there was a counter overflow

valid bit [30] // If bit 30 = 0, restart (reread) from this register counter bits [29:24]

Read reg. 129 (0x81), counter bits [23:16]

Read reg. 130 (0x82), counter bits [15:8]

Read reg. 131 (0x83), counter bits [7:0]

2. MIB Counter Read (Read port 2 "Rx64Octets" Counter)

Write to reg. 121 (0x79) with 0x1c // Read MIB counter selected

Write to reg. 122 (0x7A) with 0x2e // Trigger the read operation

Then,

Read reg. 128 (0x80), overflow bit [31] // If bit 31 = 1, there was a counter overflow

valid bit [30] // If bit 30 = 0, restart (reread) from this register counter bits [29:24]

Read reg. 129 (0x81), counter bits [23:16]

Read reg. 130 (0x82), counter bits [15:8]

Read reg. 131 (0x83), counter bits [7:0]

3. MIB Counter Read (Read "Port 1 TX Drop Packets" Counter)

Write to reg. 121 (0x79) with 0x1D // Read MIB counter selected

Write to reg. 122 (0x7A) with 0x00 // Trigger the read operation

Then

Read reg. 130 (0x82), counter bits [15:8]

Read reg. 131 (0x83), counter bits [7:0]

4.9.1 ADDITIONAL MIB COUNTER INFORMATION

"Per Port" MIB counters are designed as "read clear." These counters will be cleared after they are read.

"All Port Dropped Packet" MIB counters are not cleared after they are accessed and do not indicate overflow or validity; therefore, the application must keep track of overflow and valid conditions.

To read out all the counters, the best performance over the SPI bus is (160+3) x 8 x 200 = 260 ms, where there are 160 registers, 3 overheads, 8 clocks per access, at 5 MHz. In the heaviest condition, the counters will overflow in 2 minutes. It is recommended that the software read all the counters at least every 30 seconds.

A high performance SPI master is also recommended to prevent counters overflow.

5.0 OPERATIONAL CHARACTERISTICS

5.1 Absolute Maximum Ratings*

Supply Voltage

(V_{DDA}, V_{DDAP}, V_{DDC}) .... –0.5V to +1.8V

(V_{DDATX}, V_{DDARX}, V_{DDIO}) .... –0.5V to +4.0V

Input Voltage (all inputs) .... –0.5V to +4.0V

Output Voltage (all outputs) .... –0.5V to +4.0V

Lead Temperature (soldering, 10s) .... +260°C

Storage Temperature (T_S) .... –55°C to +150°C

*Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

5.2 Operating Ratings**

Supply Voltage

(V_{DDA}, V_{DDAP}, V_{DDC}) .... +1.14V to +1.26V

(V_{DDATX}, V_{DDARX}, V_{DDIO}) .... +3.135V to +3.465V

Ambient Temperature (T_A) .... 0°C to +70°C

Maximum Junction Temperature (T_J) .... +125°C

Thermal Resistance (Note 5-1) (Θ_{JA}) .... +32°C/W

Thermal Resistance (Note 5-1) (Θ_{JC}) .... +10°C/W

**The device is not guaranteed to function outside its operating ratings.

Note 5-1 No heat spreader (HS) in this package.

Note: Do not drive input signals without power supplied to the device.

6.0 ELECTRICAL CHARACTERISTICS

T_A = 25°C. Specification is for packaged product only. Current consumption is for the single 3.3V supply KSZ8893FQL device only, and includes the 1.2V supply voltages (V_{DDA}, V_{DDAP}, V_{DDC}) that are provided by the KSZ8893FQL via power output pin 22. Each PHY port's transformer consumes an additional 45 mA @ 3.3V for 100BASE-TX and 70 mA @ 3.3V for 10BASE-T.

TABLE 6-1: ELECTRICAL CHARACTERISTICS

Parameters	Symbol	Min.	Typ.	Max.	Units	Note
100BASE-TX Operation (All Ports @ 100% Utilization)						
100BASE-TX (Transceiver + Digital I/O)	I_{DDXIO}	—	120	—	mA	V_{DDATX}, V_{DDARX}, V_{DDIO} = 3.3V
10BASE-T Operation (All Ports @ 100% Utilization)						
10BASE-T (Transceiver + Digital I/O)	I_{DDXIO}	—	90	—	mA	V_{DDATX}, V_{DDARX}, V_{DDIO} = 3.3V
CMOS Inputs						
Input High Voltage	V_{IH}	2.0	—	—	V	—
Input Low Voltage	V_{IL}	—	—	0.8	V	—
Input Current	I_{IN}	–10	—	10	µA	V_{IN} = GND ~ V_{DDIO}
CMOS Outputs						
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = –8 mA
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output Tri-State Leakage	I_{OZ}	—	—	10	µA	—
100BASE-TX Transmit (measured differentially after 1:1 transformer)						
Peak Differential Output Voltage	V_O	0.95	—	1.05	V	100Ω termination across differential output.
Output Voltage Imbalance	V_{IMB}	—	—	2	%	100Ω termination across differential output.
Rise/Fall Time	t_r/t_f	3	—	5	ns	—
Rise/Fall Time Imbalance	—	0	—	0.5	ns	—
Duty Cycle Distortion	—	—	—	±0.25	ns	—
Overshoot	—	—	—	5	%	—
Reference Voltage of I_{SET}	V_{SET}	—	0.5	—	V	—
Output Jitter	—	—	0.7	14	ns	Peak-to-peak
10BASE-T Receive						
Squelch Threshold	V_{SQ}	—	400	—	MHz	5 MHz square wave
10BASE-T Transmit (measured differentially after 1:1 transformer)						
Peak Differential Output Voltage	V_P	—	2.4	—	V	100Ω termination across differential output.
Jitter Added	—	—	1.8	3.5	ns	Peak-to-peak
10BASE-FL to 10BASE-T Operation @ Full-Duplex and 100% Utilization						
10BASE-FL Media Conversion (Transceiver + Digital I/O)	I_{DD10FL}	—	110	—	mA	V_{DDATX}, V_{DDARX}, V_{DDIO} = 3.3V
100BASE-SX to 100BASE-TX Operation @ Full-Duplex and 100% Utilization						
100BASE-SX Media Conversion (Transceiver + Digital I/O)	$I_{DD100SX}$	—	130	—	mA	V_{DDATX}, V_{DDARX}, V_{DDIO} = 3.3V

TABLE 6-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameters	Symbol	Min.	Typ.	Max.	Units	Note
10BASE-FL/100BASE-SX Transmit						
Transmitter Output Current Pin TXM1	I_{FO}	—	60	—	mA	V_{DDATX}, V_{DDARX}, V_{DDIO} = 3.3V
10BASE-FL Receive						
Signal Detect Assertion Threshold Pin RXM1	V_{10FL}	2.5	—	—	mV_{RMS}	—
100BASE-SX Receive						
Signal Detection Assertion Threshold Pin RXM1	V_{100SX}	16	—	—	mV_{RMS}	—

7.0 TIMING SPECIFICATIONS

7.1 EEPROM Timing

FIGURE 7-1: EEPROM INTERFACE INPUT TIMING DIAGRAM

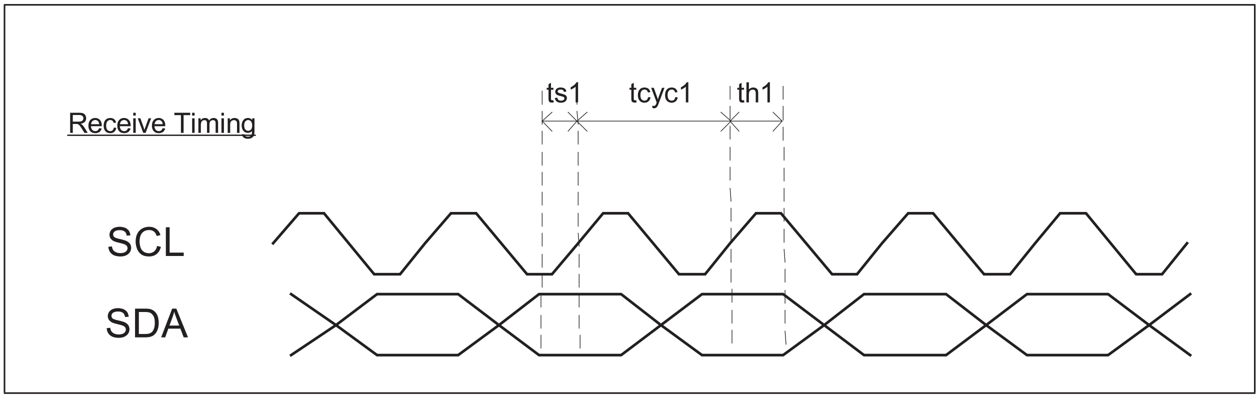


FIGURE 7-2: EEPROM INTERFACE OUTPUT TIMING DIAGRAM

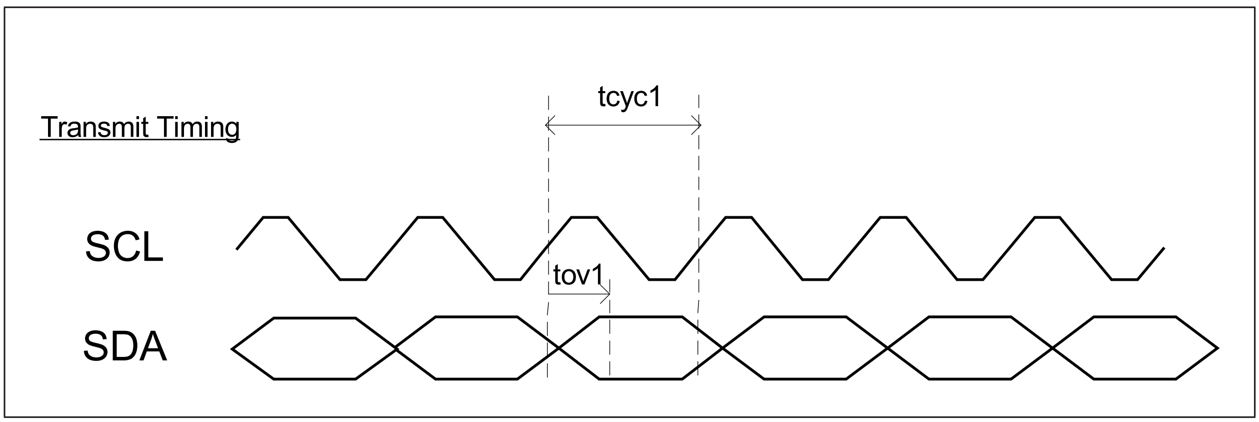


TABLE 7-1: EEPROM TIMING PARAMETERS

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{cyc1}	Clock cycle	—	16384	—	ns
t_{s1}	Setup time	20	—	—	ns
t_{h1}	Hold time	20	—	—	ns
t_{ov1}	Output valid	4096	4112	4128	ns

7.2 SNI Timing

FIGURE 7-3: SNI TIMING - DATA RECEIVED FROM SNI

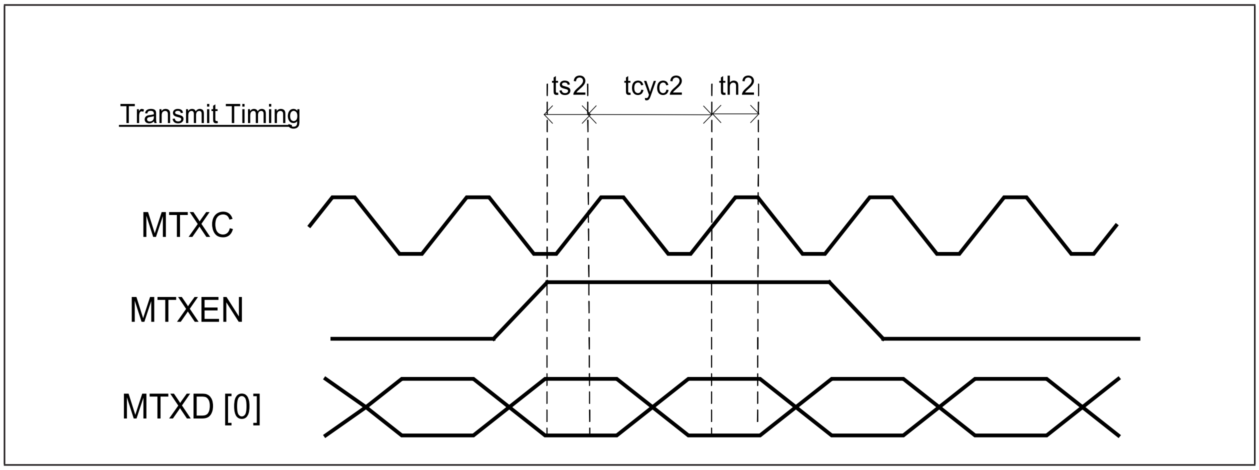


FIGURE 7-4: SNI TIMING - DATA INPUT TO SNI

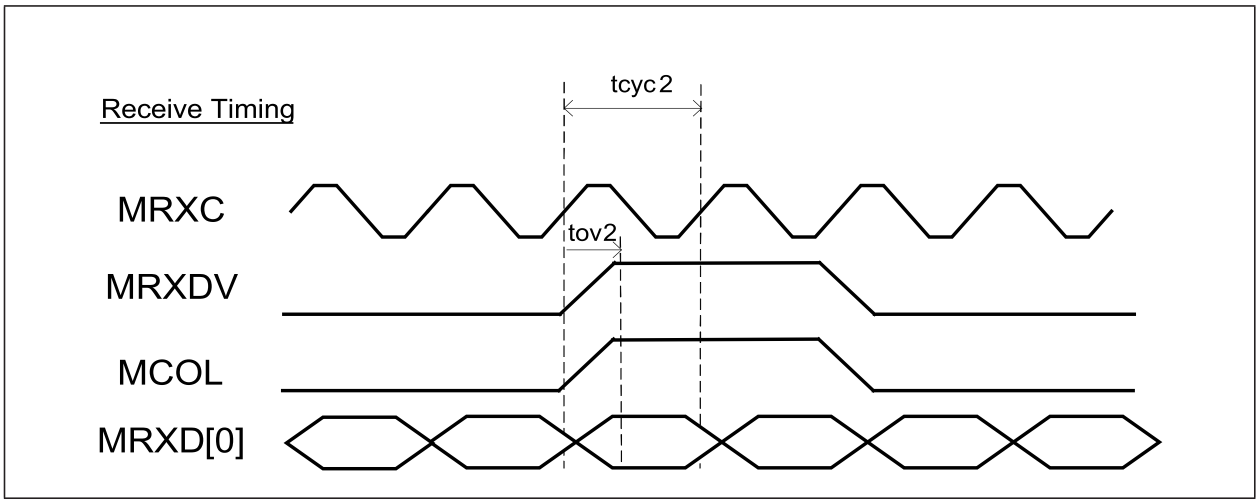


TABLE 7-2: MAC MODE MII TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{cyc2}	Clock cycle	—	100	—	ns
t_{s2}	Setup time	10	—	—	ns
t_{h2}	Hold time	0	—	—	ns
t_{ov2}	Output valid	0	3	6	ns

7.3 MII Timing

FIGURE 7-5: MII TIMING - DATA RECEIVED FROM MII

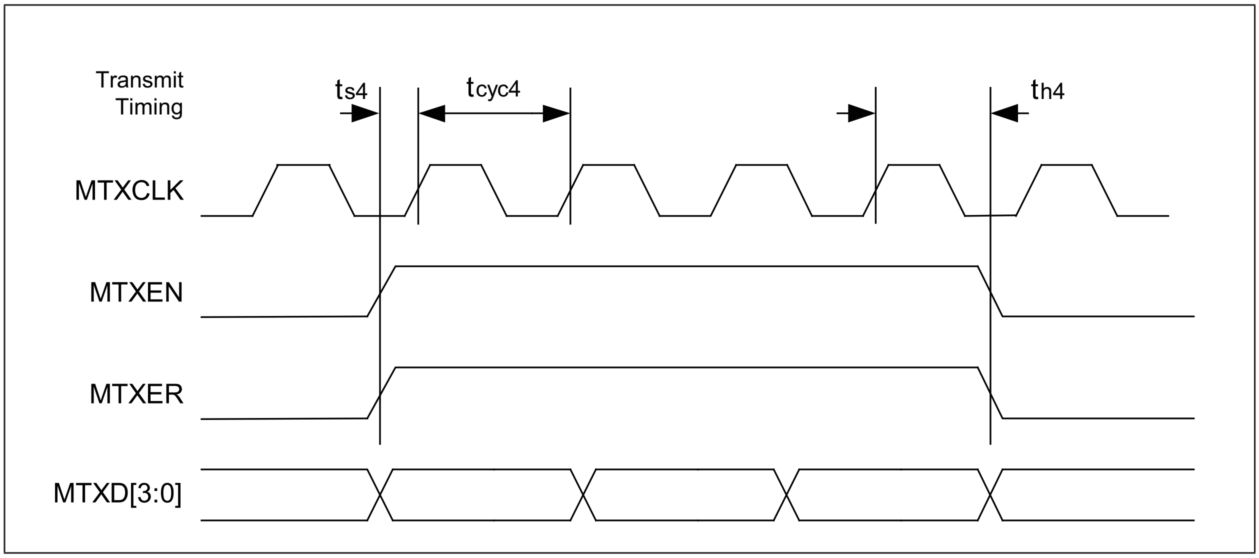


FIGURE 7-6: MII TIMING - DATA INPUT TO MII

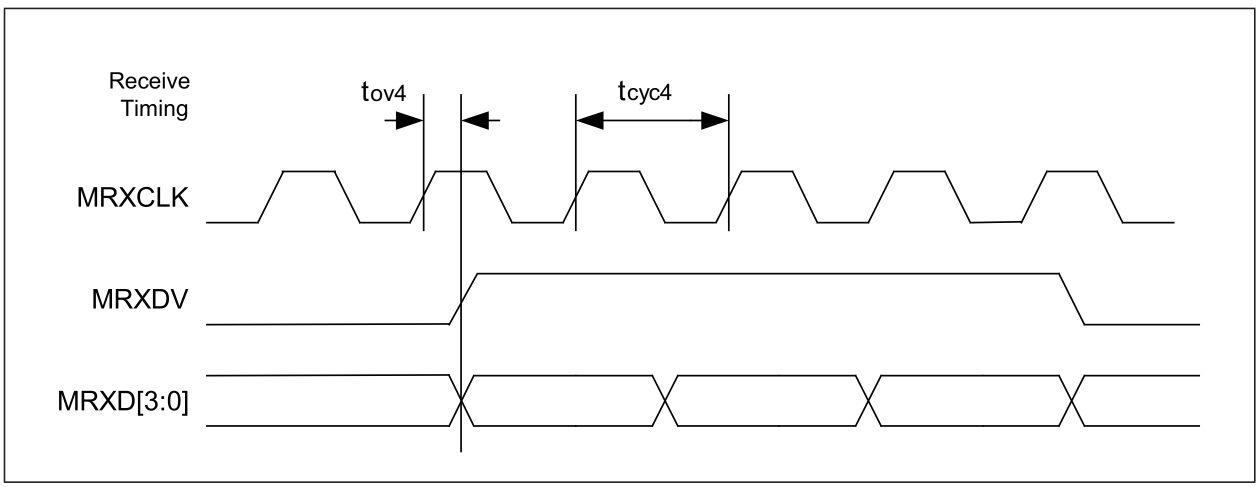


TABLE 7-3: MII TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{cyc4}	Clock cycle (100BASE-TX)	—	40	—	ns
t_{cyc4}	Clock cycle (10BASE-T)	—	400	—	ns
t_{s4}	Setup time	10	—	—	ns
t_{h4}	Hold time	10	—	—	ns
t_{ov4}	Output valid	0	—	25	ns

7.4 RMII Timing

FIGURE 7-7: RMII TIMING – DATA RECEIVED FROM RMII

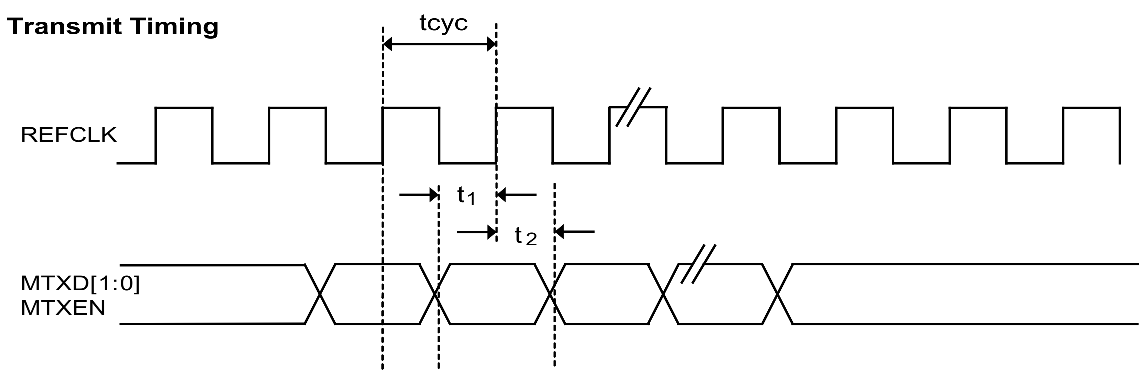


FIGURE 7-8: RMII TIMING – DATA INPUT TO RMII

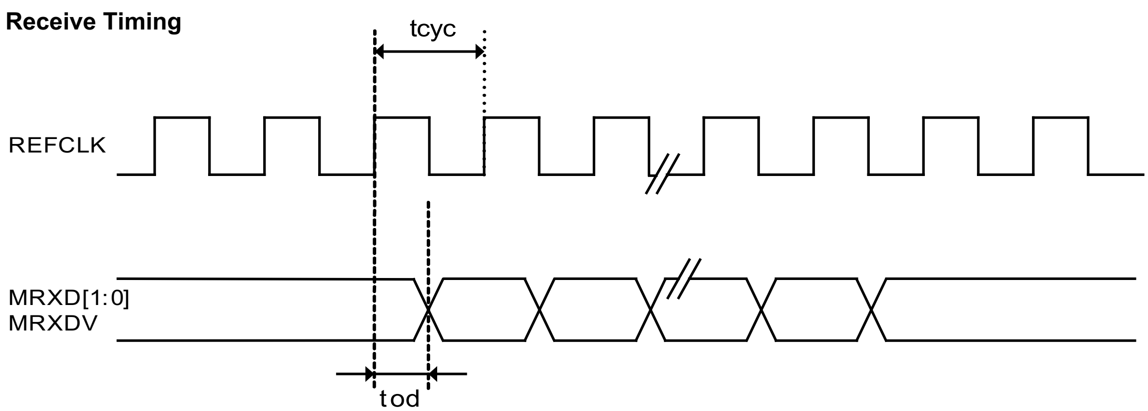


TABLE 7-4: RMII TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{cyc}	Clock cycle	—	20	—	ns
t_1	Setup time	4	—	—	ns
t_2	Hold time	2	—	—	ns
t_{od}	Output delay	2.8	—	10	ns

7.5 SPI Timing

FIGURE 7-9: SPI INPUT TIMING

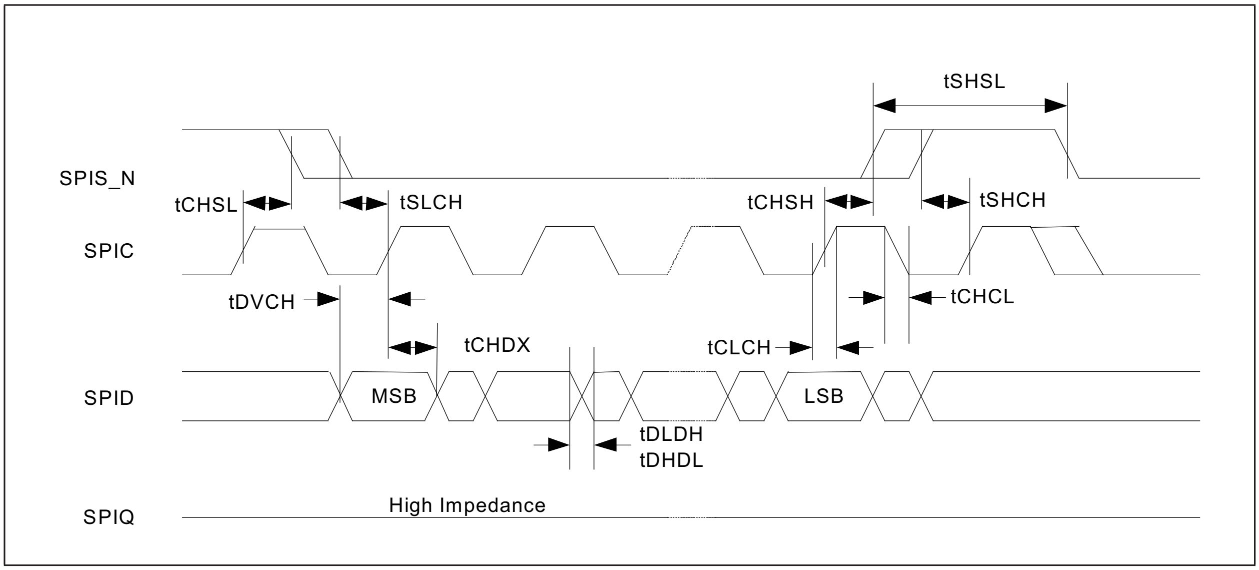


TABLE 7-5: SPI INPUT TIMING PARAMETERS

Parameter	Description	Min.	Max.	Units
f_C	Clock frequency	—	5	MHz
t_{CHSL}	SPIS_N inactive hold time	90	—	ns
t_{SLCH}	SPIS_N active setup time	90	—	ns
t_{CHSH}	SPIS_N active old time	90	—	ns
t_{SHCH}	SPIS_N inactive setup time	90	—	ns
t_{SHSL}	SPIS_N deselect time	100	—	ns
t_{DVCH}	Data input setup time	20	—	ns
t_{CHDX}	Data input hold time	30	—	ns
t_{CLCH}	Clock rise time	—	1	µs
t_{CHCL}	Clock fall time	—	1	µs
t_{DLDH}	Data input rise time	—	1	µs
t_{DHDL}	Data input fall time	—	1	µs

FIGURE 7-10: SPI OUTPUT TIMING

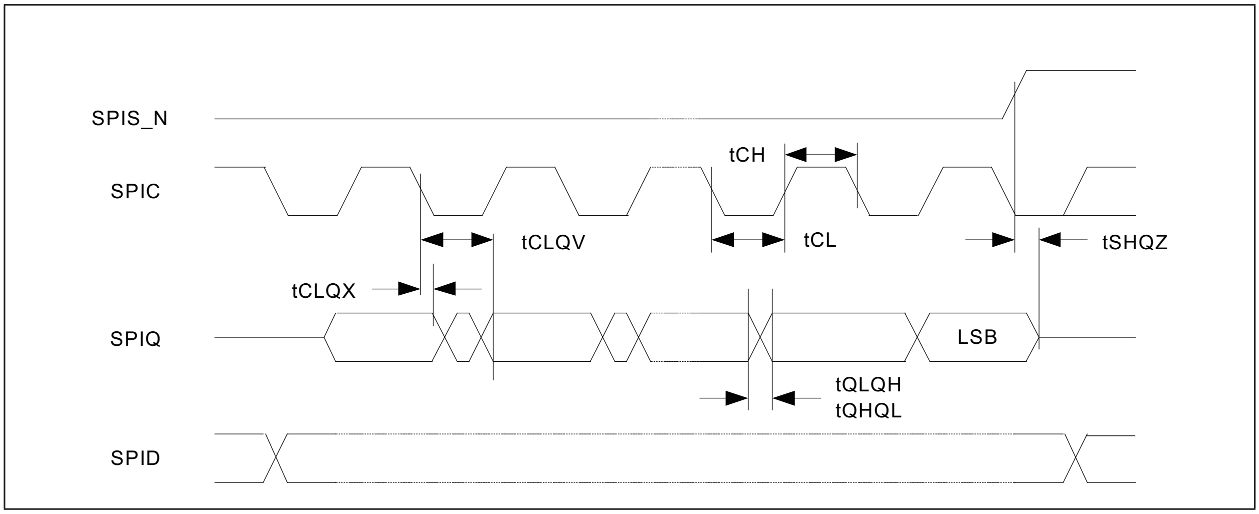


TABLE 7-6: SPI OUTPUT TIMING PARAMETERS

Parameter	Description	Min.	Max.	Units
f_C	Clock frequency	—	5	MHz
t_{CLQX}	SPIQ hold time	0	0	ns
t_{CLQV}	Clock low to SPIQ valid	—	60	ns
t_{CH}	Clock high time	90	—	ns
t_{CL}	Clock low time	90	—	ns
t_{QLQH}	SPIQ rise time	—	50	ns
t_{QHQL}	SPIQ fall time	—	50	ns
t_{SHQZ}	SPIQ disable time	—	100	ns

7.6 Auto-Negotiation Timing

FIGURE 7-11: AUTO-NEGOTIATION TIMING

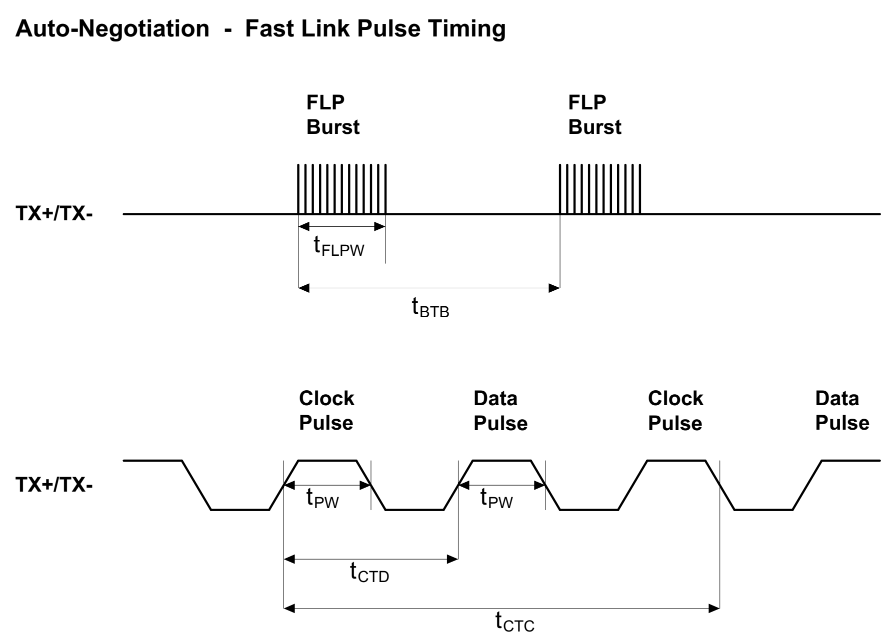


TABLE 7-7: AUTO-NEGOTIATION TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{BTB}	FLP burst to FLP burst	8	16	24	ms
t_{FLPW}	FLP burst width	—	2	—	ms
t_{PW}	Clock/Data pulse width	—	100	—	ns
t_{CTD}	Clock pulse to data pulse	55.5	64	69.5	µs
t_{CTC}	Clock pulse to clock pulse	111	128	139	µs
—	Number of clock/data pulses per burst	17	—	33	—

7.7 Reset Timing

The KSZ8893FQL reset timing requirement is summarized in Figure 7-12 and Table 7-8.

FIGURE 7-12: RESET TIMING

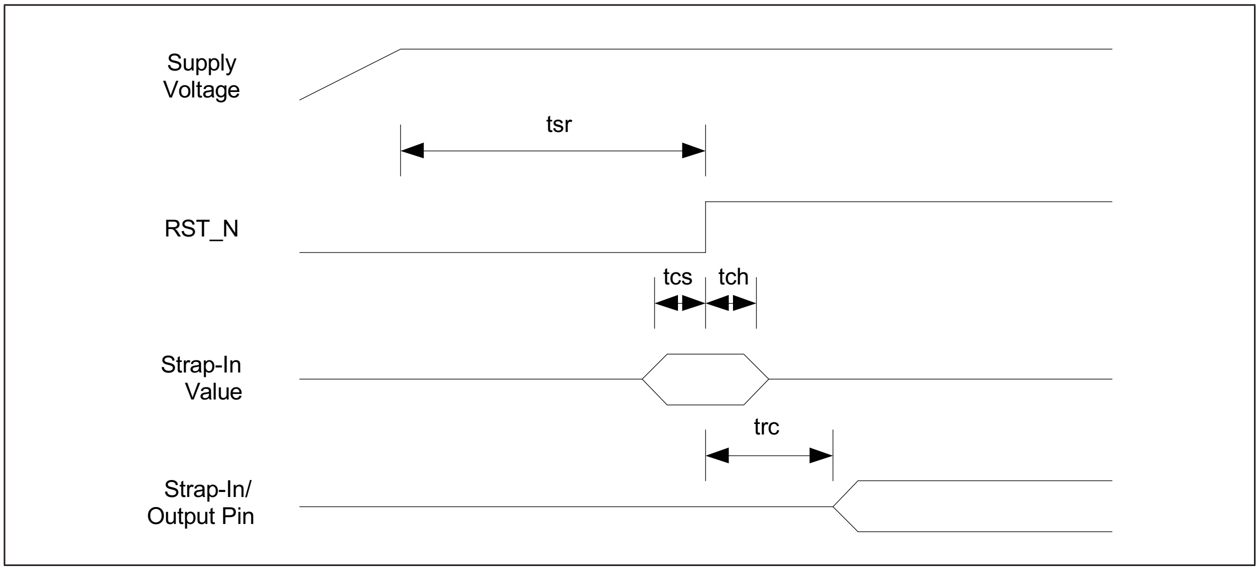


TABLE 7-8: RESET TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{SR}	Stable supply voltages to reset high	10	—	—	ms
t_{CS}	Configuration setup time	50	—	—	ns
t_{CH}	Configuration hold time	50	—	—	ns
t_{RC}	Reset to strap-in pin output	50	—	—	µs

After the deassertion of reset, wait a minimum of 100 µs before starting programming on the managed interface (I^2C slave, SPI slave, SMI, MIIM).

8.0 RESET CIRCUIT

Figure 8-1 shows a reset circuit recommended for powering up the KSZ8873MML if reset is triggered only by the power supply.

FIGURE 8-1: RECOMMENDED RESET CIRCUIT

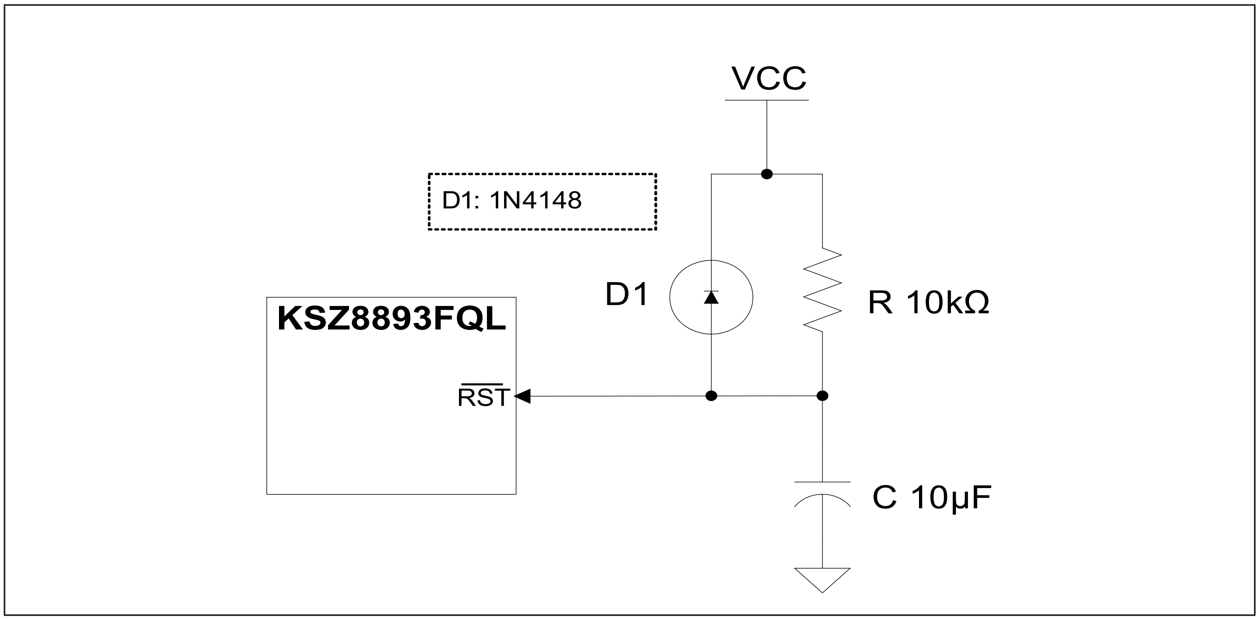
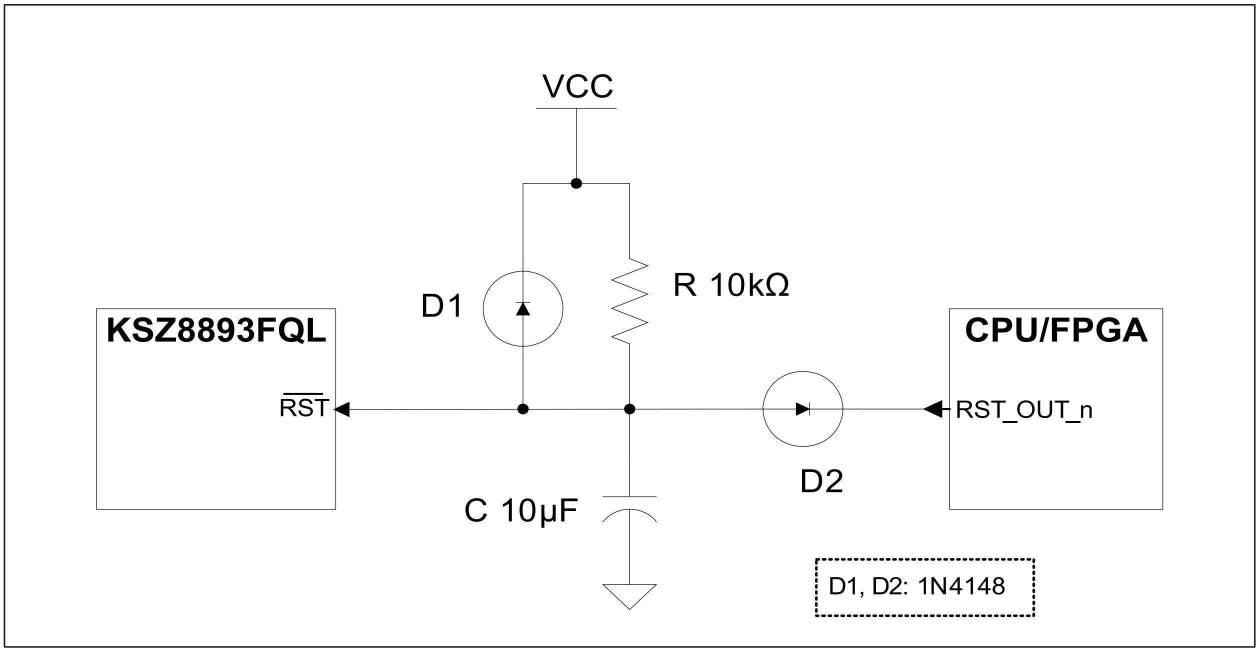


Figure 8-2 shows a reset circuit recommended for applications where reset is driven by another device (e.g., CPU, FPGA, etc),. At power-on-reset, R, C, and D1 provide the necessary ramp rise time to reset the KSZ8893FQL device. The RST_OUT_n from CPU/FPGA provides the warm reset after power up.

FIGURE 8-2: RECOMMENDED RESET CIRCUIT FOR CPU/FPGA RESET OUTPUT



9.0 SELECTION OF ISOLATION TRANSFORMERS

A 1:1 isolation transformer is required at the line interface. Use one with integrated common-mode chokes for designs exceeding FCC requirements.

Table 9-1 lists recommended transformer characteristics.

TABLE 9-1: TRANSFORMER SELECTION CRITERIA

Parameter	Value	Test Conditions
Turns Ratio	1 CT : 1 CT	—
Open-Circuit Inductance (min.)	350 µH	100 mV, 100 kHz, 8 mA
Leakage Inductance (max.)	0.4 µH	1 MHz (min.)
Interwinding Capacitance (max.)	12 pF	—
D.C. Resistance (max.)	0.9Ω	—
Insertion Loss (max.)	1.0 dB	0 MHz to 65 MHz
HIPOT (min.)	1500 V_{RMS}	—

TABLE 9-2: QUALIFIED SINGLE-PORT MAGNETICS

Manufacturer	Part Number	Auto MDI-X
Bel Fuse	S558-5999-U7	Yes
Bel Fuse (MagJack)	SI-46001	Yes
Bel Fuse (MagJack)	SI-50170	Yes
Delta	LF8505	Yes
LanKom	LF-H41S	Yes
Pulse	H1102	Yes
Pulse (Low Cost)	H1260	Yes
Transpower	HB726	Yes
YCL	LF-H41S	Yes
TDK (MagJack)	TLA-6T718	Yes

TABLE 9-3: TYPICAL REFERENCE CRYSTAL CHARACTERISTICS

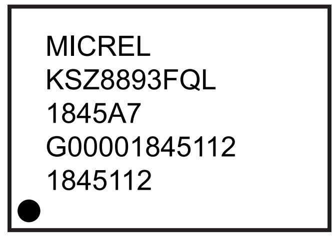
Characteristic	Value
Frequency	25 MHz
Frequency Tolerance (max.)	±50 ppm
Load Capacitance (max.)	20 pF
Series Resistance	40Ω

10.0 PACKAGE OUTLINE

10.1 Package Marking Information

128-Lead PQFP*

Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

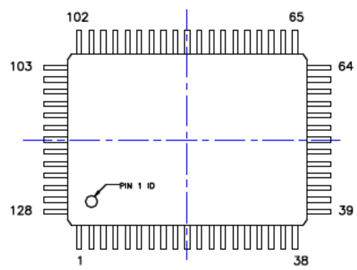
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

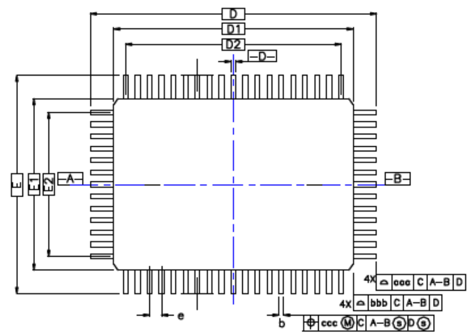
FIGURE 10-1: 128-LEAD PQFP 20 MM X 14 MM PACKAGE

TITLE
128 LEAD PQFP 14x20mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

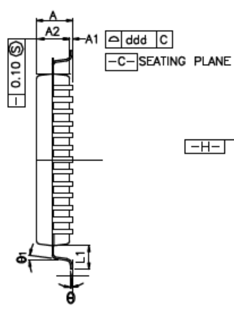
DRAWING #	PQFP14x20-128LD-PL-1	**UNIT**	MM [INCHES]



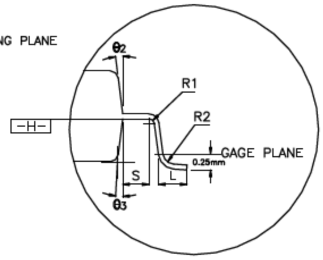
TOP VIEW
Note 1,2,3



BOTTOM VIEW
Note 1,2,3



SIDE VIEW
Note 1,2,3



DETAILED VIEW

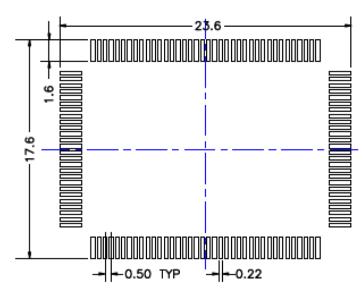
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A_1	0.25	—	—	0.010	—	—
A_2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D_1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E_1	14.00 BASIC			0.551 BASIC		
R_2	0.13	—	0.30	0.005	—	0.012
R_1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ_1	0°	—	—	0°	—	—
θ_2 , θ_3	15° REF			15° REF		

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.170	0.200	0.270	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

COTROL DIMENSIONS ARE IN MILLIMETERS.

NOTES :

1. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
3. THE DIAGRAMS DO NOT REPRESNET THE ACTUAL PIN COUNT.
4. ALL UNITS IN mm. TOLERANCE +/- 0.05 IF NOT NOTED.



RECOMMENDED LAND PATTERN
Note 4

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00003038A (4-22-19)	—	Converted Micrel data sheet KSZ8893FQL to Microchip DS00003038A. Minor text changes throughout.
DS00003038B (10-24-19)	TABLE 2-1: “Signals”	Added description for pin numbers 90 through 99 and updated the description for pin numbers 110 through 126.
	—	Updated the Examples column in the product identification system page from Fiber Interface to Fiber analog interface and MII/RMII digital interface

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PART NO.	X	X	X	X	— XX	— XX
Device	Interface	Package	Supply Voltage	Temperature	Media Type	Feature

Device:	KSZ8893
Interface:	F = Fiber Interface
Package:	Q = 128-lead 20 mm x 14 mm PQFP
Supply Voltage:	L = Single 3.3V Supply
Temperature:	blank = 0°C to +70°C (Commercial) I = –40°C to +85°C (Industrial)
Media Type:	blank = 160/Tray
Feature:	blank = Port 1 supports 10BASE-FL and 100BASE-SX with LED driver and post amp FX = Port 1 supports 100BASE-FX with TS-1000 OAM V2

Examples:

a) KSZ8893FQL
Fiber Analog Interface and MII/RMII Digital Interface
128-lead 20 mm x 14 mm PQFP
Single 3.3V Supply
Commercial Temperature Range
160/Tray
Port 1 Supports 10BASE-FL and 100BASE-SX with LED Driver and Post Amp

b) KSZ8893FQL-FX
Fiber Analog Interface and MII/RMII Digital Interface
128-lead 20 mm x 14 mm PQFP
Single 3.3V Supply
Commercial Temperature Range
160/Tray
Port 1 supports 100BASE-FX with TS-1000 OAM V2

c) KSZ8893FQLI-FX
Fiber Analog Interface and MII/RMII Digital Interface
128-lead 20 mm x 14 mm PQFP
Single 3.3V Supply
Industrial Temperature Range
160/Tray

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