

MIC28304

70V, 3A Power Module Hyper Speed Control[®] Family

Features

- · Easy to Use:
 - Stable with low-ESR ceramic output capacitor
 - No compensation and no inductor to choose
- 4.5V to 70V Input Voltage
- Single-Supply Operation
- Power Good (PG) Output
- Low Radiated Emission (EMI) per EN55022, Class B
- · Adjustable Current Limit
- Adjustable Output Voltage from 0.8V to 24V (also limited by duty cycle)
- 200 kHz to 600 kHz Programmable Switching Frequency
- · Supports Safe Start-up into a Pre-Biased Output
- -40°C to +125°C Junction Temperature Range
- Available in 64-Pin, 12 mm x 12 mm x 3 mm QFN Package

Applications

- · Distributed Power Systems
- Industrial, Medical, Telecom and Automotive

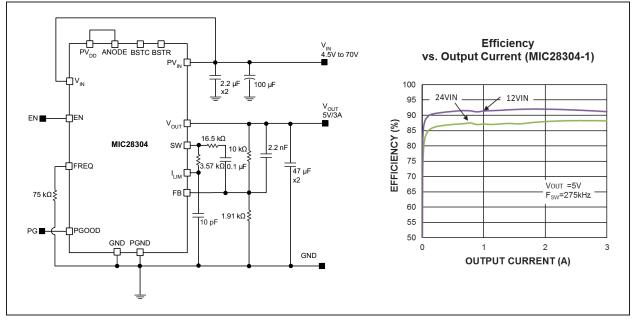
General Description

Microchip's MIC28304 is a synchronous, step-down regulator module, featuring a unique adaptive on-time control architecture. The module incorporates a DC-to-DC controller, power MOSFETs, bootstrap diode, bootstrap capacitor and an inductor in a single package. The MIC28304 operates over an input supply range from 4.5V to 70V and can be used to supply up to 3A of output current. The output voltage is adjustable down to 0.8V with an ensured accuracy of $\pm 1\%$. The device operates with a programmable switching frequency from 200 kHz to 600 kHz.

Microchip's HyperLight Load[®] architecture provides the same high-efficiency and ultra-fast transient response as the Hyper Speed Control[®] architecture under the medium to heavy loads. The architecture also maintains high efficiency under light load conditions by transitioning to Variable Frequency Discontinuous mode operation.

The MIC28304 offers a full suite of protection features. These include undervoltage lockout, internal soft start, foldback current limit, "Hiccup" mode short-circuit protection and thermal shutdown.

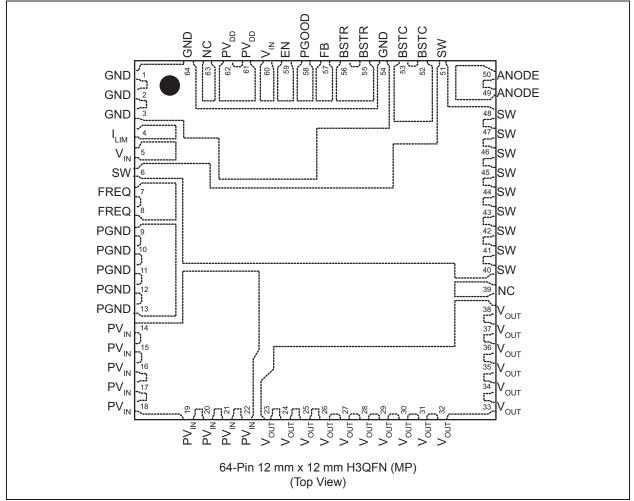
Data sheets and other support documentation can be found on the Microchip web site at: www.microchip.com.



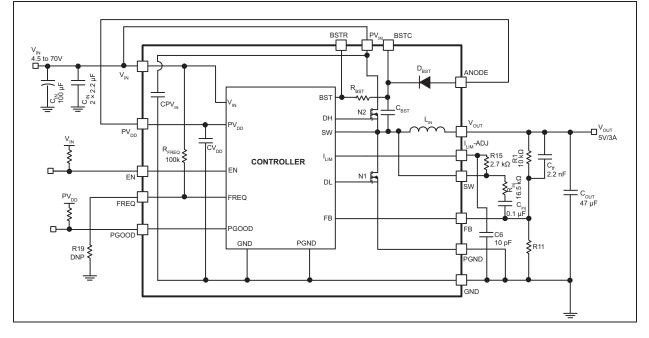
Typical Application Schematic

MIC28304

Package Types



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings⁺⁽¹⁾

PV _{IN} , V _{IN} to PGND	-0.3V to +76V
PV _{DD} , V _{ANODE} to PGND	-0.3V to +6V
V _{SW} , V _{FREQ} , V _{ILIM} , V _{EN}	0.3V to (PV _{IN} + 0.3V)
V _{BSTC/BSTR} to V _{SW}	-0.3V to 6V
V _{BSTC/BSTR} to PGND	-0.3V to 82V
V _{FB} , V _{PG} to PGND	0.3V to (PV _{DD} + 0.3V)
PGND to AGND	-0.3V to +0.3V
Junction Temperature	+150°C
Storage Temperature (T _S)	65°C to +150°C
Lead Temperature (soldering, 10s)	+260°C
ESD Rating ⁽¹⁾	ESD-Sensitive

Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Devices are ESD-sensitive. Handling precautions are recommended. Human body model, 1.5 k Ω in series with 100 pF.

Operating Ratings⁽¹⁾

t.

Supply Voltage (PV _{IN} , V _{IN})	4.5V to 70V
Enable Input (V _{EN})	0V to V _{IN}
V _{SW} , V _{FREQ} , V _{ILIM} , V _{EN}	0V to V _{IN}
Power Good (V _{PGOOD})	0V to PV _{DD}
Junction Temperature (T _J)	40°C to +125°C
Junction Thermal Resistance	
12mm × 12mm QFN-64 (θ _{JA})	20°C/W
12mm × 12mm QFN-64 (θ _{JC})	5°C/W

Note 1: The device is not ensured to function outside the operating range.

TABLE 1-1: ELECTRICAL CHARACTERISTICS⁽¹⁾

Symbol Power Supply PV _{IN} , V _{IN} IQ I _{IN} I _{SD} PV _{DD} Supply V _{PVDD} V _{UVLO}	Parameter Input Input Voltage Range Controller Supply Current Operating Current Shutdown Supply Current PV _{DD} Output Voltage PV _{DD} UVLO Threshold PV _{DD} UVLO Hysteresis Load Regulation	Min. 4.5 — — — — — 4.8 3.8	Typ. 0.4 2.1 0.1 0.7 27 4 5.2	Max. 70 0.75 3 10 	- mA - μA - mA	Test ConditionsCurrent into Pin 60, $V_{FB} = 1.5V$ (MIC28304-1)Current into Pin 60, $V_{FB} = 1.5V$ (MIC28304-2)Current into Pin 60, $V_{EN} = 0V$ I _{OUT} = 0A (MIC28304-1)I _{OUT} = 0A (MIC28304-2)PVIN = VIN = 12V, $V_{EN} = 0V$
PV _{IN} , V _{IN} I _Q I _{IN} I _{SD} PV _{DD} Supply V _{PVDD}	Input Voltage Range Controller Supply Current Operating Current Shutdown Supply Current PV _{DD} Output Voltage PV _{DD} UVLO Threshold PV _{DD} UVLO Hysteresis		2.1 0.1 0.7 27 4	0.75 3 10 —	mA μA mA	$\begin{array}{l} ({\sf MIC28304-1}) \\ {\sf Current\ into\ Pin\ 60,\ V_{\sf FB}} = 1.5 {\sf V} \\ ({\sf MIC28304-2}) \\ {\sf Current\ into\ Pin\ 60,\ V_{\sf EN}} = 0 {\sf V} \\ \\ {\sf I}_{\sf OUT} = 0 {\sf A}\ ({\sf MIC28304-1}) \\ \\ {\sf I}_{\sf OUT} = 0 {\sf A}\ ({\sf MIC28304-2}) \end{array}$
I _Q I _{IN} I _{SD} PV _{DD} Supply V _{PVDD}	Controller Supply Current Operating Current Shutdown Supply Current PV _{DD} Output Voltage PV _{DD} UVLO Threshold PV _{DD} UVLO Hysteresis		2.1 0.1 0.7 27 4	0.75 3 10 —	mA μA mA	$\begin{array}{l} ({\sf MIC28304-1}) \\ {\sf Current\ into\ Pin\ 60,\ V_{\sf FB}} = 1.5 {\sf V} \\ ({\sf MIC28304-2}) \\ {\sf Current\ into\ Pin\ 60,\ V_{\sf EN}} = 0 {\sf V} \\ \\ {\sf I}_{\sf OUT} = 0 {\sf A}\ ({\sf MIC28304-1}) \\ \\ {\sf I}_{\sf OUT} = 0 {\sf A}\ ({\sf MIC28304-2}) \end{array}$
I _{IN} I _{SD} PV _{DD} Supply V _{PVDD}	Operating Current Shutdown Supply Current PV _{DD} Output Voltage PV _{DD} UVLO Threshold PV _{DD} UVLO Hysteresis		0.1 0.7 27 4	10 	μA mA	Current into Pin 60, $V_{FB} = 1.5V$ (MIC28304-2) Current into Pin 60, $V_{EN} = 0V$ $I_{OUT} = 0A$ (MIC28304-1) $I_{OUT} = 0A$ (MIC28304-2)
I _{SD} PV _{DD} Supply V _{PVDD}	Shutdown Supply Current PV _{DD} Output Voltage PV _{DD} UVLO Threshold PV _{DD} UVLO Hysteresis	4.8	0.7 27 4		mA	Current into Pin 60, $V_{EN} = 0V$ $I_{OUT} = 0A (MIC28304-1)$ $I_{OUT} = 0A (MIC28304-2)$
I _{SD} PV _{DD} Supply V _{PVDD}	Shutdown Supply Current PV _{DD} Output Voltage PV _{DD} UVLO Threshold PV _{DD} UVLO Hysteresis	4.8	27 4		mA	I _{OUT} = 0A (MIC28304-1) I _{OUT} = 0A (MIC28304-2)
I _{SD} PV _{DD} Supply V _{PVDD}	Shutdown Supply Current PV _{DD} Output Voltage PV _{DD} UVLO Threshold PV _{DD} UVLO Hysteresis	4.8	4			I _{OUT} = 0A (MIC28304-2)
PV _{DD} Supply V _{PVDD}	PV _{DD} Output Voltage PV _{DD} UVLO Threshold PV _{DD} UVLO Hysteresis	4.8	4		μA	
PV _{DD} Supply V _{PVDD}	PV _{DD} Output Voltage PV _{DD} UVLO Threshold PV _{DD} UVLO Hysteresis		5.2	1		$ \cdot v_{\rm IN} - v_{\rm IN} - i \angle v, v_{\rm FN} - 0 v$
V _{PVDD}	PV _{DD} UVLO Threshold PV _{DD} UVLO Hysteresis		52			
	PV _{DD} UVLO Threshold PV _{DD} UVLO Hysteresis	3.8	J.Z	5.4	V	V_{IN} = 7V to 70V, I_{PVDD} = 10 m/
V _{UVLO}			4.2	4.7	V	PV _{DD} rising
	Load Regulation	_	400		mV	
LReg		0.6	2	3.6	%	I _{PVDD} = 0 to 40 mA
Reference				1	1	1 · ·
V _{REF}	Feedback Reference	0.792	0.8	0.808	V	T _J = +25°C (±1.0%)
	Voltage	0.784	0.8	0.816	V	$-40^{\circ}C \le T_{J} \le +125^{\circ}C (\pm 2\%)$
V _{FB}	FB Bias Current	_	5	500	nA	V _{FB} = 0.8V
Enable Contro	i i			•		
V _{EN_H}	EN Logic Level High	1.8	_	_	V	
V _{EN_L}	EN Logic Level Low	_	_	0.6	V	
V _{EN_HYST}	EN Hysteresis	_	200		mV	
V _{EN BIAS}	EN Bias Current	_	5	20	μA	V _{EN} = 12V
Oscillator					I .	
		400	600	750		FREQ Pin = Open
F _{SW}	Switching Frequency	_	300		kHz	R _{FREQ} = 100 kΩ (FREQ pin to GND)
D _{MAX}	Maximum Duty Cycle	_	85		%	
D _{MIN}	Minimum Duty Cycle	_	0		%	V _{FB} > 0.8V
T _{OFF MIN}	Minimum Off-Time	140	200	260	ns	
Soft Start				I		
T _{SS}	Soft Start Time	_	5	_	ms	1
Short-Circuit F				I		1
V _{CL_OFFSET}	Current-Limit Threshold	-30	-14	0	mV	V _{FB} = 0.79V
V _{SHORT}	Short-Circuit Threshold	-23	-7	9	mV	V _{FB} = 0V
	Current-Limit Source Current	60	80	100	μA	V _{FB} = 0.79V
I _{SHORT}	Short-Circuit Source Current	27	36	47	μΑ	V _{FB} = 0V
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Note 1: Specifications are for packaged product only.

ELECTRICAL CHARACTERISTICS⁽¹⁾ (CONTINUED) TABLE 1-1:

Overtemperature Shutdown

Overtemperature Shutdown

Output Voltage Ripple

Line Regulation

Load Regulation

Hysteresis

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Power Good						
V _{PG_TH}	Power Good Threshold Voltage	85	90	95	%V _{OUT}	Sweep V _{FB} from low-to-high
V _{PG_HYS}	Power Good Hysteresis	_	6	—	%V _{OUT}	Sweep V _{FB} from high-to-low
T _{PG_DLY}	Power Good Delay Time	_	100	_	μs	Sweep V _{FB} from low-to-high
V _{PG LO}	Power Good Low Voltage	_	70	200	mV	V _{FB} < 90% x V _{nom} , I _{PG} = 1 mA

160

4

16

0.36

0.75

0.05

400

500

400

500

°C

°C

mV

%

%

mV

I_{OUT} = 3A,

 $I_{OUT} = 3A$,

 $I_{OUT} = 0A$ to 3A,

 $I_{OUT} = 0A$ to 3A,

(MIC28304-1),

(MIC28304-1),

(MIC28304-2),

(MIC28304-1),

1x47 µF output capacitor

 $PV_{IN} = V_{IN} = 7V$ to 70V,

1x47 µF output capacitor

1x47 µF output capacitor

1x47 µF output capacitor

1x47 µF output capacitor I_{OUT} from 3A to 0A at 5A/µs

1x47 µF output capacitor

I_{OUT} from 3A to 0A at 5A/µs

I_{OUT} from 0A to 3A at 5A/µs

PV_{IN} = V_{IN} = 12V (MIC28304-1)

PV_{IN} = V_{IN} = 12V (MIC28304-2) I_{OUT} from 0A to 3A at 5A/µs

Note 1:	Specifications are for packaged product only.

Output Voltage Deviation

from Load Step

T_{SD}

V_{OR}

LineReg

LoadReg

T_{SD HYST}

Output Characteristic

2.0 TYPICAL PERFORMANCE CURVES (275 kHz SWITCHING FREQUENCY)

The graphs and tables provided following this note are a statistical summary based on a limited number of Note: samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

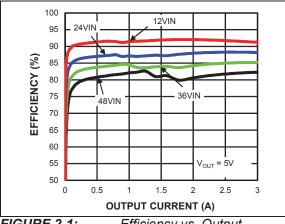
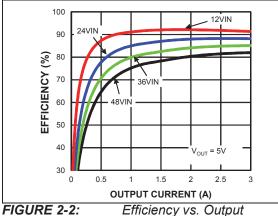
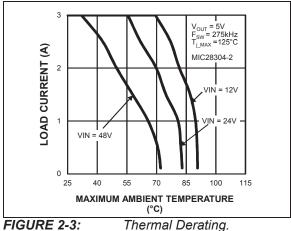


FIGURE 2-1: Efficiency vs. Output Current (MIC28304-1).



Current (MIC28304-2).



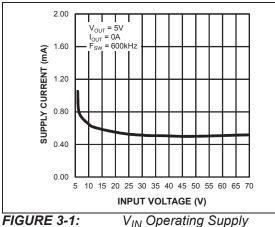
Thermal Derating.

TABLE 2-1: RE	COMMENDED COMPONENT VALUES FOR 275 kHz SWITCHING FREG	UENCY
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V _{OUT}	V _{IN}	R3 (R _{inj})	R19	R15	R1 (Top Feedback Resistor)	R11 (Bottom Feedback Resistor)	C10 (C _{inj})	C12 (C _{ff})	C _{OUT}
5V	7V to 18V	16.5 kΩ	75 kΩ	3.57k	10 kΩ	1.9 kΩ	0.1 µF	2.2 nF	2 x 47 µF/6.3V
5V	18V to 70V	39.2 kΩ	$75 \ k\Omega$	3.57k	10 kΩ	1.9 kΩ	0.1 µF	2.2 nF	2 x 47 µF/6.3V
3.3V	5V to 18V	$16.5 \ k\Omega$	$75 \ k\Omega$	3.57k	10 kΩ	3.24 kΩ	0.1 µF	2.2 nF	2 x 47 µF/6.3V
3.3V	18V to 70V	39.2 kΩ	$75 \ k\Omega$	3.57k	10 kΩ	3.24 kΩ	0.1 µF	2.2 nF	2 x 47 µF/6.3V

3.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.



Current vs. Input Voltage (MIC28304-1).

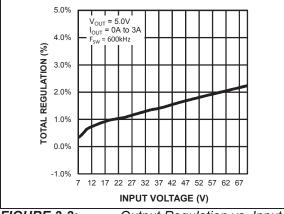


FIGURE 3-2: Output Regulation vs. Input Voltage (MIC28304-1).

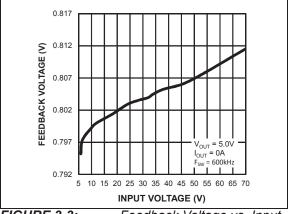


FIGURE 3-3: Feedback Voltage vs. Input Voltage (MIC28304-1).

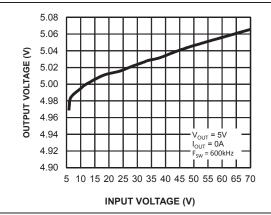


FIGURE 3-4: Output Voltage vs. Input Voltage (MIC28304-1).

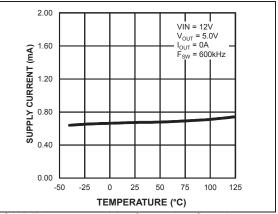


FIGURE 3-5: V_{IN} Operating Supply Current vs. Temperature (MIC28304-1).

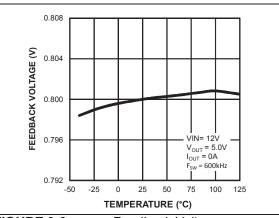
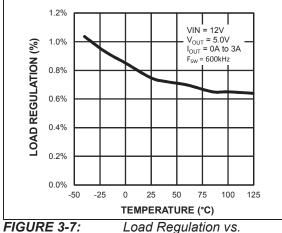


FIGURE 3-6: Feedback Voltage vs. Temperature (MIC28304-1).



Temperature (MIC28304-1).

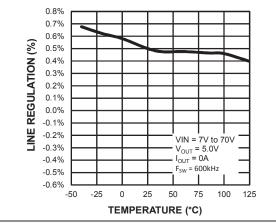


FIGURE 3-8: Line Regulation vs. Temperature (MIC28304-1).

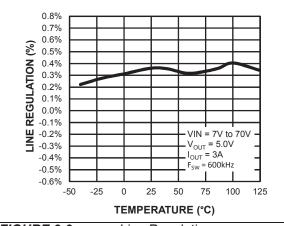


FIGURE 3-9: Line Regulation vs. Temperature (MIC28304-1).

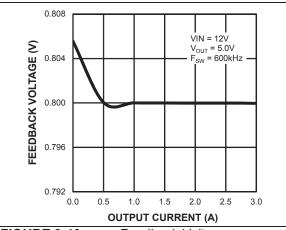


FIGURE 3-10: Feedback Voltage vs. Output Current (MIC28304-1).

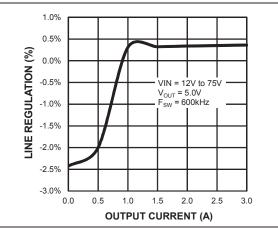
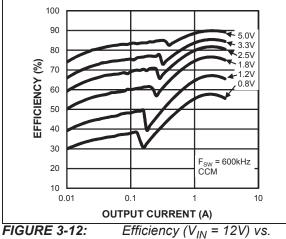


FIGURE 3-11: Line Regulation vs. Output Current (MIC28304-1).



Output Current (MIC28304-1).

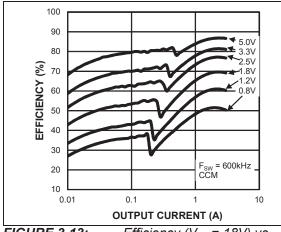


FIGURE 3-13: Efficiency ($V_{IN} = 18V$) vs. Output Current (MIC28304-1).

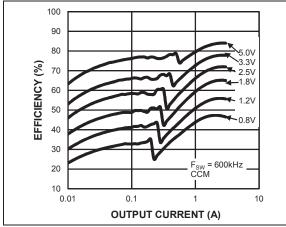


FIGURE 3-14: Efficiency ($V_{IN} = 24V$) vs. Output Current (MIC28304-1).

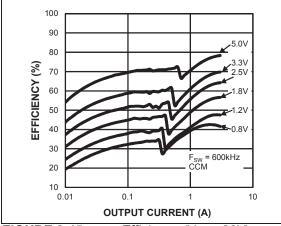


FIGURE 3-15: Efficiency ($V_{IN} = 38V$) vs. Output Current (MIC28304-1).

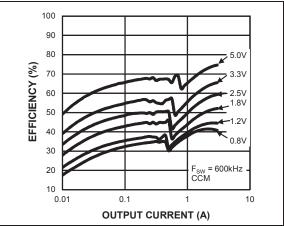


FIGURE 3-16: Efficiency ($V_{IN} = 48V$) vs. Output Current (MIC28304-1).

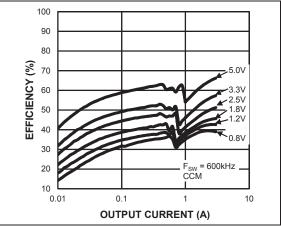


FIGURE 3-17: Efficiency ($V_{IN} = 70V$) vs. Output Current (MIC28304-1).

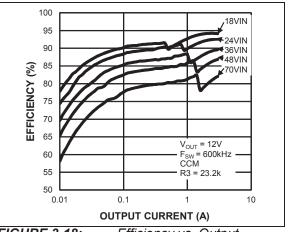
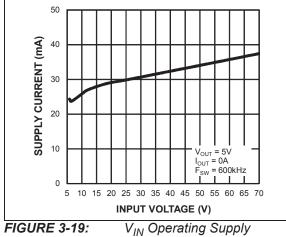


FIGURE 3-18: Efficiency vs. Output Current (MIC28304-1).



Current vs. Input Voltage (MIC28304-2).

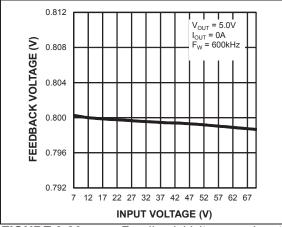
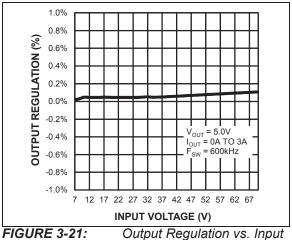
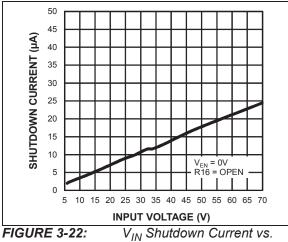


FIGURE 3-20: Feedback Voltage vs. Input Voltage (MIC28304-2).



Voltage (MIC28304-2).



Input Voltage.

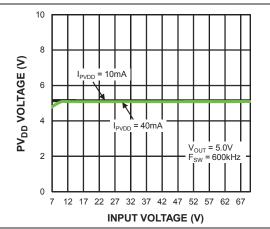
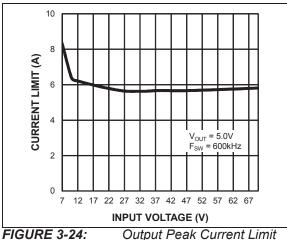
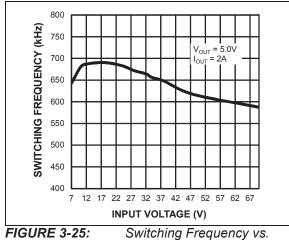


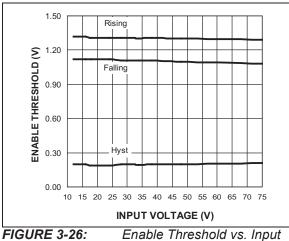
FIGURE 3-23: PV_{DD} Voltage vs. Input Voltage.



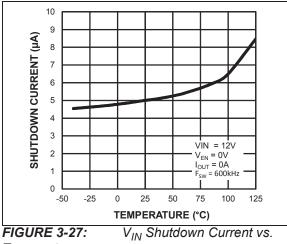
vs. Input Voltage.



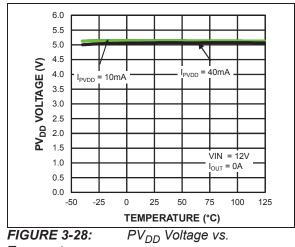




Voltage.



Temperature.





e. .

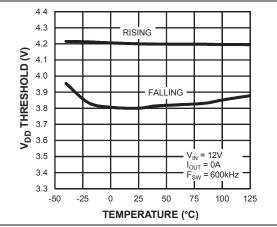
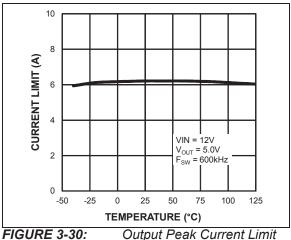
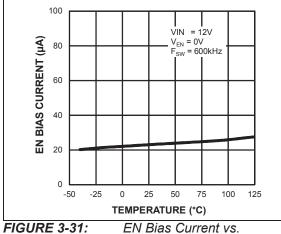


FIGURE 3-29: PV_{DD} UVLO Threshold vs. Temperature.



vs. Temperature.



Temperature.

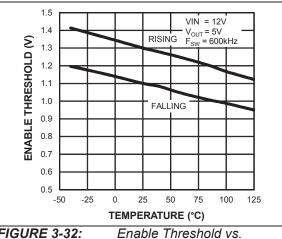


FIGURE 3-32: Temperature.

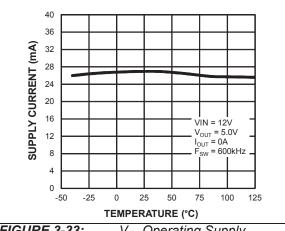


FIGURE 3-33: V_{IN} Operating Supply Current vs. Temperature (MIC28304-2).

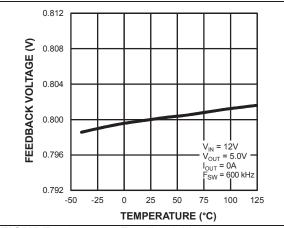


FIGURE 3-34: Feedback Voltage vs. Temperature (MIC28304-2).

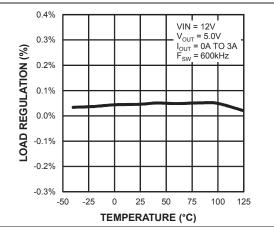


FIGURE 3-35: Load Regulation vs. Temperature (MIC28304-2).

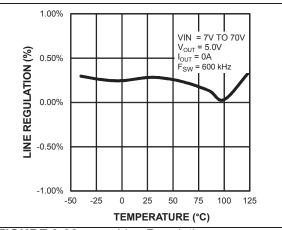


FIGURE 3-36: Line Regulation vs. Temperature (MIC28304-2).

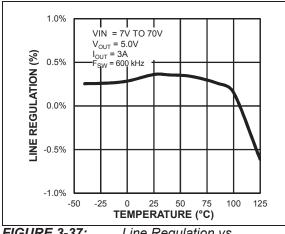


FIGURE 3-37: Line Regulation vs. Temperature (MIC28304-2).

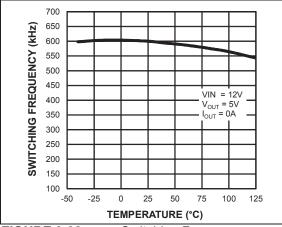


FIGURE 3-38: Switching Frequency vs. Temperature (MIC28304-2).

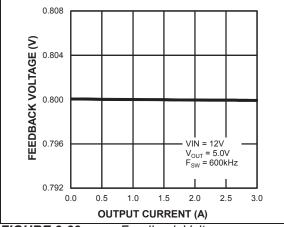


FIGURE 3-39: Feedback Voltage vs. Output Current (MIC28304-2).

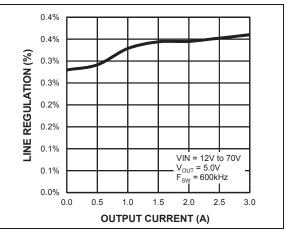


FIGURE 3-40: Line Regulation vs. Output Current (MIC28304-2).

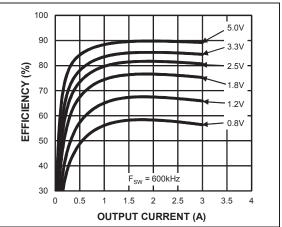


FIGURE 3-41: Efficiency ($V_{IN} = 12V$) vs. Output Current (MIC28304-2).

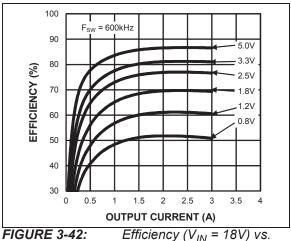
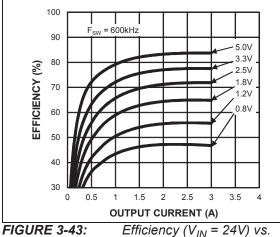


FIGURE 3-42: Efficiency $(V_{IN} = 18V)$ vs. Output Current (MIC28304-2).



Output Current (MIC28304-2).

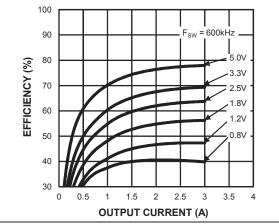


FIGURE 3-44: Efficiency ($V_{IN} = 38V$) vs. Output Current (MIC28304-2).

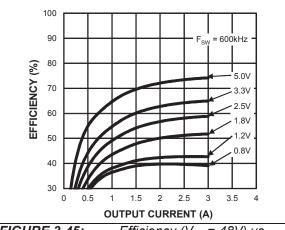


FIGURE 3-45: Efficiency ($V_{IN} = 48V$) vs. Output Current (MIC28304-2).

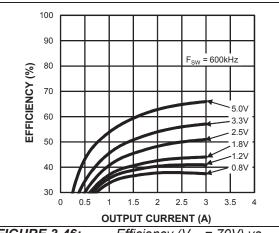
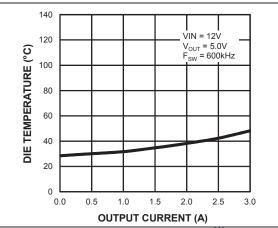
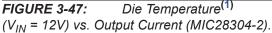
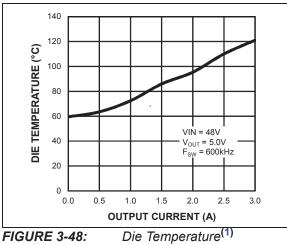
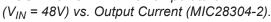


FIGURE 3-46: Efficiency ($V_{IN} = 70V$) vs. Output Current (MIC28304-2).

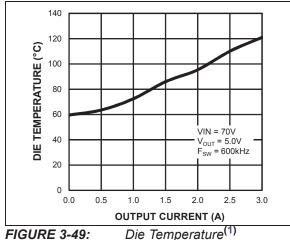




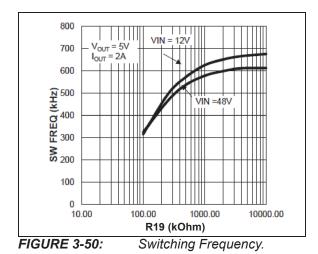




Note 1: Case Temperature: The temperature measurement was taken at the hottest point on the MIC28304 case mounted on a 5 square inch PCB (see Section 7.7 "Thermal Measurements and Safe Operating Area"). Actual results will depend upon the size of the PCB, ambient temperature and proximity to other heat emitting components.



 $(V_{IN} = 70V)$ vs. Output Current (MIC28304-2).



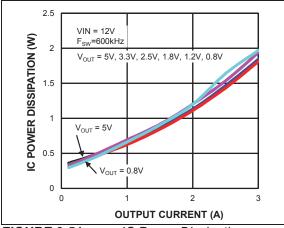


FIGURE 3-51: IC Power Dissipation vs. Output Current (MIC28304-2).

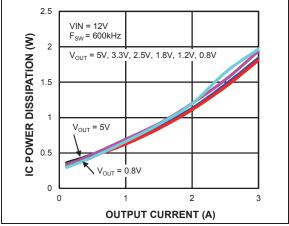


FIGURE 3-52: IC Power Dissipation vs. Output Current (MIC28304-2).

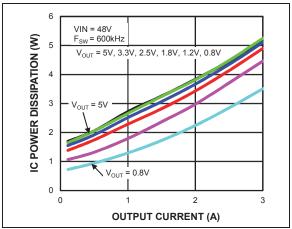
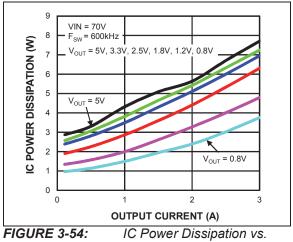


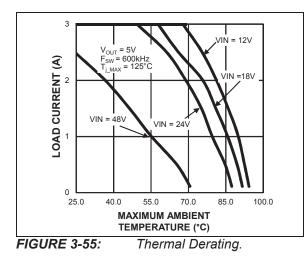
FIGURE 3-53: IC Power Dissipation vs. Output Current (MIC28304-2).

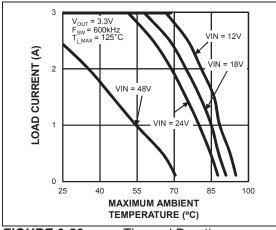


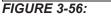
Output Current (MIC28304-2).

Note 1: Case Temperature: The temperature measurement was taken at the hottest point on the MIC28304 case mounted on a 5 square inch PCB (see Section 7.7 "Thermal Measurements and Safe Operating Area"). Actual results will depend upon the size of the PCB, ambient temperature and proximity to other heat emitting components.

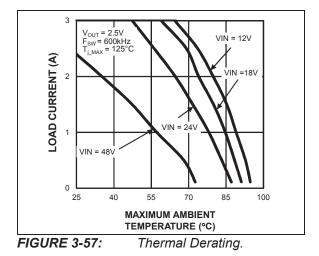
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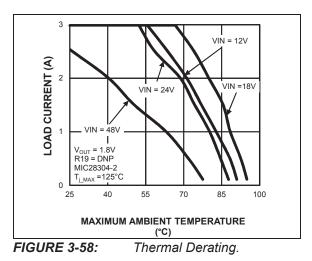


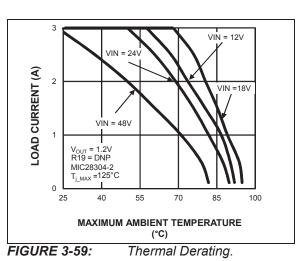


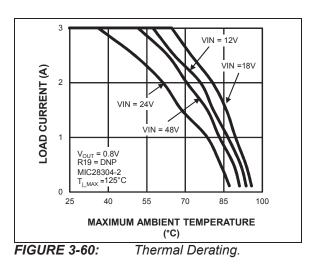


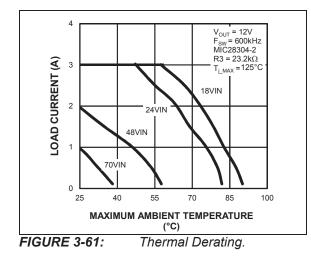
Thermal Derating.











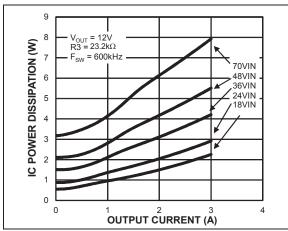


FIGURE 3-62: IC Power Dissipation vs. Output Current (MIC28304-2).

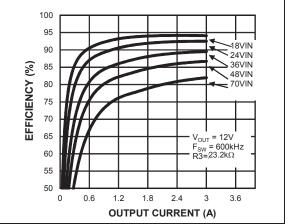
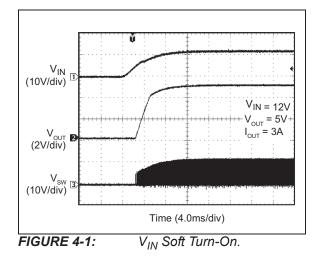


FIGURE 3-63: Efficiency vs. Output Current (MIC28304-2).

4.0 TYPICAL PERFORMANCE CURVES (600 kHz SWITCHING FREQUENCY)



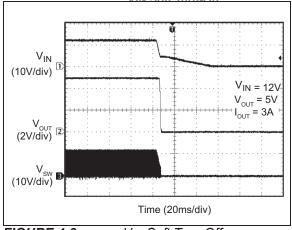
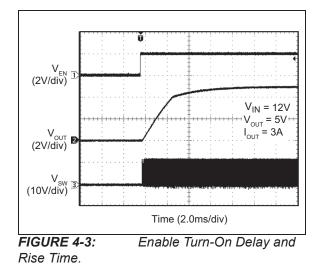


FIGURE 4-2: V

V_{IN} Soft Turn-Off.



V_{EN} (2V/div) V_{IN} = 12V V_{OUT} = 5V V_{OUT} = 3A ++ V_{OUT} = 3A ++ V_{OUT} = 3A ++ V_{OUT} = 12V V_{OUT} = 5V V_{OUT} = 3A ++ Time (1.0ms/div)

FIGURE 4-4:Enable Turn-Off Delay andFall Time.

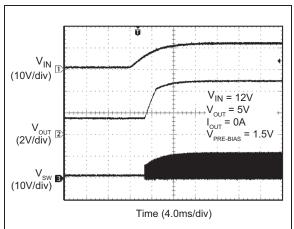


FIGURE 4-5: MIC28304-2 V_{IN} Start-up with Pre-Biased Output.

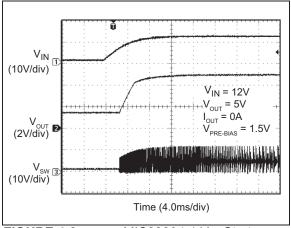


FIGURE 4-6: MIC28304-1 V_{IN} Start-up with Pre-Biased Output.

 $V_{IN} = 12V$ $V_{OUT} = 5V$ $I_{OUT} = SHORT$

 V_{IN} = 12V V_{OUT} = 5V I_{OUT} = SHORT

V_{IN} = 12V $V_{OUT} = 5V$

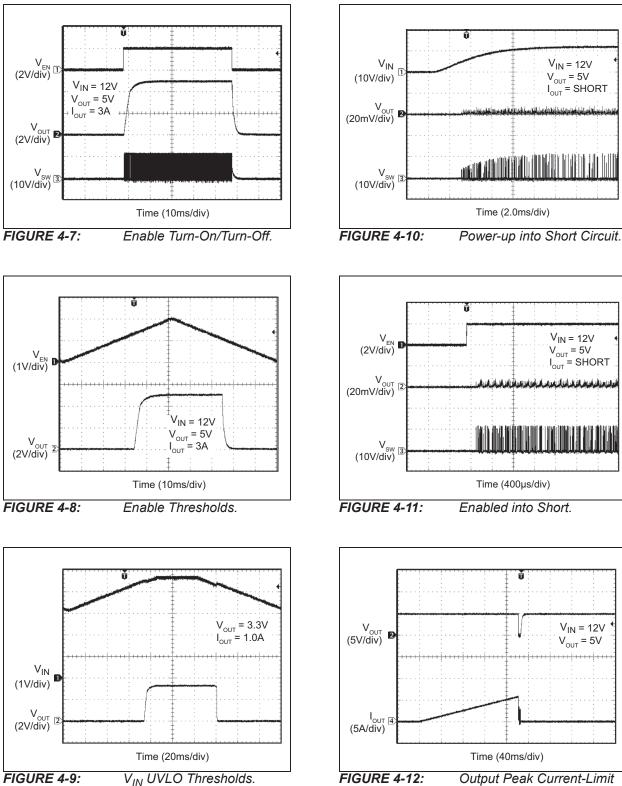


FIGURE 4-12: Threshold.

Output Peak Current-Limit

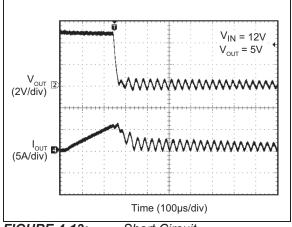


FIGURE 4-13:

Short Circuit.

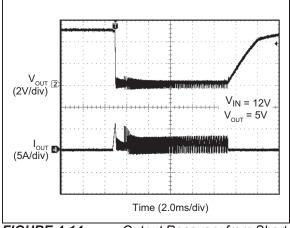


FIGURE 4-14: Output Recovery from Short Circuit.

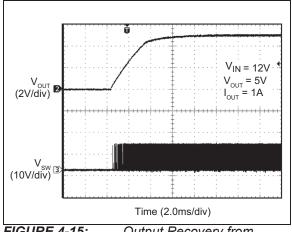


FIGURE 4-15: Output Recovery from Thermal Shutdown.

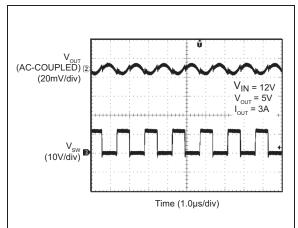


FIGURE 4-16: MIC28304-2 Switching Waveforms ($I_{OUT} = 3A$).

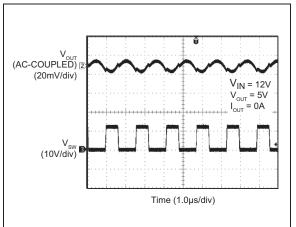


FIGURE 4-17: MIC28304-2 Switching Waveforms (I_{OUT} = 0A).

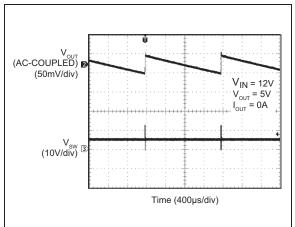


FIGURE 4-18: MIC28304-1 Switching Waveforms ($I_{OUT} = 0A$).

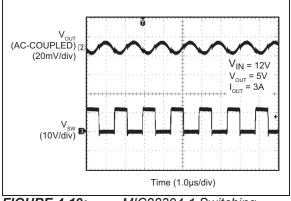
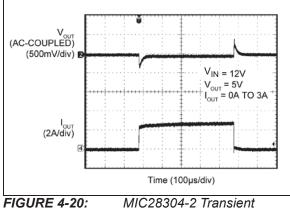
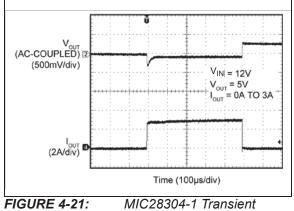


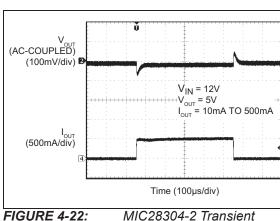
FIGURE 4-19: MIC28304-1 Switching Waveforms $(I_{OUT} = 3A)$.



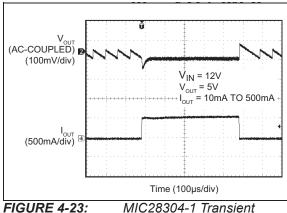
Response.



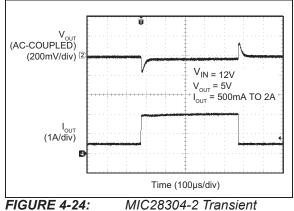
Response.



Response.



Response.



Response.

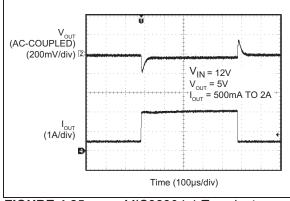


FIGURE 4-25: MIC28304-1 Transient Response.

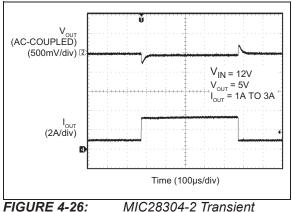


FIGURE 4-26: Response.

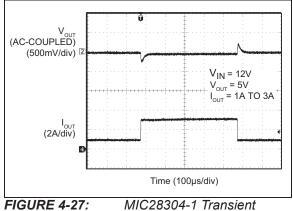
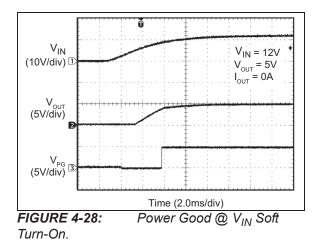
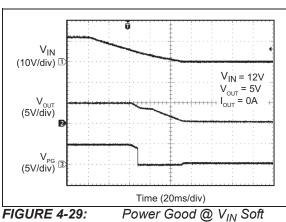


FIGURE 4-27: Response.





Turn-Off.

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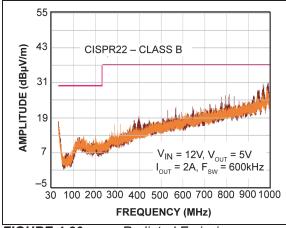


FIGURE 4-30: Radiated Emission – 30 MHz to 1000 MHz (V_{IN} = 12V/I_{OUT} = 2A).

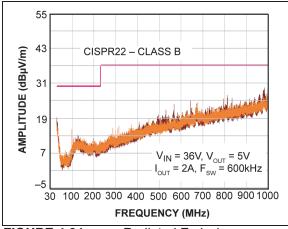
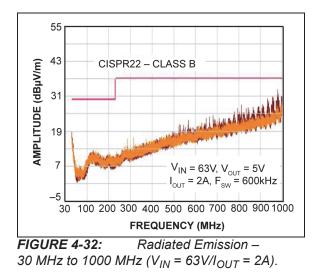


FIGURE 4-31: Radiated Emission – 30 MHz to 1000 MHz (V_{IN} = 36V/I_{OUT} = 2A).



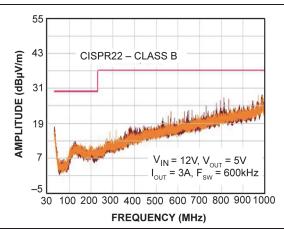


FIGURE 4-33: Radiated Emission – 30 MHz to 1000 MHz (V_{IN} = 12V/I_{OUT} = 3A).

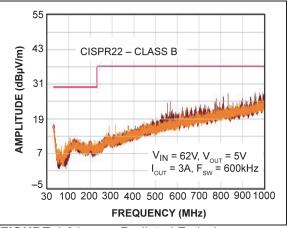


FIGURE 4-34: Radiated Emission – 30 MHz to 1000 MHz (V_{IN} = 62V/I_{OUT} = 3A).

5.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 5-1.

TABLE 5-1: PIN FUNCTION TABLE

1, 2, 3, 54, 64 GND Analog Ground: Ground for internal controller and feedback resistor network. The Analog Ground return path should be separate from the Power Ground (PGND) network path. 4 ILIM Current-Limit Setting: Connect a resistor from SW (Pin# 4) to ILIM to set the overcurrent threshold for the converter. 5, 60 VIN Supply Voltage for Controller: The V _N operating voltage range is from 4.5V to 70V. A 0.47 µF ceramic capacitor from V _{IN} (Pin# 60) to AGND is required for decoupling. Pin# 5 should be externally connected to either PV _{IN} or Pin# 60 on the PCB. 6, 40-48, 51 SW Switch Node and Current Sense Input: High-current output driver return. The SW pin should be routed away from sensitive nodes. The SW pin also senses the current by monitoring the voltage across the low-side MOSFET during off-time. 7, 8 FREQ Switching Frequency Adjust Input: Leaving this pin open will set the switching frequency. 1600 kHz. Alternatively, a resistor from this pin to ground can be used to lower the switching frequency. 9-13 PGND Power Ground: PGND is the return path for the buck converter power stage. The PGND pin connects to the sources of the low-side N-channel external MOSFET, the negative terminals of the input capacitors. The return path for the Power Ground should be a small as possible and separate from the Analog Ground (GND) return path. 14-22 PV _{IN} Power Input Voltage: Connection to the internal high-side power MOSFET. 23-38 V _{OUT} Output Voltage: Connection to the internal bootstrap capacitor should be conn	Pin Number	Pin Name	Pin Function
Image: the converter. 5.60 V _{IN} Supply Voltage for Controller: The V _{IN} operating voltage range is from 4.5V to 70V. A 0.47 μF ceramic capacitor from V _{IN} (Pin# 60) to AGND is required for decoupling. Pin# 5 should be externally connected to either PV _{IN} or Pin# 60 on the PCB. 6, 40-48, 51 SW Switch Node and Current Sense Input: High-current output driver return. The SW pin should be routed away from sensitive nodes. The SW pin also senses the current by monitoring the voltage across the low-side MOSFET during off-time. 7, 8 FREQ Switching Frequency Adjust Input: Leaving this pin open will set the switching frequency to 600 kHz. Alternatively, a resistor from this pin to ground can be used to lower the switching frequency. 9-13 PGND Power Ground: PGND is the return path for the buck converter power stage. The PGND pin connects to the sources of the low-side N-channel external MOSFET, the negative terminals of the input capacitors. The return path for the Power Ground should be as small as possible and separate from the Analog Ground (GND) return path. 14-22 PV _{IN} Power Input Voltage: Connection to the drain of the internal high-side power MOSFET. 23-38 V _{OUT} Output Voltage: Connection to the internal inductor. The output capacitor should be connected from this pin the QDD as close to the module as possible. 39 NC No Connection: Leave it floating. 49, 50 ANODE Anode Bootstrap Diode Input. Anode connection of internal bootstrap diode.	1, 2, 3, 54, 64	GND	•
Capacitor from V _{IN} (Pin# 60) to AGND is required for decoupling. Pin# 5 should be externally connected to either PV _{IN} or Pin# 60 on the PCB. 6, 40-48, 51 SW Switch Node and Current Sense Input: High-current output driver return. The SW pin should be routed away from sensitive nodes. The SW pin also senses the current by monitoring the voltage across the low-side MOSFET during off-time. 7, 8 FREQ Switching Frequency Adjust Input: Leaving this pin open will set the switching frequency to 600 kHz. Alternatively, a resistor from this pin to ground can be used to lower the switching frequency. 9-13 PGND Power Ground: PGND is the return path for the buck converter power stage. The PGND pin connects to the sources of the low-side N-channel external MOSFET, the negative terminals of the input capacitors and the negative terminals of the input capacitors. The Power Ground should be as small as possible and separate from the Analog Ground (GND) return path. 14-22 PV _{IN} Power Input Voltage: Connection to the drain of the internal high-side power MOSFET. 23-38 V _{OUT} Output Voltage: Connection to the internal inductor. The output capacitor should be connected from this pin to PGND as close to the module as possible. 39 NC No Connection: Leave it floating. 49, 50 ANODE Anode Bootstrap Diode Input: Anode connection of internal bootstrap diode. This pin should be connected to the PV _{DD} pin. 52, 53 BSTR Bootstrap Capacitor: Connection to the interna	4	I _{LIM}	
b b b b b b b b compatibility	5, 60	V _{IN}	capacitor from V _{IN} (Pin# 60) to AGND is required for decoupling. Pin# 5 should be externally
Alternatively, a resistor from this pin to ground can be used to lower the switching frequency. 9-13 PGND Power Ground: PGND is the return path for the buck converter power stage. The PGND pin connects to the sources of the low-side N-channel external MOSFET, the negative terminals of the input capacitors and the negative terminals of the output capacitors. The return path for the Power Ground should be as small as possible and separate from the Analog Ground (GND) return path. 14-22 PV _{IN} Power Input Voltage: Connection to the drain of the internal high-side power MOSFET. 23-38 V _{OUT} Output Voltage: Connection with the internal inductor. The output capacitor should be connected from this pin to PGND as close to the module as possible. 39 NC No Connection: Leave it floating. 49, 50 ANODE Anode Bootstrap Diode Input: Anode connection of internal bootstrap diode. This pin should be connected to the PV _{DD} pin. 52, 53 BSTC Bootstrap Capacitor: Connection to the internal bootstrap resistor and high-side power MOSFET drive circuitry. Leave floating, no connect. 57 FB Feedback Input: Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to set the desired output voltage. 58 PGOOD Power Good Output: Open-drain output; an external pull-up resistor to the external power rails is required. 59 Enable Input: A logic signal to enable or d	6, 40-48, 51	SW	to the Switch node. Due to the high-speed switching on this pin, the SW pin should be routed away from sensitive nodes. The SW pin also senses the current by monitoring the voltage across the
to the sources of the low-side N-channel external MOSFET, the negative terminals of the input capacitors and the negative terminals of the output capacitors. The return path for the Power Ground should be as small as possible and separate from the Analog Ground (GND) return path.14-22PV _{IN} Power Input Voltage: Connection to the drain of the internal high-side power MOSFET.23-38V _{OUT} Output Voltage: Connection with the internal inductor. The output capacitor should be connected from this pin to PGND as close to the module as possible.39NCNo Connection: Leave it floating.49, 50ANODEAnode Bootstrap Diode Input: Anode connection of internal bootstrap diode. This pin should be connected to the PV _{DD} pin.52, 53BSTCBootstrap Capacitor: Connection to the internal bootstrap capacitor. Leave floating, no connect.55, 56BSTRBootstrap Resistor: Connection to the internal bootstrap resistor and high-side power MOSFET drive circuitry. Leave floating, no connect.57FBFeedback Input: Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to set the desired output voltage.58PGOODPower Good Output: Open-drain output; an external pull-up resistor to the external power rails is required.59ENEnable Input: A logic signal to enable or disable the buck converter operation. The EN pin is CMOS compatible. Logic high enables the device, logic low shuts down the regulator. In the Disable mode, the input supply current for the device is minimized to 4 µA typically. Do not pull EN to PV _{DD} .61, 62PV _{DD} Internal +5V Linear Regulator Output: PV _{DD} is the internal sup	7, 8	FREQ	
23-38 V Output Voltage: Connection with the internal inductor. The output capacitor should be connected from this pin to PGND as close to the module as possible. 39 NC No Connection: Leave it floating. 49, 50 ANODE Anode Bootstrap Diode Input: Anode connection of internal bootstrap diode. This pin should be connected to the PV _{DD} pin. 52, 53 BSTC Bootstrap Capacitor: Connection to the internal bootstrap capacitor. Leave floating, no connect. 55, 56 BSTR Bootstrap Resistor: Connection to the internal bootstrap resistor and high-side power MOSFET drive circuitry. Leave floating, no connect. 57 FB Feedback Input: Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to set the desired output voltage. 58 PGOOD Power Good Output: Open-drain output; an external pull-up resistor to the external power rails is required. 59 EN Enable Input: A logic signal to enable or disable the buck converter operation. The EN pin is CMOS compatible. Logic high enables the device, logic low shuts down the regulator. In the Disable mode, the input supply current for the device is minimized to 4 μA typically. Do not pull EN to PV _{DD} . 61, 62 PV _{DD} Internal +5V Linear Regulator Output: PV _{DD} is the internal supply bus for the device. In the applications with V _{IN} < +5.5V, PV _{DD} should be tied to V _{IN} to bypass the linear regulator.	9-13	PGND	to the sources of the low-side N-channel external MOSFET, the negative terminals of the input capaci- tors and the negative terminals of the output capacitors. The return path for the Power Ground should
1 this pin to PGND as close to the module as possible. 39 NC No Connection: Leave it floating. 49, 50 ANODE Anode Bootstrap Diode Input: Anode connection of internal bootstrap diode. This pin should be connected to the PV _{DD} pin. 52, 53 BSTC Bootstrap Capacitor: Connection to the internal bootstrap capacitor. Leave floating, no connect. 55, 56 BSTR Bootstrap Resistor: Connection to the internal bootstrap resistor and high-side power MOSFET drive circuitry. Leave floating, no connect. 57 FB Feedback Input: Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to set the desired output voltage. 58 PGOOD Power Good Output: Open-drain output; an external pull-up resistor to the external power rails is required. 59 EN Enable Input: A logic signal to enable or disable the buck converter operation. The EN pin is CMOS compatible. Logic high enables the device, logic low shuts down the regulator. In the Disable mode, the input supply current for the device is minimized to 4 µA typically. Do not pull EN to PV _{DD} . 61, 62 PV _{DD} Internal +5V Linear Regulator Output: PV _{DD} is the internal supply bus for the device. In the applications with V _{IN} < +5.5V, PV _{DD} should be tied to V _{IN} to bypass the linear regulator.	14-22	PVIN	Power Input Voltage: Connection to the drain of the internal high-side power MOSFET.
49, 50 ANODE Anode Bootstrap Diode Input: Anode connection of internal bootstrap diode. This pin should be connected to the PV _{DD} pin. 52, 53 BSTC Bootstrap Capacitor: Connection to the internal bootstrap capacitor. Leave floating, no connect. 55, 56 BSTR Bootstrap Resistor: Connection to the internal bootstrap resistor and high-side power MOSFET drive circuitry. Leave floating, no connect. 57 FB Feedback Input: Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to set the desired output voltage. 58 PGOOD Power Good Output: Open-drain output; an external pull-up resistor to the external power rails is required. 59 EN Enable Input: A logic signal to enable or disable the buck converter operation. The EN pin is CMOS compatible. Logic high enables the device, logic low shuts down the regulator. In the Disable mode, the input supply current for the device is minimized to 4 µA typically. Do not pull EN to PV _{DD} . 61, 62 PV _{DD} Internal +5V Linear Regulator Output: PV _{DD} is the internal supply bus for the device. In the applications with V _{IN} < +5.5V, PV _{DD} should be tied to V _{IN} to bypass the linear regulator.	23-38	V _{OUT}	
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63 NC No Connection: Leave it floating.	61, 62	PV _{DD}	
	63	NC	No Connection: Leave it floating.

6.0 FUNCTIONAL DESCRIPTION

The MIC28304 is an adaptive on-time synchronous buck regulator module built for high input voltage to low output voltage conversion applications. The MIC28304 is designed to operate over a wide input voltage range, from 4.5V to 70V, and the output is adjustable with an external resistor divider. An adaptive on-time control scheme is employed to obtain a constant switching frequency and to simplify the control compensation. Hiccup mode overcurrent protection is implemented by the sensing low-side MOSFET's $R_{DS(ON)}$. The device features internal soft start, enable, UVLO and thermal shutdown. The module has integrated switching FETs, inductor, bootstrap diode, resistor and capacitor.

6.1 Theory of Operation

Per the **"Functional Block Diagram"** of the MIC28304 module, the output voltage is sensed by the MIC28304 Feedback pin, FB, via the voltage dividers, R1 and R11. Then it is compared to a 0.8V reference voltage, V_{REF} , at the error comparator through a low-gain transconductance (g_m) amplifier. If the feedback voltage decreases and the amplifier output is below 0.8V, then the error comparator will trigger the control logic and generate an on-time period. The on-time period length is predetermined by the "Fixed t_{ON} Estimator" circuitry:

EQUATION 6-1: FIXED toN ESTIMATOR

 $t_{ON(ESTIMATED)} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$

Where:

MOSFET.

 V_{OUT} = Output voltage V_{IN} = Power stage input voltage f_{SW} = Switching frequency

At the end of the on-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. In most cases, the off-time period length depends upon the feedback voltage. When the feedback voltage decreases and the output of the g_m amplifier is below 0.8V, the on-time period is triggered and the off-time period ends. If the off-time period determined by the feedback voltage is less than the minimum off-time $t_{OFF(MIN)}$, which is about 200 ns, the MIC28304 control logic will apply the $t_{OFF(MIN)}$ instead. $t_{OFF(MIN)}$ is required to maintain enough energy

in the Boost Capacitor (CBST) to drive the high-side

The maximum duty cycle is obtained from the 200 ns $t_{\mbox{OFF}(\mbox{MIN})}$:

EQUATION 6-2: OBTAINING THE MAXIMUM DUTY CYCLE

$D_{MAX} = \frac{t_S}{2}$	$\frac{200 \text{ ns}}{\text{t}_{\text{S}}}$
Where:	
$t_{\rm S}$ = 1/f _{SW}	

It is not recommended to use the MIC28304 with an off-time close to $t_{\mbox{OFF}(\mbox{MIN})}$ during steady-state operation.

The adaptive on-time control scheme results in a constant switching frequency in the MIC28304. The actual on-time and resulting switching frequency will vary with the different rising and falling times of the external MOSFETs. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications. During load transients, the switching frequency is changed due to the varying off-time.

To illustrate the control loop operation, we will analyze both the steady-state and load transient scenarios. For easy analysis, the gain of the g_m amplifier is assumed to be 1. With this assumption, the inverting input of the error comparator is the same as the feedback voltage.

Figure 6-1 shows the MIC28304 control loop timing during steady-state operation. During steady-state operation, the g_m amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple plus injected voltage ripple, to trigger the on-time period. The on-time is predetermined by the t_{ON} estimator. The termination of the off-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{FB} falls below V_{REF} , the off period ends and the next on-time period is triggered through the control logic circuitry.

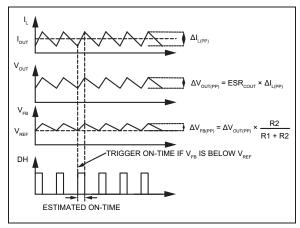


FIGURE 6-1: MIC28304 Control Loop Timing.

Figure 6-2 shows the operation of the MIC28304 during a load transient. The output voltage drops due to the sudden load increase, which causes the V_{FB} to be less than V_{REF}. This will cause the error comparator to trigger an on-time period. At the end of the on-time period, a minimum off-time (t_{OFF(MIN)}) is generated to charge the Bootstrap Capacitor (C_{BST}), since the feedback voltage is still below V_{REF}. Then, the next on-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small.

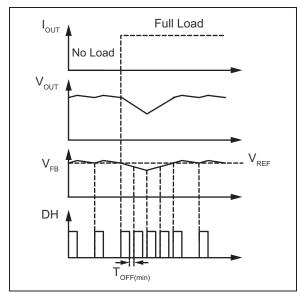


FIGURE 6-2: MIC28304 Load Transient Response.

Unlike true Current mode control, the MIC28304 uses the output voltage ripple to trigger an on-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough.

In order to meet the stability requirements, the MIC28304 feedback voltage ripple should be in phase with the inductor current ripple, and is large enough to be sensed by the g_m amplifier and the error comparator. The recommended feedback voltage ripple is 20 mV~100 mV over full input voltage range. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the gm amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation. Please refer to the subsection, Section 7.6 "Ripple Injection", in Section 7.0 "Application Information" for more details about the ripple injection technique.

6.2 Discontinuous Mode (MIC28304-1 Only)

In Continuous mode, the inductor current is always greater than zero; however, at light loads, the MIC28304-1 is able to force the inductor current to operate in Discontinuous mode. Discontinuous mode is where the inductor current falls to zero, as indicated by the trace (I_L) shown in Figure 6-3. During this period, the efficiency is optimized by shutting down all the non-essential circuits and minimizing the supply current. The MIC28304-1 wakes up and turns on the high-side MOSFET when the Feedback Voltage, V_{FB} , drops below 0.8V.

The MIC28304-1 has a Zero-Crossing (ZC) comparator that monitors the inductor current by sensing the voltage drop across the low-side MOSFET during its on-time. If the V_{FB} > 0.8V, and the inductor current goes slightly negative, then the MIC28304-1 automatically powers down most of the IC circuitry and goes into a Low-Power mode.

Once the MIC28304-1 goes into Discontinuous mode, both DL and DH are low, which turns off the high-side and low-side MOSFETs. The load current is supplied by the output capacitors and V_{OUT} drops. If the drop of V_{OUT} causes V_{FB} to go below V_{REF}, then all the circuits will wake-up into normal Continuous mode. First, the bias currents of most circuits reduced during the Discontinuous mode are restored and then a t_{ON} pulse is triggered before the drivers are turned on to avoid any possible glitches. Finally, the high-side driver is turned on. Figure 6-3 shows the control loop timing in Discontinuous mode.

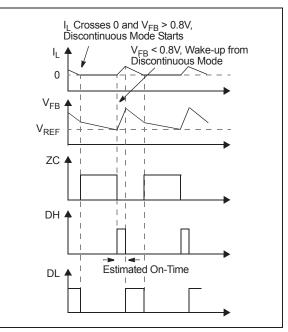


FIGURE 6-3: MIC28304-1 Control Loop Timing (Discontinuous Mode).

During Discontinuous mode, the bias current of most circuits is substantially reduced. As a result, the total power supply current during Discontinuous mode is only about 400 μ A, allowing the MIC28304-1 to achieve high efficiency in light load applications.

6.3 Soft Start

Soft start reduces the input power supply surge current at start-up by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

The MIC28304 implements an internal digital soft start by making the 0.8V Reference Voltage, V_{REF}, ramp from 0 to 100% in about 5 ms with 9.7 mV steps. Therefore, the output voltage is controlled to increase slowly by a staircase V_{FB} ramp. Once the soft start cycle ends, the related circuitry is disabled to reduce current consumption. PV_{DD} must be powered up at the same time or after V_{IN} to make the soft start function correctly.

6.4 Current Limit

The MIC28304 uses the ${\sf R}_{DS(ON)}$ of the low-side MOSFET, and an external resistor connected from the ${\sf I}_{LIM}$ pin to the SW node, to decide the current limit.

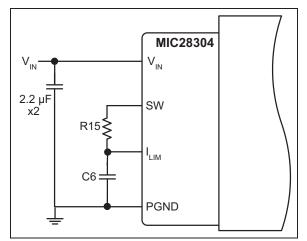


FIGURE 6-4: Circuit.

MIC28304 Current-Limiting

In each switching cycle of the MIC28304, the inductor current is sensed by monitoring the low-side MOSFET in the off period. The Sensed Voltage, V(I_{LIM}), is compared with the Power Ground (PGND) after a blanking time of 150 ns. In this way, the drop voltage over the resistor, R15 (V_{RLIM}), is compared with the drop over the bottom FET generating the short current limit. The small capacitor (C6) connected from the I_{LIM} pin to PGND filters the switching node ringing during the off-time, allowing a better short limit measurement. The time constant created by R15 and C6 should be much less than the minimum off-time.

The V_{RLIM} drop allows programming of the short limit through the value of the resistor (R15) if the absolute value of the voltage drop on the bottom FET is greater than V_{RLIM}. In that case, the V(I_{LIM}) is lower than PGND and a short-circuit event is triggered. A hiccup cycle to treat the short event is generated. The hiccup sequence, including the soft start, reduces the stress on the switching FETs, and protects the load and supply for severe short conditions.

The short-circuit current limit can be programmed by using Equation 3.

EQUATION 6-3: PROGRAMMING THE SHORT-CIRCUIT CURRENT LIMIT

$$R15 = \frac{(I_{CLIM} + \Delta I_{L(PP)} \times 0.5) \times R_{DS(ON)} + V_{CL_OFFSET}}{I_{CL}}$$

Where:

 I_{CLIM} = Desired current limit

 $R_{DS(ON)}$ = On resistance of low-side power MOSFET, 45 m Ω typically

 V_{CL_OFFSET} = Current-limit threshold (typical value is -14 mV per Section 1.0 "Electrical Characteristics"

 I_{CL} = Current-limit source current (typical value is 80 μ A per Section 1.0 "Electrical Characteristics"

 $\Delta I_{L(PP)}$ = Inductor current peak-to-peak; since the inductor is integrated, use Equation 6-4 to calculate the inductor ripple current

The peak-to-peak inductor current ripple is:

EQUATION 6-4: CALCULATING THE INDUCTOR RIPPLE CURRENT

 $\Delta I_{L(PP)} = \; \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times L} \; \label{eq:dispersive}$

The MIC28304 has 4.7 μH inductor integrated into the module.

In case of a hard short, the short limit is folded down to allow an indefinite hard short on the output without any destructive effect. It is mandatory to make sure that the inductor current used to charge the output capacitance during soft start is under the folded short limit; otherwise, the supply will go in Hiccup mode and may not be finishing the soft start successfully. Table 6-1 shows the typical output current-limit value for a given R15 with C6 = 10 pF.

TABLE 6-1:	TYPICAL OUTPUT
	CURRENT-LIMIT VALUE

R15	Typical Output Current Limit
1.81 kΩ	3A
2.7 kΩ	6.3A

7.0 APPLICATION INFORMATION

7.1 Simplified Input Transient Circuitry

The 76V absolute maximum rating of MIC28304 allows simplifying the transient voltage suppressor on the input supply side, which is very common in industrial applications. The Input Supply Voltage (V_{IN}), shown in Figure 7-1, may be operating at 12V input rail most of the time, but can encounter a noise spike of 60V for a short duration. By using MIC28304, which has 76V absolute maximum voltage rating, the input transient suppressor is not needed, which saves on component count, form factor, and ultimately, the system becomes less expensive.

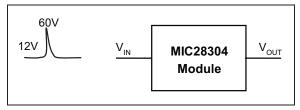


FIGURE 7-1: Simplified Input Transient Circuitry.

7.2 Setting the Switching Frequency

The MIC28304 switching frequency can be adjusted by changing the value of resistor, R19. The top resistor of 100 k Ω is internal to the module and is connected between the V_{IN} and FREQ pins, so the value of R19 sets the switching frequency. The switching frequency also depends upon V_{IN}, V_{OUT} and load conditions.

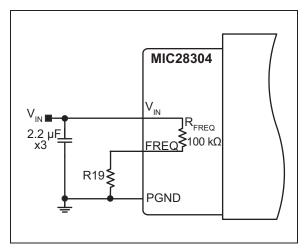


FIGURE 7-2: Adjustment.



Figure 7-1 gives the estimated switching frequency:

EQUATION 7-1: ESTIMATED SWITCHING FREQUENCY

$$f_{SW_ADJ} = f_O \times \frac{R19}{R19 + 100 \text{ k}\Omega}$$

Where:

 f_O = Switching frequency when R19 is open

For more precise setting, it is recommended to use Figure 7-3:

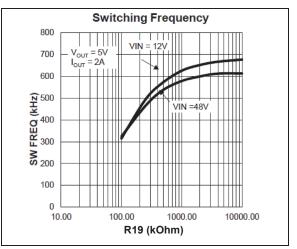


FIGURE 7-3: Switching Frequency vs. R19.

7.3 Output Capacitor Selection

The type of the output capacitor is usually determined by the application and its Equivalent Series Resistance (ESR). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are MLCC, tantalum, low-ESR aluminum electrolytic, OS-CON and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. The MIC28304 requires ripple injection and the output capacitor ESR effects the control loop from a stability point of view.

The maximum value of ESR is calculated as in Equation 7-2:

EQUATION 7-2: CALCULATING THE MAXIMUM VALUE OF ESR

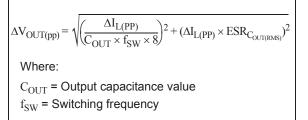
$$\text{ESR}_{\text{COUT}} \leq \frac{\Delta V_{\text{OUT(pp)}}}{\Delta I_{\text{L(PP)}}}$$

Where:

 $\Delta V_{OUT(pp)}$ = Peak-to-peak output voltage ripple $\Delta I_{L(PP)}$ = Peak-to-peak inductor current ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated in Equation 7-3:

CALCULATING THE **EQUATION 7-3:** TOTAL RIPPLE



As described in the subsection, Section 6.1 "Theory of Operation", in Section 6.0 "Functional Description", the MIC28304 requires at least 20 mV peak-to-peak ripple at the FB pin to make the ${\rm g}_{\rm m}$ amplifier and the error comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitor's value should be much smaller than the ripple caused by the output capacitor, ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide enough feedback voltage ripple. Please refer to Section 7.6 "Ripple Injection" for more details.

The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for aluminum electrolytic or OS-CON.

The output capacitor RMS current is calculated in Equation 7-4:

EQUATION 7-4: CALCULATING OUTPUT CAPACITOR RMS CURRENT

 $I_{C_{OUT(RMS)}} = \frac{\Delta I_{L(PP)}}{\sqrt{12}}$

The power dissipated in the output capacitor is:

EQUATION 7-5: DISSIPATED POWER IN OUTPUT CAPACITOR

 $P_{\text{DISS}(\text{Cout})} = I_{\text{Cout}(\text{RMS})}^2 \times \text{ESR}_{\text{Cout}}$

7.4 Input Capacitor Selection

The input capacitor for the Power Stage Input, PVIN, should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON and multilayer polymer film capacitors can handle the higher inrush currents without voltage derating. The input voltage ripple will primarily depend on the input capacitor's ESR.

The input capacitor must be rated for the input current ripple. The RMS value of the input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

CALCULATING INPUT EQUATION 7-6: CAPACITOR RATING

 $I_{C_{IN(RMS)}} \approx I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$

Where:

/

D = Duty cycle

The power dissipated in the input capacitor is:

EQUATION 7-7: POWER DISSIPATED IN THE INPUT CAPACITOR

 $P_{DISS(C_{IN})} = I_{CIN(RMS)}^2 \times ESR_{C_{IN}}$

The general rule is to pick the capacitor with a ripple current rating equal to or greater than the calculated worst-case (V_{IN_MAX}) RMS capacitor current. Its voltage rating should be 20% to 50% higher than the maximum input voltage. Typically, the input ripple (ΔV_{IN}) needs to be kept down to less than ±10% of the input voltage. The ESR also increases the input ripple.

Equation 7-8 should be used to calculate the input capacitor. Also, it is recommended to keep some margin on the calculated value:

EQUATION 7-8: CALCULATING THE **INPUT CAPACITOR**

$$\begin{split} C_{IN} &\approx \ \frac{I_{OUT(MAX)} \times (1-D)}{f_{SW} \times \Delta V_{IN}} \end{split}$$

 Where:

$$\Delta V_{IN} \ \text{= Input ripple} \\ f_{SW} \ \text{= Switching frequency} \end{split}$$

7.5 Output Voltage Setting Components

The MIC28304 requires two resistors to set the output voltage, as shown in Figure 7-4:

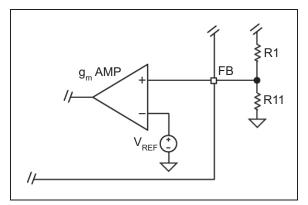


FIGURE 7-4: Voltage-Divider Configuration.

The output voltage is determined by Equation 7-9:



 $V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R11}\right)$ Where: V_{FB} = 0.8V

A typical value of R1 used on the standard evaluation board is 10 k Ω . If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small in value, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R11 can be calculated using Equation 7-10:

EQUATION 7-10: CALCULATING R11

$$R11 = \frac{V_{FB} \times R1}{V_{OUT} - V_{FB}}$$

7.6 Ripple Injection

The V_{FB} ripple required for proper operation of the MIC28304 g_m amplifier and error comparator is 20 mV to 100 mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For a low output voltage, such as 1V, the output voltage ripple is only 10 mV to 20 mV, and the feedback voltage ripple is less than 20 mV. If the feedback voltage ripple is so small that the g_m amplifier and error comparator cannot sense it, then the MIC28304 will lose control and the output voltage is not regulated. In order to have some amount of V_{FB} ripple, a ripple injection method is applied for low output voltage ripple injection component values for the ceramic output capacitor.

The applications are divided into three situations according to the amount of the feedback voltage ripple:

 Enough ripple at the feedback voltage due to the large ESR of the output capacitors (Figure 7-5):

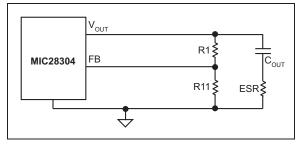


FIGURE 7-5: Enough Ripple at FB.

As shown in Figure 7-5, the converter is stable without any ripple injection.

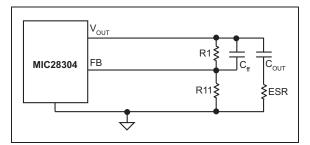


FIGURE 7-6: Inadequate Ripple at FB.

The feedback voltage ripple is:

EQUATION 7-11: FEEDBACK VOLTAGE RIPPLE

$$\Delta V_{FB(PP)} = \frac{R11}{R1 + R11} \times ESR_{COUT} \times \Delta I_{L(PP)}$$

Where:

 ${\rm \Delta I}_{L(PP)}$ = Peak-to-peak value of the inductor current ripple

 Inadequate ripple at the feedback voltage due to the small ESR of the output capacitors; such is the case with the ceramic output capacitor. The output voltage ripple is fed into the FB pin through a feed-forward Capacitor, C_{ff}, in this situation, as shown in Figure 7-7. The typical C_{ff} value is between 1 nF and 100 nF.

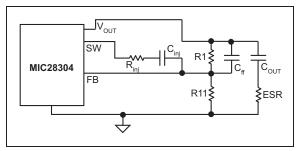


FIGURE 7-7: Invisible Ripple at FB.

With the feed-forward Capacitor, the feedback voltage ripple is very close to the output voltage ripple:

EQUATION 7-12: FEEDBACK VOLTAGE RIPPLE

 $\Delta V_{FB(PP)} \approx ESR \times \Delta I_{L(PP)}$

 Virtually no ripple at the FB pin voltage due to the very low-ESR of the output capacitors.
 In this situation, the output voltage ripple is less than 20 mV. Therefore, additional ripple is injected into the FB pin from the Switching node, SW, via a resistor, R_{inj}, and a capacitor, C_{inj}, as shown in Figure 7-7. The injected ripple is:

EQUATION 7-13: INJECTED RIPPLE

$$\Delta V_{FB(pp)} = V_{IN} \times K_{div} \times D \times (1 - D) \times \frac{1}{f_{SW} \times \tau}$$
$$K_{div} = \frac{R1/R11}{R_{inj} + R1/R11}$$

Where:

 V_{IN} = Power stage input voltage D = Duty cycle f_{SW} = Switching frequency τ = (R1//R11//R_{inj}) × C_{ff} In Equation 7-13, it is assumed that the time constant associated with $C_{\rm ff}$ must be much greater than the switching period:

EQUATION 7-14:	TIME CONSTANT
	ASSOCIATED WITH C _{ff}

$\frac{1}{f_{SW} \times \tau} = \frac{1}{\tau} \ll 1$	
---	--

If the voltage divider resistors, R1 and R11, are in the $k\Omega$ range, then a C_{ff} of 1 nF to 100 nF can easily satisfy the large time constant requirements. Also, a 100 nF injection Capacitor, C_{inj} , is used in order to be considered as short for a wide range of the frequencies.

The process of sizing the ripple injection resistor and capacitors is:

Step 1. Select C_{ff} to feed all output ripples into the Feedback pin and make sure the large time constant assumption is satisfied. The typical choice of C_{ff} is 1 nF to 100 nF if R1 and R11 are in the k Ω range.

Step 2. Select R_{inj} according to the expected feedback voltage ripple using Equation 7-16:

EQUATION 7-15: OBTAINING Kdiv

$$K_{div} = \frac{\Delta V_{FB(pp)}}{V_{IN}} \times \frac{f_{SW} \times \tau}{D \times (1 - D)}$$

Then the value of R_{inj} is obtained as:

EQUATION 7-16: OBTAINING Rini VALUE

$$R_{inj} = (R1//R11) \times \left(\frac{1}{K_{div}} - 1\right)$$

Step 3. Select C_{inj} as 100 nF, which could be considered as short for a wide range of the frequencies.

Table 7-1 summarizes the typical value of components for particular input and output voltages, and 600 kHz switching frequency design.

V _{OUT}	V _{IN}	R3 (R _{inj})	R1 (Top Feedback Resistor)	R11 (Bottom Feedback Resistor)	R19	C10 (C _{inj})	C12 (C _{ff)}	C _{OUT}
0.9V	5V to 70V	16.5 kΩ	10 kΩ	80.6 kΩ	DNP	0.1 µF	2.2 nF	47 μF/6.3V or 2 x 22 μF
1.2V	5V to 70V	16.5 kΩ	10 kΩ	20 kΩ	DNP	0.1 µF	2.2 nF	47 μF/6.3V or 2 x 22 μF
1.8V	5V to 70V	16.5 kΩ	10 kΩ	8.06 kΩ	DNP	0.1 µF	2.2 nF	47 μF/6.3V or 2 x 22 μF
2.5V	5V to 70V	16.5 kΩ	10 kΩ	4.75 kΩ	DNP	0.1 µF	2.2 nF	47 μF/6.3V or 2 x 22 μF
3.3V	5V to 70V	16.5 kΩ	10 kΩ	3.24 kΩ	DNP	0.1 µF	2.2 nF	47 μF/6.3V or 2 x 22 μF
5V	7V to 70V	16.5 kΩ	10 kΩ	1.9 kΩ	DNP	0.1 µF	2.2 nF	47 μF/6.3V or 2 x 22 μF
12V	18V to 70V	23.2 kΩ	10 kΩ	715Ω	DNP	0.1 µF	2.2 nF	47 μF/16V or 2 x 22 μF

TABLE 7-1: RECOMMENDED COMPONENT VALUES FOR 600 kHz SWITCHING FREQUENCY

7.7 Thermal Measurements and Safe Operating Area

Measuring the IC's case temperature is recommended to ensure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermocouple that comes with a thermal meter. This thermocouple wire gauge is large, typically 22 gauge, and behaves like a heatsink, resulting in a lower case measurement.

Two methods of temperature measurement are using a smaller thermocouple wire or an infrared thermometer. If a thermocouple wire is used, it must be constructed of 36-gauge wire or higher (smaller wire size) to minimize the wire heatsinking effect. In addition, the thermocouple tip must be covered in either thermal grease or thermal glue to make sure that the thermocouple junction is making good contact with the case of the IC. The Omega[®] brand thermocouple (5SC-TT-K-36-36) is adequate for most applications.

Wherever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor IC. However, an IR thermometer from Optris has a 1 mm spot size, which makes it a good choice for measuring the hottest point on the case. An optional stand makes it easy to hold the beam on the IC for long periods of time.

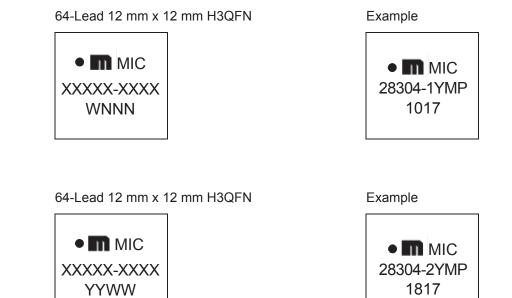
The Safe Operating Area (SOA) of the MIC28304 is shown in **Section 2.0 "Typical Performance Curves** (275 kHz Switching Frequency)". These thermal measurements were taken on the MIC28304 evaluation board. Since the MIC28304 is an entire system, comprised of a switching regulator controller, MOSFETs and inductor, the part needs to be considered as a system. The SOA curves will give guidance to reasonable use of the MIC28304.

7.8 Emission Characteristics of MIC28304

The MIC28304 integrates switching components in a single package, so the MIC28304 has reduced emission compared to a standard buck regulator with external MOSFETS and inductors. The radiated EMI scans for MIC28304 are shown in **Section 3.0 "Typical Performance Curves"**. The limit on the graph is per the EN55022 Class B standard.

8.0 PACKAGING INFORMATION

8.1 Package Marking Information



 Legend: XXX Product code or customer-specific information Y Year code (last digit of calendar year) YY Year code (last 2 digits of calendar year) WW Week code (week of January 1 is week '01') NNN Alphanumeric traceability code 				
be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	Legen	Y YY WW NNN @3 *	Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC [®] designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.	
	Note:	be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.		

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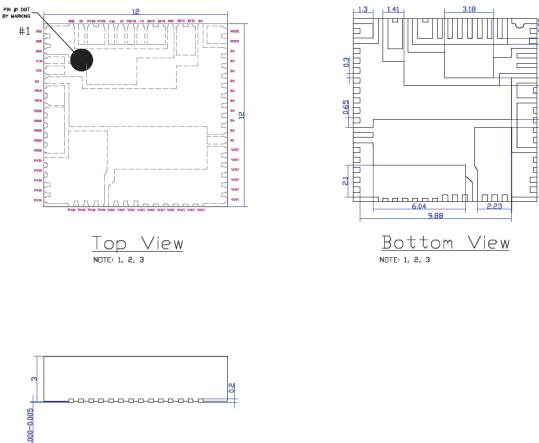
8.2 Package Details

The following sections give the technical details of the packages.

TITLE

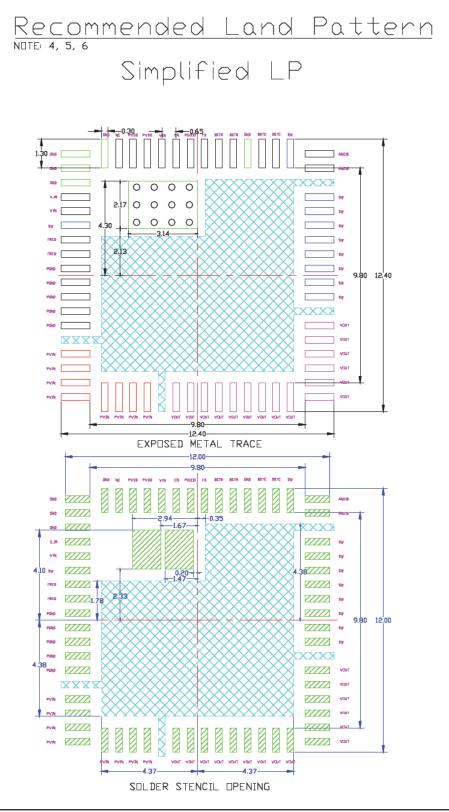
64 LEAD H3QFN 12x12mm PACKAGE (Module) OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	H3QFN1212-64LD-PL-1	UNIT	MM
Lead Frame	Copper	Lead Finish	Matte Tin



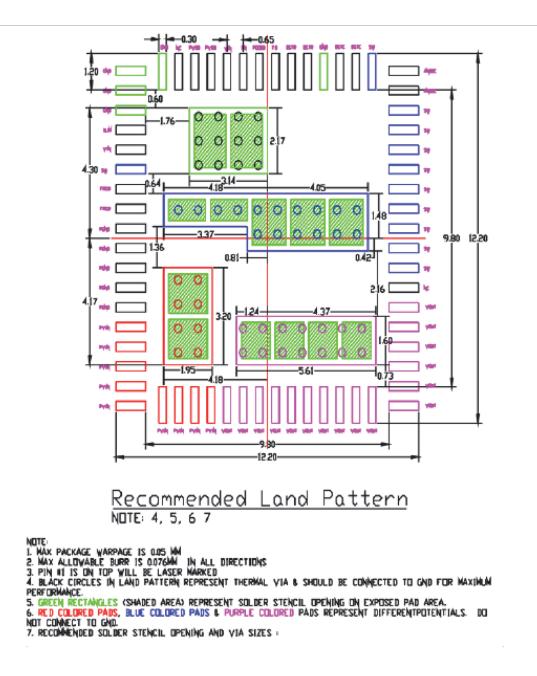


Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

Recommended Land Pattern



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging. NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2018)

- Converted Micrel document MIC28304 to Microchip data sheet DS20006093A.
- Minor text changes throughout document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

		Examples:			
	<u>PART NO.</u> – <u>X</u> XXX – XX Device Option Package Media	a) MIC28304-1YMP-T1: MIC28304, HLL, 64-Pin H3QFN, 100/Reel			
	Туре	b) MIC28304-1YMP-TR: MIC28304, HLL, 64-Pin H3QFN, 5,000/Reel			
Device:	MIC28304: 70V, 3A Power Module Hyper Speed Control [®] Family	c) MIC28304-2YMP-T1: MIC28304, HSC, 64-Pin H3QFN, 100/Reel			
Option:	1 = HLL 2 = HSC	d) MIC28304-2YMP-TR: MIC28304, HSC, 64-Pin H3QFN, 5,000/Reel			
Package:	YMP = 64-Pin 12 mm x 12 mm H3QFN				
Media Type:	T1 = 100/pcs. TR = 500/pcs.				

NOTES:

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