MIC5165

Dual Regulator Controller for DDR3 GDDR3/4/5 Memory Termination

General Description

The MIC5165 is a dual regulator controller designed specifically for low-voltage memory termination applications such as DDR3 and GDDR3/4/5. The MIC5165 offers a simple, low-cost JEDEC-compliant solution for terminating high-speed, low-voltage digital buses with a Power Good (PG) signal.

The MIC5165 controls two external N-Channel MOSFETs to form two separate regulators. It operates by switching between either the high-side MOSFET or the low-side MOSFET, depending on whether the current is being sourced to the load or being sunk by the regulator.

Designed to provide a universal solution for memory termination regardless of input voltage, output voltage, or load current, the desired MIC5165 output voltage can be programmed by forcing the reference voltage externally to the desired voltage.

The MIC5165 operates from an input voltage as low as 0.75V up to 6V, with a second bias supply input required for operation. The MIC5165 is available in a tiny MSOP-10 package with an operating junction temperature range of –40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

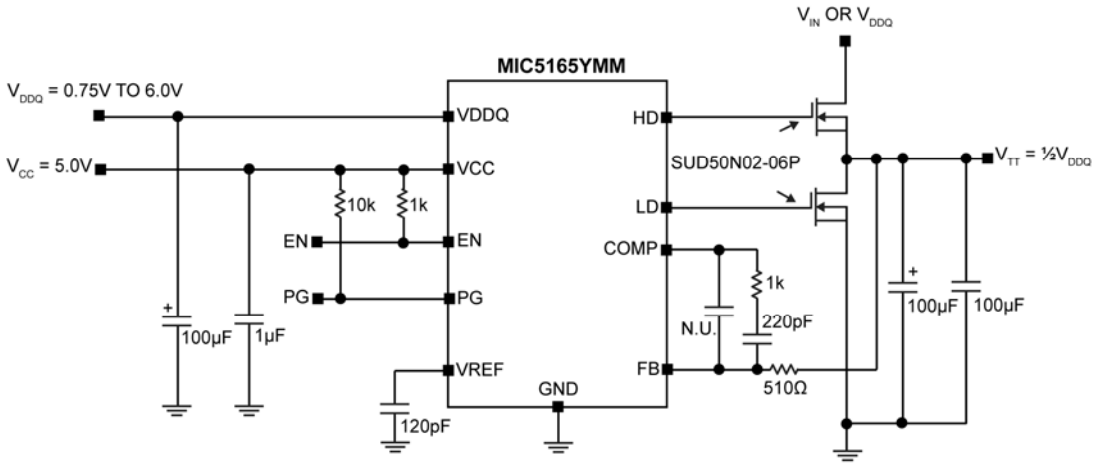
Features

- Input voltage range: 0.75V to 6V
- Up to 7A V_{TT} Current
- Tracking programmable output
- Power Good signal
- Wide bandwidth
- Logic-controlled enable input
- Requires minimal external components
- DDR3, GDDR3/4/5 memory termination
- -40°C < T_J < +125°C
- Tiny MSOP-10 package

Applications

- Desktop Computers
- Servers
- Notebook computers
- Workstations
- DDR3 andGDDR3/4/5 Memory Termination

Typical Application



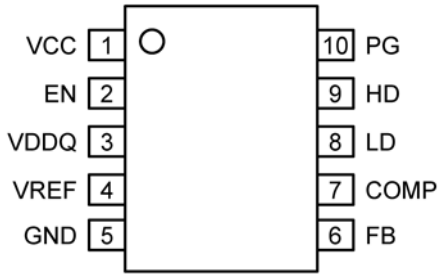
MIC5165 as a DDR3 Memory Termination Device for 3.5A Application

Ordering Information

Part Number	Temperature Range	Package	Lead Finish
MIC5165YMM	–40° to +125°C	10-Pin MSOP	Pb-Free

Note:
MSOP is a Green RoHS compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.

Pin Configuration



10-Pin MSOP (MM)

Pin Description

Pin Number	Pin Name	Pin Function
1	VCC	Bias Supply (Input): Apply 3V-6V to this input for internal bias to the controller.
2	EN	Enable (Input): CMOS compatible input. Logic high = enable, logic low = shutdown. The EN pin can be tied directly to VDDQ or VCC for functionality. Do not float the EN pin. Floating this pin causes the enable to be in an undetermined state.
3	VDDQ	Input Supply Voltage.
4	VREF	Reference voltage equal to half of VDDQ. **For internal use only.**
5	GND	Ground.
6	FB	Feedback (Input): Input to the internal error amplifier.
7	COMP	Compensation (Output): Connect a capacitor and resistor from COMP pin to FB pin for compensation of the internal control loop.
8	LD	Low-Side Drive (Output): Connects to the Gate of the external low-side MOSFET.
9	HD	High-Side Drive (Output): Connects to the Gate of the external high-side MOSFET.
10	PG	Power Good (Output): Open drain output.

Absolute Maximum Ratings[1]

VCC to GND ..... –0.3V to +7V
VDDQ to GND ..... –0.3V to +7V
EN to GND ..... –0.3V to V_{CC}
FB to GND ..... –0.3V to V_{CC}
VREF to GND ..... –0.3V to V_{DDQ}
COMP to GND ..... –0.3V to V_{CC}
HD, LD to GND ..... –0.3V to V_{CC}
PG to GND ..... –0.3V to V_{CC}
Lead Temperature (Soldering 10sec.) ..... 260°C
Storage Temperature (T_S) ..... –65°C to +150°C
ESD Rating[3]
(HBM) ..... +2kV
(MM) ..... +300V

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... 3V to 6V
Supply Voltage (V_{DDQ}) ..... 0.75V to 6V
Enable Input Voltage (V_{EN}) ..... 0V to V_{IN}
Junction Temperature Range (T_J) ..... –40°C < T_J < +125°C
Junction Thermal Resistance
MSOP-10 (θ_{JA}) ..... 130.5°C/W
MSOP-10 (θ_{JC}) ..... 42.6°C/W

Electrical Characteristics[4]

T_A = 25°C with VDDQ = 1.5V; VCC = EN = 5V, **bold** values indicate –40°C ≤ T_J ≤ +125°C, unless otherwise specified. See test circuit 1 for test circuit configuration.

Parameter	Condition	Min	Typ	Max	Units
VREF Voltage Accuracy		-1%	0.5V_{DDQ}	+1%	V
V_{TT} Voltage Accuracy (**Note 5**)	Sourcing; 100mA to 3A	-5 **-10**	0.4	+5 **+10**	mV
	Sinking; -100mA to -3A	-5 **-10**	0.4	+5 **+10**	
Supply Current (I_{DDQ})	EN = 1.2V (controller ON) No Load		25	140 **200**	µA
Supply Current (I_{CC})	No Load		15	22 **27**	mA
I_{CC} Shutdown Current (**Note 6**)	EN = 0.2V (controller OFF); No PG pull-up		0.1	5	µA
Start-Up Time (**Note 7**)	VCC = 5V external bias; EN = V_{IN}		8	15 **30**	µs
Enable Input					
Enable Input Threshold	Regulator Enabled	**1.2**			V
	Regulator Shutdown			**0.3**	
Enable Hysteresis			50		mV
EN Pin Input Current	V_{IL} < 0.2V (controller shutdown)		0.01		µA
	V_{IH} > 1.2V (controller enable)		5.75		

Electrical Characteristics[4] (Continued)

T_A = 25°C with VDDQ = 1.5V; VCC = EN = 5V, **bold** values indicate –40°C ≤ T_J ≤ +125°C, unless otherwise specified. See test circuit 1 for test circuit configuration.

Power Good Output					
Power Good Window	Threshold, ±% of V_{TT} from Nominal	**±5**	±10	**±15**	%
	Hysteresis		2		%
Power Good Output Low Voltage	I_{PG} = 2mA (sinking)		100	300	mV
Power Good Leakage Current	PG = EN = 5V, FB = VREF; Switch Leakage Current to Ground		0.01	1.0	µA
Power Good Startup Delay Time (**Note 8**)		1	2.4		ms
Power Good Deglitch (**Note 9**)	Time after FB voltage has gone outside of PG window		5	10	µs
Driver					
High Side Gate Drive Voltage	High-Side MOSFET Fully ON	**4.8**	4.97		V
	High-Side MOSFET Fully OFF		0.03	**0.2**	
Low Side Gate Drive Voltage	Low-Side MOSFET Fully ON	**4.8**	4.97		
	Low-Side MOSFET Fully OFF		0.03	**0.2**	

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model 1.5kΩ in series with 100pF.
4. Specification for packaged product only.
5. The V_{TT} voltage accuracy is measured as a delta voltage from the reference output (V_{TT} - V_{REF}).
6. Shutdown current is measured only on the VCC pin. The VDDQ pin will always draw a minimum amount of current when voltage is applied.
7. Start-up time is defined as the amount of time from EN = V_{CC} to V_{HD} = 90% of V_{CC}.
8. Power Good startup delay is defined as the amount of time from EN=VCC and V_{FB} is within ±10% of ½V_{DDQ} to V_{PG} = 90% of V_{CC} (V_{FB} = V_{REF}), during startup (V_{FB} is the sense of V_{TT}).
9. Power Good deglitch is defined as the amount of time from the voltage at FB node going out of PG window (with 10mV overdrive voltage) to PG = LOW.

Test Circuit

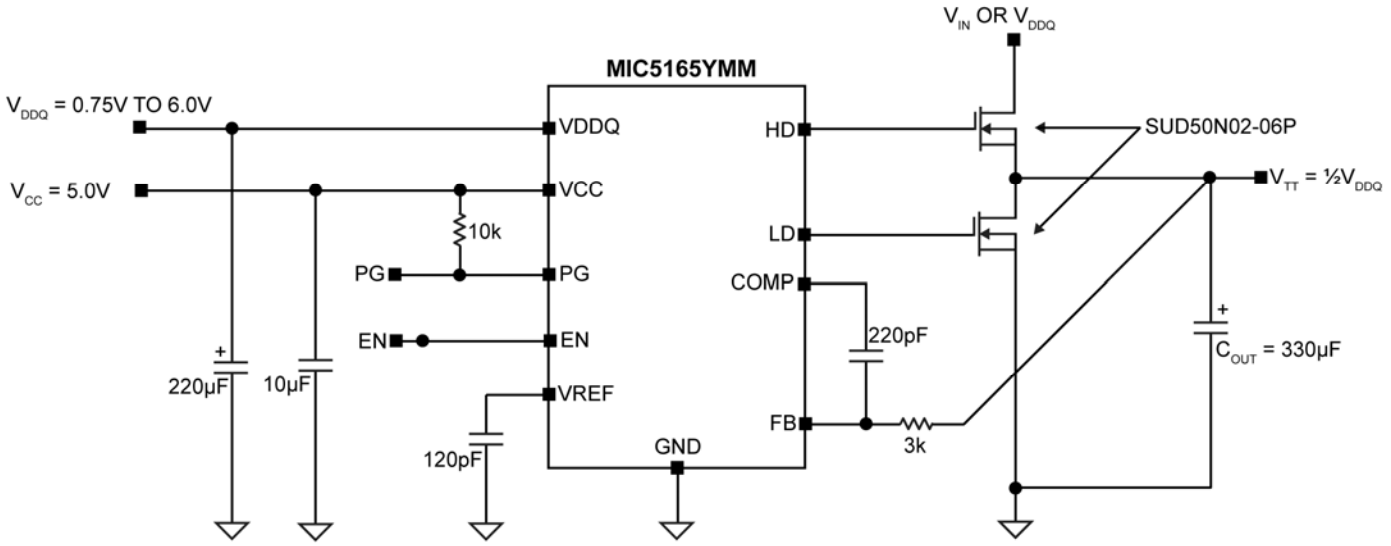
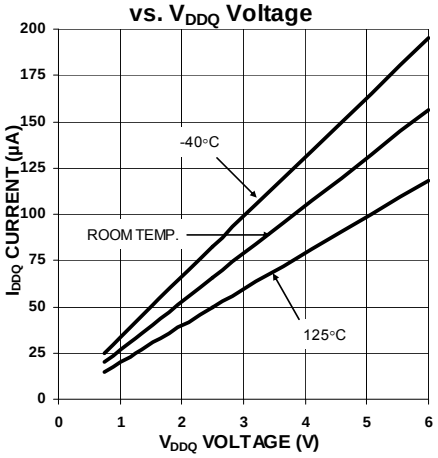


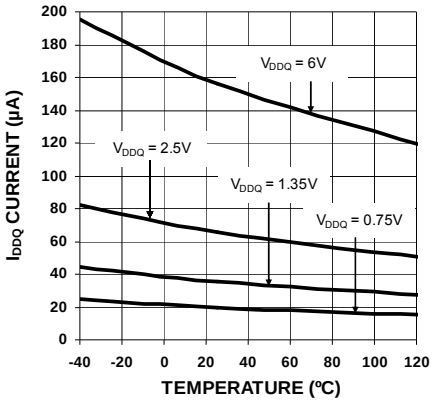
Figure 1. Test Circuit

Typical Characteristics

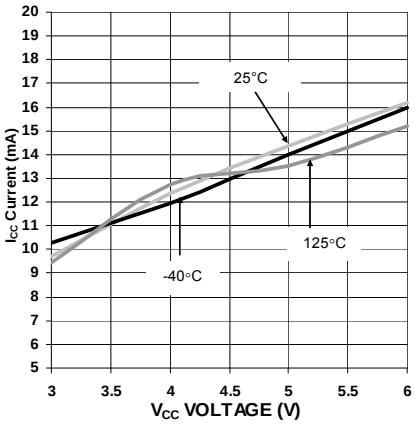
I_{DDQ} Current vs. V_{DDQ} Voltage



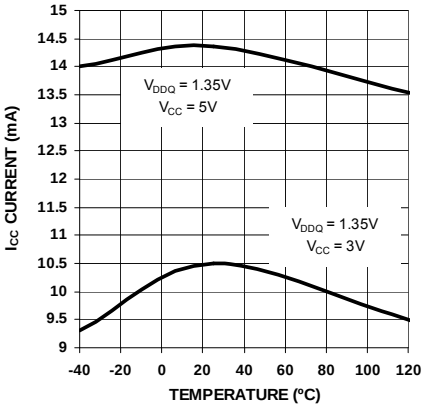
I_{DDQ} Current vs. Temperature



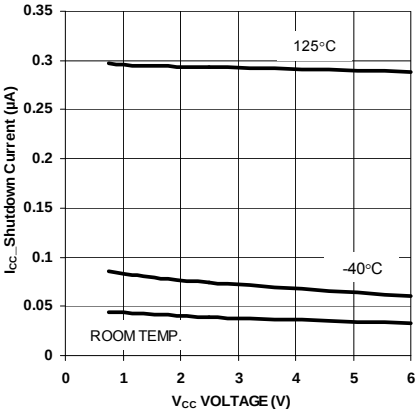
I_{CC} Current vs. Input Voltage



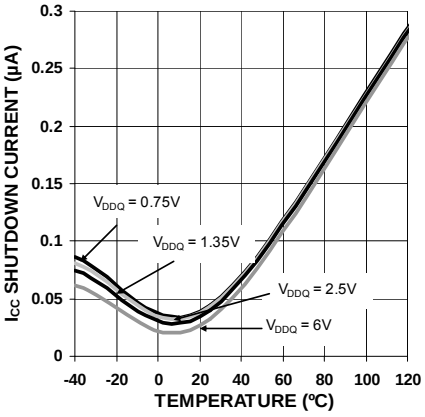
I_{CC} Current vs. Temperature



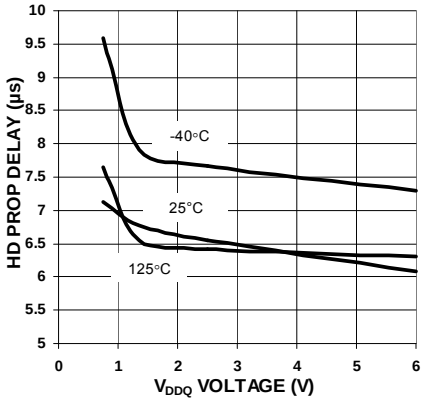
I_{CC} Shutdown Current vs. V_{CC} Voltage



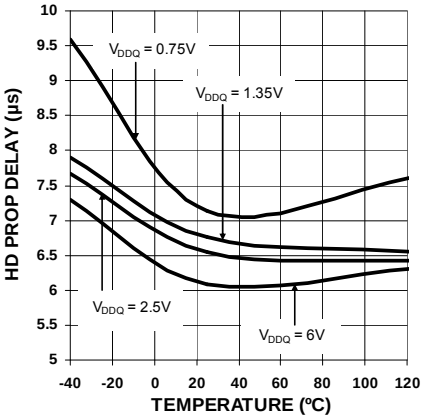
I_{CC} Shutdown Current vs. Temperature



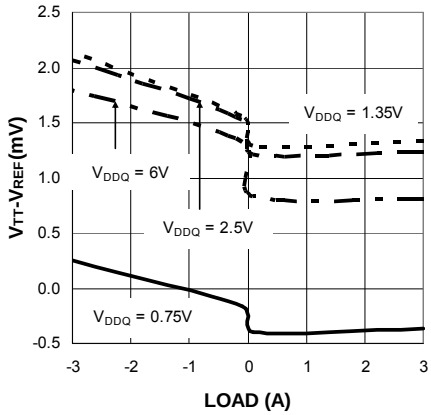
HD Prop Delay vs. V_{DDQ} Voltage



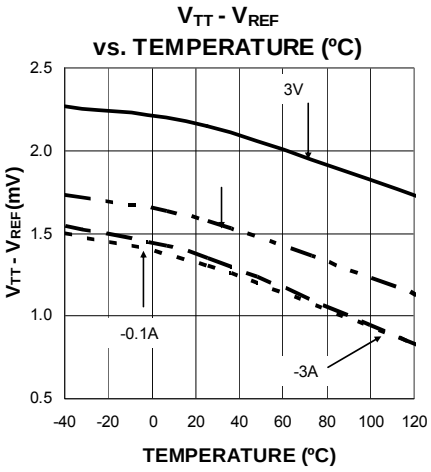
HD Prop Delay vs. Temperature



V_{TT} - V_{REF} vs. LOAD (A)

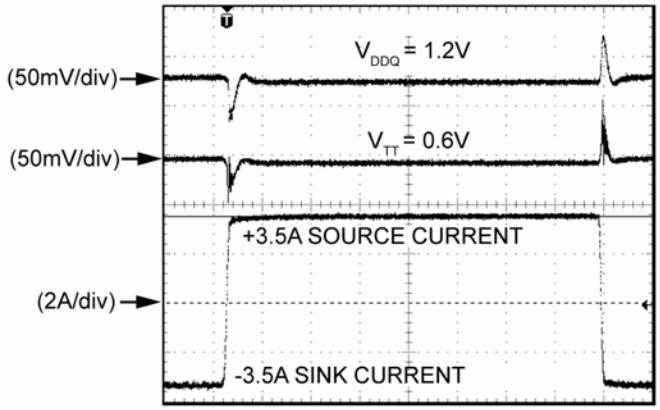


Typical Characteristics (Continued)

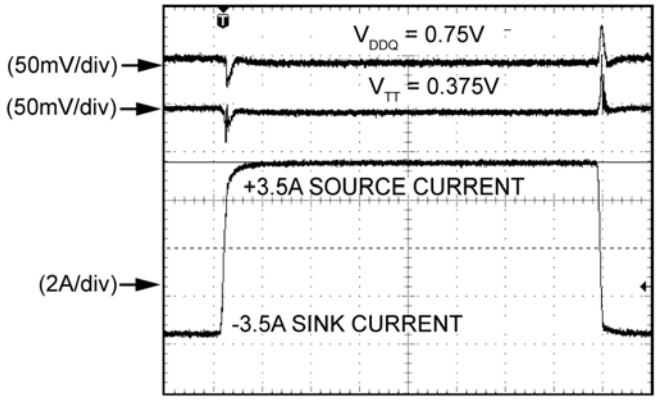


Functional Characteristics

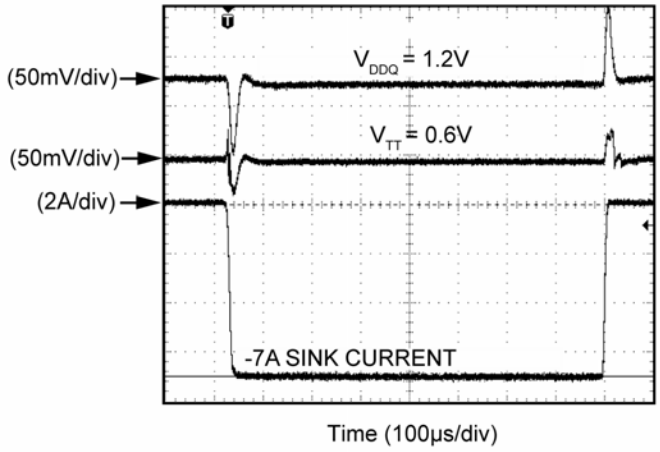
Load Transient (±3.5A)
V_{TT} = 0.6V



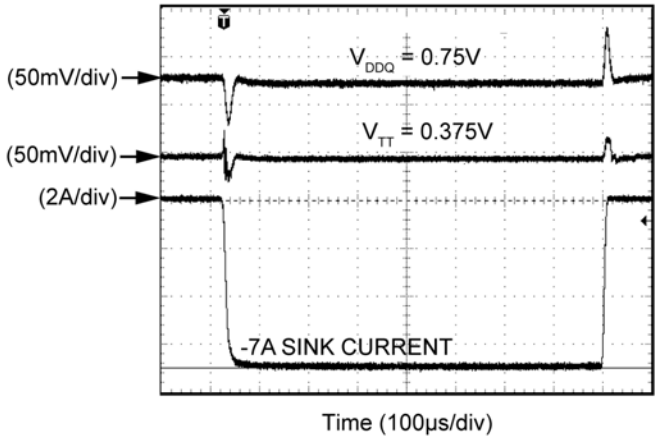
Load Transient (±3.5A)
V_{TT} = 0.375V



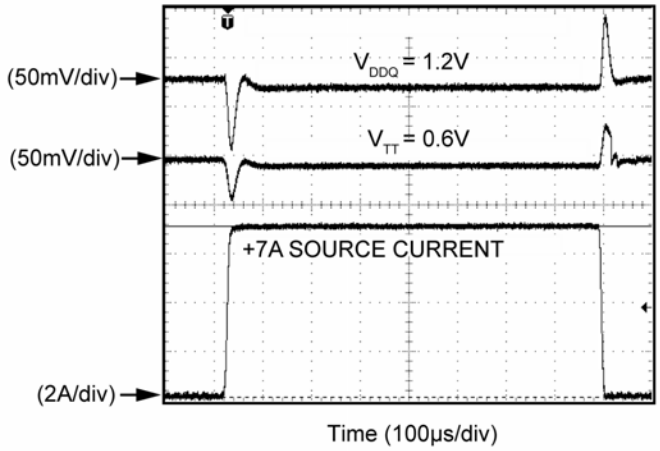
Load Transient (-7A)
V_{TT} = 0.6V



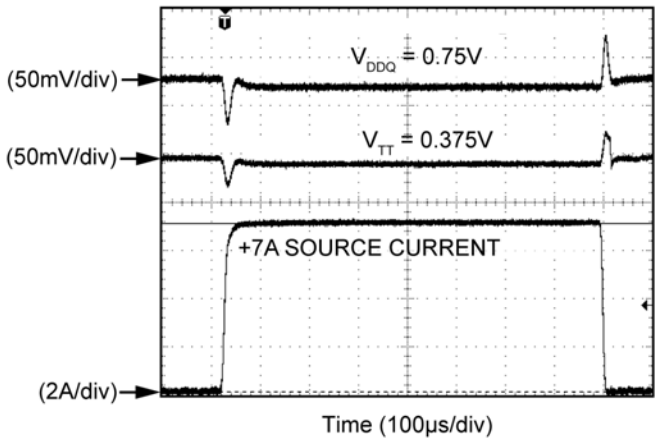
Load Transient (-7A)
V_{TT} = 0.375V



Load Transient (+7A)
V_{TT} = 0.6V



Load Transient (+7A)
V_{TT} = 0.375V



Functional Diagram

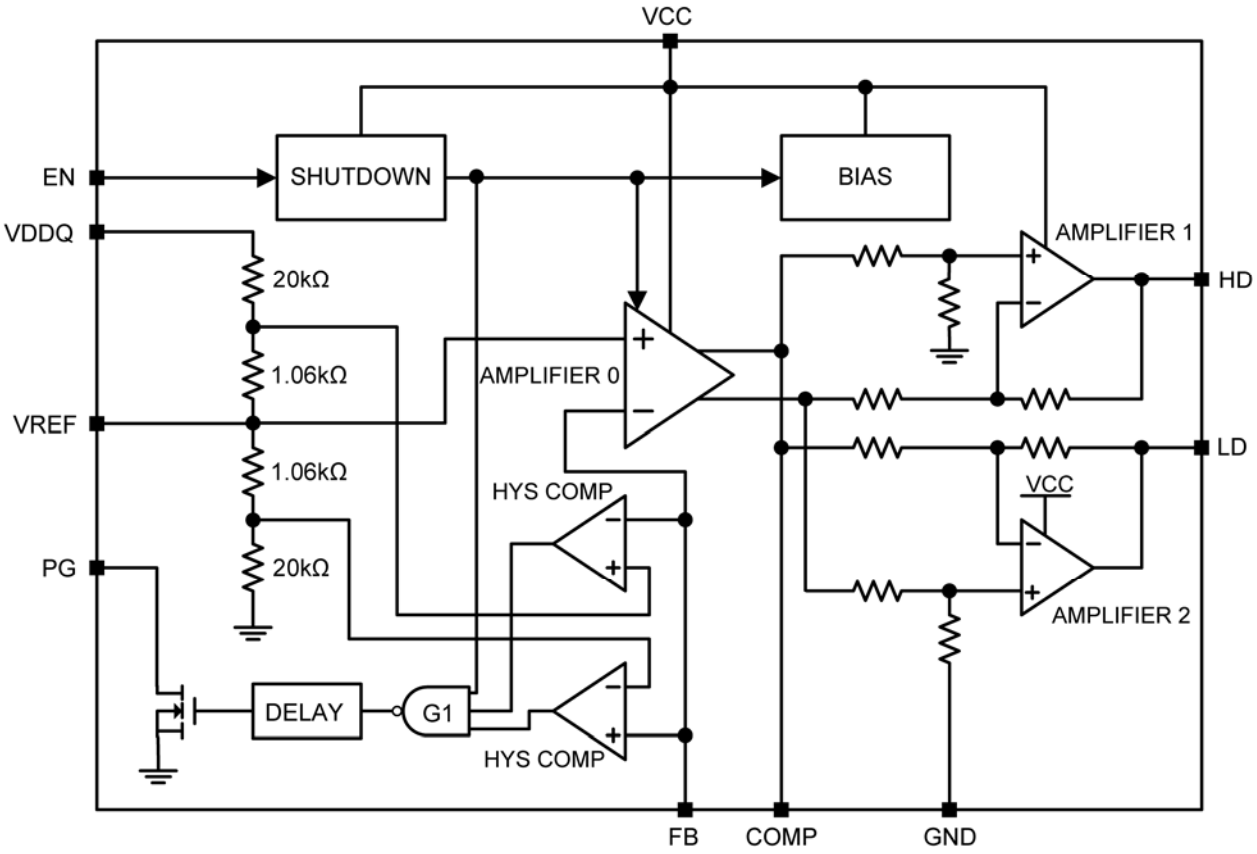


Figure 2. MIC5165 Block Diagram

Functional Description

The MIC5165 is a high-performance linear controller, utilizing scalable N-Channel MOSFETs to provide JEDEC-compliant bus termination. Termination is achieved by dividing down the V_{DDQ} voltage half, providing the reference (V_{REF}) voltage. The MIC5165 controls two external N-Channel MOSFETs to form two separate regulators. It operates by switching between either the high-side MOSFET or the low-side MOSFET, depending on whether the current is being sourced to the load or being sunk by the regulator.

VDDQ

The VDDQ pin on the MIC5165 provides the source current through the high-side N-Channel and the reference voltage to the device. The MIC5165 can operate at V_{DDQ} input voltages as low as 0.75V. A bypass capacitance will increase performance by improving the source impedance at higher frequencies.

VREF

Two resistors divide down the V_{DDQ} voltage to provide V_{REF}. The resistors are valued at around 21kΩ. A minimum capacitor value of 120pF from V_{REF} to ground is mandatory.

VCC

V_{CC} supplies the internal circuitry of the MIC5165 and provides the voltage to drive the external N-Channel MOSFETs. A small 1µF ceramic capacitor is recommended for bypassing the VCC pin.

FB and COMP

The feedback (FB) pin provides the path for the error amplifier to regulate V_{TT}. A feedback resistor is recommended and resistor values should not exceed 10kΩ. The compensation capacitors should not be less than 40pF.

EN

The MIC5165 features an active-high enable (EN) input. In the off-mode state, leakage currents are reduced to microamperes. EN has thresholds compatible with TTL/CMOS for simple logic interfacing.

PG

MIC5165 features a Power Good (PG) output. PG is an open drain output with an active high signal. PG requires a pull-up resistor to VCC.

Application Information

Synchronous Dynamic Random Access Memory (SDRAM) has continually evolved over the years to keep up with ever-increasing computing needs. The latest addition to SDRAM technology is DDR3 SDRAM. DDR3 SDRAM is the third generation of the DDR SDRAM family and offers improved power savings, higher data bandwidth and enhanced signal quality with multiple On-Die Termination (ODT) selection. In DDR3 SDRAM the values of the ODT are based on the value of an external resistor. In addition to using this external resistor for setting the ODT value, it is also used for calibrating the ODT value so that it maintains its resistance value to within a 10% tolerance.

To improve signal integrity and support higher frequency operation of memory read/write, the JEDEC committee defined a fly-by termination scheme used with the clocks, the command bus and address bus signals. The fly-by topology reduces Simultaneous Switching Noise (SSN) by deliberately causing flight-time skew between the data and strobes at every DRAM as the clock, address and command signals traverse the DIMM.

The DDR3 SDRAM uses a programmable impedance output buffer. Currently, there are two drive strength settings, 34Ω and 40Ω. The 40Ω drive strength setting is currently a reserved specification defined by JEDEC, but available on the DDR3 SDRAM.

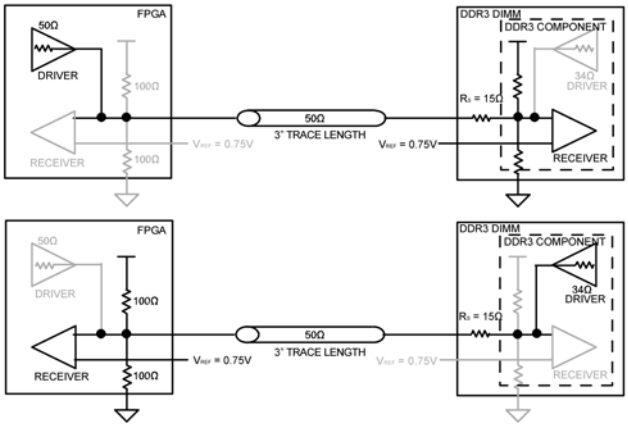


Figure 3. Dynamic OCT between Stratix III/IV FPGA Devices

The MIC5165 provides two drive signals, the high-side MOSFET acts as a pass element to provide output voltage and low side MOSFET acts as pull-down to regulate the output termination voltage (V_{TT}). An internal error amplifier compares the termination voltage (V_{TT}) and V_{REF}, controlling two external N-Channel MOSFETs to sink or source current to maintain a termination voltage (V_{TT}) equal to V_{REF}. These MOSFETs receive their enhancement voltage from a separate VCC pin on the device. Although the general discussion is focused on DDR3, the MIC5165 is also capable of providing bus terminations for DDR, DDR2 and GDDR3/4/5.

VDDQ

The MIC5165 can operate at V_{DDQ} voltages as low as 0.75V. Due to the possibility of large transient currents being sourced from this line, significant bypass capacitance will increase performance by improving the source impedance at higher frequencies. Since the reference is simply $V_{DDQ}/2$, perturbations on V_{DDQ} will also appear at half the amplitude on the reference. For this reason, low-ESR capacitors such as ceramics or OS-CON are recommended on V_{DDQ}.

V_{TT}

The proper combination and placement of the OS-CON and ceramic capacitors is important to reduce both ESR and ESL such that high-current high-speed transients do not exceed the dynamic voltage tolerance requirement of V_{TT}. The OS-CON capacitors provide bulk charge storage while the smaller ceramic capacitors provide current during the fast edges of the bus transition. Using several smaller ceramic capacitors distributed near the termination resistors is typically important to reduce the effects of PCB trace inductance.

VREF

A minimum capacitor value of 120pF from VREF to ground is required to remove high-frequency signals reflected from the source (Refer to Figure 4). Large capacitance values (>1500pF) should be avoided. Values greater than 1500pF slow down V_{REF} and detract from the reference voltage's ability to track V_{DDQ} during high speed load transients.

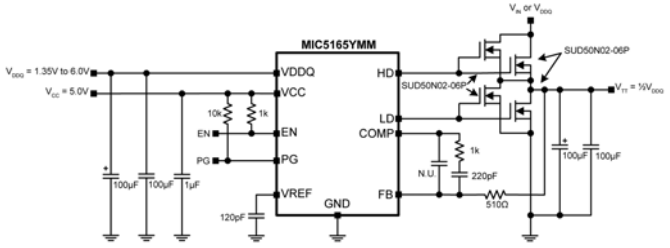


Figure 4. MIC5165 as a DDR3 Memory Termination Device for 7A Application

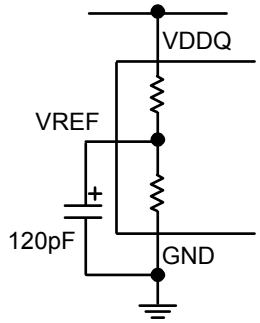


Figure 5. V_{DDQ} Divided Down to Provide V_{REF}

VREF can also be manipulated for different applications. A separate voltage source can be used to externally set the reference point, bypassing the divider network. Also, external resistors can be added from V_{REF}-to-V_{DDQ} or V_{REF}-to-ground to shift the reference point up or down.

VCC

The VCC voltage range is from 3V to 6V, but the minimum voltage on the VCC pin should consider the Gate-to-Source voltage of the MOSFET and V_{TT} voltage.

For example, on a DDR3 compliant terminator, V_{DDQ} equals 1.5V and V_{TT} equals 0.75V. If the N-Channel MOSFET selected requires a gate-source voltage of 2.5V, V_{CC} should be a minimum of 3.25V.

$$V_{CCmin}=V_{TT}+V_{GS}$$

Feedback and Compensation

The feedback provides the path for the error amplifier to regulate V_{TT}. An external resistor must be placed between the feedback and V_{TT}. This allows the error amplifier to be correctly externally compensated. For most applications, a 510Ω resistor is recommended.

The COMP pin on the MIC5165 is the output of the internal error amplifier. By placing a capacitor and resistor between the COMP pin and the FB pin, this coupled with the feedback resistor, places an external pole and zero on the error amplifier. With a 510Ω feedback resistor, a minimum 220pF capacitor is recommended for a 3.5A peak termination circuit. An increase in the load will require additional N-Channel MOSFETs and/or increase in output capacitance may require feedback and/or compensation capacitor values to be changed to maintain stability.

Enable

EN can be tied directly to V_{DDQ} or V_{CC} for functionality. Do not float the EN pin. Floating this pin causes the enable circuitry to be in an indeterminate state.

Power Good

Power Good signal output remains high as long as output is within ±10% range of regulated V_{TT} and goes low if output moves beyond this range.

Input Capacitance

The MIC5165 application operates in the linear region during the steady state condition, so there are no switching current pulses from the input capacitor. The application does not require a bulk input capacitor, but using one greatly improves device performance during fast load transients. Since output voltage V_{TT} follows the input voltage V_{DDQ} attention should be given to possible voltage dips on VDDQ pin. Capacitors with low ESR such as OS-CON and ceramics are recommended for bypassing the input. Although a 100µF ceramic capacitor will suffice for most applications, input capacitance may need to be increased in cases where the termination circuit is greater than 1-inch away from the bulk capacitance.

Output Capacitance

Large, low ESR capacitors are recommended for the output (V_{TT}) of the MIC5165. Although low ESR capacitors are not required for stability, they are recommended to reduce the effects of high-speed current transients on V_{TT}. The change in voltage during the transient condition will be the effect of the peak current multiplied by the output capacitor's ESR. For that reason, OS-CON type capacitors and ceramic are excellent choices for this application. OS-CON capacitors have extremely low ESR and a large capacitance-to-size ratio. Ceramic capacitors are also well suited to termination due to their low ESR. These capacitors should have a dielectric rating of X5R or X7R. Y5V and Z5U type capacitors are not recommended, due to their poor performance at high frequencies and over temperature. The minimum recommended capacitance for a 3.5A peak circuit is 100µF. Output capacitance can be increased to achieve greater transient performance.

MOSFET Selection

The MIC5165 utilizes external N-Channel MOSFETs to sink and source current. MOSFET selection will be determined by two main characteristics: size and gate threshold (V_{GS}).

MOSFET Power Requirements

One of the most important factors to determine is the amount of power the MOSFET is going to be required to dissipate. Power dissipation in a DDR3 circuit will be identical for both the high side and low side MOSFETs. Since the supply voltage is divided by half to supply V_{TT}, both MOSFETs have the same voltage dropped across them. They are also required to be able to sink and source the same amount of current (for either all 0s or all 1s). This equates to each side being able to dissipate the same amount of power. Power dissipation

calculation for the high-side MOSFET is as follows:

$$P_D = (V_{DDQ} - V_{TT}) \times I\_SOURCE$$

Where I_source is the average source current.

Power dissipation for the low-side MOSFET is as follows:

$$P_D = V_{TT} \times I\_SINK$$

where I_sink is the average sink current.

In a typical 3.5A peak DDR3 circuit, power considerations for MOSFET selection would occur as follows:

$$P_D = (V_{DDQ} - V_{TT}) \times I\_SOURCE$$
$$P_D = (1.5V - 0.75V) \times 1.75A$$
$$P_D = 1.3125\ W$$

This typical DDR3 application would require the high-side and low-side N-Channel MOSFETs to be able to handle 1.3125 Watts each. In higher current applications, multiple N-Channel MOSFETs may be placed in parallel to spread the power dissipation. These MOSFETs will share current, distributing power dissipation across each device.

The maximum MOSFET die (junction) temperature limits maximum power dissipation. The ability of the device to dissipate heat away from the junction is specified by the junction-to-ambient (θ_{JA}) thermal resistance. This is the sum of junction-to-case (θ_{JC}) thermal resistance, case-to-sink (θ_{CS}) thermal resistance and sink-to-ambient (θ_{SA}) thermal resistance:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

In our example of a 3.5A peak DDR3 termination circuit, we have selected a D-pack N-Channel MOSFET that has a maximum junction temperature of 125°C. The device has a junction-to-case thermal resistance of 1.5°C/W. Our application has a maximum ambient temperature of 60°C.

The required junction-to-ambient thermal resistance can be calculated as follows:

$$\theta_{JA} = \frac{T_J - T_A}{P_D}$$

Where T_J is the maximum junction temperature, T_A is the maximum ambient temperature and P_D is the power dissipation.

In our example:

$$\theta_{JA} = \frac{T_J - T_A}{P_D}$$
$$\theta_{JA} = \frac{125°C - 60°C}{1.3125W}$$
$$\theta_{JA} = 49.52\frac{°C}{W}$$

This shows that our total thermal resistance must be better than 49.52°C/W. Since the total thermal resistance is a combination of all the individual thermal resistances, the amount of heat sink required can be calculated as follows:

$$\theta_{SA} = \theta_{JA} - (\theta_{JC} + \theta_{CS})$$

In our example:

$$\theta_{SA} = \theta_{JA} - (\theta_{JC} + \theta_{CS})$$
$$\theta_{SA} = 49.52\frac{°C}{W} - (1.5\frac{°C}{W} + 0.5\frac{°C}{W})$$
$$\theta_{SA} = 47.52\frac{°C}{W}$$

In most cases, case-to-sink thermal resistance can be assumed to be about 0.5°C/W.

The DDR3 termination circuit for our example, using two D-pack N-Channel MOSFETs (one high-side and one low-side) will require enough copper area to spread the heat away from the MOSFET. In this example to dissipate 1.3W from TO-252 package a 2 oz copper of 0.4 in^2 on component side is required. In some cases, airflow may also help to reduce thermal resistance. For different MOSFET package refer to manufacturer Data Sheet for copper area requirements.

MOSFET Gate Threshold

N-Channel MOSFETs require an enhancement voltage greater than its source voltage. Typical N-Channel MOSFETs have a gate-source threshold (V_{GS}) of 1.8V or higher. Since the source of the high side N-Channel MOSFET is connected to V_{TT}, the MIC5165 VCC pin requires a voltage equal to or greater than the V_{GS} + V_{TT} voltage. For example, our DDR3 termination circuit has a V_{TT} voltage of 0.75V. For an N-Channel MOSFET that has a V_{GS} rating of 2.5V, the V_{CC} voltage can be as min as 3.25V. For an N-Channel MOSFET that has a 4.5V V_{GS}, the minimum V_{CC} required is 5.25V. It is recommended that the V_{CC} voltage has enough margin to be able to fully enhance the MOSFETs for large signal transient response. In addition, low gate thresholds MOSFETs are recommended to reduce the V_{CC} requirements.

Ripple Measurements

To properly measure ripple on either input or output of a switching regulator, a proper ring in tip measurement is required. Standard oscilloscope probes come with a grounding clip, or a long wire with an alligator clip. Unfortunately, for high frequency measurements, this ground clip can pick up high-frequency noise and erroneously inject it into the measured output ripple.

By maintaining the shortest possible ground lengths on the oscilloscope probe, true ripple measurements can be obtained. This requires the removing of the oscilloscope probe sheath and ground clip from a standard oscilloscope probe and wrapping a non-shielded bus wire around the oscilloscope probe. If there does not happen to be any non-shielded bus wire immediately available, the leads from axial resistors will work.

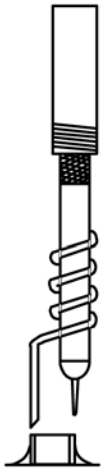


Figure 6. Low-Noise Measurement

PCB Layout Guideline

Warning!!! To minimize EMI and output noise, follow these layout recommendations.

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC5165 controller application.

IC and MOSFET

- Place the IC close to the point of load (POL).
- The trace connecting controller drive pins to MOSFETs gates should be short and wide to avoid oscillations. These oscillations are the result of tank circuit formed by trace inductance and gate capacitance.
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

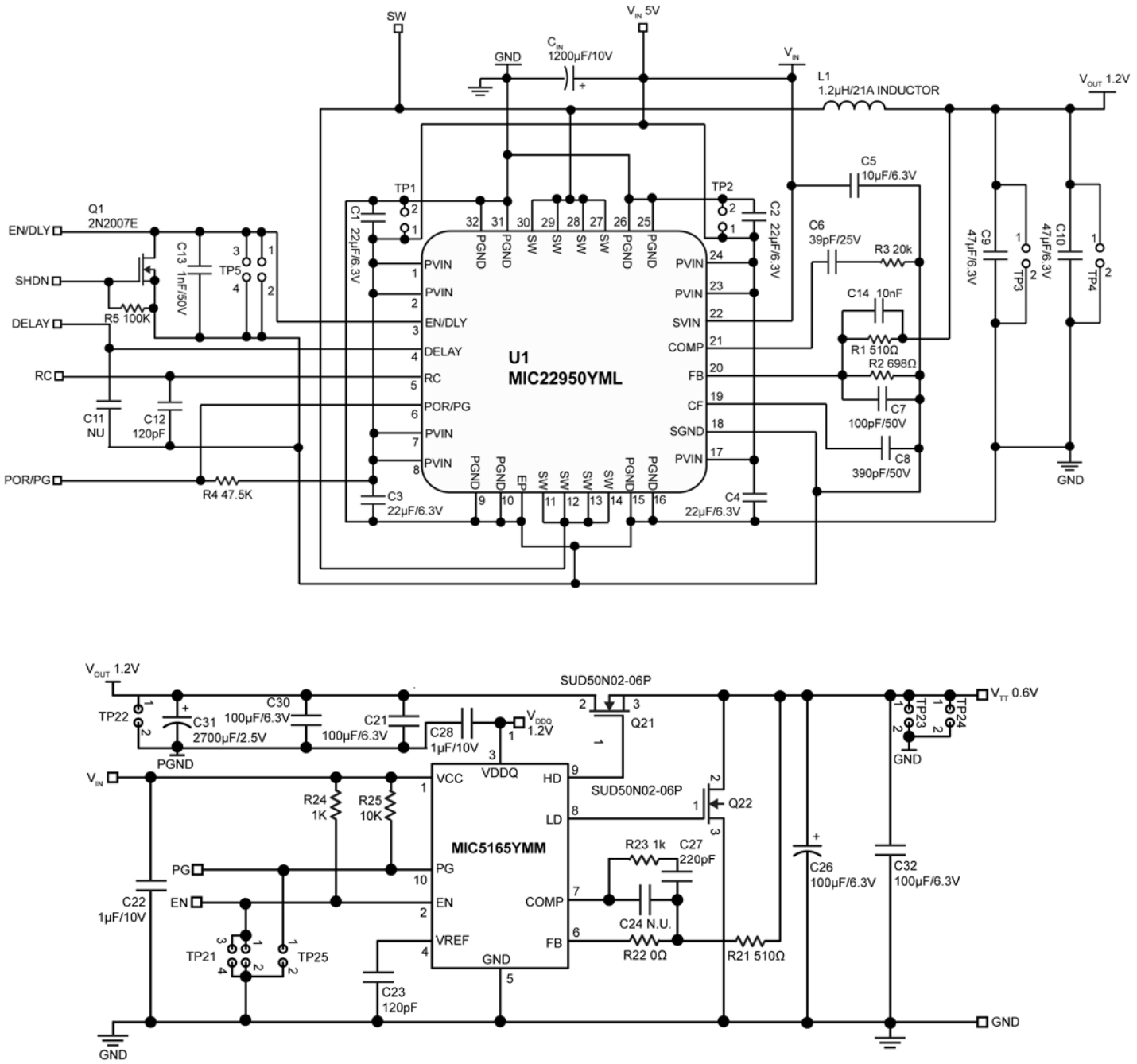
Input Capacitor

- Place the input capacitor next.
- Place the input capacitors on the same side of the board and as close to the MOSFET and IC as possible.
- Place a ceramic bypass capacitor next to MOSFET.
- Keep both the VIN and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal, but not between the input capacitors and MOSFET.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.

Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

Design Example



MIC5165 as a DDR3 Memory Termination Device for 3.5A Application (VDDQ and MOSFET Input Separated)

Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C2, C3, C4	GRM21BR60J226ME39L	Murata[1]	22µF, 6.3V, Ceramic capacitor, X5R, 0805	4
	C2012X5R0J226M	TDK[2]		
	08056D226MAT2A	AVX[3]		
C5	GRM188R60J106ME47D	Murata[1]	10µF, 6.3V, Ceramic capacitor, X5R, 0603	1
	C1608X5R0J106M	TDK[2]		
	06036D106MAT2A	AVX[3]		
C6	GRM1885C1H390JA01D	Murata[1]	39pF, 50V, Ceramic capacitor, NPO, 0603	1
	C1608C0G1H390J	TDK[2]	39pF, 25V, Ceramic capacitor, NPO, 0603	
C7	06035C101MAT2A	AVX[3]	100pF, 50V, Ceramic capacitor, X7R, 0603	1
C8	GRM188R71H391KA01D	Murata[1]	390pF, 50V, Ceramic capacitor, X7R, 0603	1
C9, C10	GRM31CR60J476ME19L	Murata[1]	47µF, 6.3V, Ceramic capacitor, X5R, 1206	2
	C3216X5R0J476M	TDK[2]		
	12066D476MAT2A	AVX[3]		
C13	GRM188R71H102KA01D	Murata[1]	1nF, 50V, Ceramic capacitor, X7R, 0603	1
C14	GRM188R71H103KA01D	Murata[1]	10nF, 50V, Ceramic capacitor, X7R, 0603	1
C22, C28	0603ZD105KAT2A	AVX[3]	1µF, 10V, Ceramic capacitor, X5R, 0603	1
	GRM188R61A105K	Murata[1]		
C23, C12	VJ0603A121JXACW1BC	Vishay[4]	120pF, 25V, Ceramic capacitor, NPO, 0603	2
	06033A121JAT2A	AVX[3]		
C27	VJ0603Y221KXACW1BC	Vishay[4]	220pF, 50V, Ceramic capacitor, X7R, 0603	1
	06033C221JAT2A	AVX[3]	220pF, 25V, Ceramic capacitor, X7R, 0603	
C26	TCJB107M006R0070	AVX[3]	100µF, 6.3V, Tantalum capacitor, 1210	1
C24, C11			N.U. 0603 ceramic cap	3
C30, C32, C21	C4532X5R0J107M	TDK[2]	100µF, 6.3V, Ceramic capacitor, X5R, 1812	1
C31	Open (2SEPC2700M)	Sanyo[5]	2700µF, 2.5V OS-CON Cap	1
CIN	EEE-FPA122UAP	Panasonic[6]	1200µF, 10V, Electrolytic capacitor, SMD, 10x10.2-case	1
L1	CDEP105ME-1R2MC	Sumida[7]	1.2µH, 21A, Inductor, 10.4mmX10.4mm	1
Q1	2N7002E(SOT-23)	Vishay[4]	Signal MOSFET, SOT-23-6	2
Q21, Q22	SUD50N02-06P	Vishay[4]	Low VGS(th) N-Channel 20-V (D-S)	1
R1	CRCW06031101FRT1	Vishay Dale[4]	510Ω, Resistor, 1%, 0603	1
R2	CRCW0603698RFRT1	Vishay Dale[4]	698Ω, Resistor, 1%, 0603	1
R3	CRCW06032002FRT1	Vishay Dale[4]	20K, Resistor, 1%, 0603	1
R4	CRCW06034752FRT1	Vishay Dale[4]	47.5K, Resistor, 1%, 0603	1

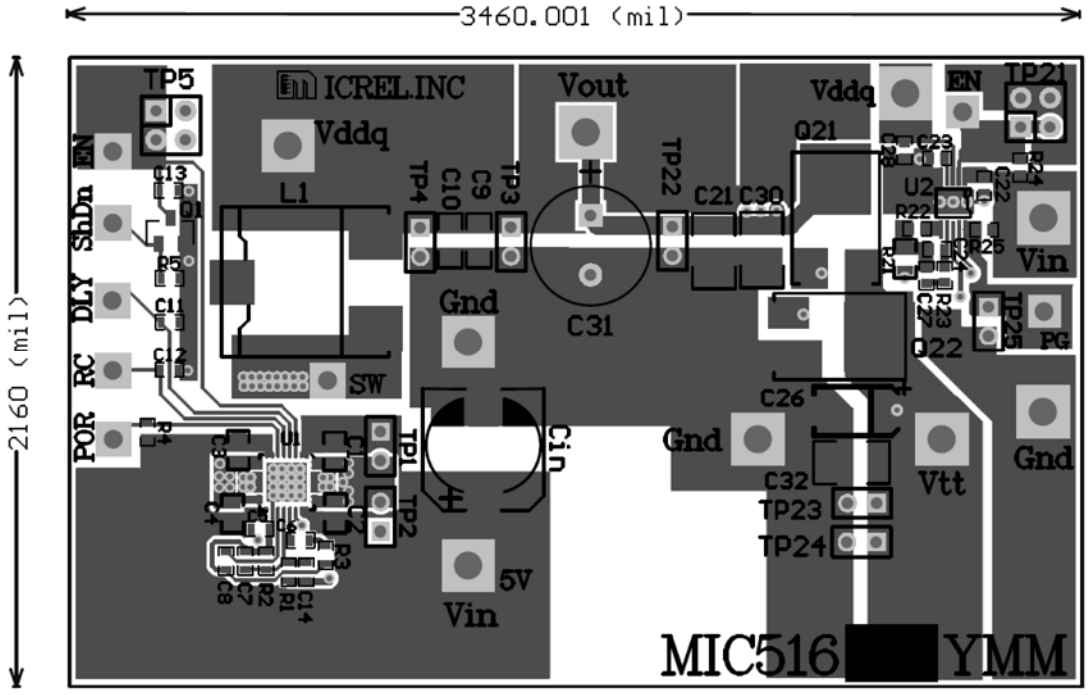
Bill of Materials (Continued)

Item	Part Number	Manufacturer	Description	Qty.
R5	CRCW06031003FRT1	Vishay Dale[4]	100K, Resistor, 1%, 0603	1
R21	CRCW0805510RFKTA	Vishay Dale[4]	510Ω, Resistor, 1%, 0805	1
R23, R24	CRCW06031K00FKTA	Vishay Dale[4]	1K, Resistor, 1%, 0603	1
R22	CRCW06030000FKTA	Vishay Dale[4]	0Ω, Resistor, 1%, 0603	1
R25	CRCW06031002FRT1	Vishay Dale[4]	10K, Resistor, 1%, 0603	1
U1	**MIC22950YML**	**Micrel[8]**	**10A, 0.4MHz-2MHz, Synchronous Buck Regulator**	**1**
U21	**MIC5165YMM**	**Micrel[8]**	**Dual Regulator Controller for DDR3**	**1**

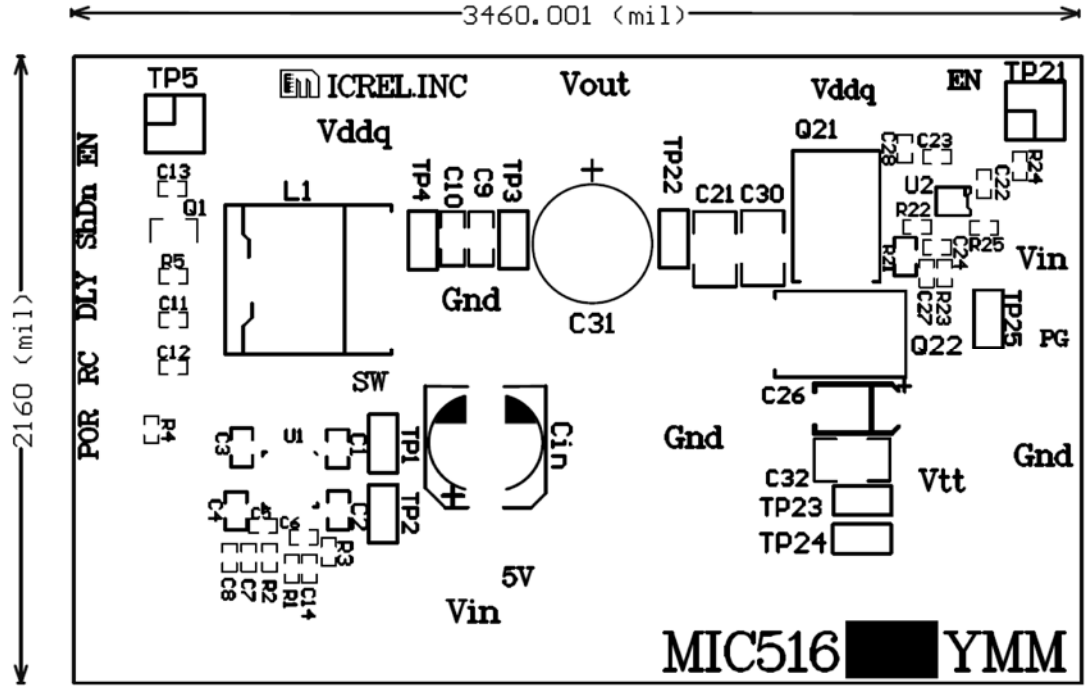
Notes:

1. Murata: www.murata.com.
2. TDK: www.tdk.com.
3. AVX: www.avx.com.
4. Vishay: www.vishay.com.
5. Sanyo: www.sanyo.com.
6. Panasonic.: www.panasonic.com.
7. Sumida: www.sumida.com.
8. Micrel, Inc.: **www.micrel.com**.

PCB Layout Recommendations

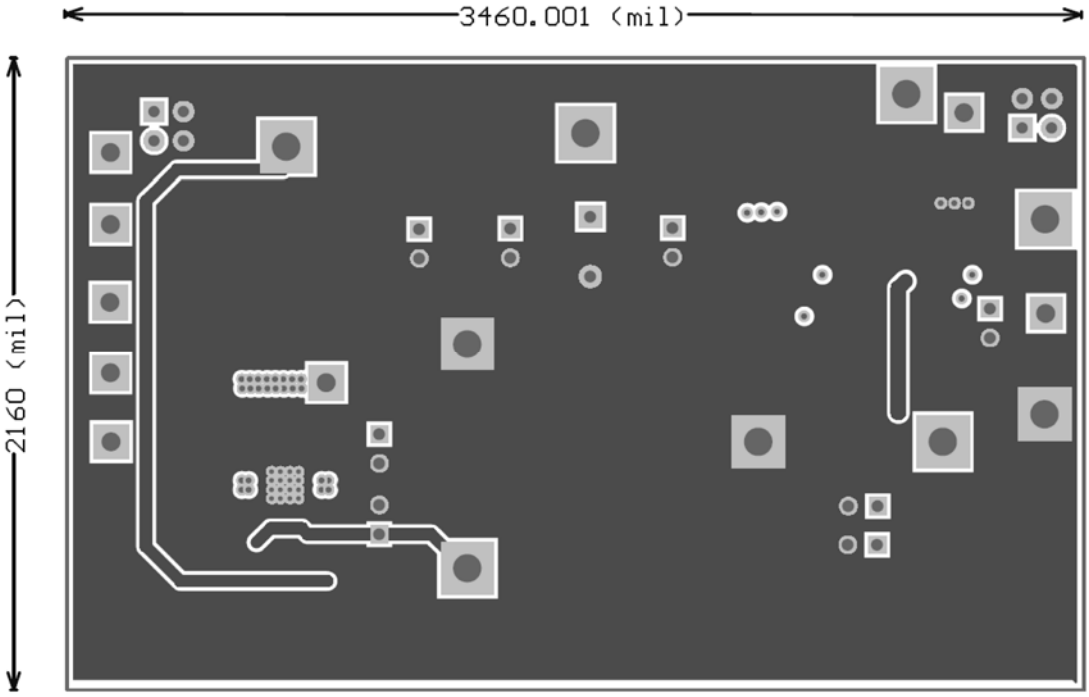


Top Layer

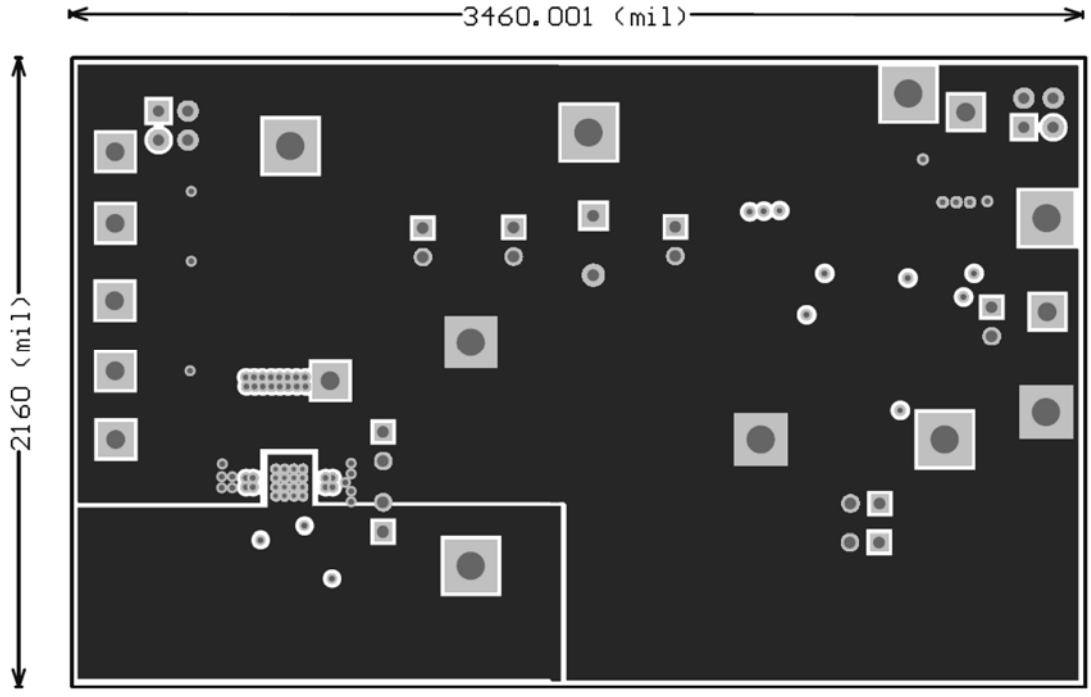


Top Component Layer

PCB Layout Recommendations (Continued)

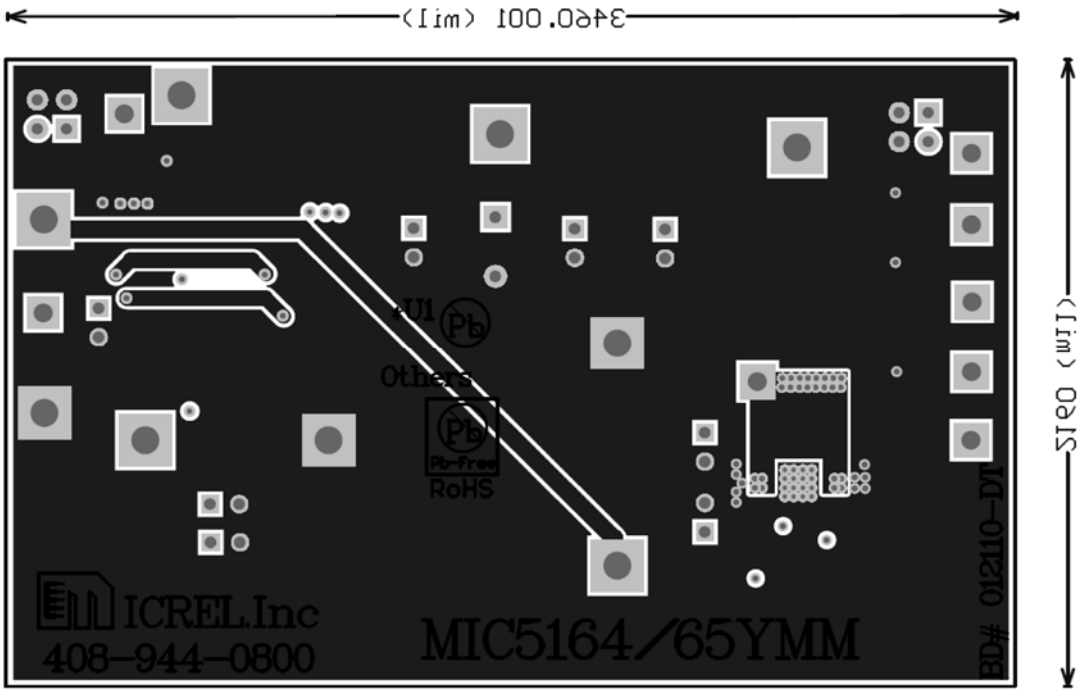


Mid-1 Layer

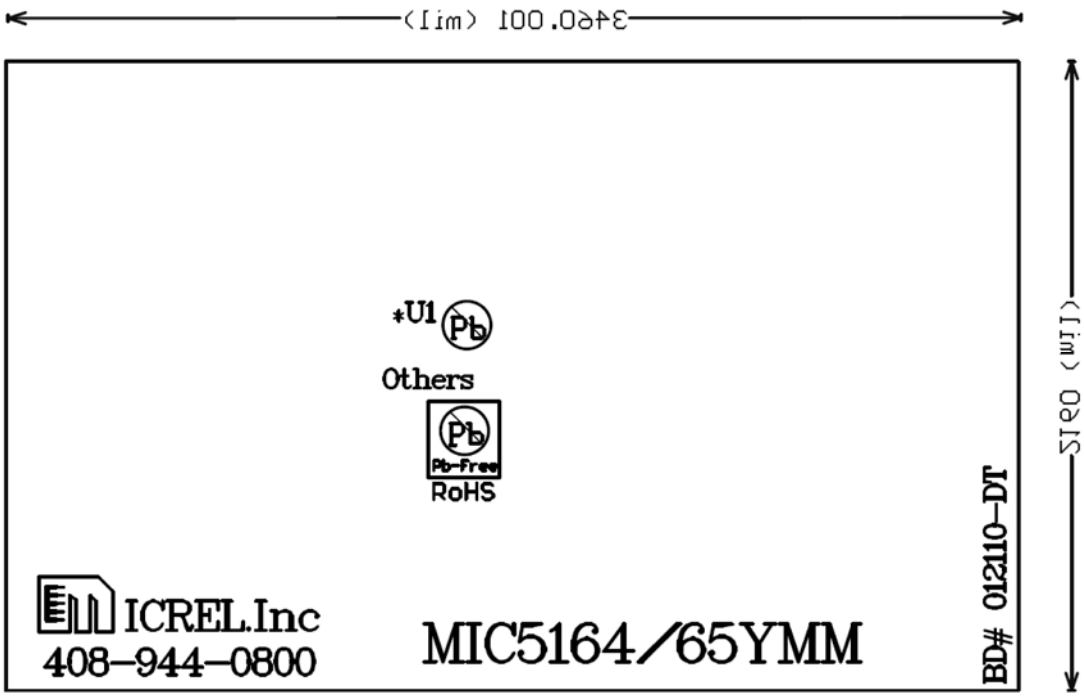


Mid-2 Layer

PCB Layout Recommendations (Continued)

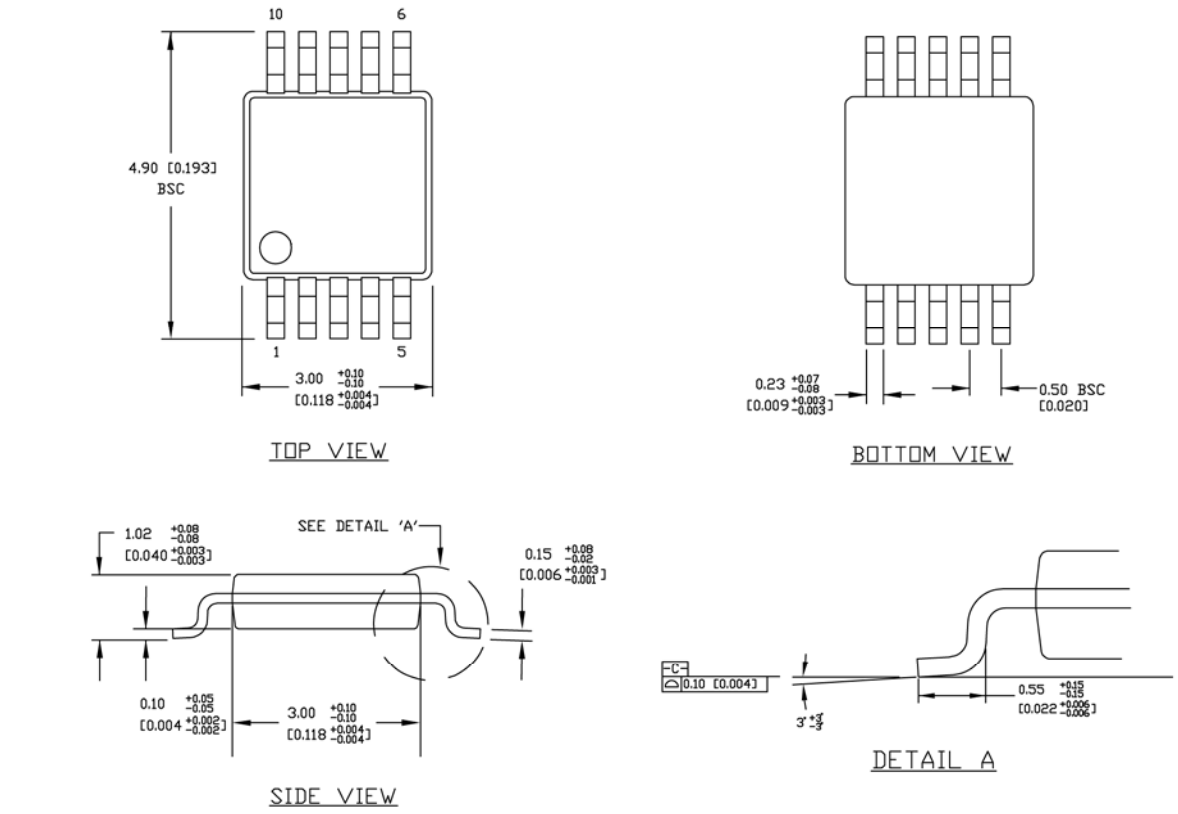


Bottom Layer



Bottom Silk

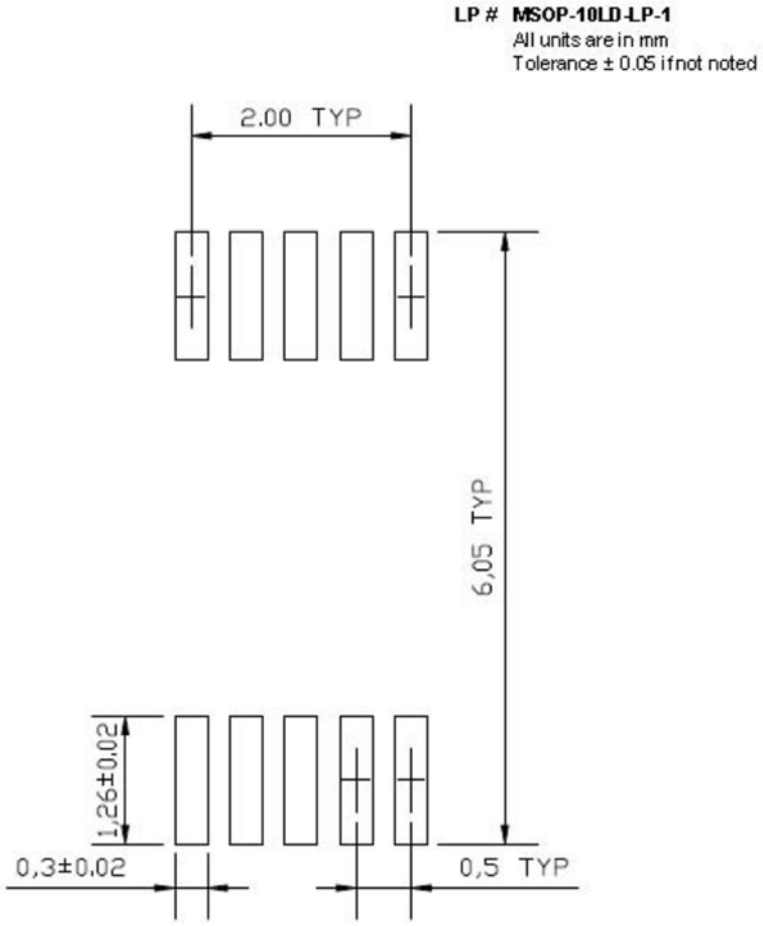
Package Information



NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

10-Pin MSOP (MM)

Recommended Land Pattern



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