## FEATURES

- 500ps max. propagation delay

■ Extended 100E VEE range of -4.2 V to -5.5 V

- True and complementary outputs
$\square$ Fully compatible with industry standard 10 KH , 100K I/O levels
■ Internal $75 \mathrm{~K} \Omega$ input pulldown resistors
■ Fully compatible with Motorola MC10E/100E101
- Available in 28-pin PLCC package


## BLOCK DIAGRAM






## DESCRIPTION

The SY10/100E101 are quad 4 -input OR/NOR gates designed for use in new, high-performance ECL systems. The E101 features both true and complementary outputs.

## PIN NAMES

| Pin | Function |
| :--- | :--- |
| Dna, Dnb, Dnc, Dnd | Data Inputs |
| Q0-Q3 | True Outputs |
| $\bar{Q}_{0}-\bar{Q}_{3}$ | Inverting Outputs |
| Vcco | Vcc to Output |

## PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information(1)

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
| :---: | :---: | :---: | :---: | :---: |
| SY10E101JI | J28-1 | Industrial | SY10E101JI | $\mathrm{Sn}-\mathrm{Pb}$ |
| SY10E101JITR ${ }^{(2)}$ | J28-1 | Industrial | SY10E101JI | $\mathrm{Sn}-\mathrm{Pb}$ |
| SY100E101JI | J28-1 | Industrial | SY100E101JI | $\mathrm{Sn}-\mathrm{Pb}$ |
| SY100E101JITR ${ }^{(2)}$ | J28-1 | Industrial | SY100E101JI | $\mathrm{Sn}-\mathrm{Pb}$ |
| SY10E101JC | J28-1 | Commercial | SY10E101JC | $\mathrm{Sn}-\mathrm{Pb}$ |
| SY10E101JCTR ${ }^{(2)}$ | J28-1 | Commercial | SY10E101JC | $\mathrm{Sn}-\mathrm{Pb}$ |
| SY100E101JC | J28-1 | Commercial | SY100E101JC | $\mathrm{Sn}-\mathrm{Pb}$ |
| SY100E101JCTR ${ }^{(2)}$ | J28-1 | Commercial | SY100E101JC | $\mathrm{Sn}-\mathrm{Pb}$ |
| SY10E101JY ${ }^{(3)}$ | J28-1 | Industrial | SY10E101JY with Pb-Free bar-line indicator | Matte-Sn |
| SY10E101JYTR ${ }^{(2,3)}$ | J28-1 | Industrial | SY10E101JY with Pb-Free bar-line indicator | Matte-Sn |
| SY100E101JY ${ }^{(3)}$ | J28-1 | Industrial | SY100E101JY with Pb-Free bar-line indicator | Matte-Sn |
| SY100E101JYTR ${ }^{(2,3)}$ | J28-1 | Industrial | SY100E101JY with Pb-Free bar-line indicator | Matte-Sn |

## Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_{A}=25^{\circ} \mathrm{C}$, DC Electricals only.
2. Tape and Reel.
3. Pb -Free package is recommended for new designs.

## LOGIC EQUATION

$Q_{n}=D_{n a}+D_{n b}+D_{n c}+D_{n d}$

## DC ELECTRICAL CHARACTERISTICS ${ }^{(1)}$

$\mathrm{Vee}=\mathrm{Vee}$ (Min.) to $\operatorname{Vee}(\mathrm{Max}.) ; \mathrm{Vcc}=\mathrm{Vcco}=\mathrm{GND}$

| Symbol | Parameter | $\mathrm{TA}=-40^{\circ} \mathrm{C}$ |  |  | $\mathrm{TA}=0^{\circ} \mathrm{C}$ |  |  | $\mathrm{TA}=+25^{\circ} \mathrm{C}$ |  |  | $\mathrm{TA}=+8{ }^{\circ} \mathrm{C}$ |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. |  |
| IIH | Input HIGH Current | - | - | 150 | - | - | 150 | - | - | 150 | - | - | 150 | $\mu \mathrm{A}$ |
| IEE | Power Supply Current 10 EL 100 EL | - | $\begin{aligned} & 30 \\ & 30 \\ & \hline \end{aligned}$ | $\begin{aligned} & 36 \\ & 36 \\ & \hline \end{aligned}$ | - | $\begin{aligned} & 30 \\ & 30 \end{aligned}$ | $\begin{aligned} & 36 \\ & 36 \end{aligned}$ | - | 30 30 | $\begin{aligned} & 36 \\ & 36 \end{aligned}$ | - | $\begin{aligned} & 30 \\ & 35 \end{aligned}$ | $\begin{aligned} & 36 \\ & 42 \end{aligned}$ | mA |

Note:

1. Specification for packaged product only.

## AC ELECTRICAL CHARACTERISTICS ${ }^{(3)}$

$\mathrm{VEE}=\mathrm{Vee}($ Min. $)$ to $\mathrm{Vee}($ Max.) $\mathrm{Vcc}=\mathrm{Vcco}=\mathrm{GND}$

|  | Parameter | $\mathrm{TA}=-40^{\circ} \mathrm{C}$ |  |  | $\mathrm{TA}=0^{\circ} \mathrm{C}$ |  |  | $\mathrm{TA}=+25^{\circ} \mathrm{C}$ |  |  | $\mathrm{TA}=+85^{\circ} \mathrm{C}$ |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol |  | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. |  |
| tPD | Propagation Delay to Output D to Q | 150 | - | 550 | 200 | 350 | 500 | 200 | 350 | 500 | 200 | 350 | 500 | ps |
| tskew | Within-Device Skew ${ }^{(1)}$ Within-Gate Skew ${ }^{(2)}$ | - | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | - | - | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | - | - | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | - | - | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | - | $\begin{aligned} & \text { ps } \\ & \text { ps } \end{aligned}$ |
| $\begin{aligned} & \mathrm{tr} \\ & \mathrm{tf} \end{aligned}$ | Rise/Fall Time $20 \%$ to $80 \%$ | 275 | - | 625 | 300 | 380 | 575 | 300 | 380 | 575 | 300 | 380 | 575 | ps |

## Notes:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Within-gate skew is defined as the variation in propagation delays through a single gate when driven from its different inputs.
3. Specification for packaged product only.

## 28-PIN PLCC (J28-1)



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