# 25AA256/25LC256

## 256K SPI Bus Serial EEPROM

### Device Selection Table

| Part Number | Vcc Range | Page Size | Temp. Ranges | Packages |
|---|---|---|---|---|
| 25LC256 | 2.5V-5.5V | 64 Bytes | I, E | MF, P, SN, SM, ST |
| 25AA256 | 1.8V-5.5V | 64 Bytes | I, E | MF, P, SN, SM, ST |

### Features

- Maximum Clock 10 MHz
- Low-Power CMOS Technology:
  - Maximum Write current: 5 mA at 5.5V, 10 MHz
  - Read current: 6 mA at 5.5V, 10 MHz
  - Standby current: 1 µA at 5.5V
- 32,768 x 8-Bit Organization
- 64-Byte Page
- Self-Timed Erase and Write Cycles (5 ms maximum)
- Block Write Protection:
  - Protect none, 1/4, 1/2 or all of array
- Built-In Write Protection:
  - Power-on/off data protection circuitry
  - Write enable latch
  - Write-protect pin
- Sequential Read
- High Reliability:
  - Endurance: 1,000,000 erase/write cycles
  - Data retention: > 200 years
  - ESD protection: > 4000V
- Temperature Ranges Supported:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C
- RoHS Compliant
- Automotive AEC-Q100 Qualified

### Packages

- 8-Lead DFN-S, 8-Lead PDIP, 8-Lead SOIC, 8-Lead SOIJ and 8-Lead TSSOP

### Pin Function Table

| Name | Function |
|---|---|
| $\overline{CS}$ | Chip Select Input |
| SO | Serial Data Output |
| $\overline{WP}$ | Write-Protect |
| Vss | Ground |
| SI | Serial Data Input |
| SCK | Serial Clock Input |
| $\overline{HOLD}$ | Hold Input |
| Vcc | Supply Voltage |

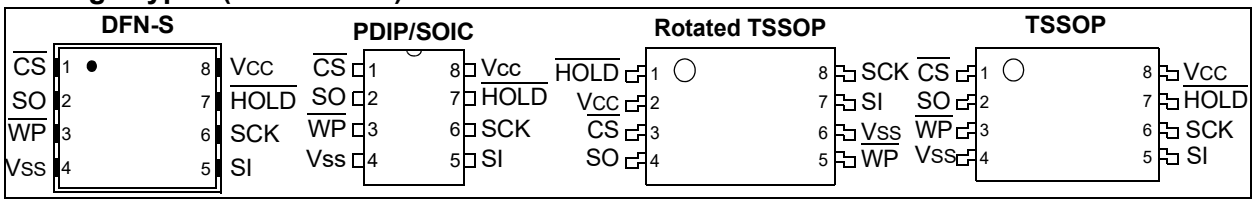
### Description

The Microchip Technology Inc. 25AA256/25LC256 (25XX256[1]) are 256-Kbit Serial Electrically Erasable PROMs. The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select ($\overline{CS}$) input.

Communication to the device can be paused via the hold pin ($\overline{HOLD}$). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

**Note 1:** 25XX256 is used in this document as a generic part number for the 25AA256/25LC256 devices.

### Package Types (not to scale)



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature under bias .....-40°C to +125°C

ESD protection on all pins .....4 kV

**† NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

**TABLE 1-1: DC CHARACTERISTICS**

| **DC CHARACTERISTICS** | | | **Industrial (I): TA = -40°C to +85°C VCC = 1.8V to 5.5V<br>Extended (E): TA = -40°C to +125°C VCC = 1.8V to 5.5V** | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristic** | **Minimum** | **Maximum** | **Units** | **Test Conditions** |
| D001 | VIH | High-Level Input Voltage | 0.7 VCC | VCC +1 | V | |
| D002 | VIL | Low-Level Input Voltage | -0.3 | 0.3 VCC | V | VCC ≥ 2.5V |
| D003 | VIL | | -0.3 | 0.2 VCC | V | VCC < 2.5V |
| D004 | VOL | Low-Level Output Voltage | — | 0.4 | V | IOL = 2.1 mA, VCC = 4.5V |
| D005 | VOL | | — | 0.2 | V | IOL = 1.0 mA, VCC = 2.5V |
| D006 | VOH | High-Level Output Voltage | VCC -0.5 | — | V | IOH = -400 µA |
| D007 | ILI | Input Leakage Current | — | ±1 | µA | $\overline{CS}$ = VCC, VIN = VSS or VCC |
| D008 | ILO | Output Leakage Current | — | ±1 | µA | $\overline{CS}$ = VCC, VOUT = VSS or VCC |
| D009 | CINT | Internal Capacitance (All Inputs and Outputs) | — | 7 | pF | TA = 25°C, FCLK = 1.0 MHz, VCC = 5.0V **(Note 2)** |
| D010 | ICC Read | Operating Current | — | 6 | mA | VCC = 5.5V; FCLK = 10.0 MHz; SO = Open |
| | | | — | 2.5 | mA | VCC = 2.5V; FCLK = 5.0 MHz; SO = Open |
| D011 | ICC Write | | — | 5 | mA | VCC = 5.5V |
| | | | — | 3 | mA | VCC = 2.5V |
| D012 | ICCS | Standby Current | — | 5 | µA | $\overline{CS}$ = VCC = 5.5V, Inputs tied to VCC or VSS, +125°C |
| | | | — | 1 | µA | $\overline{CS}$ = VCC = 5.5V, Inputs tied to VCC or VSS, +85°C |

**Note 1:** Typical measurements taken at room temperature (+25°C).

**2:** This parameter is periodically sampled and not 100% tested.

**TABLE 1-2: AC CHARACTERISTICS**

| AC CHARACTERISTICS | | | Industrial (I): TA = -40°C to +85°C VCC = 1.8V to 5.5V<br>Extended (E): TA = -40°C to +125°C VCC = 1.8V to 5.5V | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristic** | **Minimum** | **Maximum** | **Units** | **Test Conditions** |
| 1 | FCLK | Clock Frequency | — | 10 | MHz | 4.5V ≤ Vcc ≤ 5.5V |
| | | | — | 5 | MHz | 2.5V ≤ Vcc < 4.5V |
| | | | — | 3 | MHz | 1.8V ≤ Vcc < 2.5V |
| 2 | TCSS | $\overline{CS}$ Setup Time | 50 | — | ns | 4.5V ≤ Vcc ≤ 5.5V |
| | | | 100 | — | ns | 2.5V ≤ Vcc < 4.5V |
| | | | 150 | — | ns | 1.8V ≤ Vcc < 2.5V |
| 3 | TCSH | $\overline{CS}$ Hold Time | 100 | — | ns | 4.5V ≤ Vcc ≤ 5.5V |
| | | | 200 | — | ns | 2.5V ≤ Vcc < 4.5V |
| | | | 250 | — | ns | 1.8V ≤ Vcc < 2.5V |
| 4 | TCSD | $\overline{CS}$ Disable Time | 50 | — | ns | |
| 5 | TSU | Data Setup Time | 10 | — | ns | 4.5V ≤ Vcc ≤ 5.5V |
| | | | 20 | — | ns | 2.5V ≤ Vcc < 4.5V |
| | | | 30 | — | ns | 1.8V ≤ Vcc < 2.5V |
| 6 | THD | Data Hold Time | 20 | — | ns | 4.5V ≤ Vcc ≤ 5.5V |
| | | | 40 | — | ns | 2.5V ≤ Vcc < 4.5V |
| | | | 50 | — | ns | 1.8V ≤ Vcc < 2.5V |
| 7 | TR | CLK Rise Time | — | 100 | ns | **Note 1** |
| 8 | TF | CLK Fall Time | — | 100 | ns | **Note 1** |
| 9 | THI | Clock High Time | 50 | — | ns | 4.5V ≤ Vcc ≤ 5.5V |
| | | | 100 | — | ns | 2.5V ≤ Vcc < 4.5V |
| | | | 150 | — | ns | 1.8V ≤ Vcc < 2.5V |
| 10 | TLO | Clock Low Time | 50 | — | ns | 4.5V ≤ Vcc ≤ 5.5V |
| | | | 100 | — | ns | 2.5V ≤ Vcc < 4.5V |
| | | | 150 | — | ns | 1.8V ≤ Vcc < 2.5V |
| 11 | TCLD | Clock Delay Time | 50 | — | ns | |
| 12 | TCLE | Clock Enable Time | 50 | — | ns | |
| 13 | TV | Output Valid from Clock Low | — | 50 | ns | 4.5V ≤ Vcc ≤ 5.5V |
| | | | — | 100 | ns | 2.5V ≤ Vcc < 4.5V |
| | | | — | 160 | ns | 1.8V ≤ Vcc < 2.5V |
| 14 | THO | Output Hold Time | 0 | — | ns | **Note 1** |
| 15 | TDIS | Output Disable Time | — | 40 | ns | 4.5V ≤ Vcc ≤ 5.5V (**Note 1**) |
| | | | — | 80 | ns | 2.5V ≤ Vcc ≤ 4.5V (**Note 1**) |
| | | | — | 160 | ns | 1.8V ≤ Vcc ≤ 2.5V (**Note 1**) |
| 16 | THS | $\overline{HOLD}$ Setup Time | 20 | — | ns | 4.5V ≤ Vcc ≤ 5.5V |
| | | | 40 | — | ns | 2.5V ≤ Vcc < 4.5V |
| | | | 80 | — | ns | 1.8V ≤ Vcc < 2.5V |

**Note 1:** This parameter is periodically sampled and not 100% tested.

**2:** TWC begins on the rising edge of $\overline{CS}$ after a valid write sequence and ends when the internal write cycle is complete.

**3:** This parameter is not tested but ensured by characterization.

**TABLE 1-2: AC CHARACTERISTICS (CONTINUED)**

| AC CHARACTERISTICS | | | Industrial (I): TA = -40°C to +85°C VCC = 1.8V to 5.5V<br>Extended (E): TA = -40°C to +125°C VCC = 1.8V to 5.5V | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristic** | **Minimum** | **Maximum** | **Units** | **Test Conditions** |
| 17 | THH | $\overline{HOLD}$ Hold Time | 20 | — | ns | 4.5V ≤ Vcc ≤ 5.5V |
| | | | 40 | — | ns | 2.5V ≤ Vcc < 4.5V |
| | | | 80 | — | ns | 1.8V ≤ Vcc < 2.5V |
| 18 | THZ | $\overline{HOLD}$ Low to Output High-Z | — | 30 | ns | 4.5V ≤ Vcc ≤ 5.5V **(Note 1)** |
| | | | — | 60 | ns | 2.5V ≤ Vcc < 4.5V **(Note 1)** |
| | | | — | 160 | ns | 1.8V ≤ Vcc < 2.5V **(Note 1)** |
| 19 | THV | $\overline{HOLD}$ High to Output Valid | — | 30 | ns | 4.5V ≤ Vcc ≤ 5.5V |
| | | | — | 60 | ns | 2.5V ≤ Vcc < 4.5V |
| | | | — | 160 | ns | 1.8V ≤ Vcc < 2.5V |
| 20 | TWC | Internal Write Cycle Time | — | 5 | ms | **Note 2** |
| 21 | | Endurance | 1M | — | E/W Cycles | +25°C, VCC = 5.5V **(Note 3)** |

**Note 1:** This parameter is periodically sampled and not 100% tested.

**2:** TWC begins on the rising edge of $\overline{CS}$ after a valid write sequence and ends when the internal write cycle is complete.

**3:** This parameter is not tested but ensured by characterization.

**TABLE 1-3: AC TEST CONDITIONS**

| **AC Waveform** | |
|---|---|
| VLO = 0.2V | — |
| VHI = VCC – 0.2V | **Note 1** |
| VHI = 4.0V | **Note 2** |
| CL = 50 pF | — |
| **Timing Measurement Reference Level** | |
| Input | 0.5 VCC |
| Output | 0.5 VCC |

**Note 1:** For VCC ≤ 4.0V

**2:** For VCC > 4.0V

**FIGURE 1-1: HOLD TIMING**

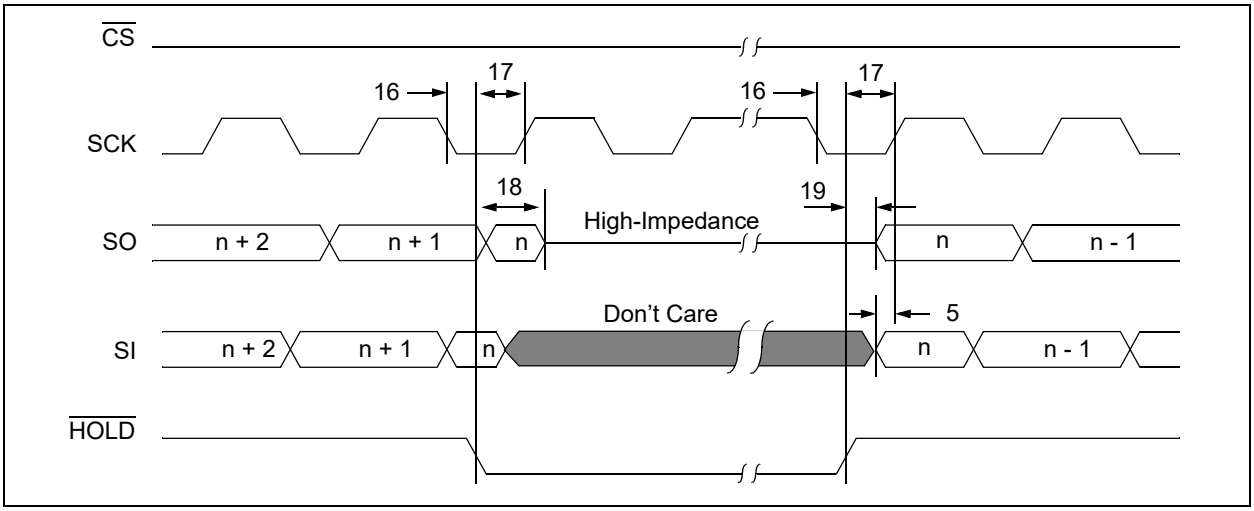



**FIGURE 1-2: SERIAL INPUT TIMING**

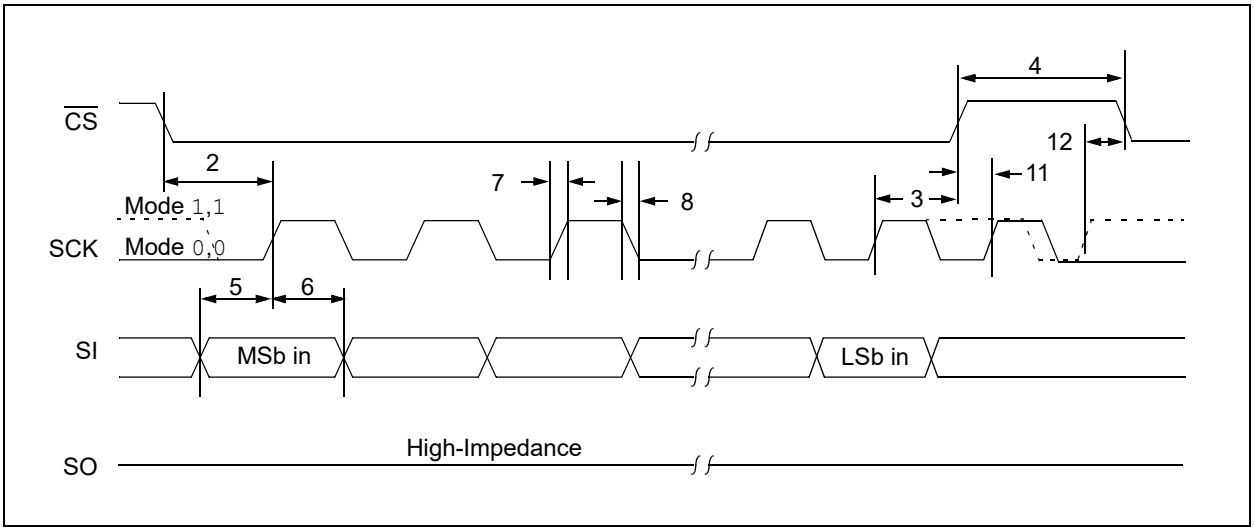
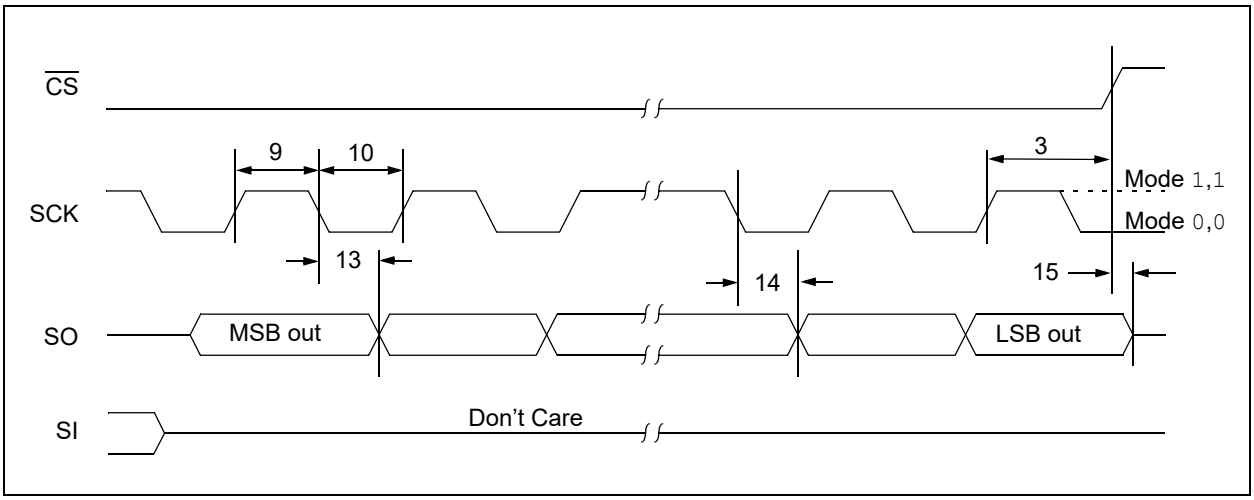



**FIGURE 1-3: SERIAL OUTPUT TIMING**



## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

**TABLE 2-1: PIN FUNCTION TABLE**

| Name | DFN-S[1] | PDIP | SOIC | TSSOP | Rotated TSSOP | Function |
|---|---|---|---|---|---|---|
| $\overline{CS}$ | 1 | 1 | 1 | 1 | 3 | Chip Select Input |
| SO | 2 | 2 | 2 | 2 | 4 | Serial Data Output |
| $\overline{WP}$ | 3 | 3 | 3 | 3 | 5 | Write-Protect Pin |
| VSS | 4 | 4 | 4 | 4 | 6 | Ground |
| SI | 5 | 5 | 5 | 5 | 7 | Serial Data Input |
| SCK | 6 | 6 | 6 | 6 | 8 | Serial Clock Input |
| $\overline{HOLD}$ | 7 | 7 | 7 | 7 | 1 | Hold Input |
| VCC | 8 | 8 | 8 | 8 | 2 | Supply Voltage |

**Note 1:** Exposed pad on DFN-S package can be connected to VSS or left floating.

### 2.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

### 2.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25XX256. During a read cycle, data are shifted out on this pin after the falling edge of the serial clock.

### 2.3 Write-Protect ($\overline{WP}$)

This pin is used in conjunction with the WPEN bit in the STATUS register to prohibit writes to the nonvolatile bits in the STATUS register. When $\overline{WP}$ is low and WPEN is high, writing to the nonvolatile bits in the STATUS register is disabled. All other operations function normally. When $\overline{WP}$ is high, all functions, including writes to the nonvolatile bits in the STATUS register, operate normally. If the WPEN bit is set, $\overline{WP}$ low during a STATUS register write sequence will disable writing to the STATUS register. If an internal write cycle has already begun, $\overline{WP}$ going low will have no effect on the write. The $\overline{WP}$ pin function is blocked when the WPEN bit in the STATUS register is low. This allows the user to install the 25XX256 in a system with $\overline{WP}$ pin grounded and still be able to write to the STATUS register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set high.

### 2.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data are latched on the rising edge of the serial clock.

### 2.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a host and the 25XX256. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

### 2.6 Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the 25XX256 while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-to-low transition. The 25XX256 must remain selected during this sequence. The SI and SCK levels are "don't cares" during the time the device is paused and any transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not be resumed until the next SCK high-to-low transition.

The SO line will tri-state immediately upon a high-to-low transition of the HOLD pin and will begin outputting again immediately upon a subsequent low-to-high transition of the HOLD pin, independent of the state of SCK.

## 3.0 FUNCTIONAL DESCRIPTION

### 3.1 Principles of Operation

The 25XX256 is a 32,768-byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular micro controller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in firmware to match the SPI protocol.

The 25XX256 contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses and data are transferred MSb first, LSb last.

Data (SI) are sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input and place the 25XX256 in HOLD mode. After releasing the $\overline{HOLD}$ pin, operation will resume from the point when the $\overline{HOLD}$ was asserted.

**BLOCK DIAGRAM**

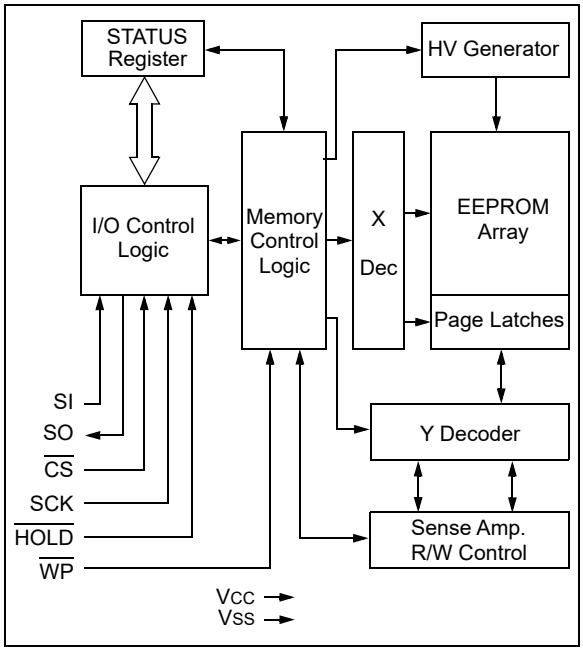



**TABLE 3-1: INSTRUCTION SET**

| Instruction Name | Instruction Format | Description |
|---|---|---|
| READ | 0000 0011 | Read data from memory array beginning at selected address |
| WRITE | 0000 0010 | Write data to memory array beginning at selected address |
| WRDI | 0000 0100 | Reset the write enable latch (disable write operations) |
| WREN | 0000 0110 | Set the write enable latch (enable write operations) |
| RDSR | 0000 0101 | Read STATUS register |
| WRSR | 0000 0001 | Write STATUS register |

## 3.2 Read Sequence

The device is selected by pulling $\overline{CS}$ low. The 8-bit READ instruction is transmitted to the 25XX256 followed by the 16-bit address, with the first MSb of the address being a “don’t care” bit. After the correct READ instruction and address are sent, the data stored in the memory at the selected address are shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (7FFFh), the address counter rolls over to address 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin (Figure 3-1).

## 3.3 Write Sequence

Prior to any attempt to write data to the 25XX256, the write enable latch must be set by issuing the WREN instruction (Figure 3-4). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25XX256. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

Once the write enable latch is set, the user may proceed by setting the $\overline{CS}$ low, issuing a WRITE instruction, followed by the 16-bit address, with the first MSb of the address being a “don’t care” bit and then the data to be written. Up to 64 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page.

| | |
|---|---|
| **Note:** | Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or ‘page size’) and, end at addresses that are integer multiples of page size – 1. If a page write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary. |

For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the Least Significant bit (D0) of the $n^{th}$ data byte has been clocked in. If $\overline{CS}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 3-2 and Figure 3-3 for more detailed illustrations on the byte write sequence and the page write sequence, respectively. While the write is in progress, the STATUS register may be read to check the status of the Write-In-Process (WIP) bit (Figure 3-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

**FIGURE 3-1: READ SEQUENCE**

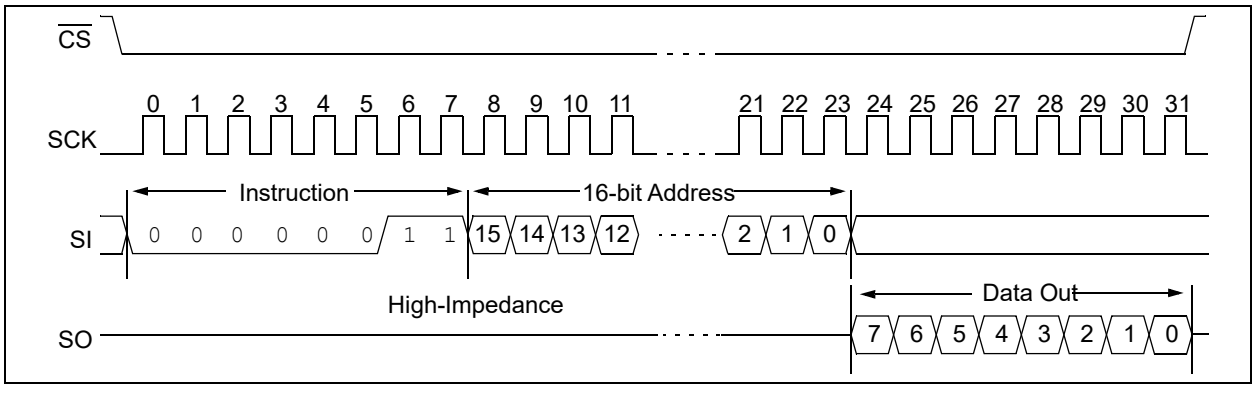
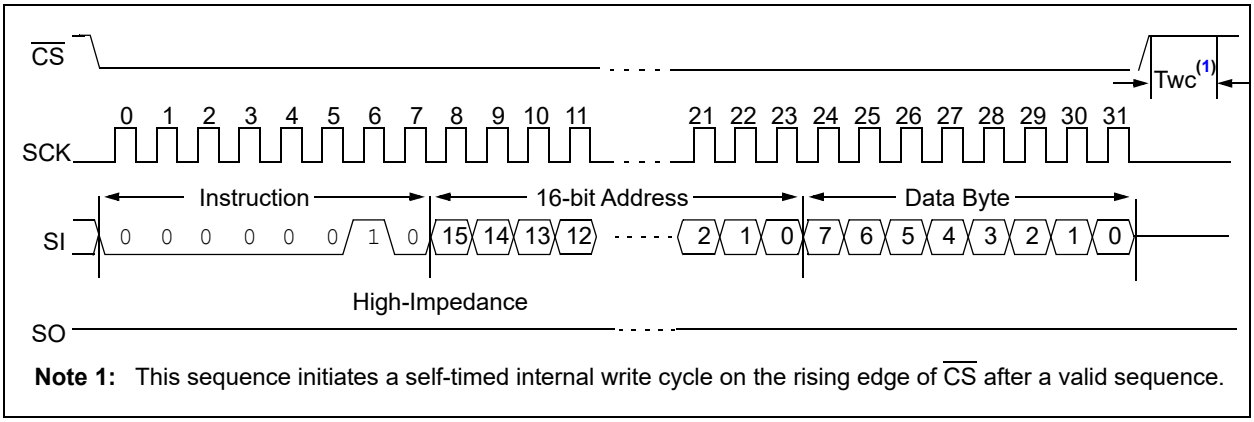
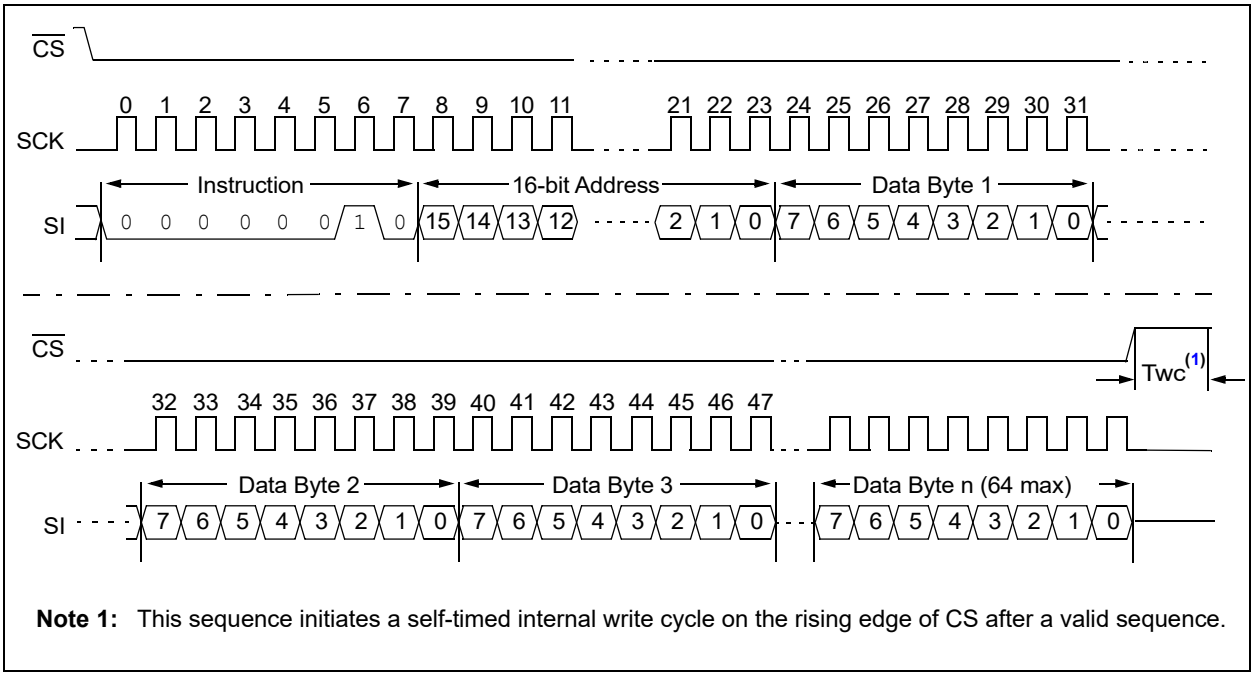


**FIGURE 3-2: BYTE WRITE SEQUENCE**




**Note 1:** This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

**FIGURE 3-3: PAGE WRITE SEQUENCE**




**Note 1:** This sequence initiates a self-timed internal write cycle on the rising edge of CS after a valid sequence.

### 3.4 Write Enable (WREN) and Write Disable (WRDI)

The 25XX256 contains a write enable latch. See Table 5-1 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed

**FIGURE 3-4: WRITE ENABLE SEQUENCE (WREN)**

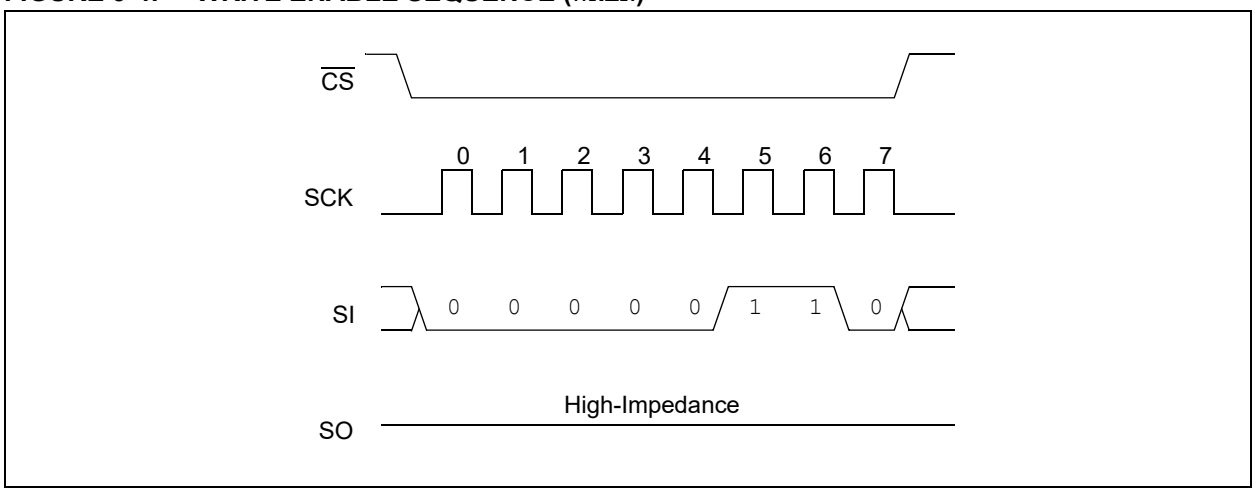
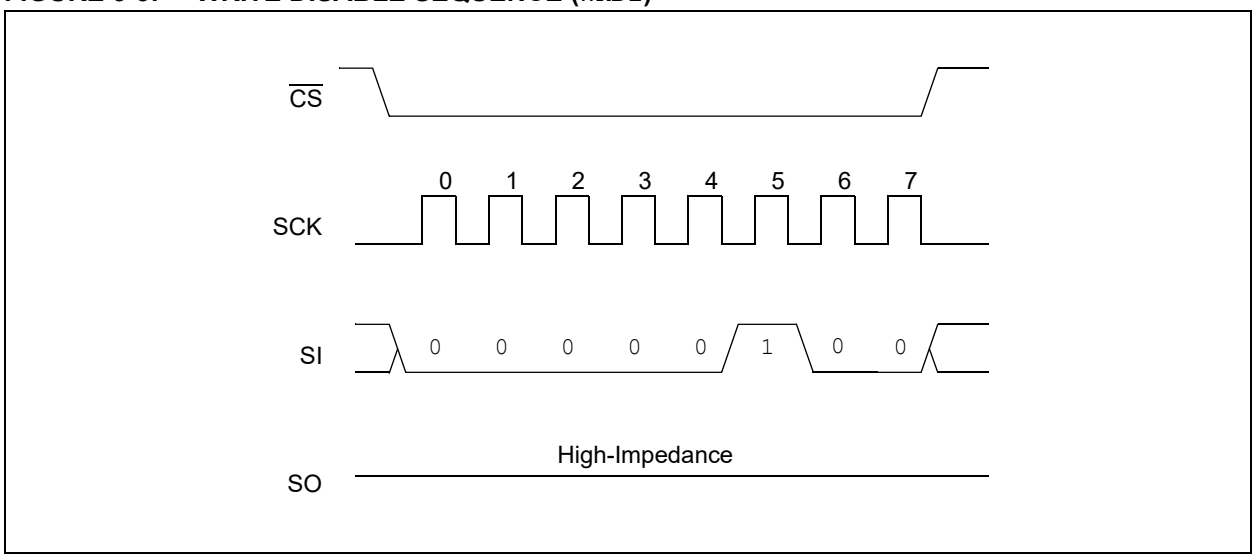



**FIGURE 3-5: WRITE DISABLE SEQUENCE (WRDI)**



## 3.5 Read STATUS Register Instruction (RDSR)

The Read STATUS Register instruction (RDSR) pr ovides access to the STATUS register. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

**TABLE 3-2: STATUS REGISTER**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| W/R | - | - | - | W/R | W/R | R | R |
| WPEN | x | x | x | BP1 | BP0 | WEL | WIP |

**Note 1:** W/R = writable/readable. R = read-only.

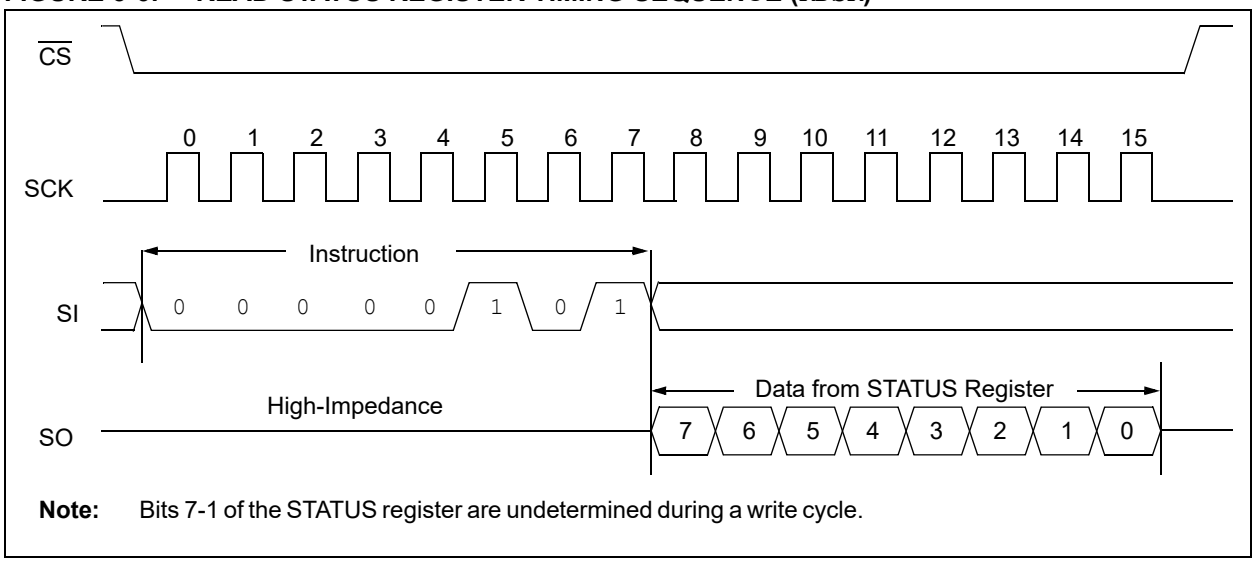
The **Write-In-Process (WIP)** bit indicates whether the 25XX256 is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the STATUS of the write enable latch and is read-only. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands, regardless of the state of write protection on the STATUS register. These commands are shown in Figure 3-4 and Figure 3-5.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the WRSR instruction. These bits are nonvolatile and are shown in Table 3-3.

See Figure 3-6 for the RDSR timing sequence.

**FIGURE 3-6: READ STATUS REGISTER TIMING SEQUENCE (RDSR)**




**Note:** Bits 7-1 of the STATUS register are undetermined during a write cycle.

## 3.6 Write STATUS Register Instruction (WRSR)

The Write STATUS Register instruction (WRSR) allows the user to write to the nonvolatile bits in the STATUS register as shown in Table 3-2. The user is able to select one of four levels of protection for the array by writing to the appropriate bits in the STATUS register. The array is divided up into four segments. The user has the ability to write-protect none, one, two or all four of the segments of the array. The partitioning is controlled as shown in Table 3-3.

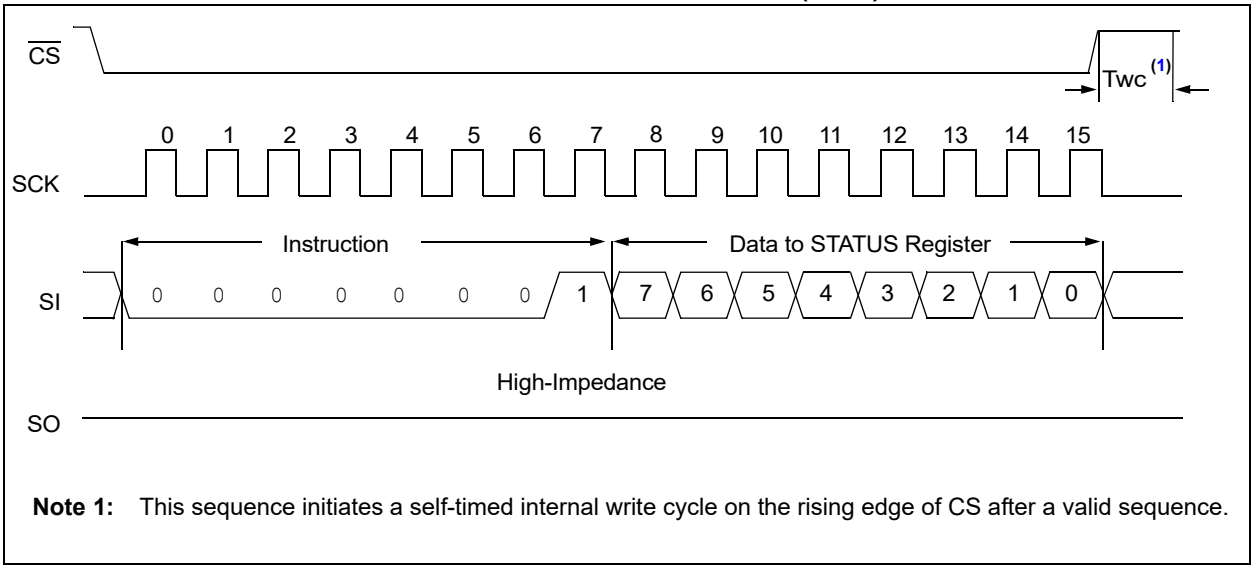
The Write-Protect Enable (WPEN) bit is a nonvolatile bit that is available as an enable bit for the $\overline{WP}$ pin. The Write-Protect ($\overline{WP}$) pin and the Write-Protect Enable (WPEN) bit in the STATUS register control the programmable hardware write-protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is low and the WPEN bit is high. Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is low. When the chip is hardware Write-Protected, only writes to nonvolatile bits in the STATUS register are disabled. See Table 5-1 for a matrix of functionality on the WPEN bit.

See Figure 3-7 for the WRSR timing sequence.

**TABLE 3-3: ARRAY PROTECTION**

| BP1 | BP0 | Array Addresses Write Protected |
|---|---|---|
| 0 | 0 | none |
| 0 | 1 | upper 1/4 (6000h-7FFFh) |
| 1 | 0 | upper 1/2 (4000h-7FFFh) |
| 1 | 1 | all (0000h-7FFFh) |

**FIGURE 3-7: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)**




**Note 1:** This sequence initiates a self-timed internal write cycle on the rising edge of CS after a valid sequence.

## 4.0 DATA PROTECTION

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or STATUS register write, the write enable latch is reset
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

## 5.0 POWER-ON STATE

The 25XX256 powers on in the following state:

- The device is in low-power Standby Mode ($\overline{CS}$ = 1)
- The write enable latch is reset
- SO is in high-impedance state
- A high-to-low-level transition on $\overline{cs}$ is required to enter active state

**TABLE 5-1: WRITE-PROTECT FUNCTIONALITY MATRIX**

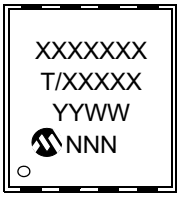
| WEL (SR bit 1) | WPEN (SR bit 7) | $\overline{WP}$ pin | Protected Blocks | Unprotected Blocks | STATUS Register |
|---|---|---|---|---|---|
| 0 | x | x | Protected | Protected | Protected |
| 1 | 0 | x | Protected | Writable | Writable |
| 1 | 1 | 0 (low) | Protected | Writable | Protected |
| 1 | 1 | 1 (high) | Protected | Writable | Writable |

**Note 1:** x = don't care

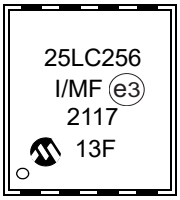
## 6.0 PACKAGING INFORMATION

### 6.1 Package Marking Information

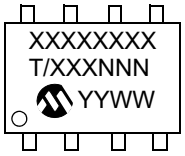
8-Lead DFN-S



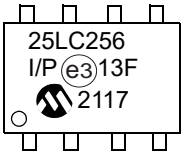

Example



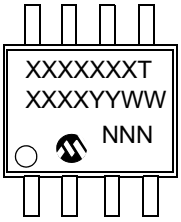

8-Lead PDIP



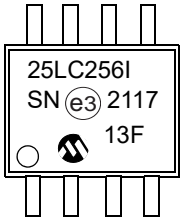

Example



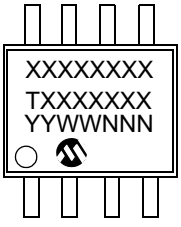

8-Lead SOIC



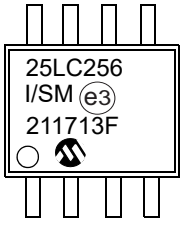

Example




8-Lead SOIJ




Example




8-Lead TSSOP


Example

| 1st Line Marking Codes | | | | | | |
|---|---|---|---|---|---|---|
| **Device** | **DFN-S** | **PDIP** | **SOIC** | **SOIJ** | **TSSOP** | **Rotated TSSOP** |
| 25AA256 | 25AA256 | 25AA256 | 25AA256T | 25AA256 | 5AE | 5AEX |
| 25LC256 | 25LC256 | 25LC256 | 25LC256T | 25LC256 | 5LE | 5LEX |

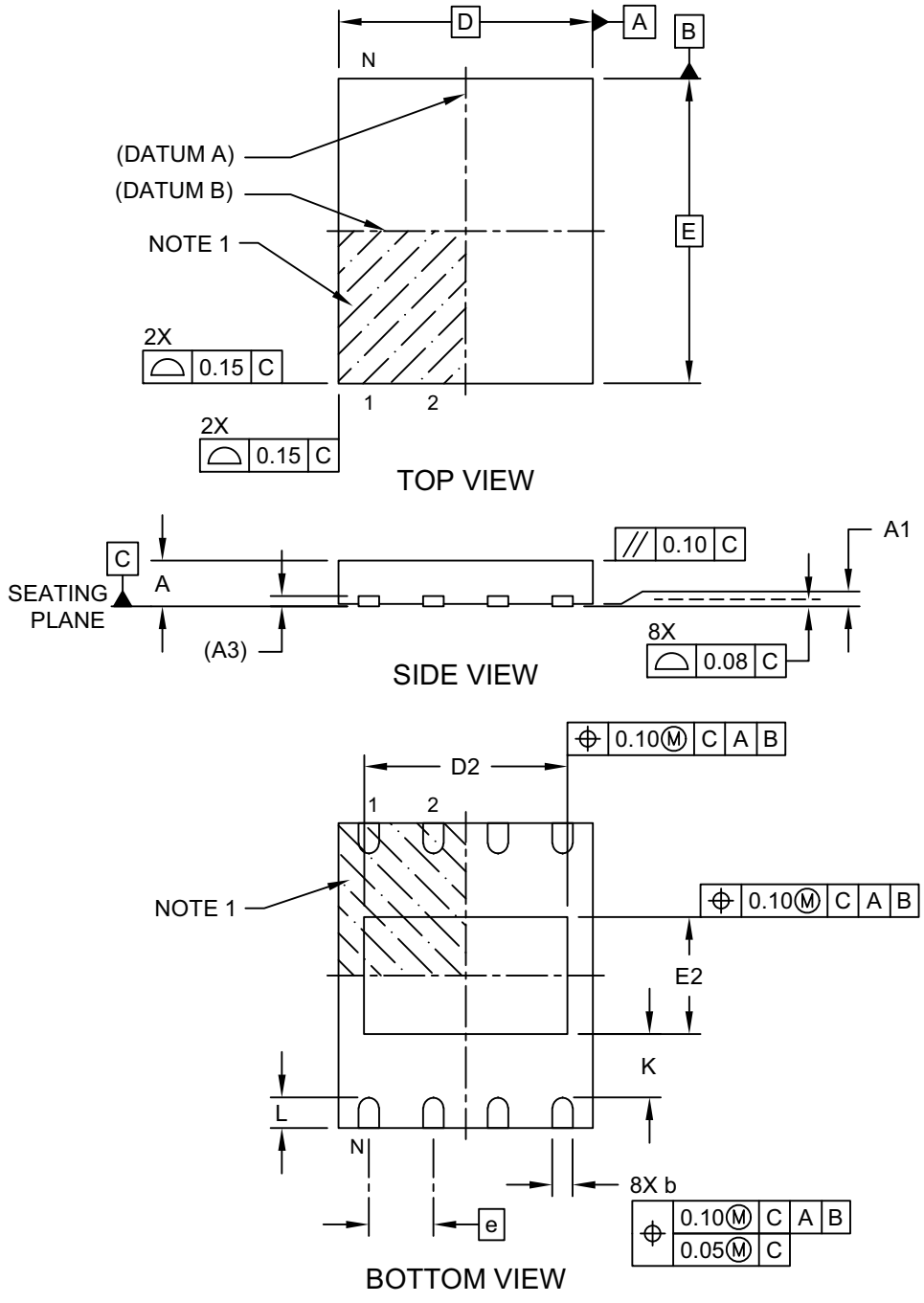
| | | |
|---|---|---|
| **Legend:** | XX...X | Part number or part number code |
| | T | Temperature (I, E) |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code (2 characters for small packages) |
| | (e3) | RoHS-compliant JEDEC designator for Matte Tin (Sn) |

**Note**: For very small packages with no room for the RoHS-compliant JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

### 8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

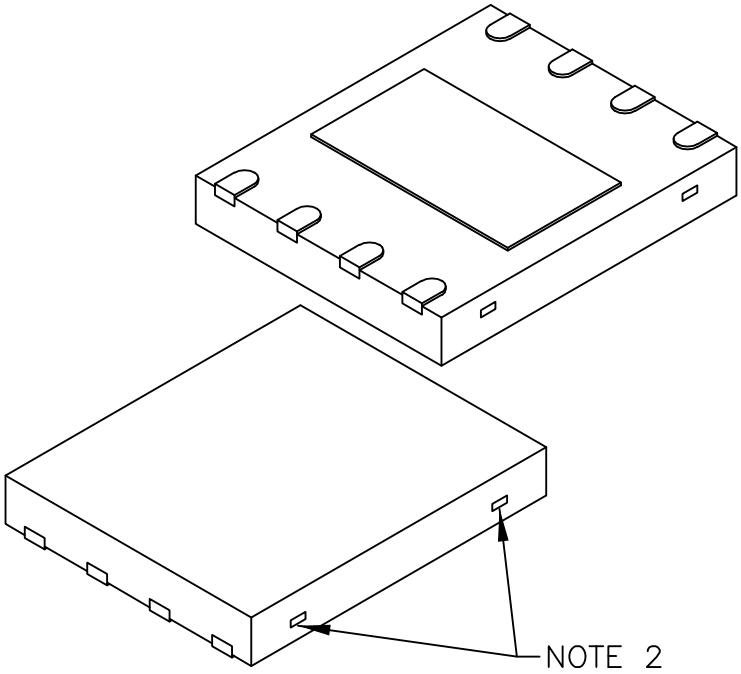
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-122 Rev C Sheet 1 of 2

## 8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | 0.80 | 0.85 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 5.00 BSC | |
| Exposed Pad Length | D2 | 3.90 | 4.00 | 4.10 |
| Overall Width | E | | 6.00 BSC | |
| Exposed Pad Width | E2 | 2.20 | 2.30 | 2.40 |
| Terminal Width | b | 0.30 | 0.40 | 0.50 |
| Terminal Length | L | 0.50 | 0.60 | 0.75 |
| Terminal-to-Exposed-Pad | K | 0.20 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one ore more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

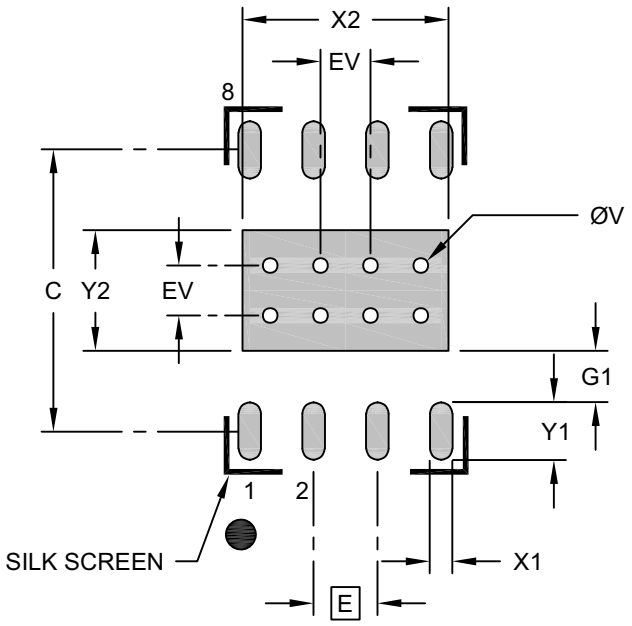
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-122 Rev C Sheet 2 of 2

### 8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Optional Center Pad Width | X2 | | | 2.40 |
| Optional Center Pad Length | Y2 | | | 4.10 |
| Contact Pad Spacing | C | | 5.60 | |
| Contact Pad Width (X20) | X1 | | | 0.45 |
| Contact Pad Length (X20) | Y1 | | | 1.15 |
| Contact Pad to Center Pad (X20) | G1 | 0.20 | | |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

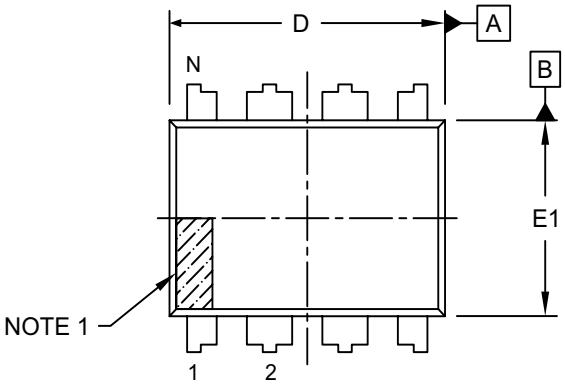
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

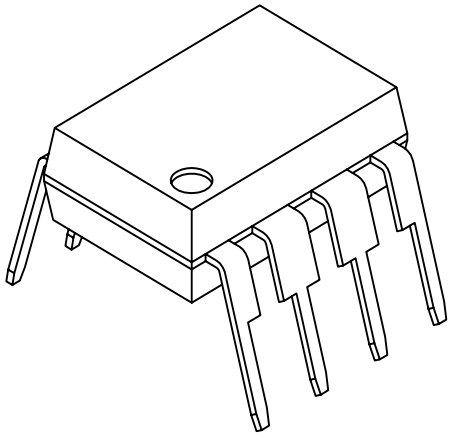
Microchip Technology Drawing C04-2122 Rev C

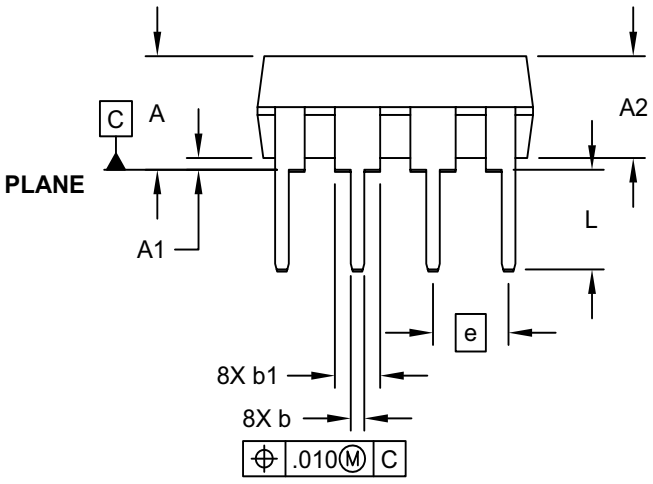
### 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

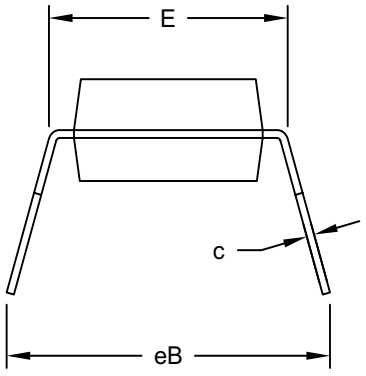



TOP VIEW






SIDE VIEW

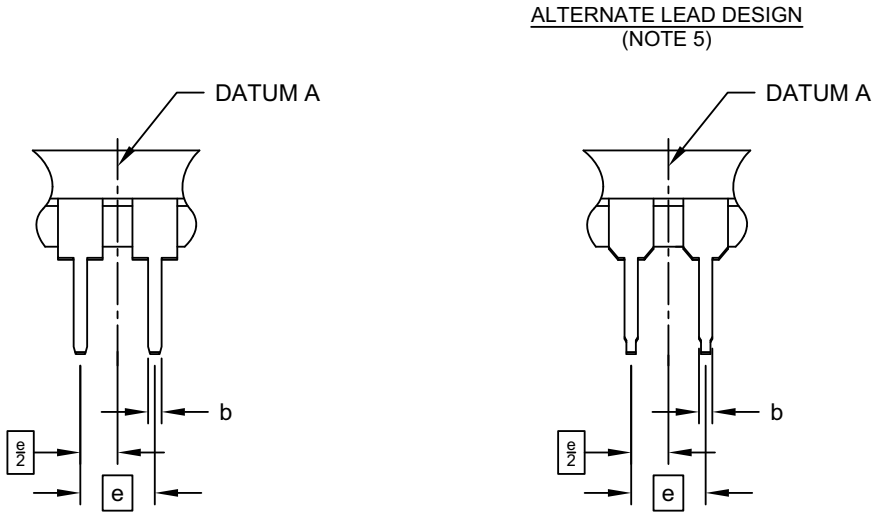



END VIEW

Microchip Technology Drawing No. C04-018-P Rev E Sheet 1 of 2

### 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | - | - | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | - | - |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | - | - | .430 |

Notes:

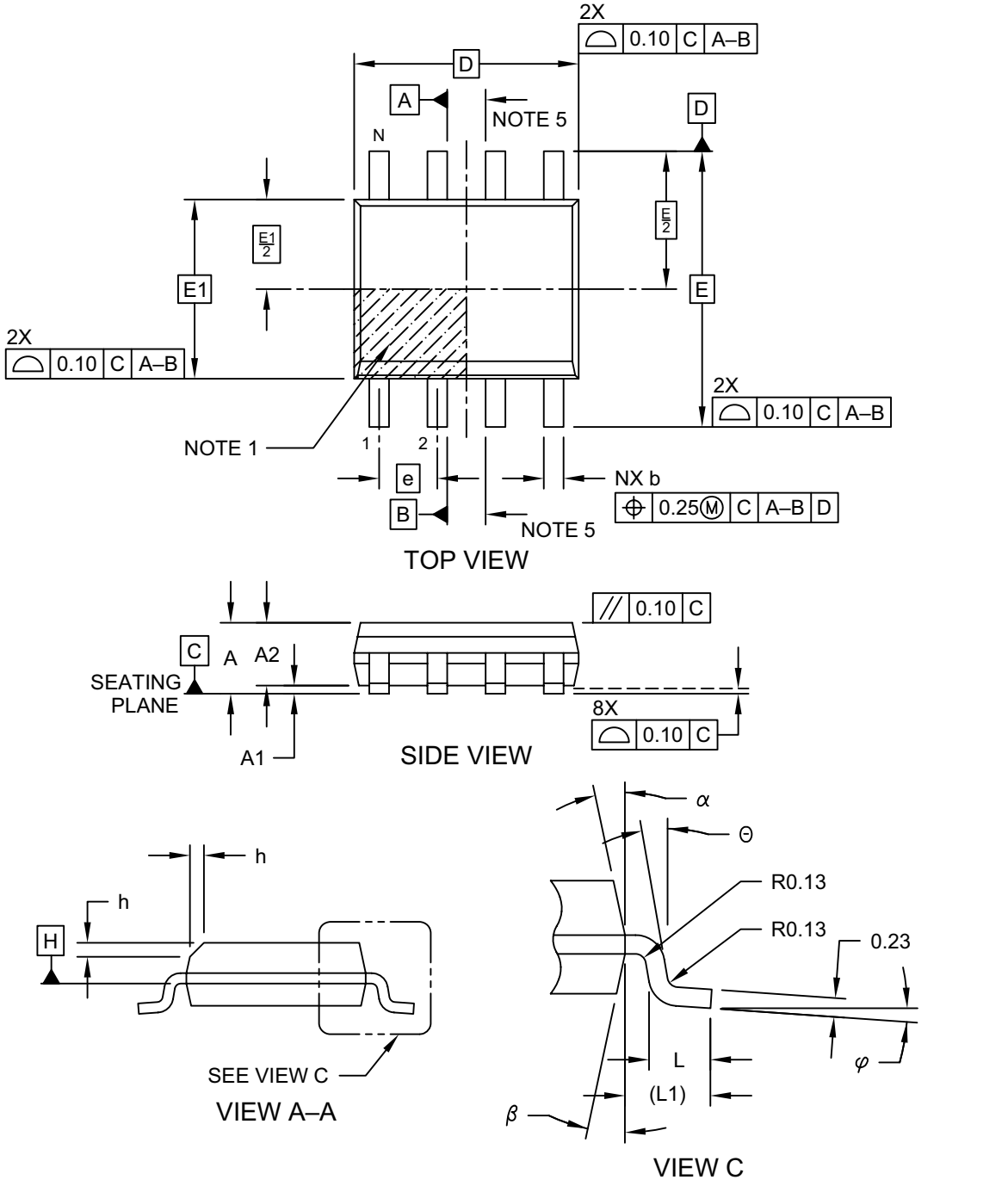
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev E Sheet 2 of 2

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

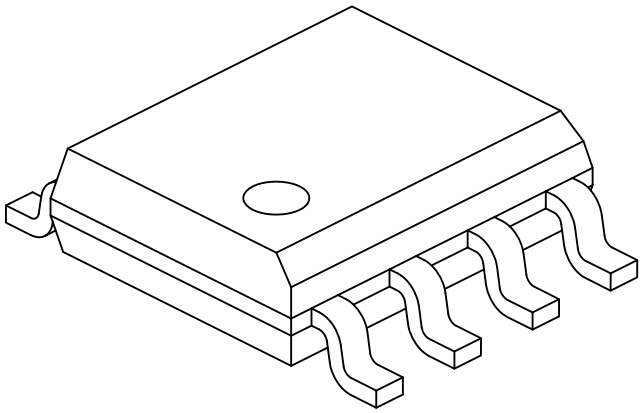
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing No. C04-057-SN Rev F Sheet 1 of 2

### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | - | - | 1.75 |
| Molded Package Thickness | A2 | 1.25 | - | - |
| Standoff § | A1 | 0.10 | - | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (Optional) | h | 0.25 | - | 0.50 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Foot Angle | $\varphi$ | 0° | - | 8° |
| Lead Thickness | c | 0.17 | - | 0.25 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | $\alpha$ | 5° | - | 15° |
| Mold Draft Angle Bottom | $\beta$ | 5° | - | 15° |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

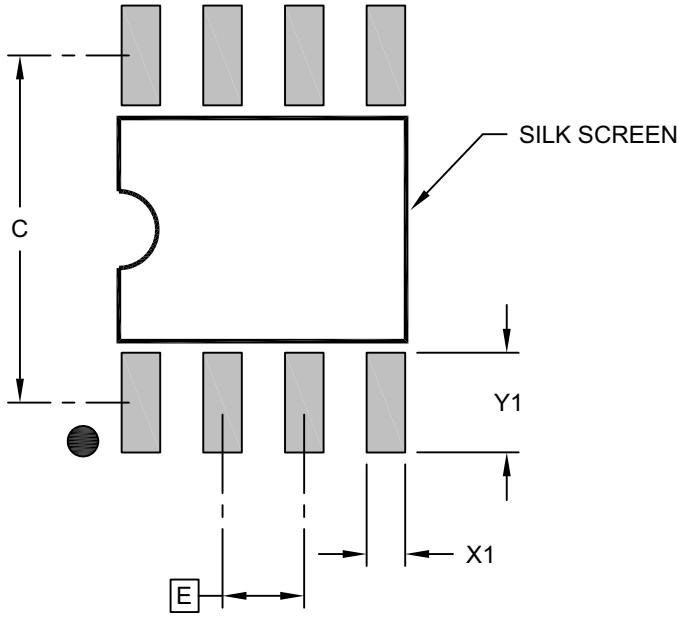
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev F Sheet 2 of 2

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

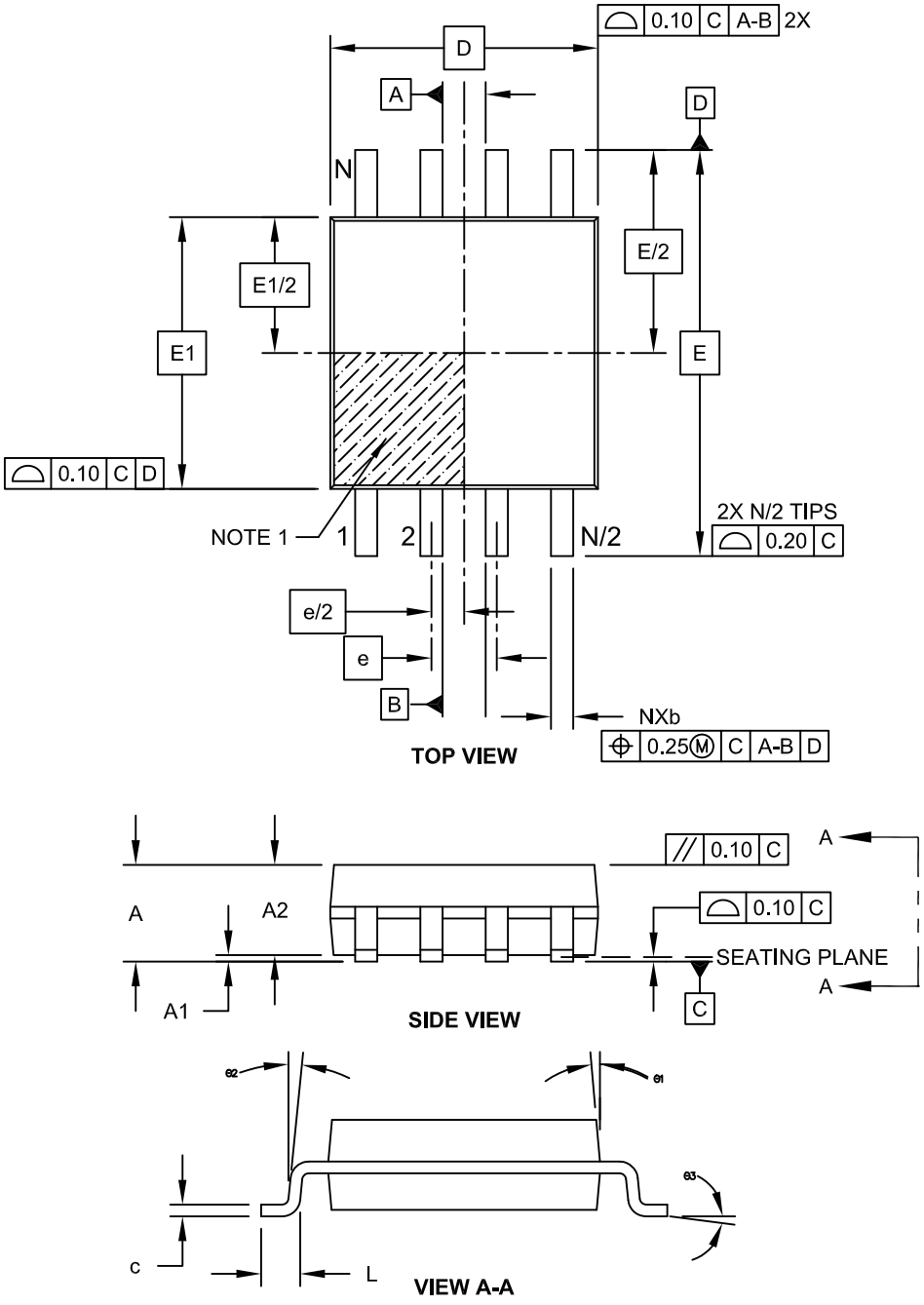
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev F

### 8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

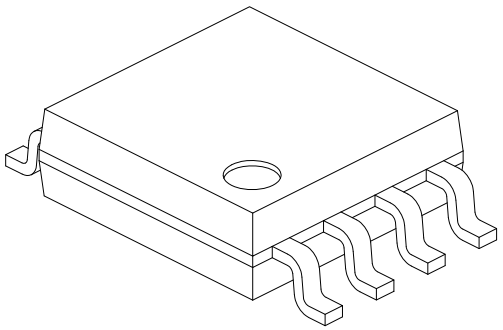
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-056C Sheet 1 of 2

### 8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | 1.77 | - | 2.03 |
| Standoff § | A1 | 0.05 | | 0.25 |
| Molded Package Thickness | A2 | 1.75 | - | 1.98 |
| Overall Width | E | | 7.94 BSC | |
| Molded Package Width | E1 | | 5.25 BSC | |
| Overall Length | D | | 5.26 BSC | |
| Foot Length | L | 0.51 | - | 0.76 |
| Lead Thickness | c | 0.15 | - | 0.25 |
| Lead Width | b | 0.36 | - | 0.51 |
| Mold Draft Angle | Θ1 | - | - | 15° |
| Lead Angle | Θ2 | 0° | - | 8° |
| Foot Angle | Θ3 | 0° | - | 8° |

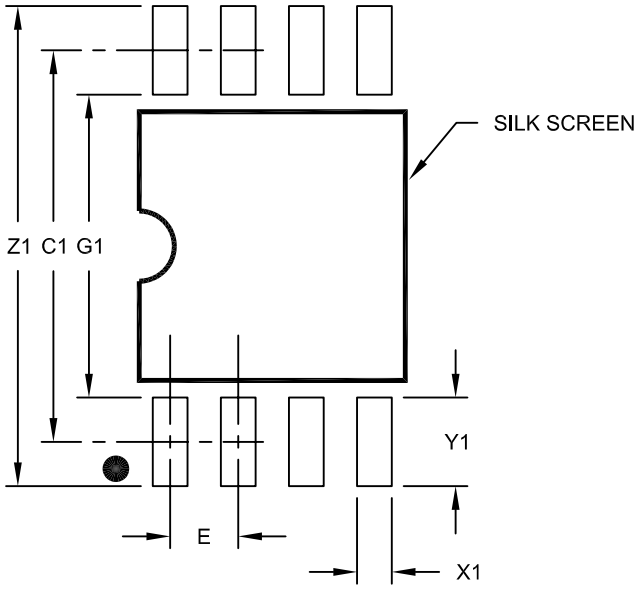
Notes:

1. SOIJ, JEITA/EIAJ Standard, Formerly called SOIC
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.

Microchip Technology Drawing No. C04-056C Sheet 2 of 2

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Overall Width | Z1 | | | 9.00 |
| Contact Pad Spacing | C1 | | 7.30 | |
| Contact Pad Width (X8) | X1 | | | 0.65 |
| Contact Pad Length (X8) | Y1 | | | 1.70 |
| Distance Between Pads | G1 | 5.60 | | |
| Distance Between Pads | G | 0.62 | | |

Notes:

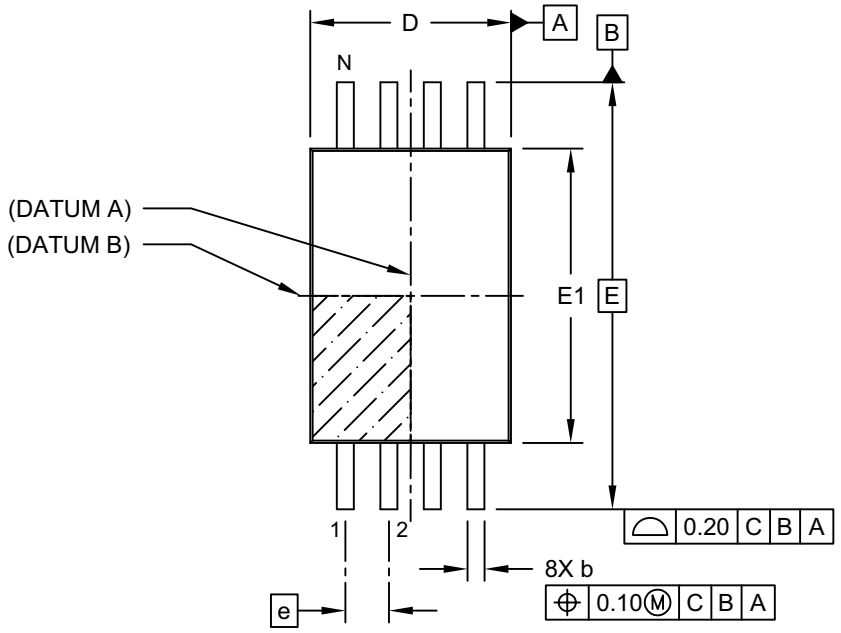
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

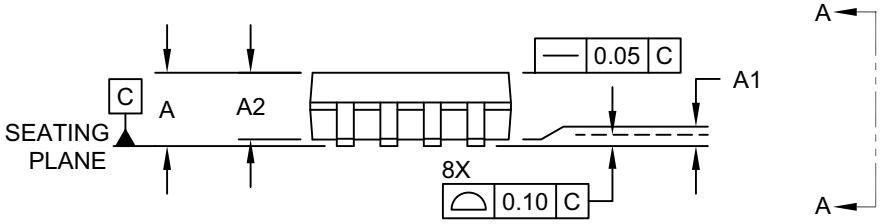
Microchip Technology Drawing No. C04-2056C

## 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

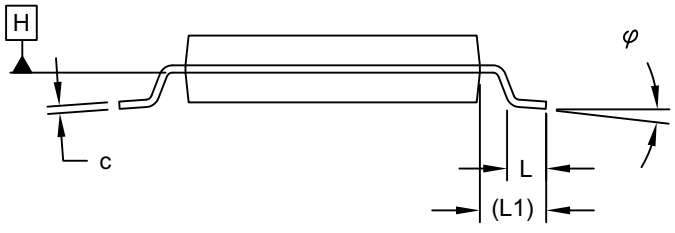
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW

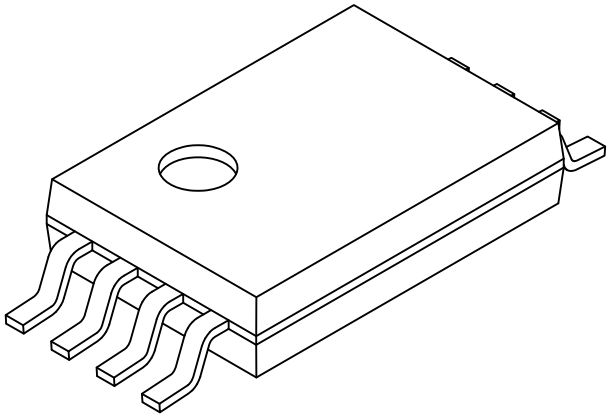



VIEW A-A

Microchip Technology Drawing C04-086 Rev C Sheet 1 of 2

### 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | - | - | 1.20 |
| Molded Package Thickness | A2 | 0.80 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | - | - |
| Overall Width | E | | 6.40 BSC | |
| Molded Package Width | E1 | 4.30 | 4.40 | 4.50 |
| Overall Length | D | 2.90 | 3.00 | 3.10 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Lead Thickness | c | 0.09 | - | 0.25 |
| Foot Angle | φ | 0° | 4° | 8° |
| Lead Width | b | 0.19 | - | 0.30 |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

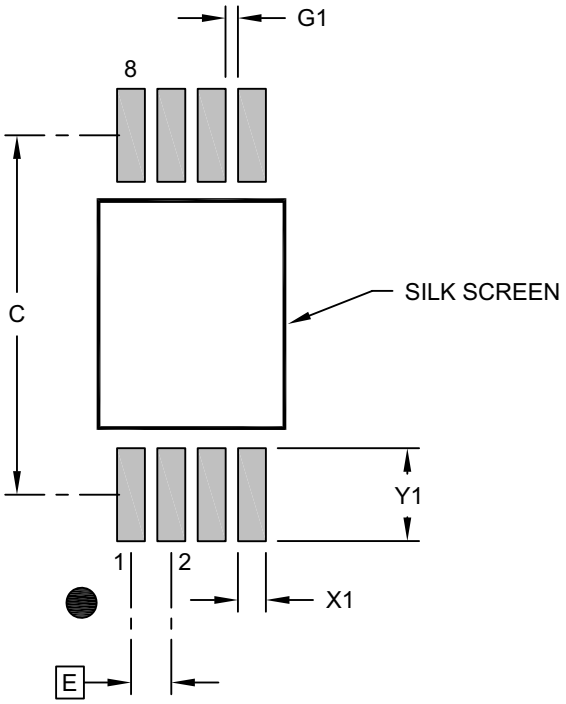
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086 Rev C Sheet 2 of 2

## 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C | | 5.80 | |
| Contact Pad Width (X8) | X1 | | | 0.45 |
| Contact Pad Length (X8) | Y1 | | | 1.50 |
| Contact Pad to Center Pad (X6) | G1 | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2086 Rev B

## APPENDIX A: REVISION HISTORY

### Revision J (07/2021)

Added Automotive Product ID section; Replaced “master” and “slave” terminology with “host” and “client”, respectively; Updated DFN-S, SOIC and TSSOP package drawings; Reformatted some sections for better readability.

### Revision H (08/2019)

Revise Product ID System, packages and notes; Clarified Extended E-Temp description; Update RoHS compliant description; Update PDIP package drawing.

### Revision G (01/2013)

Revise Automotive E Temp; Revise Table 1-2, Param. No. 21.

### Revision F (05/07)

Update Pb-free; Replace Package Drawings (Rev. AP); Update Product ID section.

### Revision E (08/05)

Remove Preliminary status. Revise Table 1-1, Params. D011 and D012.

### Revision D (06/05)

Update package information

### Revision C (11/03)

Corrections to Section 1.0, Electrical Characteristics.

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## PRODUCT IDENTIFICATION SYSTEM (NON-AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | [X] (1) | -X | /XX |
|---|---|---|---|
| Device | Tape and Reel Option | Temperature Range | Package |

| | | |
|---|---|---|
| **Device:** | 25AA256: | 256 Kbit, 1.8V, 64-Byte Page, SPI Serial EEPROM |
| | 25LC256: | 256 Kbit, 2.5V, 64-Byte Page, SPI Serial EEPROM |
| | 25AA256X: | 256 Kbit, 1.8V, 64-Byte Page, SPI Serial EEPROM, in alternate pinout (ST only) |
| | 25LC256X: | 256 Kbit, 2.5V, 64-Byte Page, SPI Serial EEPROM, in alternate pinout (ST only) |
| **Tape and Reel Option:** | Blank = | Standard packaging (tube) |
| | T = | Tape and Reel(1) |
| **Temperature Range:** | I = | -40°C to +85°C (Industrial) |
| | E = | -40°C to +125°C (Extended) |
| **Package:** | MF = | Plastic Micro Lead Frame (6 x 5 mm body), 8-lead (DFN-S) |
| | P = | Plastic Dual In-Line - 300 mil Body, 8-lead (PDIP) |
| | SN = | Plastic Small Outline - Narrow, 3.90 mm Body, 8-lead (SOIC) |
| | SM = | Plastic Small Outline - Wide, 5.28 mm Body, 8-lead (SOIJ) |
| | ST = | Plastic Thin Shrink Small Outline - 4.4 mm, 8-lead (TSSOP) |

**Examples:**

a) 25AA256T-I/SN: 256 Kbit, 1.8V Serial EEPROM, Industrial temperature, Tape and Reel, SOIC package

b) 25AA256T-I/ST: 256 Kbit, 1.8V Serial EEPROM, Industrial temperature, Tape and Reel, TSSOP package

c) 25LC256-I/P: 256 Kbit, 2.5V Serial EEPROM, Industrial temperature, PDIP package

d) 25LC256T-E/ST: 256 Kbit, 2.5V Serial EEPROM, Extended temperature, Tape and Reel, TSSOP package

e) 25LC256XT-I/ST: 256 Kbit, 2.5V Serial EEPROM, Industrial temperature, Tape and Reel, Alternate pinout, TSSOP package

f) 25AA256T-E/SM: 256 Kbit, 1.8V Serial EEPROM, Extended temperature, Tape

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes only and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

## PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | [X](1) | -X | /XX | XXX (2,3) |
|---|---|---|---|---|
| Device | Tape and Reel Option | Temperature Range | Package | Variant |

| | | |
|---|---|---|
| **Device:** | 25AA256: | 256 Kbit, 1.8V, 64-Byte Page, SPI Serial EEPROM |
| | 25LC256: | 256 Kbit, 2.5V, 64-Byte Page, SPI Serial EEPROM |
| **Tape and Reel Option:** | Blank = | Standard packaging (tube) |
| | T = | Tape and Reel(1) |
| **Temperature Range:** | I = | -40°C to +85°C (AEC-Q100 Grade 3) |
| | E = | -40°C to +125°C (AEC-Q100 Grade 1) |
| **Package:** | SN = | Plastic Small Outline - Narrow, 3.90 mm Body, 8-lead (SOIC) |
| | SM = | Plastic Small Outline - Wide, 5.28 mm Body, 8-lead (SOIJ) |
| | ST = | Plastic Thin Shrink Small Outline - 4.4 mm, 8-lead (TSSOP) |
| **Variant(2,3):** | 16KVAO = | Standard Automotive, 16K Process |
| | 16KVXX = | Customer-Specific Automotive, 16K Process |

**Examples:**

a) 25AA256T-I/SN16KVAO: 256 Kbit, 1.8V Serial EEPROM, Automotive Grade 3, Tape and Reel, SOIC package

b) 25AA256T-I/ST16KVAO:, 256 Kbit, 1.8V Serial EEPROM, Automotive Grade 3, Tape and Reel, TSSOP package

c) 25LC256-E/SN16KVAO: 256 Kbit, 2.5V Serial EEPROM, Automotive Grade 1, SOIC package

d) 25LC256T-E/ST16KVAO: 256 Kbit, 2.5V Serial EEPROM, Automotive Grade 1, Tape and Reel, Rotated TSSOP package

e) 25LC256T-E/SM16KVAO: 256 Kbit, 2.5V Serial EEPROM, Automotive Grade 1, Tape and Reel, SOIJ package

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes only and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**2:** The VAO/VXX automotive variants have been designed, manufactured, tested and qualified in accordance with AEC-Q100 requirements for automotive applications.

**3:** For customers requesting a PPAP, a customer-specific part will be generated and provided. A PPAP is not provided for VAO part numbers.

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