Poly-Phase High-Performance Wide-Span Energy Metering IC

90E36A

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Enabling Unlimited Possibilities®

Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**

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Poly-Phase High-Performance Wide-Span Energy Metering IC

90E36A

*Preliminary Information**

FEATURES

Metering Features

- Metering features fully in compliance with the requirements of IEC62052-11, IEC62053-22 and IEC62053-23, ANSI C12.1 and ANSI C12.20; applicable in class 0.5S or class 1 poly-phase watt-hour meter or class 2 poly-phase var-hour meter.
- Accuracy of ±0.1% for active energy and ±0.2% for reactive energy over the dynamic range of 6000:1.
- Temperature coefficient is 6 ppm/°C (typical) for on-chip reference voltage.
- Single-point calibration on each phase over the whole dynamic range for active energy; no calibration needed for reactive/ apparent energy.
- ±1°C (typical) temperature sensor accuracy.
- Electrical parameters measurement: less than ±0.5% fiducial error for Vrms, Irms, mean active/ reactive/ apparent power, frequency, power factor and phase angle.
- Active (forward/reverse), reactive (forward/reverse), apparent energy with independent energy registers. Active/ reactive/ apparent energy can be output by pulse or read through energy registers to adapt to different applications.
- Programmable startup and no-load power threshold, special designed of startup and no-load circuits to eliminate crosstalk among phases achieving better accuracy especially at low power conditions.
- Dedicated ADC and different gains for phase A/B/C and Neutral line current sampling circuits. Current sampled over current transformer (CT) or Rogowski coil (di/dt coil); phase A/B/C voltage sampled over resistor divider network or potential transformer (PT).
- Programmable power modes: Normal mode (N mode), Idle mode (I mode), Detection mode (D mode) and Partial Measurement mode (M mode).
- Fundamental (CF3, 0.2%) and harmonic (CF4, 1%) active energy with dedicated energy and power registers.
- Total Harmonic Distortion (THD) and Discrete Fourier Transform (DFT) functions for 2 ~ 32 order harmonic component. THD and DFT results available in SPI accessible registers. Both voltage and current of all phases processed within the same time period.
- Event detection: sag, phase loss, reverse voltage/ current phase sequence, reverse flow, calculated neutral line current I_{NC} overcurrent sampled neutral line current I_{NS} overcurrent and THD+N over-threshold.

Other Features

- 3.3V single power supply. Operating voltage range: 2.8V~3.6V. Metering accuracy guaranteed within 3.0V~3.6V.
- Four-wire SPI interface with Direct Memory Access (DMA) mode to stream out 7-channel ADC raw data.
- Parameter diagnosis function and programmable interrupt output of the IRQ interrupt signals and the WarnOut signal.
- Programmable voltage sag detection and zero-crossing output.
- CF1/CF2/CF3/CF4 output active/ reactive/ apparent energy pulses and fundamental/ harmonic energy pulses respectively.
- Crystal oscillator frequency: 16.384 MHz. On-chip two capacitors and no need of external capacitors.
- TQFP48 package.
- Operating temperature: -40°C ~ +85°C.

APPLICATION

- Poly-phase energy meters of class 0.5S and class 1 which are used in three-phase four-wire (3P4W, Y0) or three-phase three-wire (3P3W, Y or Δ) systems.
- Data Acquisition Terminal.
- Power monitoring instruments which need to measure voltage, current, THD, DFT, mean power, etc.

GENERAL DESCRIPTION

The 90E36A is a poly-phase high performance wide-dynamic range metering IC. The 90E36A incorporates 7 independent 2nd order sigma-delta ADCs, which could be employed in three voltage channels (phase A, B and C) and four current channels (phase A, B, C and neutral line) in a typical three-phase four-wire system.

The 90E36A has an embedded DSP which executes calculation of active energy, reactive energy, apparent energy, fundamental and harmonic active energy over ADC signal and on-chip reference voltage. The DSP also calculates measurement parameters such as voltage and current RMS value as well as mean active/reactive/apparent power.

A four-wire SPI interface is provided between the 90E36A and the external microcontroller. In addition, DMA mode can be used for 7-channel ADC raw data access, offering more flexibility in system application.

The 90E36A is suitable for poly-phase multi-function meters which could measure active/reactive/apparent energy and fundamental/harmonic energy either through four independent energy pulse outputs CF1/CF2/CF3/CF4 or through the corresponding registers.

With the on-chip THD and DFT engine, all phases' THD and DFT results can be directly accessed through related registers, thus simplifying hardware design in Data Acquisition Terminals.

The ADC and auto-temperature compensation technology for reference voltage ensure the 90E36A's long-term stability over variations in grid and ambient environment conditions.

BLOCK DIAGRAM

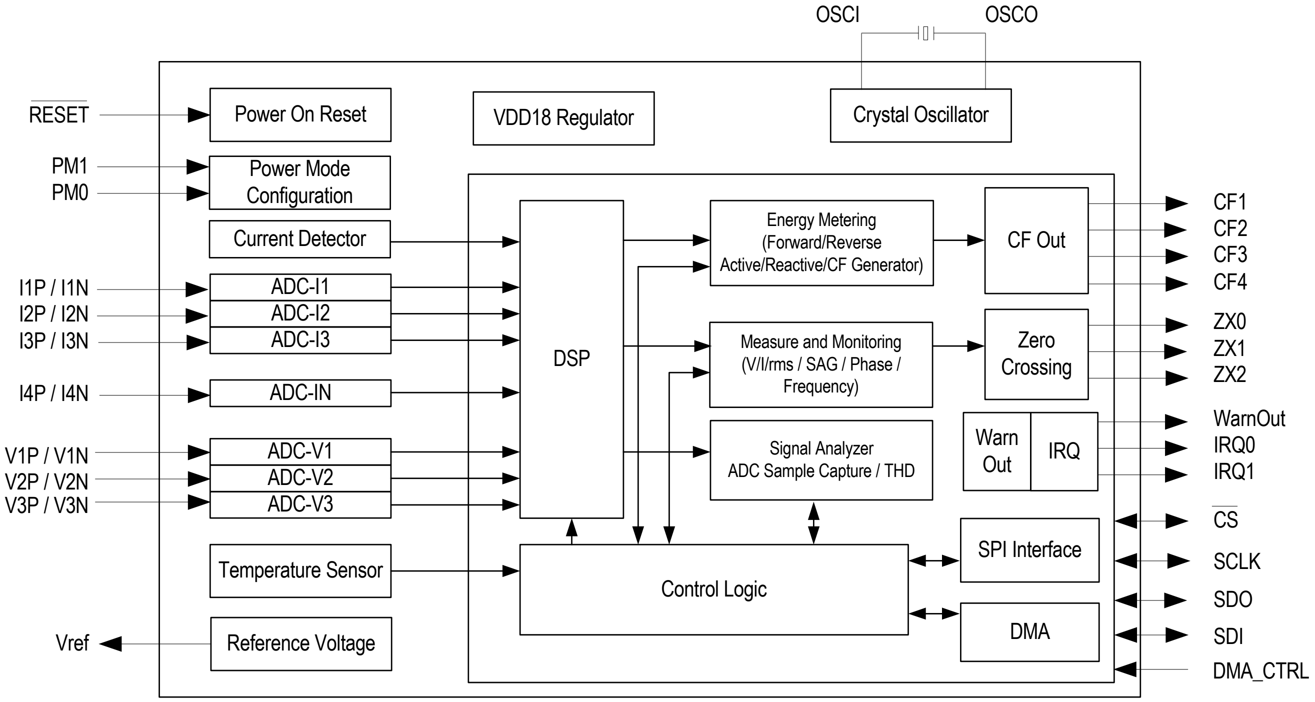


Figure-1 90E36A Block Diagram

1 PIN ASSIGNMENT

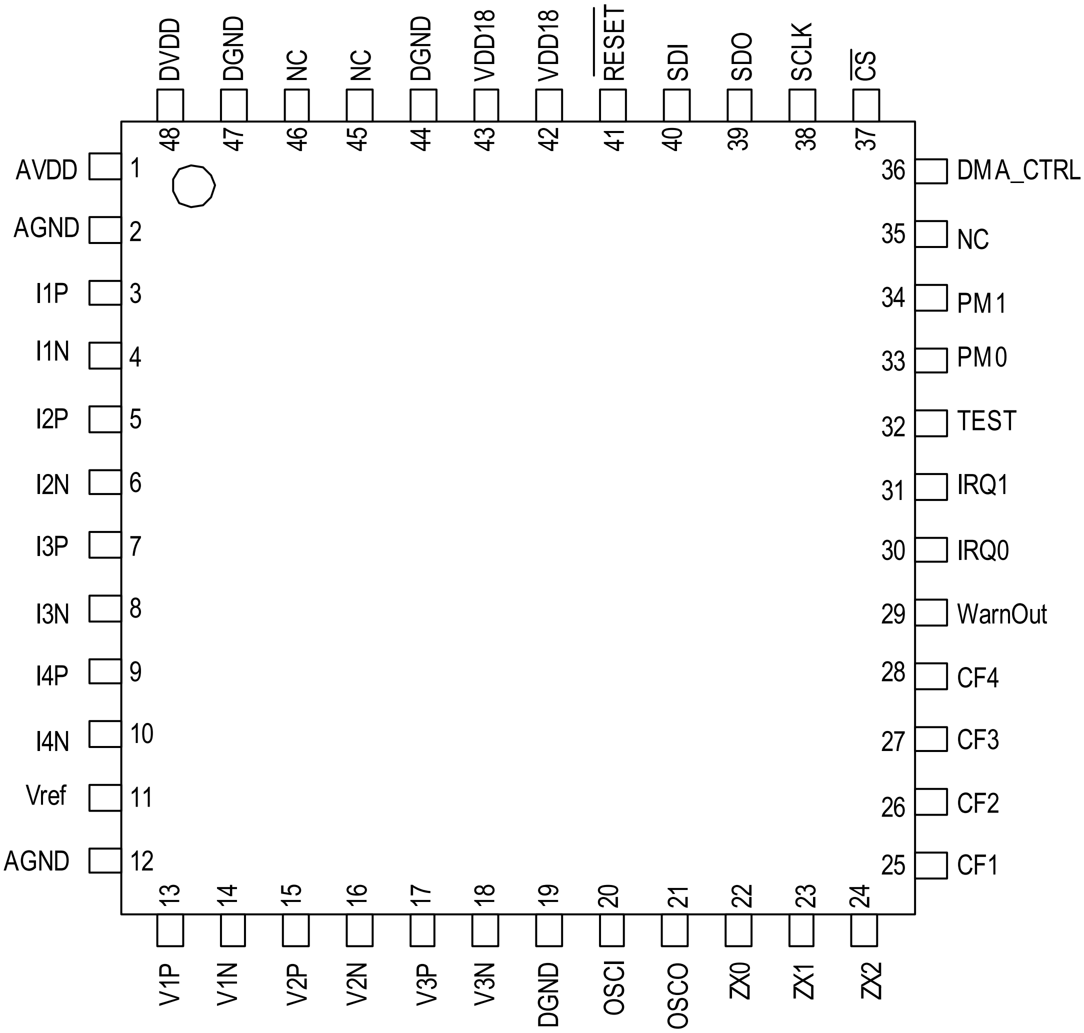


Figure-2 Pin Assignment (Top View)

2 PIN DESCRIPTION

Table-1 Pin Description

Name	Pin No.	I/O	Type	Description
$\overline{\text{Reset}}$	41	I	LVTTL	**$\overline{\text{Reset}}$: Reset Pin (active low)** This pin should connect to ground through a 0.1 µF filter capacitor and a 10kΩ resistor to VDD. In application it can also directly connect to one output pin from microcontroller (MCU).
AVDD	1	I	Power	**AVDD: Analog Power Supply** This pin provides power supply to the analog part. This pin should connect to DVDD and be decoupled with a 0.1µF capacitor.
DVDD	48	I	Power	**DVDD: Digital Power Supply** This pin provides power supply to the digital part. It should be decoupled with a 10µF capacitor and a 0.1µF capacitor.
VDD18	42, 43	P	Power	**VDD18: Digital Power Supply (1.8 V)** These two pins should be connected together and connected to ground through a 10µF capacitor.
DGND	19, 44, 47	I	Power	**DGND: Digital Ground**
AGND	2, 12	I	Power	**AGND: Analog Ground**
I1P I1N	3 4	I	Analog	**I1P: Positive Input for Phase A Current** **I1N: Negative Input for Phase A Current** These pins are differential inputs for phase A current. Note: I1 to phase A and I3 to phase C mapping can be swapped by configuring the I1I3Swap bit (b13, MMode0).
I2P I2N	5 6	I	Analog	**I2P: Positive Input for Phase B Current** **I2N: Negative Input for Phase B Current** These pins are differential inputs for phase B current.
I3P I3N	7 8	I	Analog	**I3P: Positive Input for Phase C Current** **I3N: Negative Input for Phase C Current** These pins are differential inputs for phase C current. Note: I1 to phase A and I3 to phase C mapping can be swapped by configuring the I1I3Swap bit (b13, MMode0).
I4P I4N	9 10	I	Analog	**I4P: Positive Input for N Line Current** **I4N: Negative Input for N Line Current** These pins are differential inputs for N line current.
Vref	11	O	Analog	**Vref: Output Pin for Reference Voltage** This pin should be decoupled with a 10µF capacitor, possibly a 0.1µF ceramic capacitor and a 1nF ceramic capacitor.
V1P V1N	13 14	I	Analog	**V1P: Positive Input for Phase A Voltage** **V1N: Negative Input for Phase A Voltage** These pins are differential inputs for phase A voltage.
V2P V2N	15 16	I	Analog	**V2P: Positive Input for Phase B Voltage** **V2N: Negative Input for Phase B Voltage** These pins are differential inputs for phase B voltage.
V3P V3N	17 18	I	Analog	**V3P: Positive Input for Phase C Voltage** **V3N: Negative Input for Phase C Voltage** These pins are differential inputs for phase C voltage.
OSCI	20	I	OSC	**OSCI: External Crystal Input** **OSCO: External Crystal Output** A 16.384 MHz crystal is connected between OSCI and OSCO. There are two on-chip capacitor, therefore no need of external capacitors.
OSCO	21	O	OSC	
ZX0 ZX1 ZX2	22 23 24	O	LVTTL	**ZX2/ZX1/ZX0:Zero-Crossing Output** These pins are asserted when voltage or current crosses zero. Zero-crossing mode can be configured by the ZXConfig register (07H).
CF1	25	O	LVTTL	**CF1: (all-phase-sum total) Active Energy Pulse Output**

Table-1 Pin Description (Continued)

Name	Pin No.	I/O	Type	Description
CF2	26	O	LVTTL	**CF2: (all-phase-sum total) Reactive/ Apparent Energy Pulse Output** The output of this pin is determined by the CF2varh bit (b7, MMode0) and the CF2ESV bit (b8, MMode0).
CF3	27	O	LVTTL	**CF3: (all-phase-sum total) Active Fundamental Energy Pulse Output**
CF4	28	O	LVTTL	**CF4: (all-phase-sum total) Active Harmonic Energy Pulse Output**
WarnOut	29	O	LVTTL	**WarnOut: Fatal Error Warning** This pin is asserted high when there is metering related parameter checksum error. Otherwise this pin stays low. Refer to 6.2.2 IRQ and WarnOut Signal Generation.
IRQ0	30	O	LVTTL	**IRQ0: Interrupt Output 0** This pin is asserted when one or more events in the SysStatus0 register (01H) occur. It is deasserted when there is no bit set in the SysStatus0 register (01H). In Detection mode, the IRQ0 is used to indicate the output of current detector. The IRQ0 state is cleared when entering or exiting Detection mode.
IRQ1	31	O	LVTTL	**IRQ1: Interrupt Output 1** This pin is asserted when one or more events in the SysStatus1 register (02H) occur. It is deasserted when there is no bit set in the SysStatus1 register (02H). In Detection mode, the IRQ1 is used to indicate the output of current detector. The IRQ1 state is cleared when entering or exiting Detection mode.
PM0 PM1	33 34	I	LVTTL	**PM1/0: Power Mode Configuration** These two pins define the power mode of 90E36A. Refer to Table-2.
DMA_CTRL	36	I	LVTTL	**DMA_CTRL: DMA Enable** DMA is started when this pin is asserted. DMA is stopped when this pin is deasserted. Refer to 4 SPI / DMA Interface.
$\overline{\text{CS}}$	37	B	LVTTL	**$\overline{\text{CS}}$: Chip Select (Active Low)** In SPI mode, this pin must be driven from high to low for each read/ write operation, and maintain low for the entire operation. In DMA mode, this pin is asserted during data transmission. Refer to 4 SPI / DMA Interface.
SCLK	38	B	LVTTL	**SCLK: Serial Clock** This pin is used as the clock for the SPI/DMA interface. Refer to 4 SPI / DMA Interface.
SDO	39	B	LVTTL	**SDO: Serial Data Output** This pin is used as the data output for the SPI mode and input for the DMA mode. Refer to 4 SPI / DMA Interface.
SDI	40	B	LVTTL	**SDI: Serial Data Input** This pin is used as the data input for the SPI mode and output for the DMA mode. Refer to 4 SPI / DMA Interface.
TEST	32	I	LVTTL	This pin should be always connected to DGND in system application.
NC	35, 45, 46			**NC: These pins should be left open.**

3 FUNCTION DESCRIPTION

3.1 POWER SUPPLY

The 90E36A works with single power rail 3.3V. An on-chip voltage regulator regulates the 1.8V voltage for the digital logic.

The regulated 1.8V power is connected to the VDD18 pin. It needs to be bypassed by an external capacitor.

The 90E36A has multiple power modes, in Idle and Detection modes the 1.8V power regulator is not turned on and the digital logic is not powered. When the logic is not powered, all the configured register values are not kept (all context lost) except for Detection mode related registers (10H~13H) for Detection mode configuration.

User has to re-configure the registers in Partial Measurement mode or Normal mode when transiting from Idle or Detection mode. Refer to 3.7 Power Mode for power mode details.

3.2 CLOCK

The 90E36A has an on-chip oscillator and can directly connect to an external crystal.

The OSCI pin can also be driven with a clock source.

The oscillator will be powered down in Idle and Detection power modes, as described in 3.7 Power Mode.

3.3 RESET

There are three reset sources for the 90E36A:

- $\overline{\text{RESET}}$ pin
- On-chip Power On Reset circuit
- Software Reset generated by the Software Reset register

3.3.1 $\overline{\text{RESET}}$ PIN

The $\overline{\text{RESET}}$ pin can be asserted to reset the 90E36A. The $\overline{\text{RESET}}$ pin has RC filter with typical time constant of 2µs in the I/O, as well as a 2µs (typical) de-glitch filter.

Any reset pulse that is shorter than 2µs can not reset the 90E36A.

3.3.2 POWER ON RESET (POR)

The POR circuit resets the 90E36A at power up.

POR circuit triggers reset when:

- DVDD power up, crossing the power-up threshold. Refer to Figure-20.
- VDD18 regulator changing from disable to enable, i.e. from Idle or Detection mode to Partial Measurement mode or Normal mode. Refer to Figure-19.

3.3.3 SOFTWARE RESET

Chip reset can be triggered by writing to the SoftReset register in Normal mode. The software reset is the same as the reset scope generated from the $\overline{\text{RESET}}$ pin or POR.

These three reset sources have the same reset scope.

All digital logics and registers, except for the Harmonic Ratio registers will be subject to reset. The Harmonic Ratio registers can not be reset.

- Interface logic: clock dividers
- Digital core/ logic: All registers except for the Harmonic Ratio registers and some other special registers, refer to 6.3.1 Detection Mode Registers.

3.4 METERING FUNCTION

The accumulated energy is converted to pulse frequency on the CF pins and stored in the corresponding energy registers. The 90E36A provides energy accumulation registers with 0.1 or 0.01 CF resolution. 0.01CF / 0.1CF setting is defined by the 001LSB bit (b9, MMode0).

3.4.1 THEORY OF ENERGY REGISTERS

The energy accumulation runs at 1 MHz clock rate, by accumulating the power value calculated by the DSP processor.

The power accumulation process is equivalent to digitally integrating the instantaneous power with a delta-time of about 1us. The accumulated energy is used to calculate the CF pulses and the corresponding internal energy registers.

The accumulated energy is converted to frequency of the CF pulses. One CF usually corresponds to 1KWh / MC (MC is Meter Constant, e.g. 3200 imp/kWh), and is usually referenced as an energy unit in this datasheet. The internal energy resolution for accumulation and conversion is 0.01 CF.

The 0.01 CF pulse energy constant is referenced as 'PL_constant'.

Within 0.01 CF, forward and reverse energy are counteracted. When energy exceeds 0.01 pulse, the respective forward/ reverse energy is increased.

Take the example of active energy, suppose:

T0: Forward energy register is 12.34 pulses and reverse energy register is 1.23 pulses.

From t0 to t1: 0.005 forward pulses appeared.

From t1 to t2: 0.004 reverse pulses appeared.

From t2 to t3: 0.005 reverse pulses appeared.

From t3 to t4: 0.007 reverse pulses appeared.

The following table illustrates the process of energy accumulation process:

	t0	t1	t2	t3	t4
Input energy	+ 0.005	-0.004	-0.005	-0.007	
Bidirectional energy accumulator	0.005	0.001	-0.004	-0.001	
Forward 0.01 CF	0	0	0	0	
Reverse 0.01CF	0	0	0	1	
Forward energy register	12.34	12.34	12.34	12.34	12.34
Reverse energy register	1.23	1.23	1.23	1.23	1.24

When forward/reverse energy reaches 0.1/0.01 pulse, the respective register is updated. When forward or reverse energy reaches 1 pulse, CFx pins output pulse and the REVP/REVQ bits (b7~0, SysStatus1) are updated. Refer to Figure-3.

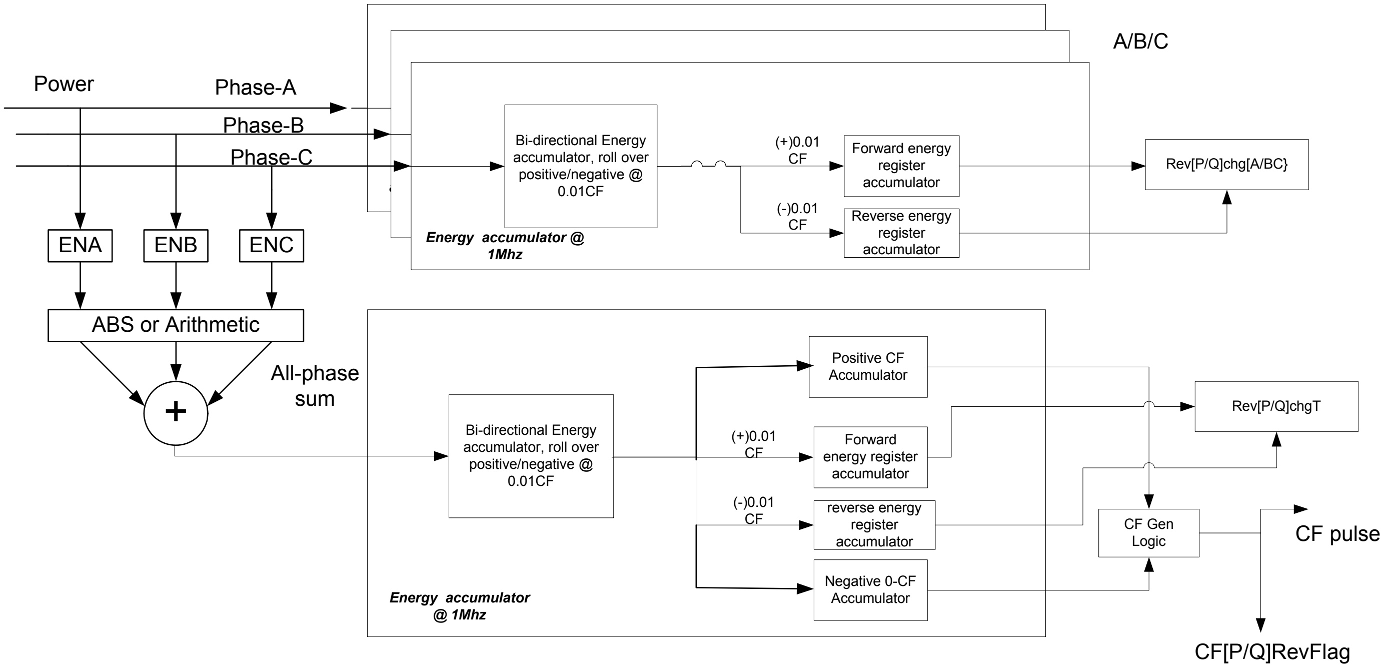


Figure-3 Energy Register Operation Diagram

For all-phase-sum total of active, reactive and (arithmetic sum) apparent energy, the associated power is obtained by summing the power of the three phases. The accumulation method of all-phase-sum energy is determined by the EnPC/EnPB/EnPA/ABSEnP/ABSEnQ bits (b0~b4, MMode0).

Note that the direction of all-phase-sum power and single-phase power might be different.

3.4.2 ENERGY REGISTERS

The 90E36A meters non-decomposed total active, reactive and apparent energy, as well as decomposed active fundamental and harmonic energy. The registers are listed as below.

3.4.2.1 Total Energy Registers

Each phase and all-phase-sum has the following registers:

- Active forward/ reverse
- Reactive forward/ reverse
- Apparent energy

In addition, there is an apparent energy all-phase vector sum register.

Altogether there are 21 energy registers. Those registers are defined in 6.5.1 Regular Energy Registers.

3.4.2.2 Fundamental and Harmonic Energy Registers

The 90E36A counts decomposed active fundamental and harmonic energy. Reactive energy is not decomposed to fundamental and harmonic.

The fundamental/harmonic energy is accumulated in the same way as active energy accumulation method described above.

Registers:

- Fundamental / harmonic
- all-phase-sum / phase A / phase B / phase C
- Forward / reverse

Altogether there are 16 energy registers. Refer to 3.4.2.2 Fundamental and Harmonic Energy Registers.

3.4.3 ENERGY PULSE OUTPUT

CF1 is fixed to be total active energy output (all-phase-sum). Both forward and reverse energy registers can generate the CF pulse (change of forward/ reverse direction can generate an interrupt if enabled).

CF2 is reactive energy output (all-phase-sum) by default. It can also be configured to be arithmetic sum apparent energy output (all-phase-sum) or vector sum apparent energy output (all-phase-sum).

CF3 is fixed to be active fundamental energy output (all-phase-sum).

CF4 is fixed to be active harmonic energy output (all-phase-sum).

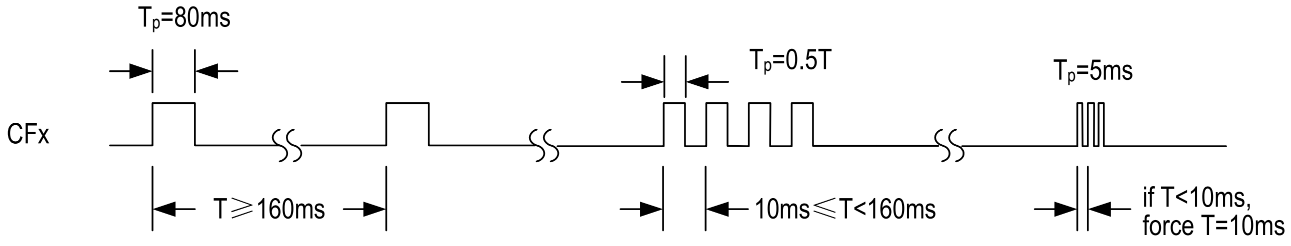


Figure-4 CFx Pulse Output Regulation

For CFx pulse width regulation, refer to Figure-4.

Case1 T>=160ms, Tp=80ms

Case 2 10ms<=T<160ms, Tp=T/2

Case 3 If Calculated T < 10ms, force T=10ms, Tp=5ms

3.4.4 STARTUP AND NO-LOAD POWER

There are startup power threshold registers (e.g. PStartTh(35H)). Refer to 6.4 Configuration and Calibration Registers. The power threshold registers are defined for all-phase-sum active, reactive and apparent power. The 90E36A starts metering when the corresponding all-phase-sum power is greater than the startup threshold. When the power value is lower than the startup threshold, energy is not accumulated and it is assumed as in no-load status. Refer to Figure-5.

There are also no-load Current Threshold registers for Active, Reactive and Apparent energy metering participation for each of the 3 phases. If |P|+|Q| is lower than the corresponding power threshold, that particular phase will not be accumulated. Refer to the PStartTh register and other threshold registers.

There are also no-load status bits (the TPnoload/TQnoload bits (b14~15, EnStatus0)) defined to reflect the no-load status. The 90E36A does not output any pulse in no-load status. The power-on state is of no-load status.

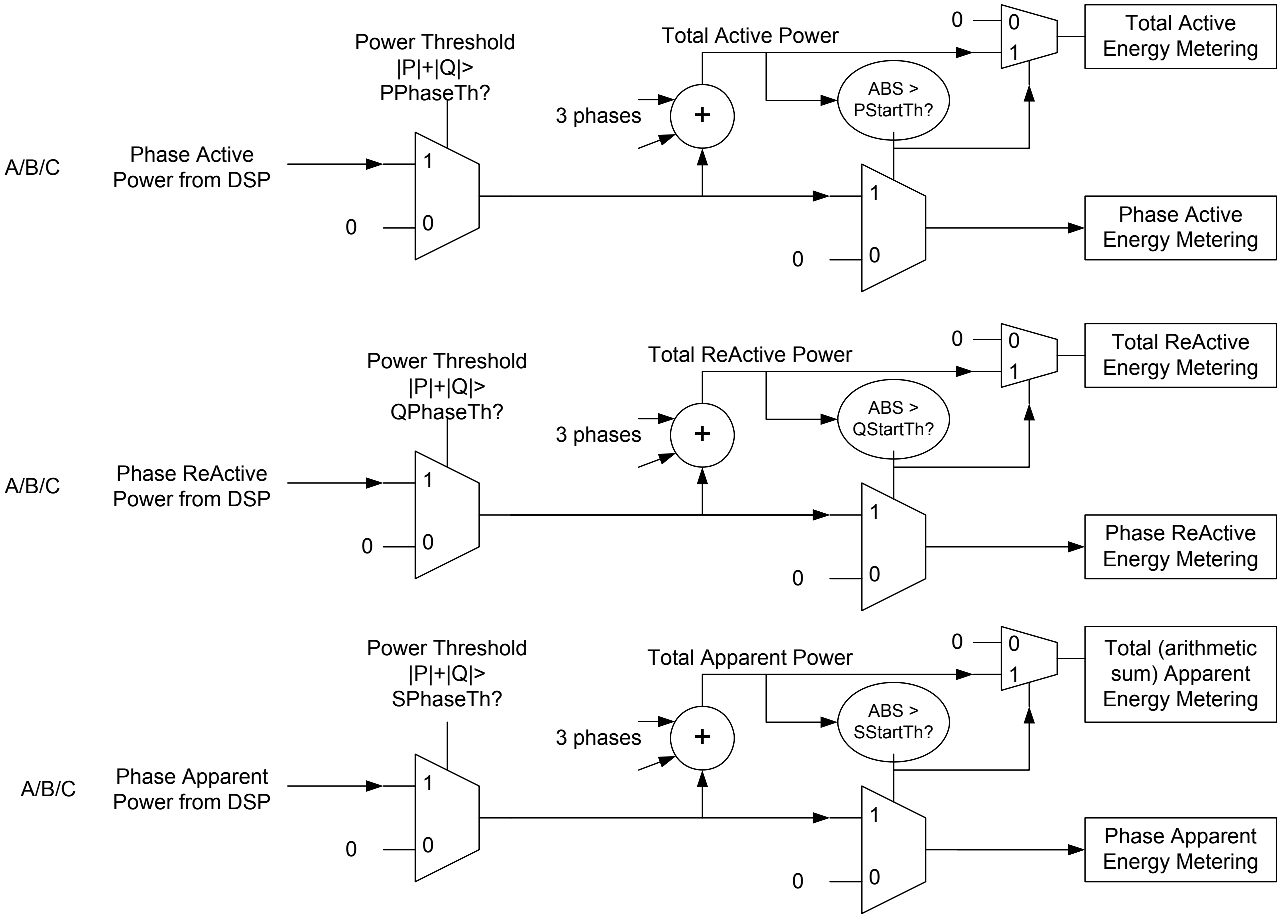


Figure-5 Metering Startup Handling

3.5 MEASUREMENT FUNCTION

Measured parameters can be divided to 7 types as follows:

- Active/ Reactive/ Apparent Power
- Fundamental/ Harmonic Power
- RMS for Voltage and Current
- Power Factor
- Phase Angle
- Frequency
- Temperature

Measured parameters are average values that are averaged among 16 phase-voltage cycles (about 320ms at 50Hz) except for the temperature. The measured parameter update frequency is approximately 3Hz. Refer to Table-15.

3.5.1 ACTIVE/ REACTIVE/ APPARENT POWER

Active/ Reactive/ Apparent Power measurement registers can be divided as below:

- active, reactive, apparent power
- all-phase-sum / phase A / phase B / phase C
- apparent power all-phase vector sum

Altogether there are 13 power registers. Refer to 6.6.1 Power and Power Factor Registers and the SVmeanT register (98H).

Per-phase apparent power is defined as the product of measured Vrms and Irms of that phase.

All-phase-sum power is measured by arithmetically summing the per-phase measured power. The summing of phases can be configured by the MMode0 register.

The 'apparent power all-phase vector sum' is done according to IEEE std 1459.

3.5.2 FUNDAMENTAL / HARMONIC ACTIVE POWER

Fundamental / harmonic active power measurement registers can be divided as below:

- fundamental and harmonic power
- all-phase-sum / phase A / phase B / phase C

Altogether there are 8 power registers. Refer to 6.6.2 Fundamental/ Harmonic Power and Voltage/ Current RMS Registers.

3.5.3 MEAN POWER FACTOR (PF)

Power Factor is defined for those cases: all-phase-sum / phase A / phase B / phase C.

Altogether there are 4 power factor registers. Refer to 6.6.1 Power and Power Factor Registers.

For all-phase:

$$\text{PF\_all} = \frac{\text{All\_phase\_ sum active\_pow er}}{\text{All\_phase\_ sum apparent\_p ower}}$$

The all-phase-sum apparent power selection is defined by the CF2ESV bit (b6, MMode0).

For each of the phase::

$$\text{PF\_phase} = \frac{\text{active\_pow er}}{\text{apparent\_p ower}}$$

3.5.4 VOLTAGE / CURRENT RMS

Voltage/current RMS registers can be divided as follows:

Per-phase: Phase A / Phase B / Phase C

Voltage / Current

Altogether there are 6 RMS registers.

Neutral Line Current RMS:

Neutral line current can be measured by A/D, or calculated by instantaneous value $i_N = i_A + i_B + i_C$.

Altogether there are 2 N line current RMS registers.

Refer to 6.6.2 Fundamental/ Harmonic Power and Voltage/ Current RMS Registers.

3.5.5 PHASE ANGLE

Phase Angle measurement registers can be divided as below:

- phase A / phase B / phase C
- voltage / current

Altogether there are 6 phase angle registers. Refer to 6.6.3 THD+N, Frequency, Angle and Temperature Registers.

Note: Calculation of phase angle is based on zero-crossing interval and frequency. There might be big error when voltage/current at low value.

3.5.6 FREQUENCY

Frequency is measured using phase A voltage by default. When phase A has voltage sag, phase C is used, and phase B is used when both phase A and C have voltage sag.

Refer to 6.6.3 THD+N, Frequency, Angle and Temperature Registers.

3.5.7 TEMPERATURE

Chip Junction-Temperature is measured roughly every 100 ms by on-chip temperature sensor.

Refer to 6.6.3 THD+N, Frequency, Angle and Temperature Registers.

3.5.8 THD+N FOR VOLTAGE AND CURRENT

Voltage THD+N is defined as:

$$\frac{\sqrt{(V_{rms\_total}{}^{2} - V_{rms\_fundam\ ental}{}^{2})}}{V_{rms\_fundam\ ental}}$$

Current THD+N's definition is similar to that of voltage.

Registers:

- voltage and current
- phase A / phase B / phase C

Altogether there are 6 THD+N registers. Refer to 6.6.3 THD+N, Frequency, Angle and Temperature Registers.

The THD+N measurement is mainly used to monitor the percentage of harmonics in the system. Accuracy is not guaranteed when THD+N is lower than 10%.

3.6 FOURIER ANALYSIS FUNCTION

The 90E36A offers a hardware DFT Engine for 2nd to 32nd order harmonic component, both V and I of each phase with the same time period.

The registers can be divided as follows:

- voltage and current for each phase
- phase A / phase B / phase C
- 32 frequency components (fundamental value, and harmonic ratios)
- Total Harmonic Distortion (THD)

The harmonic analysis is implemented with a DFT engine. The DFT period is 0.5 second, which gives a resolution frequency bin of 2Hz. The input samples are multiplied with a Hanning window before feeding to the DFT processor. The DFT processor computes the fundamental and harmonic components based on the measured line frequency and sampling rate, which is 8KHz.

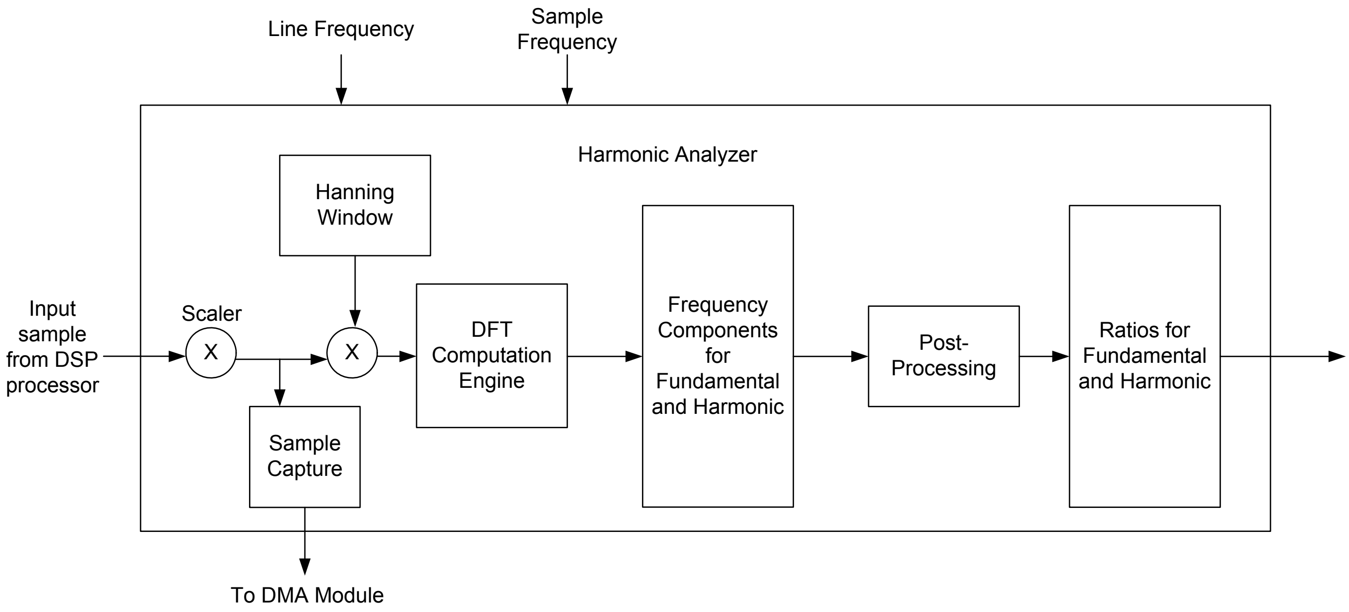


Figure-6 Analysis Function

3.7 POWER MODE

The 90E36A has four power modes. The power mode is solely defined by the PM1 and PM0 pins.

Table-2 Power Mode Mapping

PM1:PM0 Value	Power Mode
11	Normal (N mode)
10	Partial Measurement (M mode)
01	Detection (D mode)
00	Idle (I mode)

3.7.1 NORMAL MODE (N MODE)

In Normal mode, all function blocks are active except for current detector block. Refer to Figure-7.

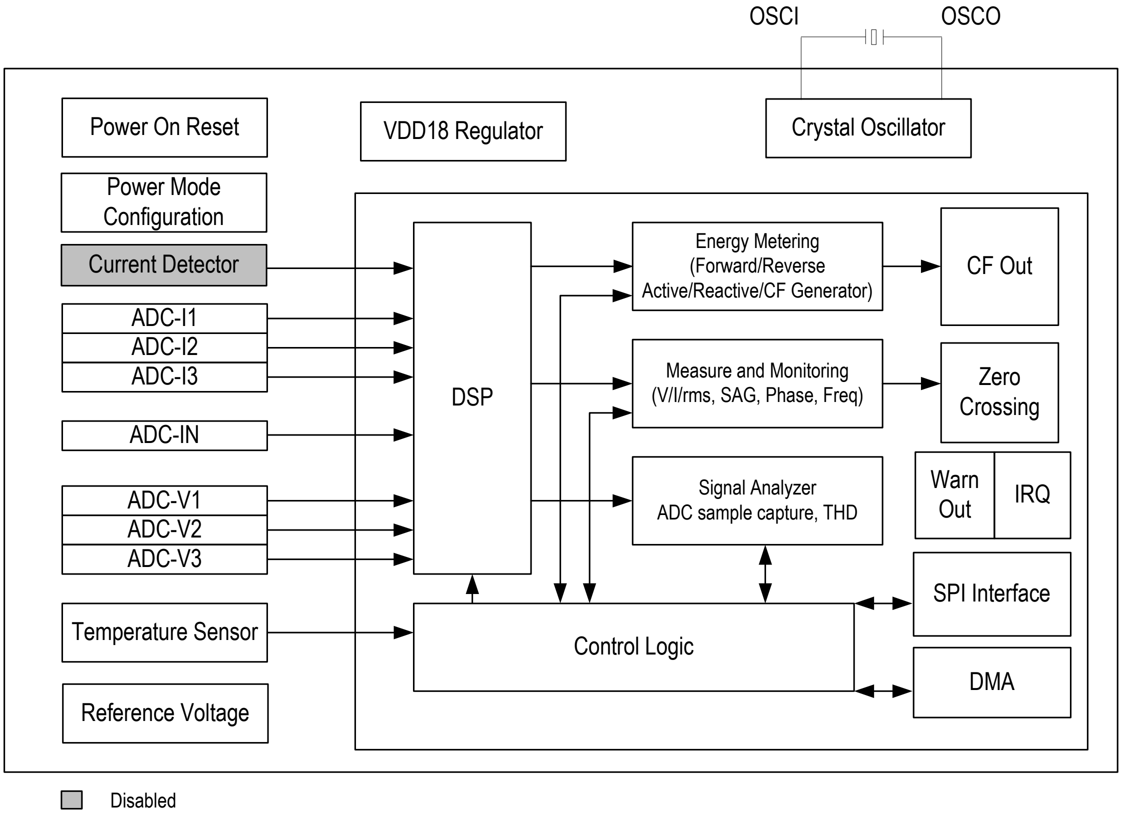


Figure-7 Block Diagram in Normal Mode

3.7.2 IDLE MODE (I MODE)

In Idle mode, all functions are shut off.

The analog blocks' power supply is powered but circuits are set into power-down mode, i.e, power supply applied but all current paths are shut off. There is very low current since only very low device leakage could exist in this mode.

The digital I/Os' supply is powered.

In I/O and analog interface, the input signals from digital core (which is not powered) will be set to known state as described in Table-3. The PM1 and PM0 pins which are controlled by external MCU are active and can configure the 90E36A to other modes.

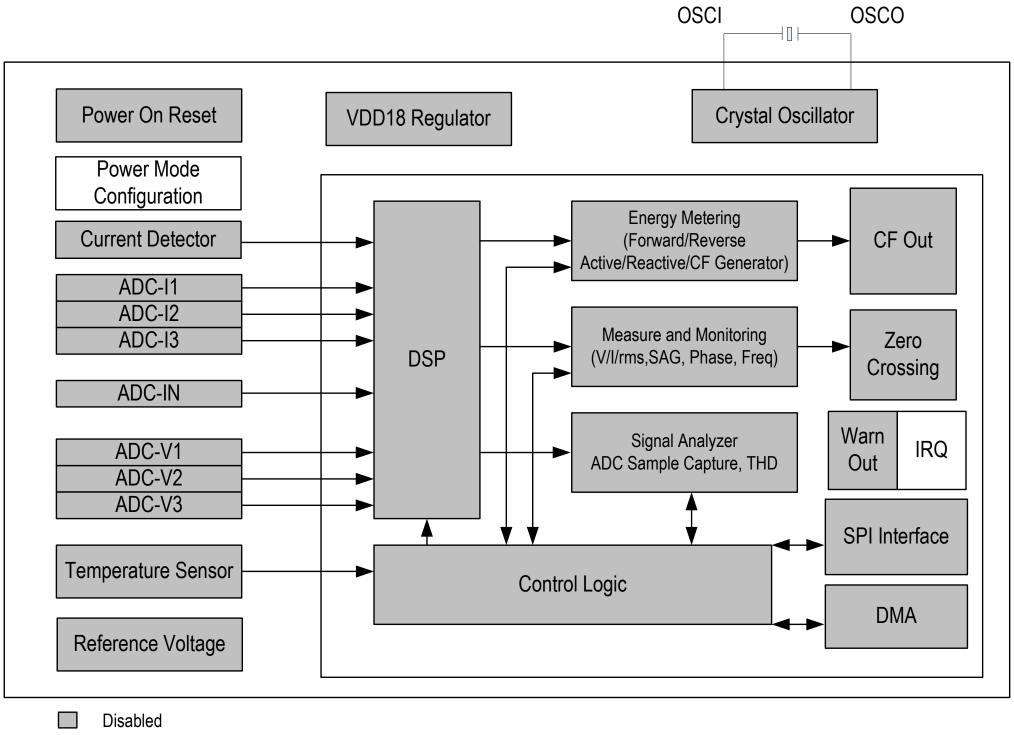


Figure-8 Block Diagram in Idle Mode

Please note that since the digital I/O is not shut off, the I/O circuit is active in the Idle mode. The application shall make sure that valid logic levels are applied to the I/O.

Table-3 lists digital I/O and power pins' states in Idle mode. It lists the requirements for inputs and the output level for output. For bi-directional pins, the direction is defined.

Table-3 Digital I/O and Power Pin States in Idle Mode

Name	I/O type	Type	Pin State in Idle Mode
$\overline{\text{Reset}}$	I	LVTTL	Input level shall be VDD33.
$\overline{\text{CS}}$	B	LVTTL	I/O set in input mode. Input level shall be VDD33 or VSS.
SCLK	B	LVTTL	I/O set in input mode. Input level shall be VDD33 or VSS.
SDO	B	LVTTL	I/O set in input mode. Input level shall be VDD33 or VSS.
SDI	B	LVTTL	I/O set in input mode. Input level shall be VDD33 or VSS.
PM1 PM0	I	LVTTL	As defined in Table-2
OSCI OSCO	I O	OSC	Oscillator powered down. OSCO stays at fixed (low) level.

Table-3 Digital I/O and Power Pin States in Idle Mode

Name	I/O type	Type	Pin State in Idle Mode
ZX0 ZX1 ZX2	O	LVTTL	0
CF1 CF2 CF3 CF4	O	LVTTL	0
WarnOut	O	LVTTL	0
IRQ0 IRQ1	O	LVTTL	0
DMA_CTRL	I	LVTTL	I/O set in input mode. Input level shall be VDD33 or VSS.
VDD18	I	Power	Regulated 1.8V: high impedance
DVDD	I	Power	Digital Power Supply: powered by system
AVDD	I	Power	Analog Power Supply: powered by system
Test	I	Input	Always tie to ground in system application

3.7.3 DETECTION MODE (D MODE)

In Detection mode, the current detector is active. The current detector compares whether any phase current exceeds the configured threshold using low-power comparators.

When the current of one phase or multiple phases exceeds the configured threshold, the 90E36A asserts the IRQ0 pin to high and hold it until power mode change. The IRQ0 state is cleared when entering or exiting Detection mode.

When the current of all three current channels exceed the configured threshold, the 90E36A asserts the IRQ1 pin to high and hold it until power mode change. The IRQ1 state is cleared when entering or exiting Detection mode.

The threshold registers need to be programmed in Normal mode before entering Detection mode.

The digital I/O state is the same as that in Idle state (except for IRQ0/IRQ1 and PM1/PM0).

The 90E36A has two comparators for detecting each phase's positive and negative current. Each comparator's threshold can be set individually. The two comparators are both active by default, which called 'double-side detection'. User also can enable one comparator only to save power consumption, which called 'single-side detection'.

Double-side detection has faster response and can detect 'half-wave' current. But it consumes nearly twice as much power as single-side detection.

Comparators can be power-down by configuring the DetectCtrl register.

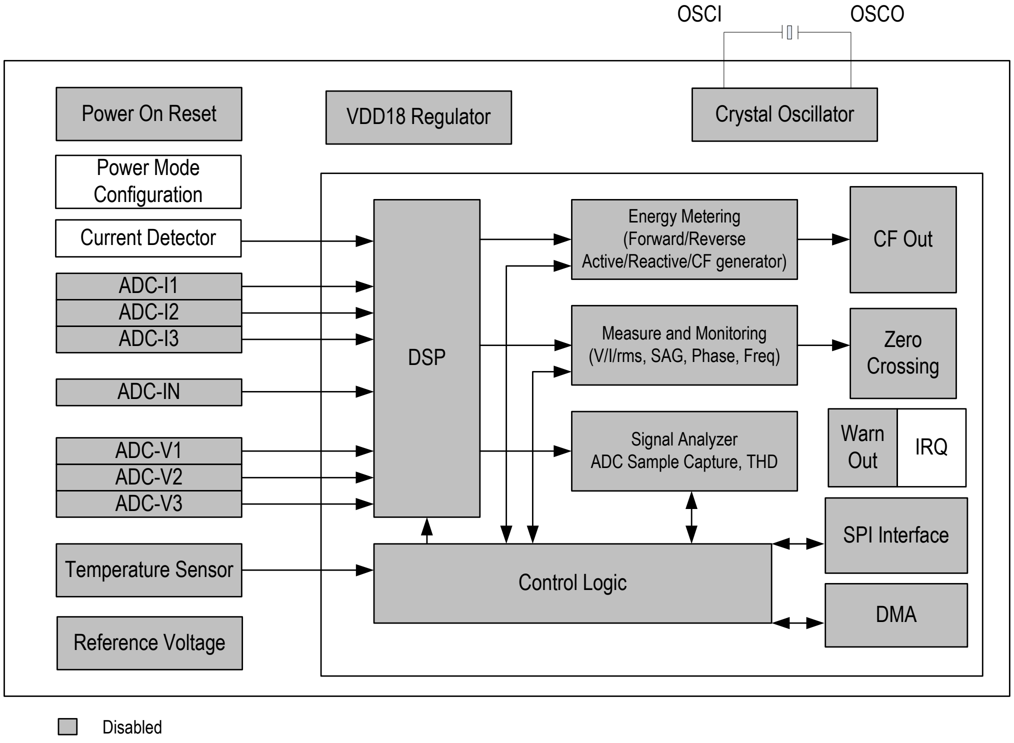


Figure-9 Block Diagram in Detection Mode

3.7.4 PARTIAL MEASUREMENT MODE (M MODE)

In this mode, Voltage ADCs, Neutral Line ADC and digital circuits are inactive.

The 90E36A measures the current RMS of one line cycle.

When the measurement is done, the 90E36A asserts the IRQ0 pin high until the Partial Measurement mode exits.

In this mode, the user needs to program the related registers (including PGA gain, channel gain, offset, etc.) to make the current RMS measurement accurate. Refer to 5.2 Partial Measurement mode Calibration. Please note that not all registers in this mode is accessible. Only the Partial Measurement related registers (14H~1DH) and some special registers (00H, 01H, 03H, 07H,0EH, 0FH) can be accessed.

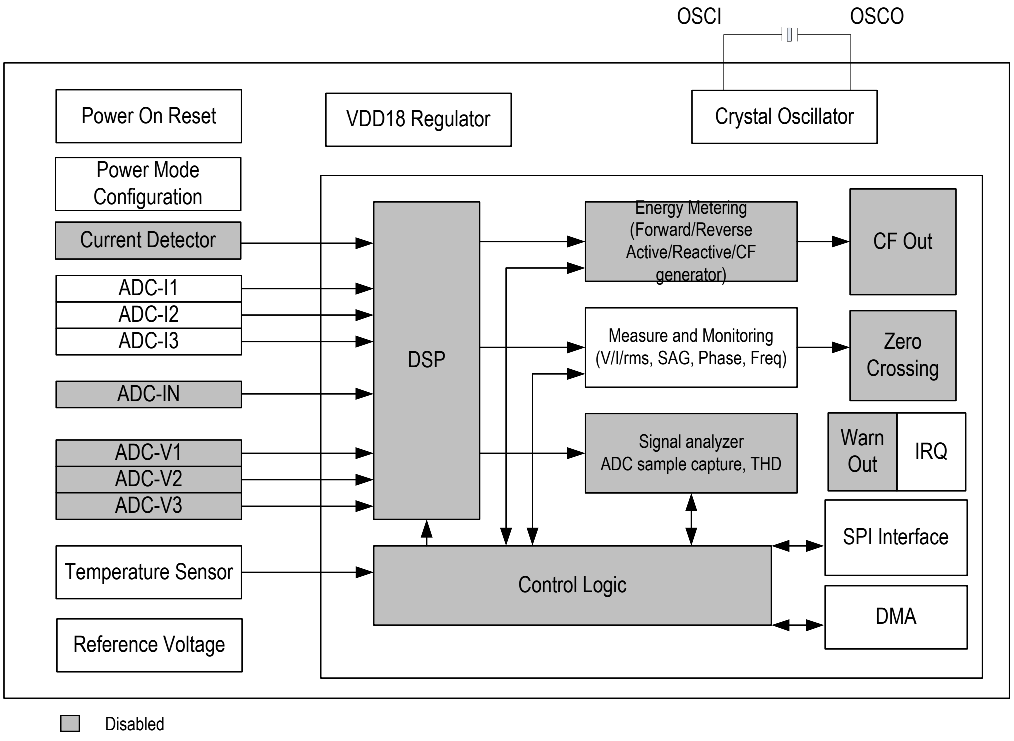


Figure-10 Block Diagram in Partial Measurement mode

3.7.5 TRANSITION OF POWER MODES

The above power modes are controlled by the PM0 and PM1 pins. In application, the PM0 and PM1 pins are connected to external MCU. The PM0 and PM1 pins have internal RC- filters.

Generally, the 90E36A stays in Idle mode most of the time while outage. It enters Detection mode at a certain interval (for example 5s) as controlled by the MCU. It informs the MCU if the current exceeds the configured threshold. The MCU then commands the 90E36A to enter Partial Measurement mode at a certain interval (e.g. 60s) to read related current. After current reading, the 90E36A gets back to the Idle mode.

The measured current may be used to count energy according to some metering model (like current RMS multiplying the rated voltage to compute the power).

Any power mode transition goes through the Idle mode, as shown in Figure-11.

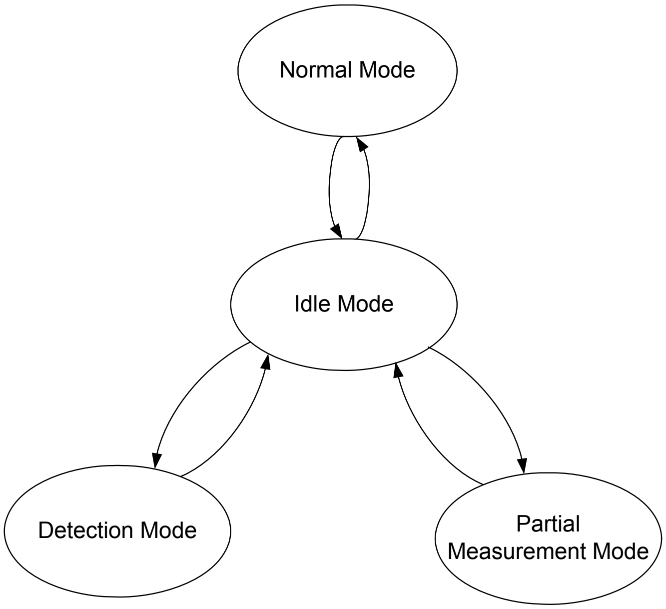


Figure-11 Power Mode Transition

3.8 EVENT DETECTION

3.8.1 ZERO-CROSSING DETECTION

Zero-crossing detector detects the zero-crossing point of the fundamental component of voltage and current for each of the 3 phases.

Zero-crossing signal can be independently configured and output. Refer to the definition of the ZXConfig register.

3.8.2 SAG DETECTION

Usually in the application the Sag threshold is set to be 78% of the reference voltage. The 90E36A generates Sag event when there are less than three 8KHz samples (absolute value) greater than the sag threshold during two continuous 11ms time-window.

For the computation of Sag threshold register value, refer to AN-644.

The Sag event is captured by the SagWarn bit (b3, SysStatus0). If the corresponding IRQ enable bit the SagWnEn bit (b3, FuncEn0) is set, IRQ can be generated. Refer to Figure-22.

3.8.3 PHASE LOSS DETECTION

The phase loss detection detects if there is one or more phases' voltage is less than the phase-loss threshold voltage.

The processing and handling is similar to sag detection, only the threshold is different. The threshold computation flow is also similar. The typical threshold setting could be 10% Un or less.

If any phase line is detected as in phase-loss mode, that phase's zero-crossing detection function (both voltage and current) is disabled.

3.8.4 NEUTRAL LINE OVERCURRENT DETECTION

3.8.4.1 Sampled N-Line

The neutral line measured RMS is checked with the threshold defined in the INWarnTh1 register. If the N Line current is greater than the threshold, the INOv1 bit (b15, SysStatus1) is set. IRQ1 is generated if the corresponding Enable bit (the INOv1En bit (b15, FuncEn1)) is set.

3.8.4.2 Computed N-Line

The neutral line computed current (calculated) RMS is checked with the threshold defined in the INWarnTh0 register. If the N Line current is greater than the threshold, the INOv0 bit (b14, SysStatus1) bit is set. IRQ1 is generated if the corresponding Enable bit the INOv0En bit (b14, FuncEn1) is set.

3.8.5 PHASE SEQUENCE ERROR DETECTION

The phase sequence is detected in two cases: 3P4W and 3P3W, which is defined by the 3P3W bit (b8, MMode0).

3P4W case:

Correct sequence: Voltage/current zero-crossing sequence: phase-A, phase-B and phase-C.

3P3W case:

Correct sequence: Voltage/current zero-crossing between phase-A and phase-C is greater than 180 degree.

If the above mentioned criteria are violated, it is assumed as a phase sequence error.

3.9 DC AND CURRENT RMS ESTIMATION

The 90E36A has a module named 'PMS' which can estimate current channel RMS or current channel arithmetic average (DC component). The measurement type is defined in the PMConfig register. It can be used to estimate current RMS in Partial Measurement mode. Since the PMS block only consume very small power, it can be also used to estimate current RMS in Normal mode. The PMS module is turned on in both Partial Measurement mode and Normal mode.

The result is in different format and different scale for the RMS and average respectively. The RMS result is unsigned; while current average is signed.

Refer to 6.3.2 Partial Measurement mode Registers for associated register definition.

4 SPI / DMA INTERFACE

4.1 INTERFACE DESCRIPTION

The interface can work in two modes: Slave (SPI) mode and Master mode, which is also named DMA (Direct Memory Access) mode. The interface mode is determined by the DMA_CTRL pin as below:

Mode	DMA_CTRL	Description
Slave (SPI) Mode	0	The interface works as normal four-wire SPI interface.
Master (DMA) Mode	1	The interface operates as a master and dumps data to the other devices.

Five pins are associated with the interface as below:

- SDI – Data pin, bi-directional.
- SDO – Data pin, bi-directional.
- SCLK – Bi-directional pin. It is a clock output pin in master mode and clock input pin in slave mode.
- $\overline{CS}$ – Bi-directional chip select pin . It is an output pin in master mode and input pin in slave mode.
- DMA_CTRL – Uni-directional input pin. The external device pull this pin high to control the interface work in master mode for data dumping in DMA mode.

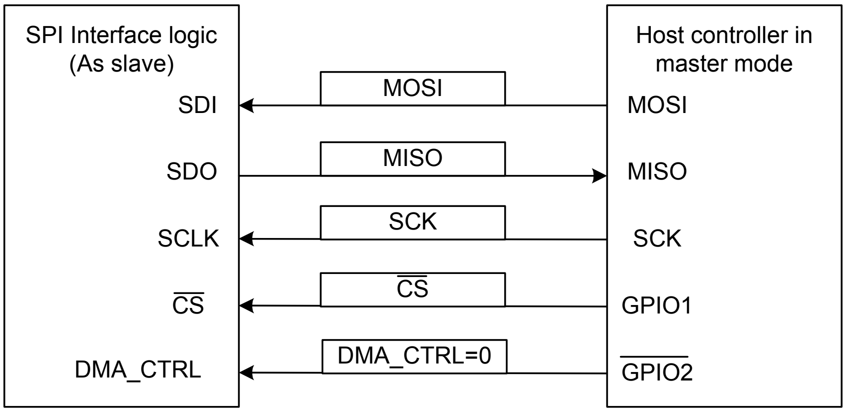


Figure-12 Slave Mode

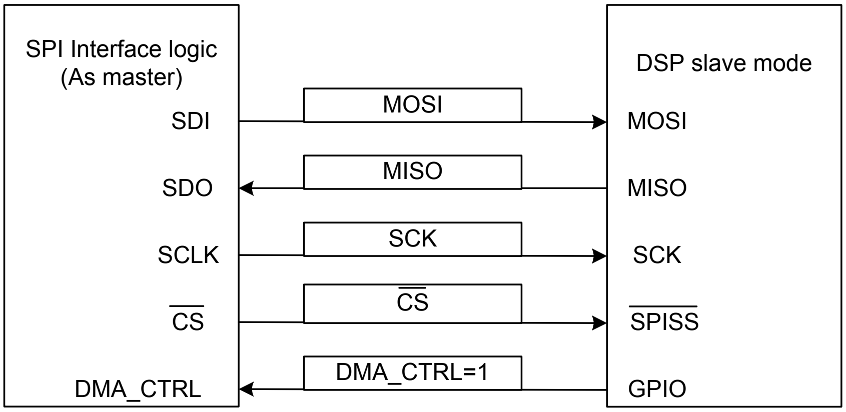


Figure-13 Master Mode (PIN_DIR_SEL=0)

4.2 SLAVE MODE: SPI INTERFACE

The interface works in slave mode when the DMA_CTRL pin is low as shown in Figure-12.

4.2.1 SPI SLAVE INTERFACE FORMAT

In the SPI mode, data on SDI is shifted into the chip on the rising edge of SCLK while data on SDO is shifted out of the chip on the falling edge of SCLK.

Refer to Figure-14 and Figure-15 below for the timing diagram.

Access type:

The first bit on SDI defines the access type as below:

Instruction	Description	Instruction Format
Read	read from registers	1
Write	write to registers	0

Address:

Fixed 15-bit, following the access type bits. The lower 10-bit is decoded as address; the higher 5 bits are 'Don't Care'.

Read/Write data:

Fixed as 16 bits.

Read Sequence:

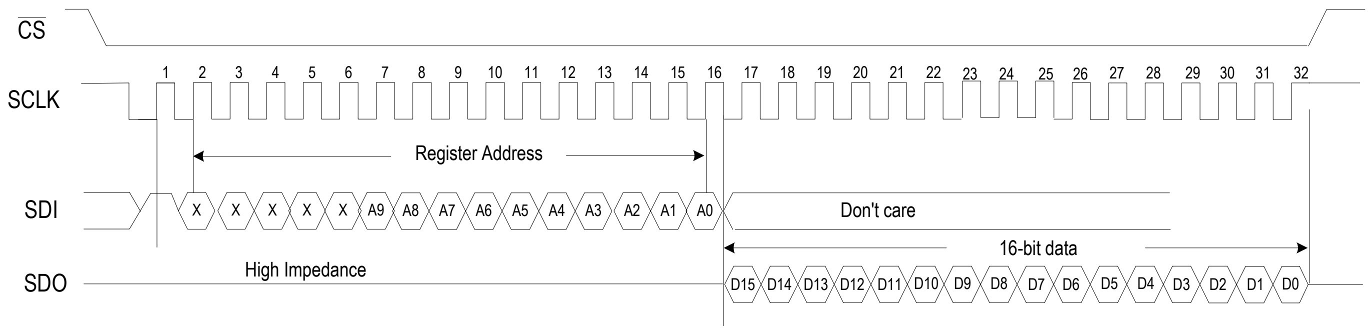


Figure-14 Read Sequence

Write Sequence:

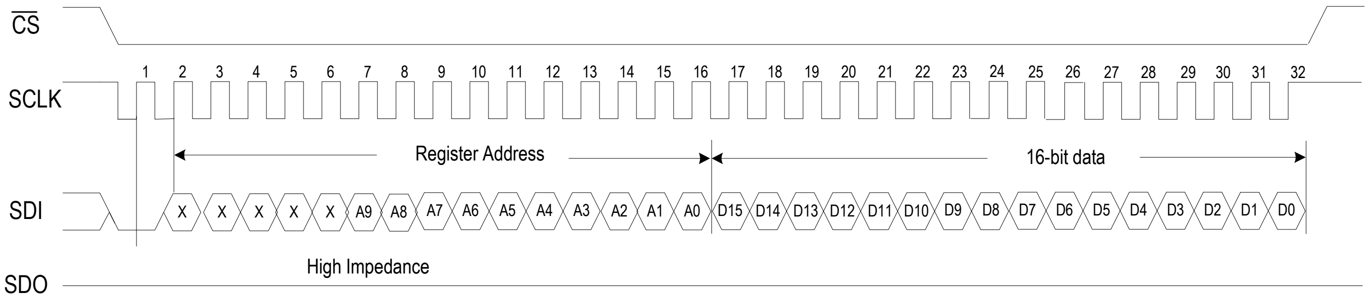


Figure-15 Write Sequence

4.2.2 RELIABILITY ENHANCEMENT FEATURE

The SPI read/write transaction is $\overline{CS}$-low defined. Each transaction can only access one register.

Within each $\overline{CS}$-low defined transaction:

Write: access occurs only when $\overline{CS}$ goes from low to high and there are exactly 32 SCLK cycles received during $\overline{CS}$ low period.

Read: if SCLK>=16 (full address received), data is read out from internal registers and gets to the SDO pin; and the LastSPIData register is updated. The R/C registers can only be cleared after the LastSPIData register is updated.

4.3 MASTER MODE: DMA

The interface is defined to connect with various DSP processors for ADC samples dumping.

For DMA configure please refer to DMACtrl register definition in 6.2 Special Registers.

The interface works in Master mode when the DMA_CTRL pin is pulled high by the external device. In Master mode, registers in 90E36A cannot be accessed. The dump transaction can be stopped by the external device via pulling the DMA_CTRL pin to low at any time.

Figure-13 shows a connection between 90E36A and a DSP processor where 90E36A acts as the master.

4.3.1 DMA BURST TRANSFER FOR ADC SAMPLING

When the DMA_CTRL pin changes from low to high, the voltage and current channel ADC samples (after decimation and frequency compensation) are dumped out serially through the interface with SCLK frequency defined by the CLK_DIV[3:0] bits (b3~0, DMACtrl).

When the 90E36A detects that the DMA_CTRL pin is de-asserted, it stops the DMA transaction after the current sample has been sent.

Clock Dividing Ratio

The SCLK frequency of SPI interface is defined by the CLK_DIV[3:0] bits (b3~0, DMACtrl) as the following equation:

$$f_{SCLK} = \frac{f_{sys\_clk}}{CLK\_DIV \quad * 2 + 2}$$

Here f_{sys_clk} means system's oscillator frequency.

Interface Direction

In DMA mode, the interface direction of SDI/SDO pins are normally defined as Figure-13. But the direction also can be swapped by configuring the PIN_DIR_SEL bit (b8, DMACtrl).

ADC Channel Selection

Internally, the 90E36A has 7 ADC channels. The user can select which channel's samples to be dumped out via configuring the ADC_CH_SEL[15:9] bits (b15~9, DMACtrl).

Each bit of the 7-bit field ADC_CH_SEL enables the data dumping for one ADC channel. Set '1' to a bit enables the dump of the corresponding ADC channel samples.

Clock Modes

Four clock modes are defined in master mode according to the CLK_DRV bit (b4, DMACtrl) and CLK_IDLE bit (b5, DMACtrl) configuration as the following diagram shows.

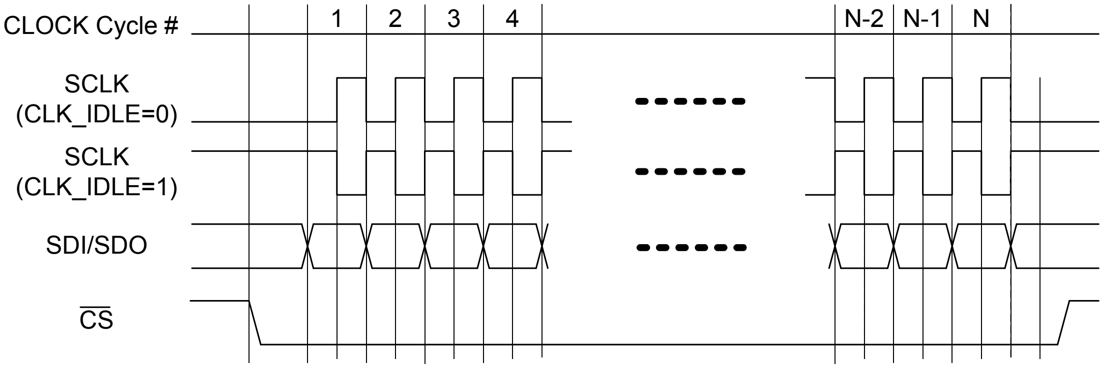


Figure-16 Clock Mode0 (CLK_DRV=0, CLK_IDLE=0) and Mode1 (CLK_DRV=0, CLK_IDLE=1)

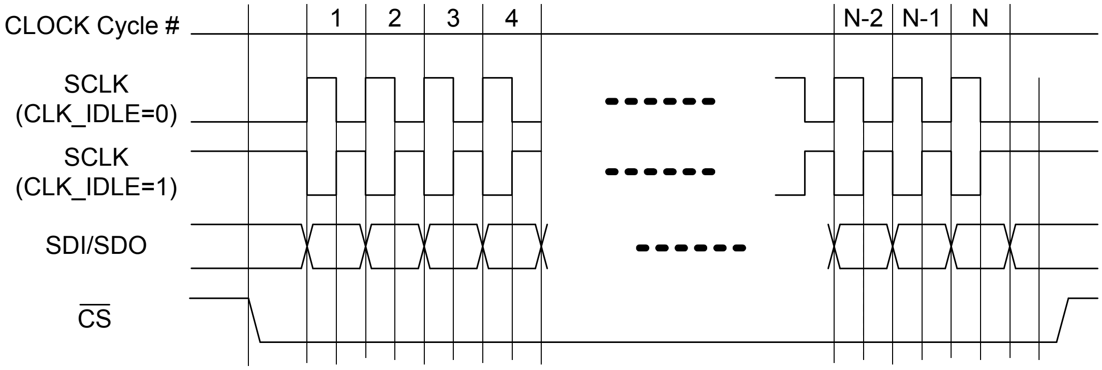


Figure-17 Clock Mode2 (CLK_DRV=1, CLK_IDLE=0) and Mode3 (CLK_DRV=1, CLK_IDLE=1)

For mode0 and mode1 (CLK_DRV = 0), the first edge of SCLK is used by the slave to sample the data.

For mode2 and mode3 (CLK_DRV=1), the first edge of SCLK is used by the master to drive out the data.

$\overline{CS}$ Deactivation for Rate Adaptation

Since the bit rate may be higher than the equivalent bit rate of the samples (For example, for 24-bit non-frame mode, the equivalent bit-rate is sample_rate*6*24bps). To compensate for that, the $\overline{CS}$ signal is de-asserted to wait for the new samples and be asserted again once the new sample arrives.

There are at least 2 SCLK clock periods for $\overline{CS}$ resume from de-asserted state to assert state depending on the Clock Dividing Ratio and ADC Channel Selection. During $\overline{CS}$ de-asserted state, the SCLK stays in idle state as configured by the CLK_IDLE bit (b5, DMACtrl).

Data Frame Format and Sample Sequence in DMA Mode

The 90E36A sends the ADC samples (In 8K sample rate) continuously in DMA mode.

The samples of all enabled ADC channels are sent out in interleaved manner, with the sequence of I4, I1, V1, I2, V2, and I3, V3 (If any channel is disabled, remove it from the list while maintaining the sequence of the other channels). Figure-18 shows an example of the sample sequence when the ADC_CH_SEL[15:9] bits (b15~9, DMACtrl) are configured to be '0101001'.

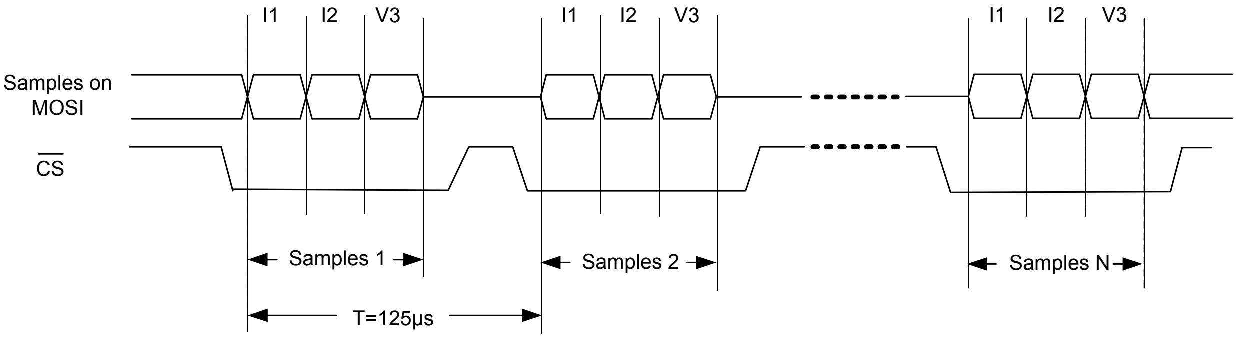


Figure-18 Sample Sequence Example

Bit Sequence

The samples sent over the interfaces are the processed data according to the CH_BITWIDTH[7:6] bits (b7~6, DMACtrl). All the samples sent are MSB first. Figure-19 shows an example of sample bit sequence for 32-bit sample bit width.

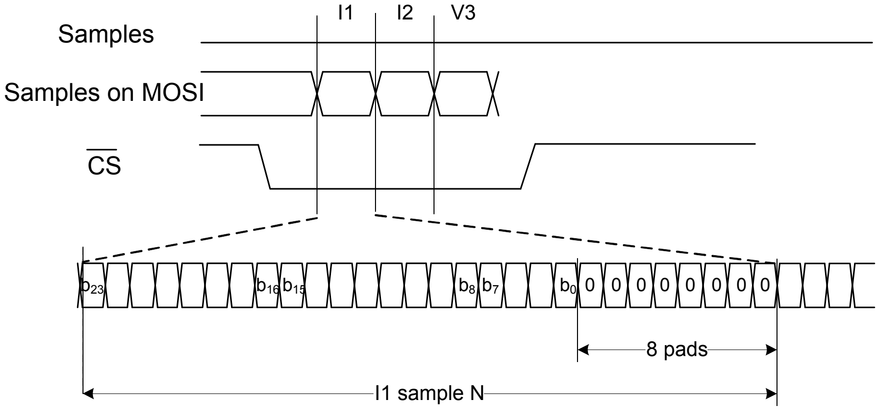


Figure-19 Sample Bit Sequence Example

4.3.2 CONTROL SEQUENCE FOR EXTERNAL DEVICE

To start and stop the DMA dump sequence, the external device follows the rules described below:

- Start of the dump process:

a) The external device configures the DMACtrl register.

b) The external device switches to SPI slave mode. Note that the parameters of clock idle state / driving edge, sample bit width and pin direction of SPI_D0/SPI_D1 configured to 90E36A should match with external device's settings.

c) The external device asserts the DMA_CTRL signal. The 90E36A swaps I/O direction if necessary after it has detected that master has asserted the DMA. The samples are dumped out with a delay of at most 1 sample period (125us).

- Stop of the dump process:

a) The external device de-asserts the DMA_CTRL signal. The 90E 36A stops the transaction after current (all selected) samples have been successfully sent out.

b) The external device waits one sample period of 125us or detects that the $\overline{\text{CS}}$ signal is pulled high, then switches the interface back to master mode.

5 CALIBRATION METHOD

5.1 NORMAL MODE OPERATION CALIBRATION

Calibration is done per phase and there is no need to calibrate for the all-phase-sum (total) parameters. The calibration method is as follows:

Step-1: Register configuration for calibration

- Start to configure the System configuration Registers by writing 5678H to the ConfigStart register.
- The 90E36A automatically reset the configuration registers to their default value.
- Program all the system configuration registers.
- Calculate and write the checksum to the CS0 register.
- Write 8765H to the ConfigStart register (enable checksum checking).
- System may check the WarnOut pin to see if there is a checksum error.

The start register and checksum handling scheme is the same throughout the calibration process, so the following section does not describe the start and checksum operation.

Step-2: Measurement calibration (per-phase)

- First calibrate offset at I = 0, U = 0 for current or/and voltage;
  - Configure calculated channel Gain (The user needs to program the PGA gain and DPGA gain properly in order to get the calculated gain within 0 to 2 in step-1).
  - Read Irms/ Urms value.
  - Calculate the compensation value.
  - Write the calculated value to the offset register.
- Then calibrate gain at I = In (Ib), U = Un for current and voltage;
  - Read Irms/ Urms value.
  - Calculate the compensation value.
  - Write the calculated value to the Gain register.

Step-3: Metering calibration (per phase)

- First calibrate the Power/ Energy offset.
  - U = Un, I = 0.
  - Read full 32 bits (or lower 16 bits) Active and Reactive Power
  - Calculate the compensation values
  - Write the calculated values to the offset registers respectively.
- Then calibrate Energy gain at unity power factor:
  - PF=1.0, U = Un, I = In (Ib).
  - Connect CF1 to the calibration bench;
  - User/ PC calculate the energy gain according to the data got from calibration bench
  - Write the calculated value to the Energy Gain register.
- Then calibrate the phase angle compensation at 0.5 inductive power factor.
  - PF=0.5L, U = Un, I = In (Ib), Rated frequency = 50Hz, or 60Hz according to the application;
  - CF1 connected to the calibration bench;
  - User/ PC calculate the phase angle according to the data got from calibration bench;
  - Write the calculated value to the Phase angle register.

5.2 PARTIAL MEASUREMENT MODE CALIBRATION

The calibration method is as follows:

Step-1: Set the input current to zero and measure the current mean value (set MeasureType = 1, write 1 to the ReMeasure bit (b14, PMConfig) to trigger the measurement. Refer to the PMIrmsA register). Negate the result register (the PMIrmsA/PMIrmsB/PMIrmsC registers) reading (16-bit) and then write the result to the offset register.

Step-2: The output of Partial Measurement result = ADC_input_voltage *PGA_gain*DPGA_gain*65536 / 1.2. For instance, a 150 mVrms signal (from CT) with PGA = 1 gets 8192 in the RMS result register.

Step-3: The user needs to do its own conversion to get meaningful result. The scaling factor in user's software could be calibrated device per device.

6 REGISTER

6.1 REGISTER LIST

Table-4 Register List

Register Address	Register Name	Read/Write Type	Functional Description	Comment	Page
Status and Special Register					
00H	SoftReset	W	Software Reset		P 36
01H	SysStatus0	R/C	System Status 0		P 38
02H	SysStatus1	R/C	System Status 1		P 38
03H	FuncEn0	R/W	Function Enable 0		P 40
04H	FuncEn1	R/W	Function Enable 1		P 40
07H	ZXConfig	R/W	Zero-Crossing Configuration	Configuration of ZX0/1/2 pins' source	P 42
08H	SagTh	R/W	Voltage Sag Threshold		P 42
09H	PhaseLossTh	R/W	Voltage Phase Losing Threshold	Similar to Voltage Sag Threshold register	P 42
0AH	INWarnTh0	R/W	Threshold for calculated (Ia + Ib +Ic) N line rms current	Check SysStatus0/1 register.	P 43
0BH	INWarnTh1	R/W	Threshold for sampled (from ADC) N line rms current	Check SysStatus0/1 register.	P 43
0CH	THDNUTh	R/W	Voltage THD Warning Threshold	Check SysStatus0/1 register.	P 43
0DH	THDNITh	R/W	Current THD Warning Threshold	Check SysStatus0/1 register.	P 43
0EH	DMACtrl	R/W	DMA Mode Interface Control	DMA mode interface control	P 44
0FH	LastSPIData	R	Last Read/ Write SPI Value	Refer to 4.2.2 Reliability Enhancement Feature	P 44
Low Power Mode Register					
10H	DetectCtrl	R/W	Current Detect Control		P 45
11H	DetectTh1	R/W	Channel 1 current threshold in Detection mode		P 46
12H	DetectTh2	R/W	Channel 2 current threshold in Detection mode		P 46
13H	DetectTh3	R/W	Channel 3 current threshold in Detection mode		P 47
14H	PMOffsetA	R/W	Ioffset for phase A in Partial Measurement mode		P 47
15H	PMOffsetB	R/W	Ioffset for phase B in Partial Measurement mode		P 47
16H	PMOffsetC	R/W	Ioffset for phase C in Partial Measurement mode		P 47
17H	PMPGA	R/W	PGAgain Configuration in Partial Measurement mode		P 48
18H	PMIrmsA	R	Irms for phase A in Partial Measurement mode		P 48
19H	PMIrmsB	R	Irms for phase B in Partial Measurement mode		P 48
1AH	PMIrmsC	R	Irms for phase C in Partial Measurement mode		P 48
1BH	PMConfig	R/W	Measure configuration in Partial Measurement mode		P 49
1CH	PMAvgSamples	R/W	Number of 8K samples to be averaged in RMS/ mean computation		P 49
1DH	PMIrmsLSB	R	LSB bits of PMRrms[A/B/C]	It returns MSB of the mean measurement data in Mean value test	P 49

Table-4 Register List (Continued)

Register Address	Register Name	Read/Write Type	Functional Description	Comment	Page
Configuration Registers					
30H	ConfigStart	R/W	Calibration Start Command		P 51
31H	PLconstH	R/W	High Word of PL_Constant		P 51
32H	PLconstL	R/W	Low Word of PL_Constant		P 51
33H	MMode0	R/W	Metering method configuration		P 52
34H	MMode1	R/W	PGA gain configuration		P 53
35H	PStartTh	R/W	Active Startup Power Threshold.	Refer to Table-5.	
36H	QStartTh	R/W	Reactive Startup Power Threshold.		
37H	SStartTh	R/W	Apparent Startup Power Threshold.		
38H	PPhaseTh	R/W	Startup Power Threshold (Active Energy Accumulation)		
39H	QPhaseTh	R/W	Startup Power Threshold (ReActive Energy Accumulation)		
3AH	SPhaseTh	R/W	Startup Power Threshold (Apparent Energy Accumulation)		
3BH	CS0	R/W	Checksum 0		P 54
Calibration Registers					
40H	CalStart	R/W	Calibration Start Command	Refer to Table-6.	
41H	PoffsetA	R/W	Phase A Active Power Offset		P 55
42H	QoffsetA	R/W	Phase A Reactive Power Offset		P 55
43H	POffsetB	R/W	Phase B Active Power Offset		
44H	QOffsetB	R/W	Phase B Reactive Power Offset		
45H	POffsetC	R/W	Phase C Active Power Offset		
46H	QOffsetC	R/W	Phase C Reactive Power Offset		
47H	GainA	R/W	Phase A calibration gain		P 55
48H	PhiA	R/W	Phase A calibration phase angle		P 55
49H	GainB	R/W	Phase B calibration gain		
4AH	PhiB	R/W	Phase B calibration phase angle		
4BH	GainC	R/W	Phase C calibration gain		
4CH	PhiC	R/W	Phase C calibration phase angle		
4DH	CS1	R/W	Checksum 1		
Fundamental/ Harmonic Energy Calibration registers					
50H	HarmStart	R/W	Harmonic Calibration Startup Command	Refer to Table-7.	
51H	POffsetAF	R/W	Phase A Fundamental Active Power Offset		
52H	POffsetBF	R/W	Phase B Fundamental Active Power Offset		
53H	POffsetCF	R/W	Phase C Fundamental Active Power Offset		
54H	PGainAF	R/W	Phase A Fundamental Active Power Gain		
55H	PGainBF	R/W	Phase B Fundamental Active Power Gain		
56H	PGainCF	R/W	Phase C Fundamental Active Power Gain		
57H	CS2	R/W	Checksum 2		

Table-4 Register List (Continued)

Register Address	Register Name	Read/Write Type	Functional Description	Comment	Page
Measurement Calibration					
60H	AdjStart	R/W	Measurement Calibration Startup Command	Refer to Table-8.	
61H	UgainA	R/W	Phase A Voltage RMS Gain		
62H	IgainA	R/W	Phase A Current RMS Gain		
63H	UoffsetA	R/W	Phase A Voltage RMS Offset		
64H	IoffsetA	R/W	Phase A Current RMS Offset		
65H	UgainB	R/W	Phase B Voltage RMS Gain		
66H	IgainB	R/W	Phase B Current RMS Gain		
67H	UoffsetB	R/W	Phase B Voltage RMS Offset		
68H	IoffsetB	R/W	Phase B Current RMS Offset		
69H	UgainC	R/W	Phase C Voltage RMS Gain		
6AH	IgainC	R/W	Phase C Current RMS Gain		
6BH	UoffsetC	R/W	Phase C Voltage RMS Offset		
6CH	IoffsetC	R/W	Phase C Current RMS Offset		
6DH	IgainN	R/W	Sampled N line Current RMS Gain		
6EH	IoffsetN	R/W	Sampled N line Current RMS Offset		
6FH	CS3	R/W	Checksum 3		
Energy Register					
80H	APenergyT	R/C	Total Forward Active Energy	Refer to Table-9.	
81H	APenergyA	R/C	Phase A Forward Active Energy		
82H	APenergyB	R/C	Phase B Forward Active Energy		
83H	APenergyC	R/C	Phase C Forward Active Energy		
84H	ANenergyT	R/C	Total Reverse Active Energy		
85H	ANenergyA	R/C	Phase A Reverse Active Energy		
86H	ANenergyB	R/C	Phase B Reverse Active Energy		
87H	ANenergyC	R/C	Phase C Reverse Active Energy		
88H	RPenergyT	R/C	Total Forward Reactive Energy		
89H	RPenergyA	R/C	Phase A Forward Reactive Energy		
8AH	RPenergyB	R/C	Phase B Forward Reactive Energy		
8BH	RPenergyC	R/C	Phase C Forward Reactive Energy		
8CH	RNenergyT	R/C	Total Reverse Reactive Energy		
8DH	RNenergyA	R/C	Phase A Reverse Reactive Energy		
8EH	RNenergyB	R/C	Phase B Reverse Reactive Energy		
8FH	RNenergyC	R/C	Phase C Reverse Reactive Energy		
90H	SAenergyT	R/C	Total (Arithmetic Sum) Apparent Energy		
91H	SenergyA	R/C	Phase A Apparent Energy		
92H	SenergyB	R/C	Phase B Apparent Energy		
93H	SenergyC	R/C	Phase C Apparent Energy		
94H	SVenergyT	R/C	(Vector Sum) Total Apparent Energy		
95H	EnStatus0	R	Metering Status 0		P 58
96H	EnStatus1	R	Metering Status 1		P 58
98H	SVmeanT	R	(Vector Sum) Total Apparent Power		
99H	SVmeanTLSB	R	LSB of (Vector Sum) Total Apparent Power		

Table-4 Register List (Continued)

Register Address	Register Name	Read/Write Type	Functional Description	Comment	Page
Fundamental / Harmonic Energy Register					
A0H	APenergyTF	R/C	Total Forward Active Fundamental Energy	Refer to Table-10.	P 59
A1H	APenergyAF	R/C	Phase A Forward Active Fundamental Energy		
A2H	APenergyBF	R/C	Phase B Forward Active Fundamental Energy		
A3H	APenergyCF	R/C	Phase C Forward Active Fundamental Energy		
A4H	ANenergyTF	R/C	Total Reverse Active Fundamental Energy		
A5H	ANenergyAF	R/C	Phase A Reverse Active Fundamental Energy		
A6H	ANenergyBF	R/C	Phase B Reverse Active Fundamental Energy		
A7H	ANenergyCF	R/C	Phase C Reverse Active Fundamental Energy		
A8H	APenergyTH	R/C	Total Forward Active Harmonic Energy		
A9H	APenergyAH	R/C	Phase A Forward Active Harmonic Energy		
AAH	APenergyBH	R/C	Phase B Forward Active Harmonic Energy		
ABH	APenergyCH	R/C	Phase C Forward Active Harmonic Energy		
ACH	ANenergyTH	R/C	Total Reverse Active Harmonic Energy		
ADH	ANenergyAH	R/C	Phase A Reverse Active Harmonic Energy		
AEH	ANenergyBH	R/C	Phase B Reverse Active Harmonic Energy		
AFH	ANenergyCH	R/C	Phase C Reverse Active Harmonic Energy		

Table-4 Register List (Continued)

Register Address	Register Name	Read/Write Type	Functional Description	Comment	Page
Power and Power Factor Registers					
B0H	PmeanT	R	Total (all-phase-sum) Active Power	Refer to Table-11.	P 59
B1H	PmeanA	R	Phase A Active Power		
B2H	PmeanB	R	Phase B Active Power		
B3H	PmeanC	R	Phase C Active Power		
B4H	QmeanT	R	Total (all-phase-sum) Reactive Power		
B5H	QmeanA	R	Phase A Reactive Power		
B6H	QmeanB	R	Phase B Reactive Power		
B7H	QmeanC	R	Phase C Reactive Power		
B8H	SAmeanT	R	Total (Arithmetic Sum) apparent power		
B9H	SmeanA	R	phase A apparent power		
BAH	SmeanB	R	phase B apparent power		
BBH	SmeanC	R	phase C apparent power		
BCH	PFmeanT	R	Total power factor		
BDH	PFmeanA	R	phase A power factor		
BEH	PFmeanB	R	phase B power factor		
BFH	PFmeanC	R	phase C power factor		
C0H	PmeanTLSB	R	Lower word of Total (all-phase-sum) Active Power		
C1H	PmeanALSB	R	Lower word of Phase A Active Power		
C2H	PmeanBLSB	R	Lower word of Phase B Active Power		
C3H	PmeanCLSB	R	Lower word of Phase C Active Power		
C4H	QmeanTLSB	R	Lower word of Total (all-phase-sum) Reactive Power		
C5H	QmeanALSB	R	Lower word of Phase A Reactive Power		
C6H	QmeanBLSB	R	Lower word of Phase B Reactive Power		
C7H	QmeanCLSB	R	Lower word of Phase C Reactive Power		
C8H	SAmeanTLSB	R	Lower word of Total (Arithmetic Sum) apparent power		
C9H	SmeanALSB	R	Lower word of phase A apparent power		
CAH	SmeanBLSB	R	Lower word of phase B apparent power		
CBH	SmeanCLSB	R	Lower word of phase C apparent power		

Table-4 Register List (Continued)

Register Address	Register Name	Read/Write Type	Functional Description	Comment	Page
Fundamental / Harmonic Power and Voltage / Current RMS Registers					
D0H	PmeanTF	R	Total active fundamental power	Refer to Table-12.	P 60
D1H	PmeanAF	R	phase A active fundamental power		
D2H	PmeanBF	R	phase B active fundamental power		
D3H	PmeanCF	R	phase C active fundamental power		
D4H	PmeanTH	R	Total active harmonic power		
D5H	PmeanAH	R	phase A active harmonic power		
D6H	PmeanBH	R	phase B active harmonic power		
D7H	PmeanCH	R	phase C active harmonic power		
D8H	IrmsN1	R	N Line Sampled current RMS		
D9H	UrmsA	R	phase A voltage RMS		
DAH	UrmsB	R	phase B voltage RMS		
DBH	UrmsC	R	phase C voltage RMS		
DCH	IrmsN0	R	N Line calculated current RMS		
DDH	IrmsA	R	phase A current RMS		
DEH	IrmsB	R	phase B current RMS		
DFH	IrmsC	R	phase C current RMS		
E0H	PmeanTFLSB	R	Lower word of Total active fundamental Power		
E1H	PmeanAFLSB	R	Lower word of phase A active fundamental Power		
E2H	PmeanBFLSB	R	Lower word of phase B active fundamental Power		
E3H	PmeanCFLSB	R	Lower word of phase C active fundamental Power		
E4H	PmeanTHLSB	R	Lower word of Total active harmonic Power		
E5H	PmeanAHLSB	R	Lower word of phase A active harmonic Power		
E6H	PmeanBHLSB	R	Lower word of phase B active harmonic Power		
E7H	PmeanCHLSB	R	Lower word of phase C active harmonic Power		
E9H	UrmsALSB	R	Lower word of phase A voltage RMS		
EAH	UrmsBLSB	R	Lower word of phase B voltage RMS		
EBH	UrmsCLSB	R	Lower word of phase C voltage RMS		
EDH	IrmsALSB	R	Lower word of phase A current RMS		
EEH	IrmsBLSB	R	Lower word of phase B current RMS		
EFH	IrmsCLSB	R	Lower word of phase C current RMS		

Table-4 Register List (Continued)

Register Address	Register Name	Read/Write Type	Functional Description	Comment	Page
THD+N, Frequency, Angle and Temperature Registers					
F1H	THDNUA	R	phase A voltage THD+N	Refer to Table-12.	P 61
F2H	THDNUB	R	phase B voltage THD+N		
F3H	THDNUC	R	phase C voltage THD+N		
F5H	THDNIA	R	phase A current THD+N		
F6H	THDNIB	R	phase B current THD+N		
F7H	THDNIC	R	phase C current THD+N		
F8H	Freq	R	Frequency		
F9H	PAngleA	R	phase A mean phase angle		
FAH	PAngleB	R	phase B mean phase angle		
FBH	PAngleC	R	phase C mean phase angle		
FCH	Temp	R	Measured temperature		
FDH	UangleA	R	phase A voltage phase angle		
FEH	UangleB	R	phase B voltage phase angle		
FFH	UangleC	R	phase C voltage phase angle		
Harmonic Fourier Analysis Registers					
100H ~ 1BFH		R		Refer to Table-13.	P 62
1D0H ~ 1D1H		R/W			

6.2 SPECIAL REGISTERS

6.2.1 SOFT RESET REGISTER

SoftReset
Software Reset

Address: 00H
Type: Write
Default Value: 0000H

Bit	Name	Description
15 - 0	SoftReset[15:0]	Software reset register. The 90E36A resets only if 789AH is written to this register. The reset domain is the same as the $\overline{\text{RESET}}$ pin or Power On Reset. Reading this register always return 0.

6.2.2 IRQ AND WARNOUT SIGNAL GENERATION

Status bits in the SysStatus0 register generate an interrupt and get the IRQ0 pin to be asserted if the corresponding enable bits are set in the FuncEn0 register.

Status bits in the SysStatus1 register generate an interrupt and get the IRQ1 pin to be asserted, if the corresponding enable bits are set in the FuncEn1 register.

Some of the status signals can also assert the WarnOut pin.

The following diagram illustrates how the status bits, enable bits and IRQ/ WarnOut pins work together.

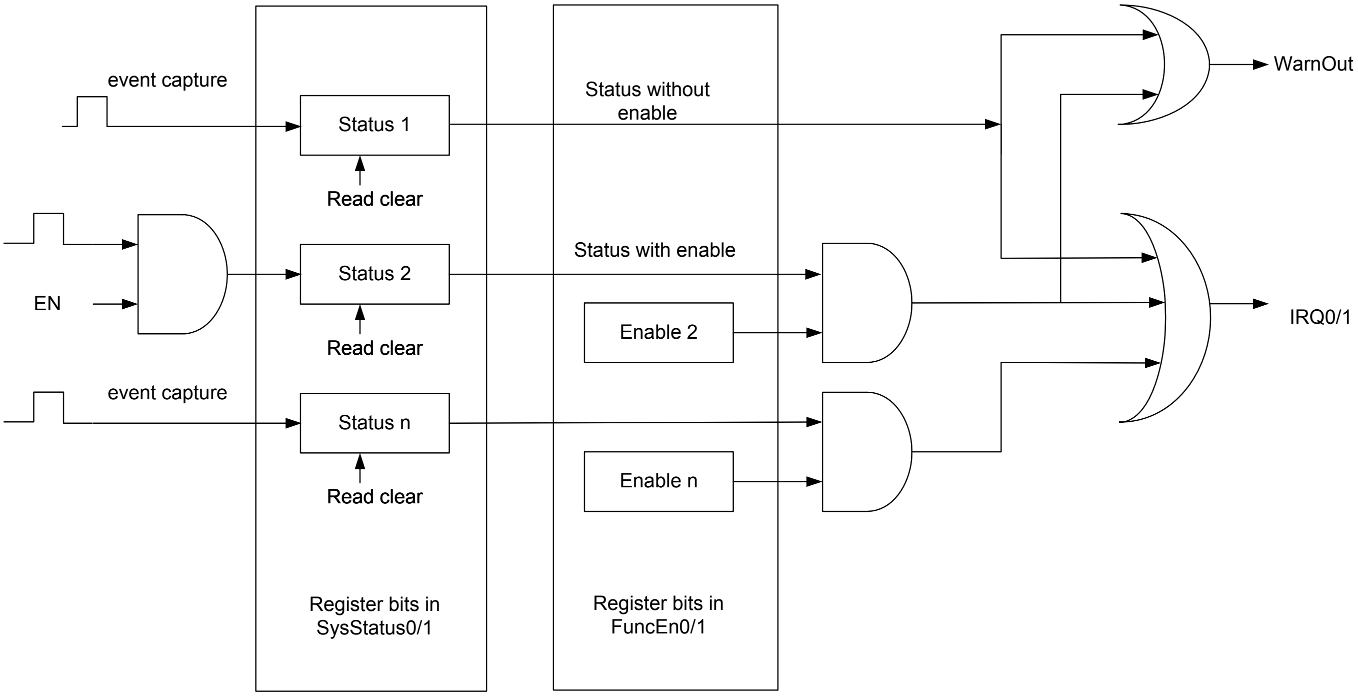


Figure-14 IRQ and WarnOut Generation

SysStatus0
System Status 0

Address: 01H
Type: Read/Clear
Default Value: 0000H

Bit	Name	Description
15	-	Reserved. *
14	CS0Err	This bit indicates CS0 (3BH) checksum status. 0: CS0 checksum correct (default) 1: CS0 checksum error. The WarnOut pin is asserted at the same time.
13	-	Reserved.
12	CS1Err	This bit indicates CS1 (4DH) checksum status. 0: CS1 checksum correct (default) 1: CS1 checksum error. The WarnOut pin is asserted at the same time.
11	-	Reserved.
10	CS2Err	This bit indicates CS2 (57H) checksum status. 0: CS2 checksum correct (default) 1: CS2 checksum error. The WarnOut pin is asserted at the same time.
9	-	Reserved.
8	CS3Err	This bit indicates CS3 (6FH) checksum status. 0: CS3 checksum correct (default) 1: CS3 checksum error. The WarnOut pin is asserted at the same time.
7	URevWn	This bit indicates whether there is any error with the voltage phase sequence. 0: No error with the voltage phase sequence (default) 1: Error with the voltage phase sequence.
6	IRevWn	This bit indicates whether there is any error with the current phase sequence. 0: No error with the current phase sequence (default) 1: Error with the current phase sequence.
5 - 4	-	Reserved.
3	SagWarn	This bit indicates whether there is any voltage sag (voltage lower than threshold) in one phase or more. 0: No voltage sag (default) 1: Voltage sag.
2	PhaseLoseWn	This bit indicates whether there is any voltage phase losing in one phase or more. 0: No voltage phase losing (default) 1: Voltage phase losing.
1-0	-	Reserved.

Note: All reserved bits of any register should be ignored when reading and should be written with zero.

SysStatus1
System Status 1

Address: 02H
Type: Read/Clear
Default Value: 0000H

Bit	Name	Description
15	INOv1	This bit indicates whether the N line current sampling value is greater than the threshold set by the INWarnTh1 register. 0: Not greater than the threshold (default) 1: Greater than the threshold.
14	INOv0	This bit indicates whether the calculated N line current is greater than the threshold set by the INWarnTh0 register. 0: Not greater than the threshold (default) 1: Greater than the threshold.
13-12	-	Reserved.
11	THDUOv	This bit indicates whether one or more voltage THDUx (THDUA/ THDUB/ THDUC) is greater than the threshold set by the THDNUTh register. 0: Not greater than the threshold (default) 1: Greater than the threshold.
10	THDIOv	This bit indicates whether one or more current THDIx (THDIA/ THDIB/ THDIC) is greater than the threshold set by the THDNITh register. 0: Not greater than the threshold (default) 1: Greater than the threshold.
9	DFTDone	This bit indicates whether the DFT data is ready. 0: Not ready (default) 1: Ready.
8	-	Reserved.
7	RevQchgT	When there is any direction change of active/reactive energy for all-phase-sum or individual phase (from forward to reverse, or from reverse to forward), the corresponding status bit is set. The judgment of direction change is solely based on the energy register (not related to the CF pulses), and dependent on the energy register resolution (0.01CF / 0.1CF setting set by the 001LSB bit (b9, MMode0)). 0: direction of active/reactive energy no change (default) 1: direction of active/reactive energy changed The status bits are RevQchgT/ RevPchgT are status bits for all-phase-sum and RevQchgA/ RevQchgB/ RevQchgC/ RevPchgA/ RevPchgB/ RevPchgC are for individual phase.
6	RevQchgA	
5	RevQchgB	
4	RevQchgC	
3	RevPchgT	
2	RevPchgA	
1	RevPchgB	
0	RevPchgC	

FuncEn0
Function Enable 0

Address: 03H
Type: Read/Write
Default Value: 0000H

Bit	Name	Description
15-11	-	Reserved.
10	CS2ErrEn	This bit determines whether to enable the interrupt when the CS2Err bit (b10, SysStatus0) is set. 0: disable (default) 1: enable
9-8	-	Reserved.
7	URevWnEn	This bit determines whether to enable the interrupt when the URevWn bit (b7, SysStatus0) is set. 0: disable (default) 1: enable
6	IRevWnEn	This bit determines whether to enable the interrupt when the IRevWn bit (b6, SysStatus0) is set. 0: disable (default) 1: enable
5-4	-	Reserved.
3	SagWnEn	This bit determines whether to enable the voltage sag interrupt when the SagWarn bit (b3, SysStatus0) is set. 0: disable (default) 1: enable
2	PhaseLoseWnEn	This bit determines whether to enable the interrupt when the PhaseLoseWn bit (b2, SysStatus0) is set. 0: disable (default) 1: enable
1-0	-	Reserved.

FuncEn1
Function Enable 1

Address: 04H
Type: Read/Write
Default Value: 0000H

Bit	Name	Description
15	INOv1En	This bit determines whether to enable the interrupt when the INOv1 bit (b15, SysStatus1) is set. 0: disable (default) 1: enable
14	INOv0En	This bit determines whether to enable the interrupt when the INOv0 bit (b14, SysStatus1) is set. 0: disable (default) 1: enable
13-12	-	Reserved.
11	THDUOvEn	This bit determines whether to enable the interrupt when the THDUOv bit (b11, SysStatus1) is set. 0: disable (default) 1: enable
10	THDIOvEn	This bit determines whether to enable the interrupt when the THDIOv bit (b10, SysStatus1) is set. 0: disable (default) 1: enable
9	DFTDone	This bit determines whether to enable the interrupt when the DFTDone bit (b9, SysStatus1) is set. 0: disable (default) 1: enable
8	-	Reserved.
7	RevQchgTEn	These bits determine whether to enable the corresponding interrupt when any of the direction change bits (b7~b0, SysStatus1) is set. 0: disable (default) 1: enable
6	RevQchgAEn	
5	RevQchgBEn	
4	RevQchgCEn	
3	RevPchgTEn	
2	RevPchgAEn	
1	RevPchgBEn	
0	RevPchgCEn	

6.2.3 SPECIAL CONFIGURATION REGISTERS

ZXConfig
Zero-Crossing Configuration

<table>
<tr><td colspan="3">Address: 07H
Type: Read/Write
Default Value: 0001H</td></tr>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15:13</td><td>ZX2Src[2:0]</td><td rowspan="3">These bits select the signal source for the ZX2, ZX1 or ZX0 pins.
<table>
<tr><th>Code</th><th>Source</th></tr>
<tr><td>011</td><td>Fixed-0</td></tr>
<tr><td>000</td><td>Ua</td></tr>
<tr><td>001</td><td>Ub</td></tr>
<tr><td>010</td><td>Uc</td></tr>
<tr><td>111</td><td>Fixed-0</td></tr>
<tr><td>100</td><td>Ia</td></tr>
<tr><td>101</td><td>Ib</td></tr>
<tr><td>110</td><td>Ic</td></tr>
</table></td></tr>
<tr><td>12:10</td><td>ZX1Src[2:0]</td></tr>
<tr><td>9:7</td><td>ZX0Src[2:0]</td></tr>
<tr><td>6:5</td><td>ZX2Con[1:0]</td><td rowspan="3">These bits configure zero-crossing mode for the ZX2, ZX1 and ZX0 pins.
<table>
<tr><th>Code</th><th>Zero-Crossing Configuration</th></tr>
<tr><td>00</td><td>positive zero-crossing</td></tr>
<tr><td>01</td><td>negative zero-crossing</td></tr>
<tr><td>10</td><td>all zero-crossing</td></tr>
<tr><td>11</td><td>no zero-crossing output</td></tr>
</table></td></tr>
<tr><td>4:3</td><td>ZX1Con[1:0]</td></tr>
<tr><td>2:1</td><td>ZX0Con[1:0]</td></tr>
<tr><td>0</td><td>ZXdis</td><td>This bit determines whether to disable the ZX signals:
0: enable
1: disable all the ZX signals to ‘0’ (default).</td></tr>
</table>

SagTh
Voltage Sag Threshold

<table>
<tr><td colspan="3">Address: 08H
Type: Read/Write
Default Value: 0000H</td></tr>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15:0</td><td>SagTh</td><td>Unsigned 16-bit integer with unit related to PGA and voltage sense circuits. Refer to 3.8.2 Sag Detection.</td></tr>
</table>

PhaseLossTh
Voltage Phase Losing Threshold

<table>
<tr><td colspan="3">Address: 09H
Type: Read/Write
Default Value: 0000H</td></tr>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15:0</td><td>PhaseLossTh</td><td>Unsigned 16-bit integer with unit related to PGA and voltage sense circuits. Refer to 3.8.3 Phase Loss Detection.</td></tr>
</table>

INWarnTh0
Neutral Current (Calculated) Warning Threshold

Address: 0AH
Type: Read/Write
Default Value: FFFFH

Bit	Name	Description
15:0	INWarnTh0	Neutral current (calculated) warning threshold. Threshold for calculated (Ia + Ib +Ic) N line rms current. Unsigned 16 bit, unit 1mA. If N line rms current is greater than the threshold, The INOv0 bit (b14, SysStatus1) will be asserted if enabled. Refer to 3.8.4.2 Computed N-Line.

INWarnTh1
Neutral Current (Sampled) Warning Threshold

Address: 0BH
Type: Read/Write
Default Value: FFFFH

Bit	Name	Description
15:0	INWarnTh1	Neutral Current (Sampled) Warning threshold. Threshold for sampled (from ADC) N line rms current. Unsigned 16 bit, unit 1mA. If N line rms current is greater than the threshold, The INOv1 bit (b15, SysStatus1) will be asserted if enabled. Refer to 3.8.4.1 Sampled N-Line.

THDNUTh
Voltage THD Warning Threshold

Address: 0CH
Type: Read/Write
Default Value: FFFFH

Bit	Name	Description
15:0	THDNUTh	Voltage THD Warning threshold. Voltage THD+N Threshold. Unsigned 16 bit, unit 0.01%. Exceeding the threshold will assert the THDUOv bit (b11, SysStatus1) if enabled.

THDNITh
Current THD Warning Threshold

Address: 0DH
Type: Read/Write
Default Value: FFFFH

Bit	Name	Description
15:0	THDNITh	Current THD Warning threshold. Current THD+N Threshold. Unsigned 16-bit, unit 0.01%. Exceeding the threshold will assert the THDIOv bit (b10, SysStatus1) if enabled.

DMACtrl
DMA Mode Interface Control

<table>
<tr><td colspan="3">Address: 0EH
Type: Read/Write
Default Value: 7E44H</td></tr>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15:9</td><td>ADC_CH_SEL</td><td>These bits configure the data source of the ADC channel. Each bit enables the data dumping for one ADC channel as the following diagram shows. Set a ‘1’ to a bit enables the dumping of the corresponding ADC channel samples.
<table>
<tr><td>b15</td><td>b14</td><td>b13</td><td>b12</td><td>b11</td><td>b10</td><td>b9</td></tr>
<tr><td>↓</td><td>↓</td><td>↓</td><td>↓</td><td>↓</td><td>↓</td><td>↓</td></tr>
<tr><td>I4</td><td>I1</td><td>V1</td><td>I2</td><td>V2</td><td>I3</td><td>V3</td></tr>
</table>
Note: I1 to phase A and I3 to phase C mapping can be swapped by configuring the I1I3Swap bit (b13, MMode0).</td></tr>
<tr><td>8</td><td>PIN_DIR_SEL</td><td>This bit configures the direction of the SDI and SDO pins.
<table>
<tr><th>PIN_DIR_SEL</th><th>Master Mode (DMA_Ctrl=1)</th></tr>
<tr><td rowspan="2">0</td><td>SDI→MOSI</td></tr>
<tr><td>SDO←MISO</td></tr>
<tr><td rowspan="2">1</td><td>SDI←MISO</td></tr>
<tr><td>SDO→MOSI</td></tr>
</table></td></tr>
<tr><td>7:6</td><td>CH_BIT_WIDTH</td><td>These bits configure the bit width for each channel.
<table>
<tr><th>Code</th><th>Channel Bit Width</th></tr>
<tr><td>00</td><td>32 bits</td></tr>
<tr><td>01</td><td>24 bits (default)</td></tr>
<tr><td>10</td><td>16 bits</td></tr>
<tr><td>11</td><td>reserved</td></tr>
</table></td></tr>
<tr><td>5</td><td>CLK_IDLE</td><td>This bit configures the Idle state clock level.
0: Idle low (default)
1: Idle High</td></tr>
<tr><td>4</td><td>CLK_DRV</td><td>This bit configures which edge to drive data out.
0: Second edge drives data out. (default)
1: First edge drives data out.</td></tr>
<tr><td>3:0</td><td>CLK_DIV</td><td>Divide ratio to generate SCLK frequency from SYS_CLK. Default value is ‘100’.</td></tr>
</table>

6.2.4 LAST SPI DATA REGISTER

LastSPIData
Last Read/Write SPI Value

<table>
<tr><td colspan="3">Address: 0FH
Type: Read
Default Value: 0000H</td></tr>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15:0</td><td>LastSPIData15 - LastSPIData0</td><td>This register is a special register which logs data of the previous SPI Read or Write access especially for Read/Clear registers.
This register is useful when the user wants to check the integrity of the last SPI access.</td></tr>
</table>

6.3 LOW-POWER MODES REGISTERS

6.3.1 DETECTION MODE REGISTERS

Current Detection register latching scheme is:

When any of the 4 current detection registers (0x10 - 0x13) were programmed, all the 4 current detection registers (including the registers that not being programmed) will be automatically latched into the current detector's internal configuration latches at the same time. Those latched configuration values are not subject to digital reset signals and will be kept in all the 4 power modes. The power up value of those latches is not deterministic, so user needs to program the current detection registers to update.

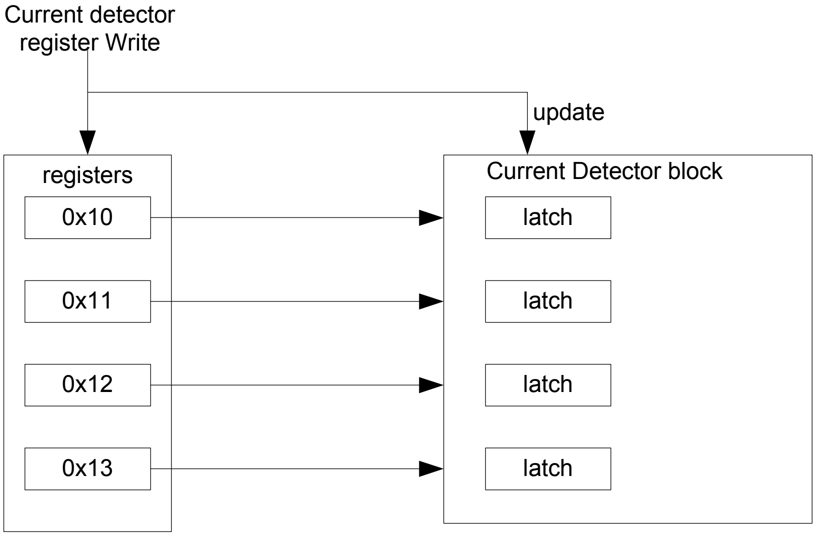


Figure-15 Current Detection Register Latching Scheme

DetectCtrl
Current Detect Control

Address: 10H
Type: Read/Write
Default Value: 0000H

Bit	Name	Description
15:6	-	Reserved.
5:0	DetectCtrl	Detector power-down, active high: [5:3]: Power-down for negative detector of channel 3/2/1; [2:0]: Power-down for positive detector of channel 3/2/1.

DetectTh1
Channel 1 Current Threshold in Detection Mode

Address: 11H
Type: Read/Write
Default Value: 0000H

Bit	Name	Description
15	-	Reserved.
14:8	CalCodeN	Channel 1 current negative detector calculation code. Code mapping: 7'b000-0000, Vc=-4.28mV=-3.03mVrms (Vc is the threshold of low power computation) 7'b111-1111, Vc=12.91mV=9.14mVrms DAC typical resolution is [12.91-(-4.28)]/127=135.4µV=95.7µVrms
7	-	Reserved.
6:0	CalCodeP	Channel 1 current positive detector calculation code. Code mapping: 7'b000-0000, Vc=-4.28mV=-3.03mVrms (Vc is the threshold of low power computation) 7'b111-1111, Vc=12.91mV=9.14mVrms DAC typical resolution is [12.91-(-4.28)]/127=135.4µV=95.7µVrms

DetectTh2
Channel 2 Current Threshold in Detection Mode

Address: 12H
Type: Read/Write
Default Value: 0000H

Bit	Name	Description
15	-	Reserved.
14:8	CalCodeN	Channel 2 current negative detector calculation code. Code mapping: 7'b000-0000, Vc=-4.28mV=-3.03mVrms (Vc is the threshold of low power computation) 7'b111-1111, Vc=12.91mV=9.14mVrms DAC typical resolution is [12.91-(-4.28)]/127=135.4µV=95.7µVrms
7	-	Reserved.
6:0	CalCodeP	Channel 2 current positive detector calculation code. Code mapping: 7'b000-0000, Vc=-4.28mV=-3.03mVrms (Vc is the threshold of low power computation) 7'b111-1111, Vc=12.91mV=9.14mVrms DAC typical resolution is [12.91-(-4.28)]/127=135.4µV=95.7µVrms

DetectTh3
Channel 3 Current Threshold in Detection Mode

Address: 13H Type: Read/Write Default Value: 0000H		
Bit	**Name**	**Description**
15	-	Reserved.
14:8	CalCodeN	Channel 3 current negative detector calculation code. Code mapping: 7'b000-0000, Vc=-4.28mV=-3.03mVrms (Vc is the threshold of low power computation) 7'b111-1111, Vc=12.91mV=9.14mVrms DAC typical resolution is [12.91-(-4.28)]/127=135.4µV=95.7µVrms
7	-	Reserved.
6:0	CalCodeP	Channel 3 current positive detector calculation code. Code mapping: 7'b000-0000, Vc=-4.28mV=-3.03mVrms (Vc is the threshold of low power computation) 7'b111-1111, Vc=12.91mV=9.14mVrms DAC typical resolution is [12.91-(-4.28)]/127=135.4µV=95.7µVrms

The calibration method is that, the user program the detection threshold and test with the standard input signal until the output trips.

6.3.2 PARTIAL MEASUREMENT MODE REGISTERS

PMOffsetA
Ioffset for phase A in Partial Measurement mode

Address: 14H Type: Read/Write Default Value: 0000H		
Bit	**Name**	**Description**
15-14	-	Reserved.
13:0	PMOffsetA	Phase A current offset in Partial Measurement mode.

PMOffsetB
Ioffset for phase B in Partial Measurement mode

Address: 15H Type: Read/Write Default Value: 0000H		
Bit	**Name**	**Description**
15-14	-	Reserved.
13:0	PMOffsetB	Phase B current offset in Partial Measurement mode.

PMOffsetC
Ioffset for phase C in Partial Measurement mode

Address: 16H Type: Read/Write Default Value: 0000H		
Bit	**Name**	**Description**
15-14	-	Reserved.
13:0	PMOffsetC	Phase C current offset in Partial Measurement mode.

PMPGA
PGAgain Configuration in Partial Measurement mode

Address: 17H Type: Read/Write Default Value: 0000H		
Bit	**Name**	**Description**
15-14	DPGA	DPGA in Partial Measurement mode.
13:0	PGAGain	PGAGain in Partial Measurement mode Refer to the MMode1 register for encoding and mapping.

PMIrmsA
Irms for phase A in Partial Measurement mode

Address: 18H Type: Read Default Value: 0000H		
Bit	**Name**	**Description**
15:0	PMIrmsA*	Current RMS/mean result in Partial Measurement mode. Format: It is unsigned for RMS while signed for mean value.
Note: For current measuring in Partial Measurement mode, current gain is suggested to realized by external MCU and current RMS value shall not exceed 40A.		

PMIrmsB
Irms for phase B in Partial Measurement mode

Address: 19H Type: Read Default Value: 0000H		
Bit	**Name**	**Description**
15:0	PMIrmsB*	Current RMS/mean result in Partial Measurement mode. Format: It is unsigned for RMS while signed for mean value.
Note: For current measuring in Partial Measurement Mode, current gain is suggested to realized by external MCU and current RMS value shall not exceed 40A.		

PMIrmsC
Irms for phase C in Partial Measurement mode

Address: 1AH Type: Read Default Value: 0000H		
Bit	**Name**	**Description**
15:0	PMIrmsC*	Current RMS/mean result in Partial Measurement mode. Format: It is unsigned for RMS while signed for mean value.
Note: For current measuring in Partial Measurement Mode, current gain is suggested to realized by external MCU and current RMS value shall not exceed 40A.		

PMConfig
Measure Configuration in Partial Measurement mode

Address: 1BH
Type: Read/Write
Default Value: 0000H

Bit	Name	Description
15	-	Reserved.
14	ReMeasure	This bit is ‘1’-write-only. Write ‘1’ to this bit will trigger another measurement cycle.
13	MeasureStartZX	This bit configures start of measurement whether starts from zero crossing point. 0: Measurement start immediately (default) 1: Measurement start from zero-crossing point
12	MeasureType	This bit indicates the measurement type. 0: RMS measurement (default) 1: Mean Value (DC Average) measurement
11-1	-	Reserved.
0	PMBusy	This bit indicates the measure status. This bit is read-only. 0: Measurement done (default) 1: Measurement in progress

PMAvgSamples
Number of 8K Samples to be Averaged

Address: 1CH
Type: Read
Default Value: 00A0H

Bit	Name	Description
15:0	-	Number of 8K samples to be averaged in RMS/mean computation.

PMIrmsLSB
LSB bits of PMRrms[A/B/C]

Address: 1DH
Type: Read
Default Value: 0000H

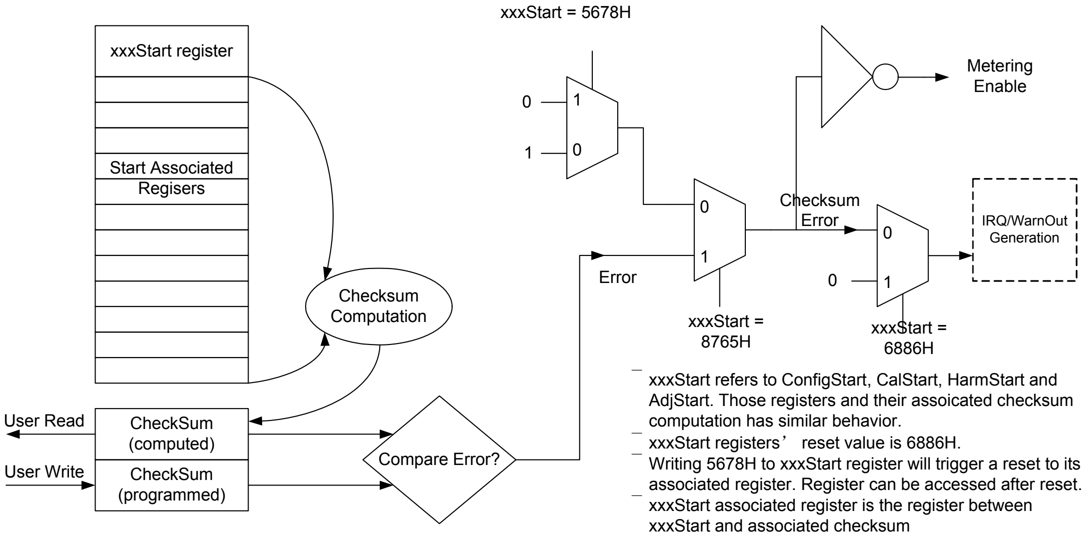
Bit	Name	Description
15:12	-	Reserved.
11:8	IrmsCLSB	These bits indicate LSB of the corresponding phase RMS measurement result if the MeasureType bit (b12, PMConfig) =0. These bits indicate MSB of the corresponding phase mean measurement result if the MeasureType bit (b12, PMConfig) =1.
7:4	IrmsBLSB	
3:0	IrmsALSB	

6.4 CONFIGURATION AND CALIBRATION REGISTERS

6.4.1 START REGISTERS AND ASSOCIATED CHECKSUM OPERATION SCHEME

The Start Registers (ConfigStart (30H), CalStart (40H), HarmStart (50H) and AdjStart (60H)) and associated registers / checksum have a special operation scheme to protect important configuration data, illustrated below in the diagram. Start registers have multiple valid settings for different operation modes.

Start Register Value	Usage	Operation
6886H	Power up state	It is the value after reset. This state blocks checksum checking error generation
5678H	Calibration	Similar like 6886H, This state blocks checksum checking error generation. Writing with this value trigger a reset to the associated registers.
8765H	Operation	Checksum checking is enabled and if error detected, IRQ/Warn is asserted and Metering stopped.
Other	Error	Force checksum error generation and system stop.



- xxxStart refers to ConfigStart, CalStart, HarmStart and AdjStart. Those registers and their assoicated checksum computation has similar behavior.
- xxxStart registers’ reset value is 6886H.
- Writing 5678H to xxxStart register will trigger a reset to its associated register. Register can be accessed after reset.
- xxxStart associated register is the register between xxxStart and associated checksum

Figure-16 Start and Checksum Register Operation Scheme

6.4.2 CONFIGURATION REGISTERS

Table-5 Configuration Registers

Register Address	Register Name	Read/Write Type	Functional Description	Power-on Value and Comments
		Configuration Registers*		
30H	ConfigStart	R/W	Calibration Start Command	6886H
31H	PLconstH	R/W	High Word of PL_Constant	0861H
32H	PLconstL	R/W	Low Word of PL_Constant	C468H
33H	MMode0	R/W	HPF/Integrator On/off, CF and all-phase energy computation configuration	0087H
34H	MMode1	R/W	PGA gain configuration	0000H
35H	PStartTh	R/W	Active Startup Power Threshold. 16 bit unsigned integer, Unit: 0.00032 Watt	0000H.
36H	QStartTh	R/W	Reactive Startup Power Threshold. 16 bit unsigned integer, Unit: 0.00032 var	0000H
37H	SStartTh	R/W	Apparent Startup Power Threshold. 16 bit unsigned integer, Unit: 0.00032 VA	0000H

Table-5 Configuration Registers

Register Address	Register Name	Read/Write Type	Functional Description	Power-on Value and Comments
38H	PPhaseTh	R/W	Startup power threshold (for |P|+|Q| of a phase) for any phase participating Active Energy Accumulation. Common for phase A/B/C.	0000H 16 bit unsigned integer, Unit: 0.00032 Watt/var
39H	QPhaseTh	R/W	Startup power threshold (for |P|+|Q| of a phase) for any phase participating ReActive Energy Accumulation. Common for phase A/B/C.	0000H 16bit unsigned integer, Unit: 0.00032 Watt/var
3AH	SPhaseTh	RW	Startup power threshold (for |P|+|Q| of a phase) for any phase participating Apparent Energy Accumulation. Common for phase A/B/C.	0000H 16 bit unsigned integer, Unit: 0.00032 Watt/var
3BH	CS0	R/W	Checksum 0 Checksum register.	421CH (calculated value after reset)
Note: For details, please refer to application note AN-644.				

ConfigStart
Configure Start Command

Address: 30H
Type: Read/Write
Default Value: 6886H

Bit	Name	Description
15 - 0	CalStart[15:0]	Refer to 6.4.1 Start Registers and Associated Checksum Operation Scheme.

PLconstH
High Word of PL_Constant

Address: 31H
Type: Read/Write
Default Value: 0861H

Bit	Name	Description
15 - 0	PLconstH[15:0]	The PLconstH[15:0] and PLconstL[15:0] bits are high word and low word of PL_Constant respectively. PL_Constant is a constant which is proportional to the sampling ratios of voltage and current, and inversely proportional to the Meter Constant. PL_Constant is a threshold for energy calculated inside the chip, i.e., energy larger than PL_Constant will be accumulated as 0.01CFx in the corresponding energy registers and then output on CFx if one CF reaches. It is suggested to set PL_constant as a multiple of 4 so as to double or redouble Meter Constant in low current state to save verification time.

PLconstL
Low Word of PL_Constant

Address: 32H
Type: Read/Write
Default Value: C468H

Bit	Name	Description
15 - 0	PLconstL[15:0]	The PLconstH[15:0] and PLconstL[15:0] bits are high word and low word of PL_Constant respectively. It is suggested to set PL_constant as a multiple of 4.

MMode0
Metering method configuration

Address: 33H
Type: Read/Write
Default Value: 0087H

Bit	Name	Description
15-14	-	Reserved.
13	I1I3Swap	This bit defines phase mapping for I1 and I3: 0: I1 maps to phase A, I3 maps to phase C (default) 1: I1 maps to phase C, I3 maps to phase A Note: I2 always maps to phase B.
12	Freq60Hz	Current Grid operating line frequency. 0: 50Hz (default) 1: 60Hz
11	HPFOff	Disable HPF in the signal processing path.
10	didtEn	Enable Integrator for didt current sensor. 0: disable (default) 1: enable
9	001LSB	Energy register LSB configuration for all energy registers: 0: 0.1CF (default) 1: 0.01CF
8	3P3W	This bit defines the voltage/current phase sequence detection mode: 0: 3P4W (default) 1: 3P3W (Ua is Uab, Uc is Ucb, Ub is not used)
7	CF2varh	CF2 pin source: 0: apparent energy 1: reactive energy (default)
6	CF2ESV	This bit is to configure the apparent energy type in power factor calibration, and in CF2 output if apparent energy is selected by setting CF2varh=0. 0:All-phase apparent energy arithmetic sum (default) 1:All-phase apparent energy vector sum
5	-	Reserved.
4	ABSEnQ	These bits configure the calculation method of total (all-phase-sum) reactive/active energy and power: 0: Arithmetic sum: (default) ET=EA*EnPA+ EB*EnPB+ EC*EnPC PT= PA*EnPA+ PB*EnPB+ PC*EnPC 1: Absolute sum: ET=|EA|*EnPA+ |EB|*EnPB+ |EC|*EnPC PT=|PA|*EnPA+ |PB|*EnPB+ |PC|*EnPC Note: ET is the total (all-phase-sum) energy, EA/EB/EC are the signed phase A/B/C energy respectively. Reverse energy is negative. PT is the total (all-phase-sum) power, PA/PB/PC are the signed phase A/B/C power respectively. Reverse power is negative.
3	ABSEnP	
2	EnPA	These bits configure whether Phase A/B/C are counted into the all-phase sum energy/power (P/Q/S). 1: Corresponding Phase A/B/C to be counted into the all-phase sum energy/power (P/Q/S) (default) 0: Corresponding Phase A/B/C not counted into the all-phase sum energy/power (P/Q/S)
1	EnPB	
0	EnPC	

MMode1
PGA Gain Configuration

Address: 34H
Type: Read/Write
Default Value: 0000H

Bit	Name	Description
15-14	DPGA_GAIN	Digital PGA gain for the 4 current channels. This gain is implemented at the end of decimation filter. 00: Gain = 1 (default) 01: Gain = 2 10: Gain = 4 11: Gain = 8
13-0	PGA_GAIN	PGA gain for all ADC channels. Mapping: [13:12]: V3 [11:10]: V2 [9:8]: V1 [7:6]: I4 [5:4]: I3 [3:2]: I2 [1:0]: I1 Encoding: 00: 1X (default) 01: 2X 10: 4X 11: N/A

CS0
Checksum 0

<table>
<tr><td colspan="3">Address: 3BH
Type: Read/Write
Default Value: 421CH</td></tr>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15 - 0</td><td>CS0[15:0]</td><td>This register should be written after the 31H-3AH registers are written. Suppose the high byte and the low byte of the 31H-3AH registers are shown in the below table.
<table>
<tr><th>Register Address</th><th>High Byte</th><th>Low Byte</th></tr>
<tr><td>31H</td><td>H_{31}</td><td>L_{31}</td></tr>
<tr><td>32H</td><td>H_{32}</td><td>L_{32}</td></tr>
<tr><td>33H</td><td>H_{33}</td><td>L_{33}</td></tr>
<tr><td>34H</td><td>H_{34}</td><td>L_{34}</td></tr>
<tr><td>35H</td><td>H_{35}</td><td>L_{35}</td></tr>
<tr><td>36H</td><td>H_{36}</td><td>L_{36}</td></tr>
<tr><td>37H</td><td>H_{37}</td><td>L_{37}</td></tr>
<tr><td>38H</td><td>H_{38}</td><td>L_{38}</td></tr>
<tr><td>39H</td><td>H_{39}</td><td>L_{39}</td></tr>
<tr><td>3AH</td><td>H_{3A}</td><td>L_{3A}</td></tr>
</table>
The calculation of the CS0 register is as follows:

The low byte of 3BH register is: $\mathbf{L_{3B}}$=MOD($\mathbf{H_{31}}$+$\mathbf{H_{32}}$+...+$\mathbf{H_{3A}}$+$\mathbf{L_{31}}$+$\mathbf{L_{32}}$+...+$\mathbf{L_{3A}}$, 2^8)
The high byte of 3BH register is: $\mathbf{H_{3B}}$=$\mathbf{H_{31}}$ XOR $\mathbf{H_{32}}$ XOR... XOR $\mathbf{H_{3A}}$ XOR $\mathbf{L_{31}}$ XOR $\mathbf{L_{32}}$ XOR... XOR $\mathbf{L_{3A}}$

The 90E36A calculates CS0 regularly. If the value of the CS0 register and the calculation by the 90E36A is different when ConfigStart=8765H, the CS0Err bit (b14, SysStatus0) is set and the WarnOut and IRQ pins are asserted.
Note: The readout value of the CS0 register is the calculation by the 90E36A, which is different from what is written.</td></tr>
</table>

There are multiple Start register and Checksum (CS0/CS1/CS2/CS3) registers for different crucial register blocks. Those registers are handled in the similar way.

6.4.3 ENERGY CALIBRATION REGISTERS

Table-6 Calibration Registers

Register Address	Register Name	Read/Write Type	Functional Description	Power-on Value
Calibration Registers				
40H	CalStart	R/W	Calibration Start Command	6886H
41H	POffsetA	R/W	Phase A Active Power Offset	0000H
42H	QOffsetA	R/W	Phase A Reactive Power Offset	0000H
43H	POffsetB	R/W	Phase B Active Power Offset	0000H
44H	QOffsetB	R/W	Phase B Reactive Power Offset	0000H
45H	POffsetC	R/W	Phase C Active Power Offset	0000H
46H	QOffsetC	R/W	Phase C Reactive Power Offset	0000H
47H	GainA	R/W	Phase A Active/Reactive Energy calibration gain	0000H
48H	PhiA	R/W	Phase A calibration phase angle	0000H
49H	GainB	R/W	Phase B Active/Reactive Energy calibration gain	0000H

Table-6 Calibration Registers

Register Address	Register Name	Read/Write Type	Functional Description	Power-on Value
4AH	PhiB	R/W	Phase B calibration phase angle	0000H
4BH	GainC	R/W	Phase C Active/Reactive Energy calibration gain	0000H
4CH	PhiC	R/W	Phase C calibration phase angle	0000H
4DH	CS1*	R/W	Checksum 1	0000H
Note: The calculation of the CS1 register is similar as the CS0 register by calculating the 41H-4CH registers. For details, please refer to application note AN-644.				

PoffsetA
Phase A Active Power Offset

Address: 41H
Type: Read/Write
Default Value: 0000H

Bit	Name	Description
15-0	Offset	Power offset. Signed 16-bit integer.

QoffsetA
Phase A Reactive Power Offset

Address: 42H
Type: Read/Write
Default Value: 0000H

Bit	Name	Description
15-0	Offset	Power offset. Signed 16-bit integer.

GainA
Phase A Active/Reactive Energy calibration gain

Address: 47H
Type: Read/Write
Default Value: 0000H

Bit	Name	Description
15-0	Gain	Energy calibration gain. Signed integer. Actual power gain = (1+ Gain)

PhiA
Phase A calibration phase angle

Address: 48H
Type: Read/Write
Default Value: 0000H

Bit	Name	Description
15	DelayV	0: Delay Cycles are applied to current channel. (default) 1: Delay Cycles are applied to voltage channel.
14:10	-	Reserved.
9:0	DelayCycles	Unit is 2.048MHz cycle. It is an unsigned 10 bit integer.

The phase B and phase C's calibration registers are similar as phase A.

6.4.4 FUNDAMENTAL/HARMONIC ENERGY CALIBRATION REGISTERS

Table-7 Fundamental/Harmonic Energy Calibration Registers

Register Address	Register Name	Read/Write Type	Functional Description	Power-on Value
50H	HarmStart	R/W	Harmonic Calibration Startup Command	6886H
51H	POffsetAF	R/W	Phase A Fundamental Active Power Offset	0000H
52H	POffsetBF	R/W	Phase B Fundamental Active Power Offset	0000H
53H	POffsetCF	R/W	Phase C Fundamental Active Power Offset	0000H
54H	PGainAF	R/W	Phase A Fundamental Active Power Gain	0000H
55H	PGainBF	R/W	Phase B Fundamental Active Power Gain	0000H
56H	PGainCF	R/W	Phase C Fundamental Active Power Gain	0000H
57H	CS2*	R/W	Checksum 2	0000H
Note: The calculation of the CS2 register is similar as the CS0 register by calculating the 51H-56H registers. For details, please refer to application note AN-644.				

6.4.5 MEASUREMENT CALIBRATION

Table-8 Measurement Calibration Registers

Register Address	Register Name	Read/Write Type	Functional Description	Power-on Value
60H	AdjStart	R/W	Measurement Calibration Startup Command	6886H
61H	UgainA	R/W	Phase A Voltage RMS Gain	CE40H
62H	IgainA	R/W	Phase A Current RMS Gain	7530H
63H	UoffsetA	R/W	Phase A Voltage RMS Offset	0000H
64H	IoffsetA	R/W	Phase A Current RMS Offset	0000H
65H	UgainB	R/W	Phase B Voltage RMS Gain	CE40H
66H	IgainB	R/W	Phase B Current RMS Gain	7530H
67H	UoffsetB	R/W	Phase B Voltage RMS Offset	0000H
68H	IoffsetB	R/W	Phase B Current RMS Offset	0000H
69H	UgainC	R/W	Phase C Voltage RMS Gain	CE40H
6AH	IgainC	R/W	Phase C Current RMS Gain	7530H
6BH	UoffsetC	R/W	Phase C Voltage RMS Offset	0000H
6CH	IoffsetC	R/W	Phase C Current RMS Offset	0000H
6DH	IgainN	R/W	Sampled N line Current RMS Gain	7530H
6EH	IoffsetN	R/W	Sampled N line Current RMS Offset	0000H
6FH	CS3*	R/W	Checksum 3	8EBEH
Note: The calculation of the CS3 register is similar as the CS0 register by calculating the 61H-6EH registers.				

6.5 ENERGY REGISTER

6.5.1 REGULAR ENERGY REGISTERS

Table-9 Regular Energy Registers

Register Address	Register Name	Read/Write Type	Functional Description	Comment
80H	APenergyT	R/C	Total Forward Active Energy	Resolution is 0.1CF/0.01CF. 0.01CF / 0.1CF setting is defined by the 001LSB bit (b9, MMode0). Cleared after read.
81H	APenergyA	R/C	Phase A Forward Active Energy	
82H	APenergyB	R/C	Phase B Forward Active Energy	
83H	APenergyC	R/C	Phase C Forward Active Energy	
84H	ANenergyT	R/C	Total Reverse Active Energy	
85H	ANenergyA	R/C	Phase A Reverse Active Energy	
86H	ANenergyB	R/C	Phase B Reverse Active Energy	
87H	ANenergyC	R/C	Phase C Reverse Active Energy	
88H	RPenergyT	R/C	Total Forward Reactive Energy	
89H	RPenergyA	R/C	Phase A Forward Reactive Energy	
8AH	RPenergyB	R/C	Phase B Forward Reactive Energy	
8BH	RPenergyC	R/C	Phase C Forward Reactive Energy	
8CH	RNenergyT	R/C	Total Reverse Reactive Energy	
8DH	RNenergyA	R/C	Phase A Reverse Reactive Energy	
8EH	RNenergyB	R/C	Phase B Reverse Reactive Energy	
8FH	RNenergyC	R/C	Phase C Reverse Reactive Energy	
90H	SAenergyT	R/C	Total (Arithmetic Sum) Apparent Energy	
91H	SenergyA	R/C	Phase A Apparent Energy	
92H	SenergyB	R/C	Phase B Apparent Energy	
93H	SenergyC	R/C	Phase C Apparent Energy	
94H	SVenergyT	R/C	(Vector Sum) Total Apparent Energy	
95H	EnStatus0	R	Metering Status 0	
96H	EnStatus1	R	Metering Status 1	
98H	SVmeanT	R	(Vector Sum) Total Apparent Power	Complement, MSB is always ‘0’; XX.XXX kVA
99H	SVmeanTLSB	R	LSB of (Vector Sum) Total Apparent Power	LSB of SVmeanT. Unit/LSB is 4/65536 VA

EnStatus0
Metering Status 0

Address: 95H
Type: Read
Default Value: F000H

Bit	Name	Description
15	TQNoload	all-phase-sum reactive power no-load condition detected.
14	TPNoload	all-phase-sum active power no-load condition detected.
13	TASNoload	all-phase-sum apparent power no-load condition detected.
12	TVSNoload	all-phase-sum vectored sum apparent active power no-load condition detected.
11-4	-	Reserved.
3	CF4RevFlag	CF4/CF3/CF2/CF1 Forward/Reverse Flag – reflect the direction of the current CF pulse. 0: Forward (default) 1: Reverse
2	CF3RevFlag	
1	CF2RevFlag	
0	CF1RevFlag	

EnStatus1
Metering Status 1

Address: 96H
Type: Read
Default Value: 0000H

Bit	Name	Description
15-7	-	Reserved.
6	SagPhaseA	These bits indicate whether there is voltage sag on phase A, B or C respectively. 0: no voltage sag (default) 1: voltage sag
5	SagPhaseB	
4	SagPhaseC	
3	-	Reserved.
2	PhaseLossA	These bits indicate whether there is a phase loss in Phase A/B/C. 0: no phase loss (default) 1: phase loss.
1	PhaseLossB	
0	PhaseLossC	

6.5.2 FUNDAMENTAL / HARMONIC ENERGY REGISTER

Table-10 Fundamental / Harmonic Energy Register

Register Address	Register Name	Read/Write Type	Functional Description	Comment
A0H	APenergyTF	R/C	Total Forward Active Fundamental Energy	Resolution is 0.1CF / 0.01CF. 0.01CF / 0.1CF setting is defined by the 001LSB bit (b9, MMode0). Cleared after read.
A1H	APenergyAF	R/C	Phase A Forward Active Fundamental Energy	
A2H	APenergyBF	R/C	Phase B Forward Active Fundamental Energy	
A3H	APenergyCF	R/C	Phase C Forward Active Fundamental Energy	
A4H	ANenergyTF	R/C	Total Reverse Active Fundamental Energy	
A5H	ANenergyAF	R/C	Phase A Reverse Active Fundamental Energy	
A6H	ANenergyBF	R/C	Phase B Reverse Active Fundamental Energy	
A7H	ANenergyCF	R/C	Phase C Reverse Active Fundamental Energy	
A8H	APenergyTH	R/C	Total Forward Active Harmonic Energy	
A9H	APenergyAH	R/C	Phase A Forward Active Harmonic Energy	
AAH	APenergyBH	R/C	Phase B Forward Active Harmonic Energy	
ABH	APenergyCH	R/C	Phase C Forward Active Harmonic Energy	
ACH	ANenergyTH	R/C	Total Reverse Active Harmonic Energy	
ADH	ANenergyAH	R/C	Phase A Reverse Active Harmonic Energy	
AEH	ANenergyBH	R/C	Phase B Reverse Active Harmonic Energy	
AFH	ANenergyCH	R/C	Phase C Reverse Active Harmonic Energy	

6.6 MEASUREMENT REGISTERS

6.6.1 POWER AND POWER FACTOR REGISTERS

Table-11 Power and Power Factor Register

Register Address	Register Name	Read/Write Type	Functional Description	Comment
B0H	PmeanT	R	Total (all-phase-sum) Active Power	Complement, MSB as the sign bit XX.XXX kW 1LSB corresponds to 1Watt for phase A/B/C, and 4Watt for Total (all-phase-sum)
B1H	PmeanA	R	Phase A Active Power	
B2H	PmeanB	R	Phase B Active Power	
B3H	PmeanC	R	Phase C Active Power	
B4H	QmeanT	R	Total (all-phase-sum) Reactive Power	Complement, MSB as the sign bit XX.XXX kvar 1LSB corresponds to 1var for phase A/B/C, and 4var for Total (all-phase-sum)
B5H	QmeanA	R	Phase A Reactive Power	
B6H	QmeanB	R	Phase B Reactive Power	
B7H	QmeanC	R	Phase C Reactive Power	
B8H	SAmeanT	R	Total (Arithmetic Sum) apparent power	Complement, MSB always '0' XX.XXX kVA 1LSB corresponds to 1va for phase A/B/C, and 4va for Total (all-phase-sum)
B9H	SmeanA	R	phase A apparent power	
BAH	SmeanB	R	phase B apparent power	
BBH	SmeanC	R	phase C apparent power	
BCH	PFmeanT	R	Total power factor	Signed, MSB as the sign bit X.XXX LSB is 0.001. Range from -1000 to +1000
BDH	PFmeanA	R	phase A power factor	
BEH	PFmeanB	R	phase B power factor	
BFH	PFmeanC	R	phase C power factor	
C0H	PmeanTLSB	R	Lower word of Total (all-phase-sum) Active Power	Lower word of Active Powers. 1LLSB* corresponds to 4/256 Watt

Table-11 Power and Power Factor Register

Register Address	Register Name	Read/Write Type	Functional Description	Comment
C1H	PmeanALSB	R	Lower word of Phase A Active Power	Lower word of Active Powers. 1LLSB corresponds to 1/256 Watt
C2H	PmeanBLSB	R	Lower word of Phase B Active Power	
C3H	PmeanCLSB	R	Lower word of Phase C Active Power	
C4H	QmeanTLSB	R	Lower word of Total (all-phase-sum) Reactive Power	Lower word of ReActive Powers. 1LLSB corresponds to 4/256 var
C5H	QmeanALSB	R	Lower word of Phase A Reactive Power	Lower word of ReActive Powers. 1LLSB corresponds to 1/256 var
C6H	QmeanBLSB	R	Lower word of Phase B Reactive Power	
C7H	QmeanCLSB	R	Lower word of Phase C Reactive Power	
C8H	SAmeanTLSB	R	Lower word of Total (Arithmetic Sum) apparent power	Lower word of Apparent Powers. 1LLSB corresponds to 4/256 VA
C9H	SmeanALSB	R	Lower word of phase A apparent power	Lower word of Apparent Powers. 1LLSB corresponds to 1/256 VA
CAH	SmeanBLSB	R	Lower word of phase B apparent power	
CBH	SmeanCLSB	R	Lower word of phase C apparent power	

Note: All the lower 8 bits of C0H-CBH registers and E0H-EFH registers are always zero. Only the higher 8 bits of these registers are valid.
In this document, LLSB means bit 8 of the lower registers as below:

b15	b14	b13	b12	b11	b10	b9	b8 (LLSB)	b7	b6	b5	b4	b3	b2	b1	b0

6.6.2 FUNDAMENTAL/ HARMONIC POWER AND VOLTAGE/ CURRENT RMS REGISTERS

Table-12 Fundamental/ Harmonic Power and Voltage/ Current RMS Registers

Register Address	Register Name	Read/Write Type	Functional Description	Comment
D0H	PmeanTF	R	Total active fundamental power	Complement, 16-bit integer with unit of 4Watt. 1LSB corresponds to 4Watt
D1H	PmeanAF	R	phase A active fundamental power	Complement, 16-bit integer with unit of 1Watt. 1LSB corresponds to 1Watt
D2H	PmeanBF	R	phase B active fundamental power	
D3H	PmeanCF	R	phase C active fundamental power	
D4H	PmeanTH	R	Total active harmonic power	Complement, 16-bit integer with unit of 4Watt. 1LSB corresponds to 4Watt
D5H	PmeanAH	R	phase A active harmonic power	Complement, 16-bit integer with unit of 1Watt. 1LSB corresponds to 1Watt
D6H	PmeanBH	R	phase B active harmonic power	
D7H	PmeanCH	R	phase C active harmonic power	
D8H	IrmsN1	R	N Line Sampled current RMS	unsigned 16-bit integer with unit of 0.001A 1LSB corresponds to 0.001 A
D9H	UrmsA	R	phase A voltage RMS	1LSB corresponds to 0.01 V
DAH	UrmsB	R	phase B voltage RMS	
DBH	UrmsC	R	phase C voltage RMS	
DCH	IrmsN0	R	N Line calculated current RMS	unsigned 16-bit integer with unit of 0.001A 1LSB corresponds to 0.001 A
DDH	IrmsA	R	phase A current RMS	
DEH	IrmsB	R	phase B current RMS	
DFH	IrmsC	R	phase C current RMS	
E0H	PmeanTFLSB	R	Lower word of Total active fundamental Power	Lower word of D0H register. 1LLSB* corresponds to 4/256 Watt

Register Address	Register Name	Read/Write Type	Functional Description	Comment
E1H	PmeanAFLSB	R	Lower word of phase A active fundamental Power	Lower word of registers from D1H to D3H. 1LLSB corresponds to 1/256 Watt
E2H	PmeanBFLSB	R	Lower word of phase B active fundamental Power	
E3H	PmeanCFLSB	R	Lower word of phase C active fundamental Power	
E4H	PmeanTHLSB	R	Lower word of Total active harmonic Power	Lower word of D4H register. 1LLSB corresponds to 4/256 Watt
E5H	PmeanAHLSB	R	Lower word of phase A active harmonic Power	Lower word of registers from D5H to D7H. 1LLSB corresponds to 1/256 Watt
E6H	PmeanBHLSB	R	Lower word of phase B active harmonic Power	
E7H	PmeanCHLSB	R	Lower word of phase C active harmonic Power	
E9H	UrmsALSB	R	Lower word of phase A voltage RMS	Lower word of registers from D9H to DBH. 1LLSB corresponds to 0.01/256V
EAH	UrmsBLSB	R	Lower word of phase B voltage RMS	
EBH	UrmsCLSB	R	Lower word of phase C voltage RMS	
EDH	IrmsALSB	R	Lower word of phase A current RMS	Lower word of registers from DDH to DFH. 1LLSB corresponds to 0.001/256A
EEH	IrmsBLSB	R	Lower word of phase B current RMS	
EFH	IrmsCLSB	R	Lower word of phase C current RMS	

Note: All the lower 8 bits of C0H-CBH registers and E0H-EFH registers are always zero. Only the higher 8 bits of these registers are valid.
In this document, LLSB means bit 8 of the lower registers as below:

b15	b14	b13	b12	b11	b10	b9	b8 (LLSB)	b7	b6	b5	b4	b3	b2	b1	b0

6.6.3 THD+N, FREQUENCY, ANGLE AND TEMPERATURE REGISTERS

Table-13 THD+N, Frequency, Angle and Temperature Registers

Register Address	Register Name	Read/Write Type	Functional Description	Comment
F1H	THDNUA	R	phase A voltage THD+N	1LSB corresponds to 0.01%
F2H	THDNUB	R	phase B voltage THD+N	
F3H	THDNUC	R	phase C voltage THD+N	
F5H	THDNIA	R	phase A current THD+N	1LSB corresponds to 0.01%
F6H	THDNIB	R	phase B current THD+N	
F7H	THDNIC	R	phase C current THD+N	
F8H	Freq	R	Frequency	1LSB corresponds to 0.01% Hz
F9H	PAngleA	R	phase A mean phase angle	Signed, MSB as the sign bit 1LSB corresponds to 0.1-degree, -180.0°~+180.0°
FAH	PAngleB	R	phase B mean phase angle	
FBH	PAngleC	R	phase C mean phase angle	
FCH	Temp	R	Measured temperature	1LSB corresponds to 1 °C Signed, MSB as the sign bit
FDH	UangleA	R	phase A voltage phase angle	Always ‘0’
FEH	UangleB	R	phase B voltage phase angle	Signed, MSB as the sign bit Take phase A voltage as base voltage 1LSB corresponds to 0.1 degree, -180.0°~+180.0°
FFH	UangleC	R	phase C voltage phase angle	

6.7 HARMONIC FOURIER ANALYSIS REGISTERS

Table-14 Harmonic Fourier Analysis Results Registers

Register Address	Register Name	Read/Write Type	Functional Description	Comment
100H	AI_HR2	R	phase A, Current, Harmonic Ratio for 2-th order component	Harmonic Ratio (%) = Register Value / 163.84
101H	AI_HR3	R	phase A, Current, Harmonic Ratio for 3-th order component	
102H	AI_HR4	R	phase A, Current, Harmonic Ratio for 4-th order component	
…		R		
11EH	AI_HR32	R	phase A, Current, Harmonic Ratio for 32-th order component	
11FH	AI_THD	R	phase A, Current, Total Harmonic Distortion Ratio	
120H	BI_HR2	R	phase B, Current, Harmonic Ratio for 2-th order component	Harmonic Ratio (%) = Register Value / 163.84
121H	BI_HR3	R	phase B, Current, Harmonic Ratio for 3-th order component	
122H	BI_HR4	R	phase B, Current, Harmonic Ratio for 4-th order component	
…		R		
13EH	BI_HR32	R	phase B, Current, Harmonic Ratio for 32-th order component	
13FH	BI_THD	R	phase B, Current, Total Harmonic Distortion Ratio	
140H	CI_HR2	R	phase C, Current, Harmonic Ratio for 2-th order component	Harmonic Ratio (%) = Register Value / 163.84
141H	CI_HR3	R	phase C, Current, Harmonic Ratio for 3-th order component	
142H	CI_HR4	R	phase C, Current, Harmonic Ratio for 4-th order component	
…		R		
15EH	CI_HR32	R	phase C, Current, Harmonic Ratio for 32-th order component	
15FH	CI_THD	R	phase C, Current, Total Harmonic Distortion Ratio	
160H	AV_HR2	R	phase A, Voltage, Harmonic Ratio for 2-th order component	Harmonic Ratio (%) = Register Value / 163.84
161H	AV_HR3	R	phase A, Voltage, Harmonic Ratio for 3-th order component	
162H	AV_HR4	R	phase A, Voltage, Harmonic Ratio for 4-th order component	
…		R		
17EH	AV_HR32	R	phase A, Voltage, Harmonic Ratio for 32-th order component	
17FH	AV_THD	R	phase A, Voltage, Total Harmonic Distortion Ratio	

Table-14 Harmonic Fourier Analysis Results Registers

Register Address	Register Name	Read/Write Type	Functional Description	Comment
180H	BV_HR2	R	phase B, Voltage, Harmonic Ratio for 2-th order component	Harmonic Ratio (%) = Register Value / 163.84
181H	BV_HR3	R	phase B, Voltage, Harmonic Ratio for 3-th order component	
182H	BV_HR4	R	phase B, Voltage, Harmonic Ratio for 4-th order component	
…		R		
19EH	BV_HR32	R	phase B, Voltage, Harmonic Ratio for 32-th order component	
19FH	BV_THD	R	phase B, Voltage, Total Harmonic Distortion Ratio	
1A0H	CV_HR2	R	phase C, Voltage, Harmonic Ratio for 2-th order component	Harmonic Ratio (%) = Register Value / 163.84
1A1H	CV_HR3	R	phase C, Voltage, Harmonic Ratio for 3-th order component	
1A2H	CV_HR4	R	phase C, Voltage, Harmonic Ratio for 4-th order component	
…		R		
1BEH	CV_HR32	R	phase C, Voltage, Harmonic Ratio for 32-th order component	
1BFH	CV_THD	R	phase C, Voltage, Total Harmonic Distortion Ratio	
1C0H	AI_FUND	R	phase A, Current, Fundamental component value	Current, Fundamental component value = Register Value * $3.2656*10^{-3}$ / 2^scale, Register (1C0H, 1C2H, 1C4H); Voltage, Fundamental component value = Register Value * $3.2656*10^{-2}$/ 2^scale, Register (1C1H, 1C3H, 1C5H). The scale is defined by the DFT_SCALE (1D0H) register.
1C1H	AV_FUND	R	phase A, Voltage, Fundamental component value	
1C2H	BI_FUND	R	phase B, Current, Fundamental component value	
1C3H	BV_FUND	R	phase B, Voltage, Fundamental component value	
1C4H	CI_FUND	R	phase C, Current, Fundamental component value	
1C5H	CV_FUND	R	phase C, Voltage, Fundamental component value	
1D0H	DFT_SCALE	RW	Input Gain = 2^Scale, i.e. Scale = # of bit shifts [2:0]: Scale for Channel A-I. [5:3]: Scale for Channel B-I. [8:6]: Scale for Channel C-I. [10:9]: Scale for Channel A-V. [12:11]: Scale for Channel B-V. [14:13]: Scale for Channel C-V. [15]: Window disable. ‘1’ disable the Hanning window.	Input data is scaled before sampling or DFT.
1D1H	DFT_CTRL	RW	Bit[0]: DFT_START. 0: Reset and abort the DFT computation. 1: Start the DFT. This bit is automatically cleared after DFT finishes.	

7 ELECTRICAL SPECIFICATION

7.1 ELECTRICAL SPECIFICATION

Parameter	Min	Typ	Max	Unit	Test Condition/ Comments
Accuracy					
DC Power Supply Rejection Ratio (PSRR)			±0.1	%	VDD=3.3V±0.3V, I=5A, V=220V, CT 1000:1, sampling resistor 4.8Ω
AC Power Supply Rejection Ratio (PSRR)			±0.1	%	VDD=3.3V superimposes 400mVrms, I=5A, V=220V, CT 1000:1, sampling resistor 4.8Ω
Active Energy Error (Dynamic Range 6000:1)			±0.1	%	CT 1000:1, sampling resistor 4.8Ω
ADC Channel					
Differential Input Voltage	0.12 0.07 0.04		720 360 180	mVrms	PGA=1 PGA=2 PGA=4
Analog Input Pin Absolute Voltage Range	GND-300		VDD-1200	mV	
Channel Input Impedance		120 80 50		KΩ	PGA=1 PGA=2 PGA=4
Channel Sampling Frequency		8		kHz	
Channel Sampling Bandwidth		2		kHz	
Temperature Sensor and Reference					
Temperature Sensor Accuracy		1		°C	
Reference voltage		1.2			3.3 V, 25 °C
Reference voltage temperature coefficient		6	15	ppm/°C	From -40 to 85 °C
Current detectors					
Current Detector threshold range	2	3	4	mVrms	3.3 V, 25 °C
Current Detector threshold setting step/ resolution		0.096		mVrms	3.3 V, 25 °C
Current Detector detection time (single-side)	32			ms	
Current Detector detection time (double-side)	17			ms	
Crystal Oscillator					
Oscillator Frequency (f_{sys_clk})		16.384		MHz	The Accuracy of crystal or external clock is ±20 ppm, 10pF ~ 20pF crystal load capacitor integrated.
Power Supply					
AVDD	2.8	3.3	3.6		
DVDD	2.8	3.3	3.6		
VDD18		1.8		V	
Operating Currents					
Normal mode operating current (I-Normal)		23		mA	3.3 V, 25 °C
Normal mode operating current with DFT engine on (I-Normal + DFT)		23.5		mA	3.3 V, 25 °C
Idle mode operating current (I-Idle)		0.1	4	µA	
Detection mode operating current (I-Detection)		180 100	250 140	µA	Double-side detection (at 3.3 V, 25 °C) Single-side detection (at 3.3 V, 25 °C)
Partial Measurement mode operating current (I-Measurement)		6.8		mA	3.3 V, 25°C
SPI					
Slave mode (SPI) bit rate	100		1200k[note 1]	bps	
Master mode (DMA) bit rate			1800k	bps	
ESD					
Machine Model (MM)	400			V	JESD22-A115
Charged Device Model (CDM)	1000			V	JESD22-C101
Human Body Model (HBM)	6000			V	JESD22-A114
Latch Up			±100	mA	JESD78A
Latch Up			5.4	V	JESD78A

Parameter	Min	Typ	Max	Unit	Test Condition/ Comments
DC Characteristics					
Digital Input High Level (all digital pins except OSCI)	2.4		VDD	V	VDD=3.3V
Digital Input Low Level (all digital pins except OSCI)			0.8	V	VDD=3.3V
Digital Input Leakage Current			±1	µA	VDD=3.6V, VI=VDD or GND
Digital Output Low Level (CF1, CF2, CF3, CF4)			0.4	V	VDD=3.3V, I_{OL}=8mA
Digital Output Low Level (IRQ0, IRQ1, WarnOut, ZX0, ZX1, ZX2, SDO)			0.4	V	VDD=3.3V, I_{OL}=5mA
Digital Output High Level (CF1, CF2, CF3, CF4)	2.8			V	VDD=3.3V, I_{OH}=-8mA, by separately
Digital Output High Level (IRQ0, IRQ1, WarnOut, ZX0, ZX1, ZX2, SDO)	2.8			V	VDD=3.3V, I_{OH}=-5mA, by separately
Note 1: The maximum SPI bit rate during current detector calibration is 900k bps.					

7.2 METERING/ MEASUREMENT ACCURACY

7.2.1 METERING ACCURACY

Metering accuracy or energy accuracy is calculated with relative error:

$$\gamma = \frac{E_{mea} - E_{real}}{E_{real}} \times 100\%$$

Where E_{mea} is the energy measured by the meter, E_{real} is the actual energy measured by a high accurate normative meter.

Table-14 Metering Accuracy for Different Energy within the Dynamic Range

Energy Type	Energy Pulse	ADC Range When Gain=1	Metering Accuracy[note 1]
Active energy (Per phase and all-phase-sum)	CF1	PF=1.0 120µV-720mV	0.1%
		PF=0.5L, 180µV-720mV	
		PF=0.8C, 150µV-720mV	
Reactive energy (Per phase and all-phase-sum)	CF2	sinΦ=1.0 120µV-720mV	0.2%
		sinΦ=0.5L, 180µV-720mV	
		sinΦ=0.8C, 150µV-720mV	
Apparent energy (Per phase and arithmetic all-phase-sum)	CF2	600µV-720mV[note 2]	0.2%
Apparent energy (Vector sum)	CF2	120µV-720mV	0.5%
Fundamental active energy (Per phase and all-phase-sum)	CF3	PF=1.0 120µV-720mV	0.2%
		PF=0.5L, 180µV-720mV	
		PF=0.8C, 150µV-720mV	
Harmonic active energy (Per phase and all-phase-sum)	CF4	PF=1.0 120µV-720mV	0.5%
		PF=0.5L, 180µV-720mV	
		PF=0.8C, 150µV-720mV	

Note 1: All the parameters in this table is tested on Atmel's test platform.

Note 2: Apparent energy is tested using active energy with unity power factor since there's no standard for apparent energy. Signal below 600 µV is not tested.

7.2.2 MEASUREMENT ACCURACY

The measurements are all calculated with fiducial error except for frequency and THD.

Fiducial error is calculated as follows:

$$\text{Fiducial\_Error} = \frac{U_{mea} - U_{real}}{U_{FV}} * 100\%$$

Where U_{mea} means the measured data of one measurement parameter, and U_{real} means the real/actual data of the parameter,

U_{FV} means the fiducial value of this measurement parameter, which can be defined as Table-15.

Table-15 Measurement Parameter Range and Format

Measurement	Fiducial Value (FV)	90E36A Defined Format	Range	Comment
Voltage	reference voltage Un	XXX.XX	0 ~ 655.35V	Unsigned integer with unit of 0.01V
Current	maximum current Imax (4×In is recommended)	XX.XXX	0 ~ 65.535A	Unsigned integer with unit of 0.001A
Voltage rms	Un	XXX.XX	0 ~ 655.35V	Unsigned integer with unit of 0.01V
Current rms $^{\text{note 1}}$	Ib/In	XX.XXX	0 ~ 65.535A	Unsigned integer with unit of 0.001A
Active/ Reactive Power $^{\text{note 1}}$	Un×4Ib	XX.XXX	-32.768 ~ +32.767 kW/kvar	Signed integer with unit/LSB of 1 Watt/var
Apparent Power	Un×4Ib	XX.XXX	0 ~ +32.767 kVA	Unsigned integer with unit/LSB of 1 VA
Frequency	Reference Frequency 50 Hz	XX.XX	45.00~65.00 Hz	Signed integer with unit/LSB of 0.01Hz
Power Factor	1.000	X.XXX	-1.000 ~ +1.000	Signed integer, LSB/Unit = 0.001
Phase Angle $^{\text{note 2}}$	180°	XXX.X	-180° ~ +180°	Signed integer, unit/LSB = 0.1°
THD+N	Relative error is adopted, no Fiducial Value	XX.XX	0.00%-99.99%	Unit is 0.01%
THD			0.00%-399%	Arithmetic ratio, 2 bit integer and 14 bit fractional.
Harmonic Component			0.00%-399%	

Note 1:
All registers are of 16-bit. For cases when the current or active/reactive/apparent power goes beyond the above range, it is suggested to be handled by MCU in application. For example, register value can be calibrated to 1/2 of the actual value during calibration, then multiply 2 in application.
Note 2:
Phase angle is obtained when voltage/current crosses zero at the sampling frequency of 256kHz.

For the above mentioned parameters, the measurement accuracy requirement is 0.5% maximum.

For frequency, temperature, THD+N, THD and Harmonic analysis:

Parameter Accuracy

Frequency: 0.01Hz

Temperature: 1 °C

THD/Harmonics: 5% relative error

Accuracy of all orders of harmonics: 5% relative error

$$\text{Harmonic component\%} = \left| \frac{u(i)_h - u(i)_{hN}}{u(i)_{hN}} \right| \times 100$$

Where

$u(i)_h$ means the measuring value of the hth harmonic voltage/ current;

$u(i)_{hN}$ means the given or actual value of the hth harmonic voltage/ current.

7.3 INTERFACE TIMING

7.3.1 SPI INTERFACE TIMING (SLAVE MODE)

The SPI interface timing is as shown in Figure-17 and Table-16.

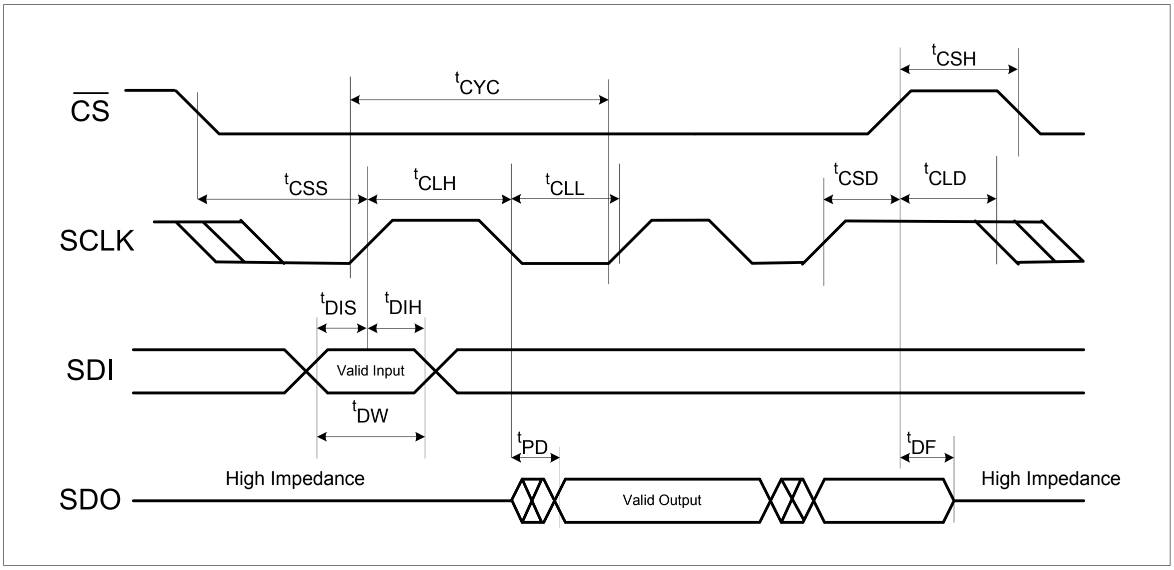


Figure-17 SPI Timing Diagram

Table-16 SPI Timing Specification

Symbol	Description	Min.	Typical	Max.	Unit
t_{CSH}	Minimum $\overline{CS}$ High Level Time	$2T^{note\ 1}+10$			ns
t_{CSS}	$\overline{CS}$ Setup Time	2T+10			ns
t_{CSD}	$\overline{CS}$ Hold Time	3T+10			ns
t_{CLD}	Clock Disable Time	1T			ns
t_{CYC}	SCLK cycle	7T+10			ns
t_{CLH}	Clock High Level Time	5T+10			ns
t_{CLL}	Clock Low Level Time	2T+10			ns
t_{DIS}	Data Setup Time	2T+10			ns
t_{DIH}	Data Hold Time	1T+10			ns
t_{DW}	Minimum Data Width	3T+10			ns
t_{PD}	Output Delay			2T+20	ns
t_{DF}	Output Disable Time			2T+20	ns

Note:

1. T means system clock cycle. $T=1/f_{sys\_clk}$

7.3.2 DMA TIMING (MASTER MODE)

The DMA timing is as shown in Figure-18 and Table-17.

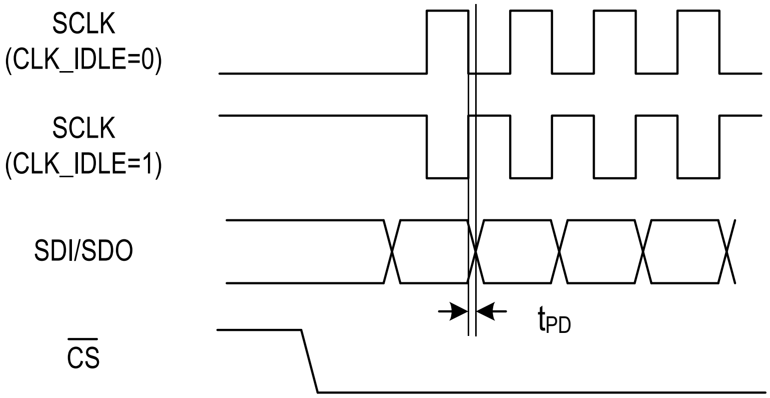


Figure-18 DMA Timing Diagram

Table-17 DMA Timing Specification

Symbol	Description	Min.	Typical	Max.	Unit
t_{PD}	Output Delay			50	ns

7.4 POWER ON RESET TIMING

In most case, the power of 90E36A and MCU are both derived from 220V power lines. To make sure 90E36A is reset and can work properly, MCU must force 90E36A into idle mode firstly and then into normal mode. In this operation, $\overline{\text{RESET}}$ is held to high in idle mode and de-asserted by delay T1 after idle-normal transition. Refer to Figure-19.

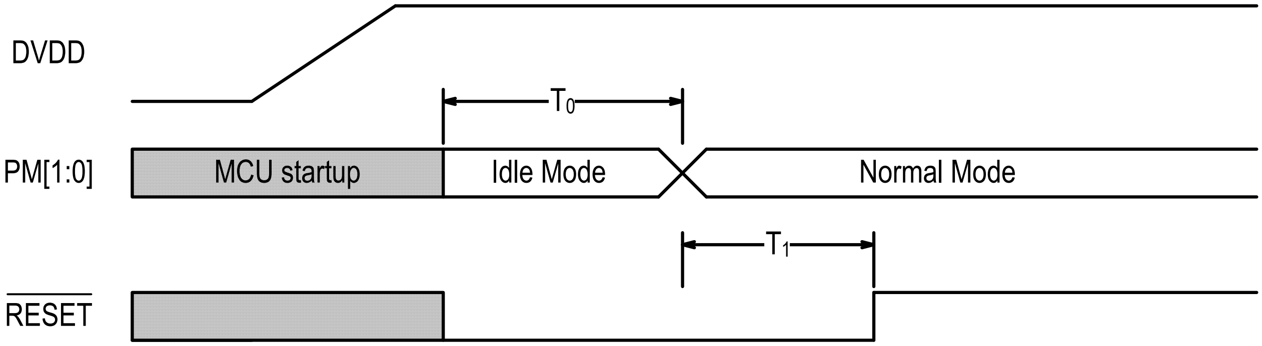


Figure-19 Power On Reset Timing (90E36A and MCU are Powered on Simultaneously)

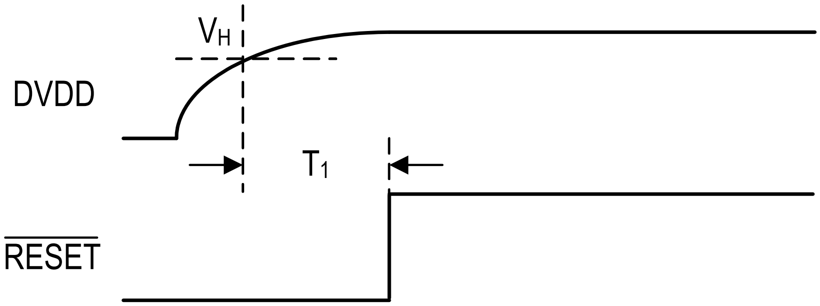


Figure-20 Power On Reset Timing in Normal & Partial Measurement Mode

Table-18 Power On Reset Specification

Symbol	Description	Min	Typ	Max	Unit
V_H	Power On Trigger Voltage		2.5	2.7	V
T_0	Duration forced in idle mode after power on	1			ms
T_1	Delay time after power on or exit idle mode	5	16	40	ms

7.5 ZERO-CROSSING TIMING

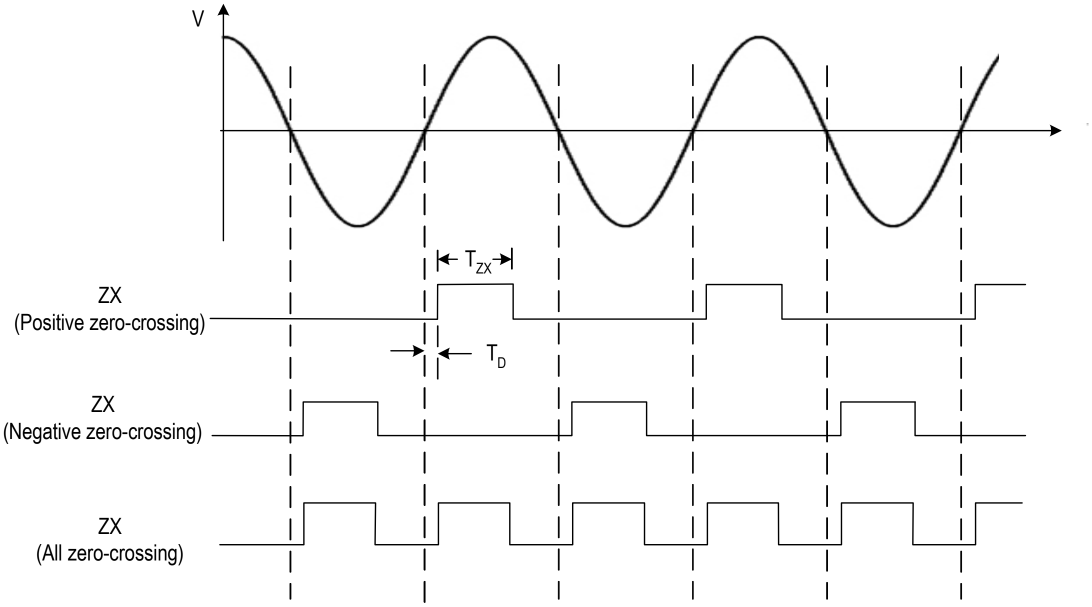


Figure-21 Zero-Crossing Timing Diagram (per phase)

Table-19 Zero-Crossing Specification

Symbol	Description	Min	Typ	Max	Unit
T_{ZX}	High Level Width		5		ms
T_D	Delay Time		0.2	0.5	ms

7.6 VOLTAGE SAG AND PHASE LOSS TIMING

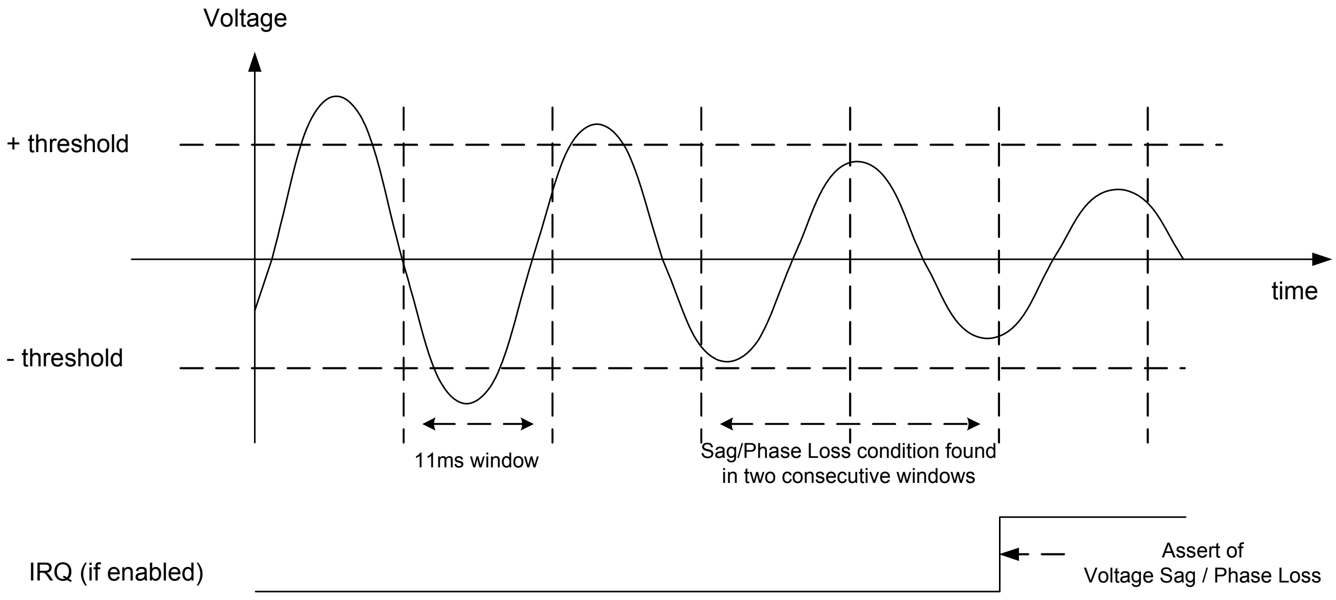


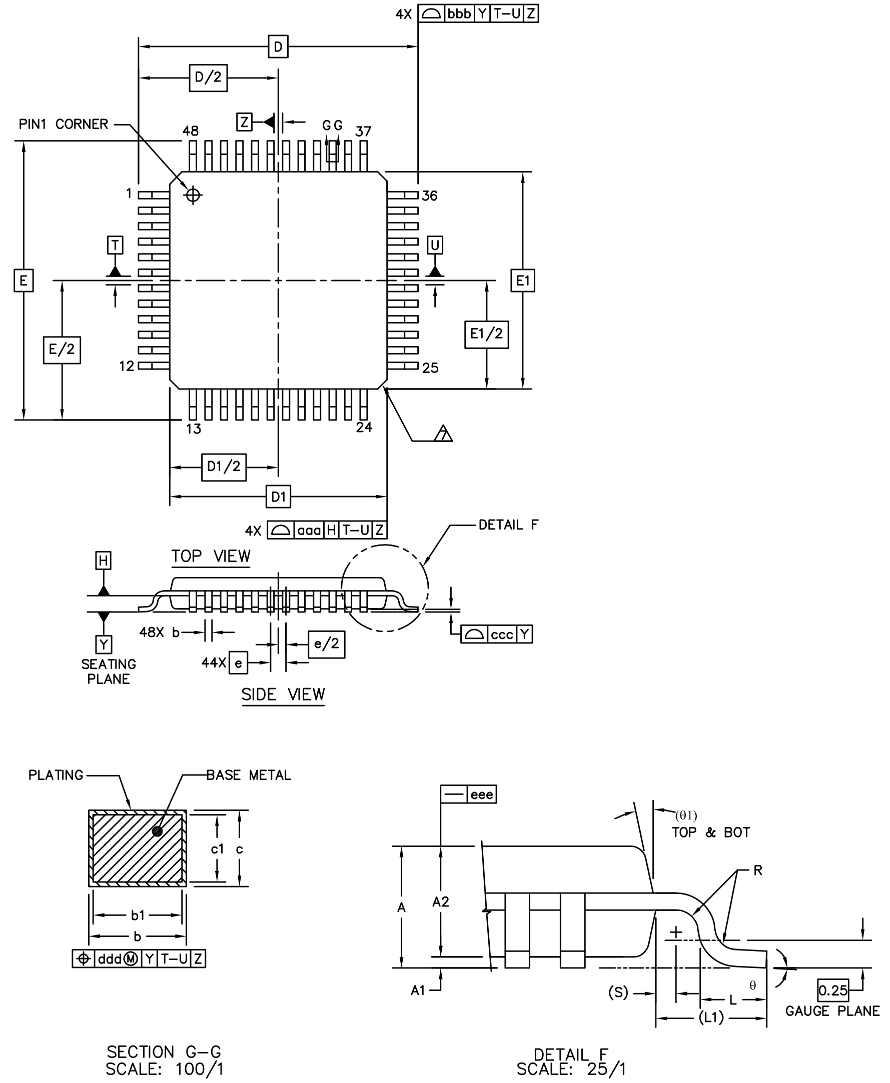
Figure-22 Voltage Sag and Phase Loss Timing Diagram

7.7 ABSOLUTE MAXIMUM RATING

Parameter	Maximum Limit
Relative Voltage Between AVDD and AGND	-0.3V~3.7V
Relative Voltage Between DVDD and DGND	-0.3V~3.7V
Analog Input Voltage (I1P, I1N, I2P, I2N, I3P, I3N, I4P, I4N, V1P, V1N, V2P, V2N, V3P, V3N)	-0.6V~AVDD
Digital Input Voltage	-0.3V~3.6V
Operating Temperature Range	-40~85 °C
Maximum Junction Temperature	150 °C

Package Type	Thermal Resistance θ_{JA}	Unit	Condition
TQFP48	58.5	°C/W	No Airflow

PACKAGE DIMENSIONS



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	1	---	1.2
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	0.95	---	1.05
LEAD WIDTH(PLATING)		b	0.17	---	0.27
LEAD WIDTH		b1	0.17	---	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D		9 BSC	
	Y	E		9 BSC	
BODY SIZE	X	D1		7 BSC	
	Y	E1		7 BSC	
LEAD PITCH		e		0.5 BSC	
		L	0.5	---	0.7
FOOTPRINT		L1		1 REF	
		θ	1°	---	5°
		θ1		12° REF	
		R	0.15	---	0.25
		S		0.2 REF	
PACKAGE EDGE TOLERANCE		aaa		0.2	
LEAD EDGE TOLERANCE		bbb		0.2	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.08	
MOLD FLATNESS		eee		0.05	

NOTES

1. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

2. DATUMS T, U AND Z TO BE DETERMINED AT DATUM PLANE H.

3. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.

4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE B DIMENSION TO EXCEED 0.35.

6. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. UNIT IN MM.

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

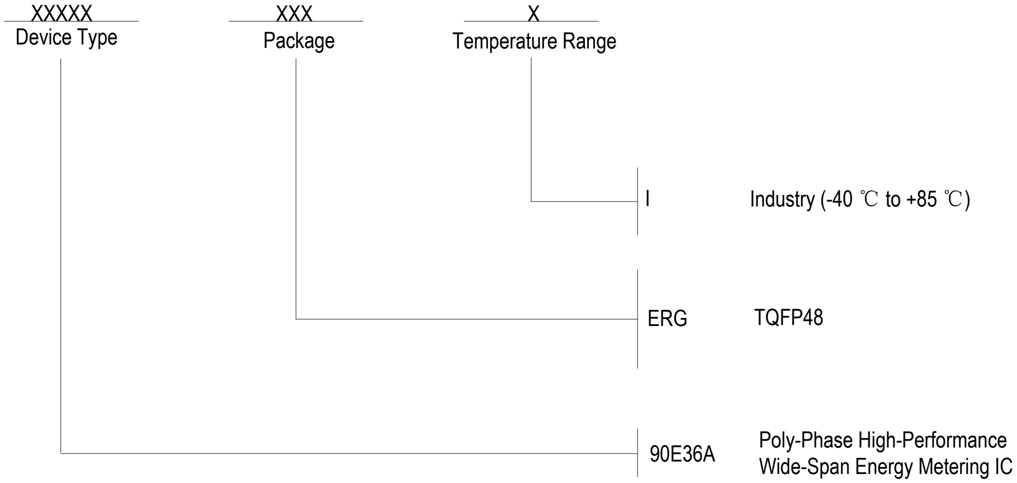
APPROVALS	DATE
DRAWN CJC	06/09/11
CHECKED	

Atmel

TITLE
ER/ERG48 TQFP PACKAGE OUTLINE
7.0 X 7.0 X 1.0 PKG. 0.5MM PITCH

SIZE C
DRAWING No. PSC−4167
REV 00
DO NOT SCALE DRAWING
SHEET 1 OF 2

ORDERING INFORMATION



DATASHEET DOCUMENT HISTORY