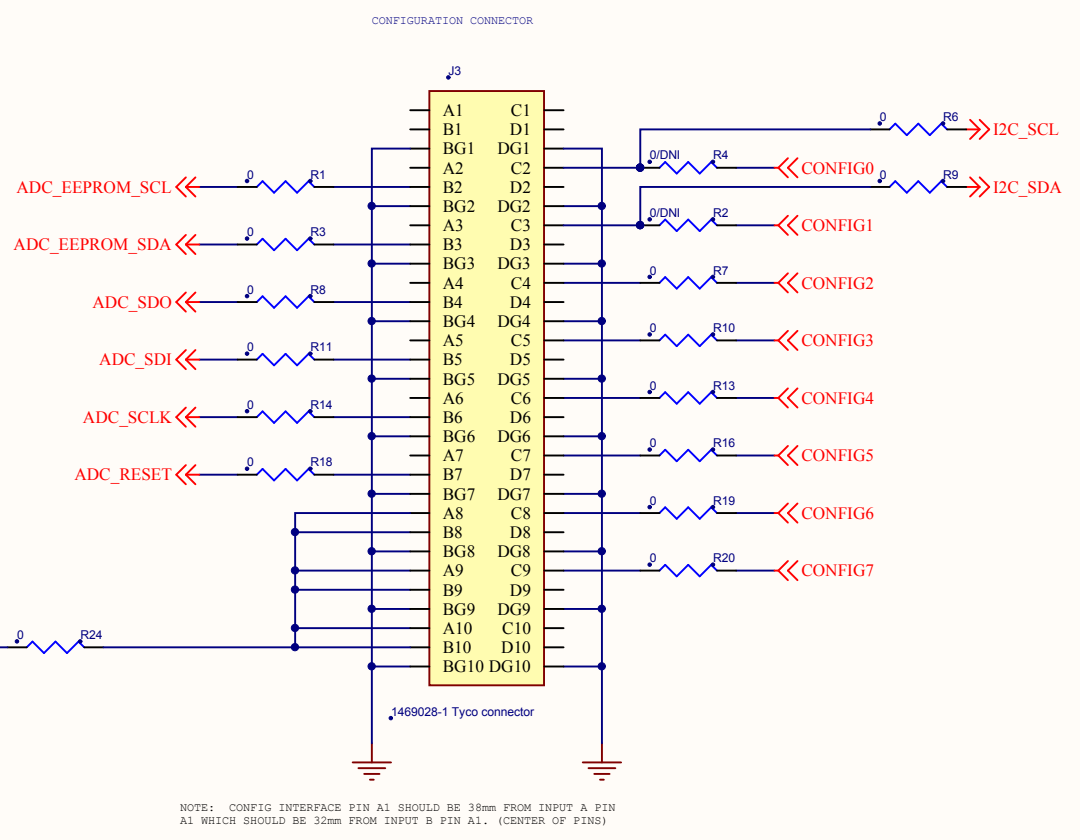
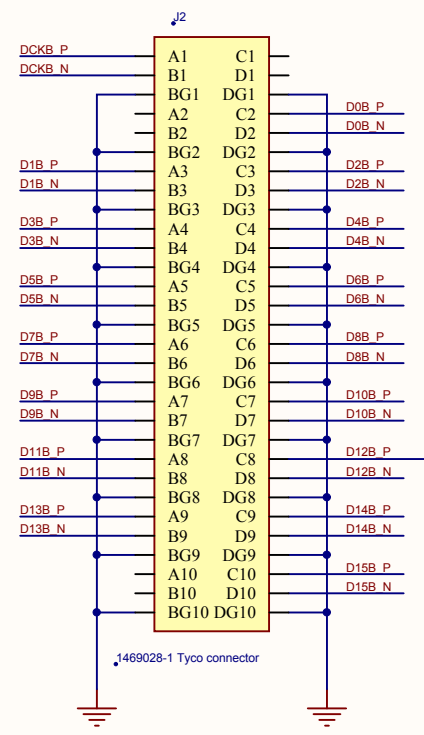
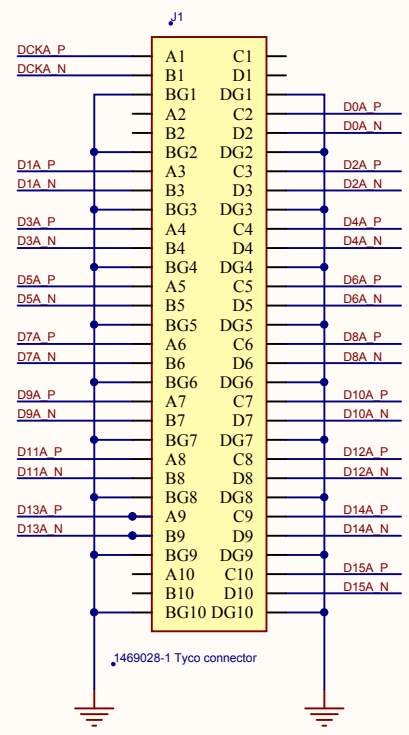


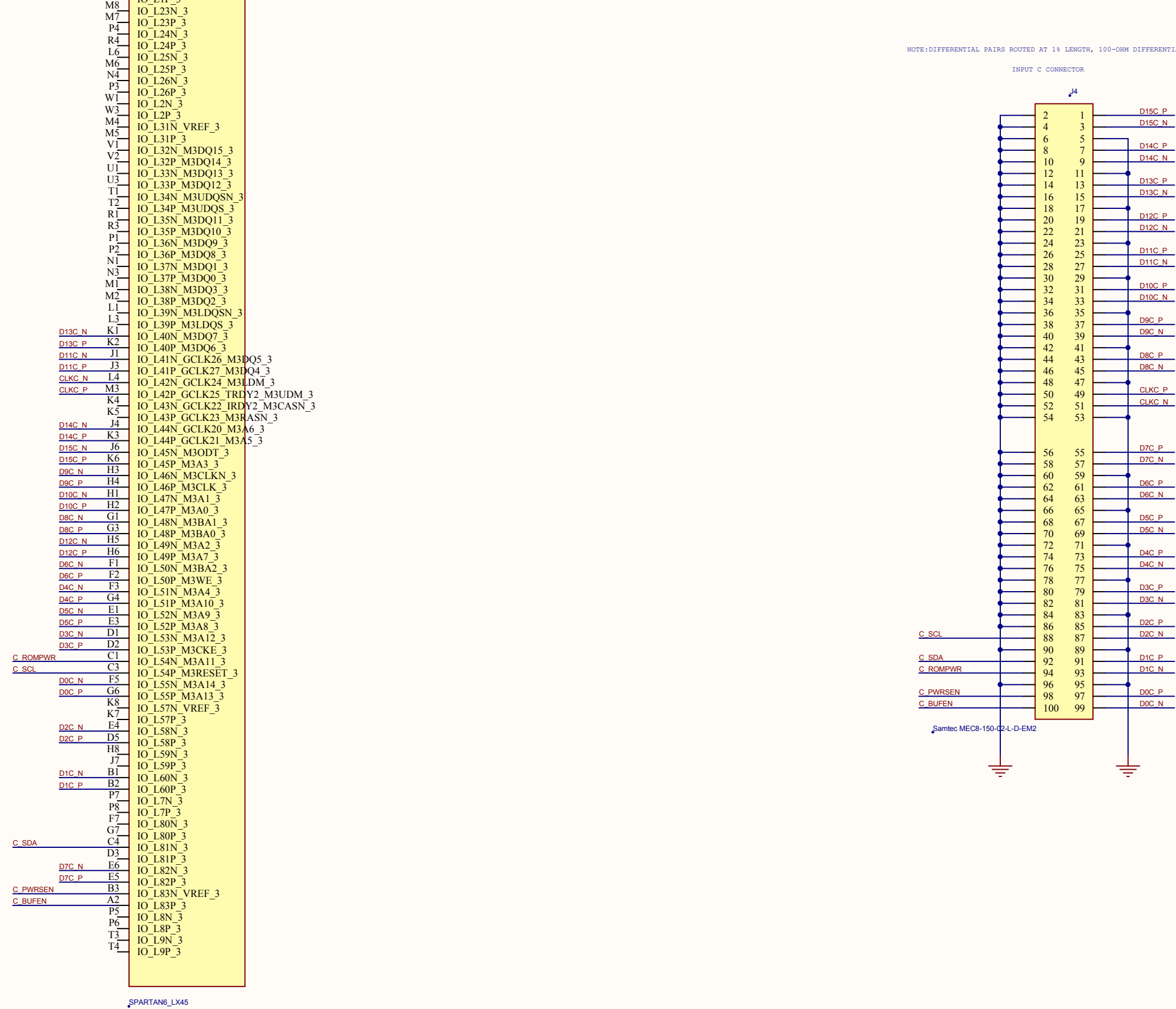
D5B_P	AA17	IO_L14P_D11_2
D4B_N	AB17	IO_L15N_2
D4B_P	Y17	IO_L15P_2
D10B_N	AB14	IO_L16N_VREF_2
D10B_P	AA14	IO_L16P_2
D9B_N	W15	IO_L17N_2
D9B_P	Y16	IO_L17P_2
D14B_N	W13	IO_L18N_2
D14B_P	V13	IO_L18P_2
D6B_N	AB16	IO_L19N_2
D6B_P	AA16	IO_L19P_2
	AA22	IO_L1N_M0_CMPMISO_2
D13B_N	Y14	IO_L20N_2
D13B_P	W14	IO_L20P_2
D11B_N	AB15	IO_L21N_2
D11B_P	Y15	IO_L21P_2
	U12	IO_L22N_2
	T12	IO_L22P_2
	R13	IO_L23N_2
	T14	IO_L23P_2
DCKB_N	Y12	IO_L29N_GCLK2_2
DCKB_P	W12	IO_L29P_GCLK3_2
D0B_N	AB21	IO_L2N_CMPMISO_2
D0B_P	AA21	IO_L2P_CMPCLK_2
	AB13	IO_L30N_GCLK0_USERCCLK_2
	Y13	IO_L30P_GCLK1_D13_2
	AB12	IO_L31N_GCLK30_D15_2
	AA12	IO_L31P_GCLK31_D14_2
DCKA_N	AB11	IO_L32N_GCLK28_2
DCKA_P	Y11	IO_L32P_GCLK29_2
	AB20	IO_L3N_MOSI_CSI_B_MISO0_2
	T11	IO_L40N_2
	R11	IO_L40P_2
D0A_N	AB10	IO_L41N_VREF_2
D0A_P	AA10	IO_L41P_2
D2A_N	W11	IO_L42N_2
D2A_P	V11	IO_L42P_2
D3A_N	AB9	IO_L43N_2
D3A_P	Y9	IO_L43P_2
D1A_N	Y10	IO_L44N_2
D1A_P	W10	IO_L44P_2
D5A_N	AB8	IO_L45N_2
D5A_P	AA8	IO_L45P_2
D6A_N	V7	IO_L46N_2
D6A_P	W8	IO_L46P_2
	Y8	IO_L47N_2
	W9	IO_L47P_2
D7A_N	AB7	IO_L48N_RDWR_B_VREF_2
D7A_P	Y7	IO_L48P_D7_2
D8A_N	AB6	IO_L49N_D4_2
D8A_P	AA6	IO_L49P_D3_2
	T17	IO_L4N_VREF_2
	T18	IO_L4P_2
D4A_N	V9	IO_L50N_2
D4A_P	U9	IO_L50P_2
D13A_N	U8	IO_L51N_2
D13A_P	T8	IO_L51P_2
	U10	IO_L52N_2
	T10	IO_L52P_2
D11A_N	Y6	IO_L53N_2
D11A_P	W6	IO_L53P_2
D9A_N	AB5	IO_L54N_2
D9A_P	Y5	IO_L54P_2
D10A_N	AB4	IO_L57N_2
D10A_P	AA4	IO_L57P_2
D12A_N	AB3	IO_L58N_2
D12A_P	Y3	IO_L58P_2
	R8	IO_L59N_2
	R9	IO_L59P_2
D3B_N	AB19	IO_L5N_2
D3B_P	Y19	IO_L5P_2
	R7	IO_L60N_2
	T7	IO_L60P_2
D14A_N	Y4	IO_L62N_D6_2
D14A_P	W4	IO_L62P_D5_2
D15A_N	V5	IO_L63N_2
D15A_P	U6	IO_L63P_2
	AB2	IO_L64N_D9_2
	AA2	IO_L64P_D8_2
	T5	IO_L65N_CSO_B_2
D2B_N	Y18	IO_L6N_2
D2B_P	W18	IO_L6P_2
D8B_N	T15	IO_L7N_2
D8B_P	T16	IO_L7P_2
D1B_N	U16	IO_L8N_2
D1B_P	U17	IO_L8P_2
	V18	IO_L9N_2
	V19	IO_L9P_2
	Y20	CMPCS_B_2

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INPUT C CONNECTOR

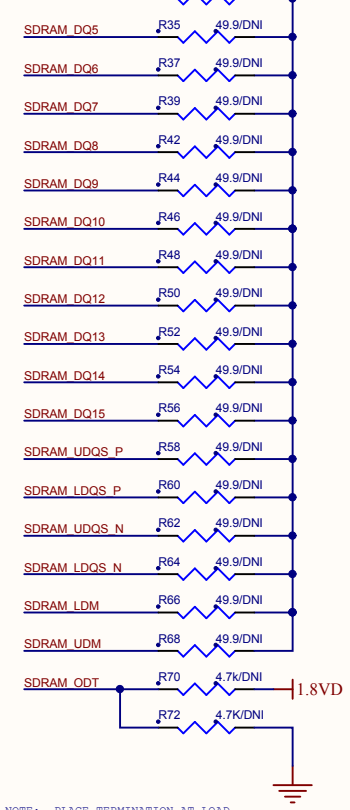


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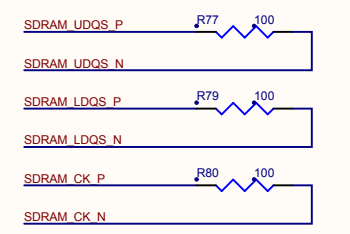
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Microchip Technology	
Size	Document Number
A	ADM00506 (Data Capture Card)
Date:	

SDRAM_DQ1	M21	IO_M1DQ1_1
SDRAM_DQ2	M22	IO_M1DQ2_1
SDRAM_DQ3	J20	IO_M1DQ3_1
SDRAM_DQ4	J20	IO_M1DQ4_1
SDRAM_DQ5	J22	IO_M1DQ5_1
SDRAM_DQ6	K21	IO_M1DQ6_1
SDRAM_DQ7	K22	IO_M1DQ7_1
SDRAM_DQ8	P21	IO_M1DQ8_1
SDRAM_DQ9	P22	IO_M1DQ9_1
SDRAM_DQ10	R20	IO_M1DQ10_1
SDRAM_DQ11	R22	IO_M1DQ11_1
SDRAM_DQ12	U20	IO_M1DQ12_1
SDRAM_DQ13	U22	IO_M1DQ13_1
SDRAM_DQ14	V21	IO_M1DQ14_1
SDRAM_DQ15	V22	IO_M1DQ15_1
SDRAM_A0	F21	IO_M1A0_1
SDRAM_A1	F22	IO_M1A1_1
SDRAM_A2	E22	IO_M1A2_1
SDRAM_A3	G20	IO_M1A3_1
SDRAM_A4	F20	IO_M1A4_1
SDRAM_A5	K20	IO_M1A5_1
SDRAM_A6	K19	IO_M1A6_1
SDRAM_A7	E20	IO_M1A7_1
SDRAM_A8	C20	IO_M1A8_1
SDRAM_A9	C22	IO_M1A9_1
SDRAM_A10	G19	IO_M1A10_1
SDRAM_A11	F19	IO_M1A11_1
SDRAM_A12	D22	IO_M1A12_1
SDRAM_A13	D19	IO_M1A13_1
SDRAM_A14	D20	IO_M1A14_1
SDRAM_BA0	J17	IO_M1BA0_1
SDRAM_BA1	K17	IO_M1BA1_1
SDRAM_BA2	H18	IO_M1BA2_1
SDRAM_CK_P	J19	IO_M1CK_P_1
SDRAM_CK_N	H20	IO_M1CK_N_1
SDRAM_ODT	G22	IO_M1ODT_1
SDRAM_CAS	H22	IO_M1CASN_1
SDRAM_RAS	H21	IO_M1RASN_1
SDRAM_LDM	L19	IO_M1LDM_1
SDRAM_UDM	M20	IO_M1UDM_1
SDRAM_LDQS_P	L20	IO_M1LDQS_P_1
SDRAM_LDQS_N	L22	IO_M1LDQS_N_1
SDRAM_UDQS_P	T21	IO_M1UDQS_P_1
SDRAM_UDQS_N	T22	IO_M1UDQS_N_1
SDRAM_WE	H19	IO_M1WE_1
SDRAM_CKE	D21	IO_M1CKE_1
	F18	IO_M1RESET_1
	F17	IO_L10N_1
	F16	IO_L10P_1
	B22	IO_L19N_1
	B21	IO_L19P_1
	C19	IO_L1P_A25_1
	A21	IO_L20N_1
	A20	IO_L20P_1
	J16	IO_L21N_1
	K16	IO_L21P_1
	H16	IO_L28P_1
	M19	IO_L53P_1
	L15	IO_L58N_1
	M16	IO_L58P_1
	P20	IO_L59N_1
	P19	IO_L59P_1
	W22	IO_L60N_1
	W20	IO_L60P_1
	K18	IO_L61N_1
	L17	IO_L61P_1
	V20	IO_L70N_1
	U19	IO_L70P_1
	M18	IO_L71N_1
	M17	IO_L71P_1
	N16	IO_L72N_1
	N16	IO_L72P_1
	P17	IO_L73N_1
	R19	IO_L73P_1
	P18	IO_L74N_DOUT_BUSY_1
	T20	IO_L74P_AWAKE_1
	T19	IO_L9N_1
	G17	IO_L9P_1
	G16	IO_L1N_A24_VREF_1
	B20	IO_L28N_VREF_1
	H17	IO_L28P_VREF_1
	N19	IO_L53N_VREF_1

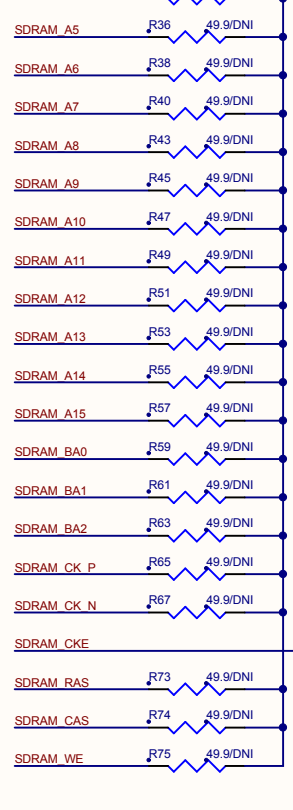
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NOTE: PLACE TERMINATION AT LOAD



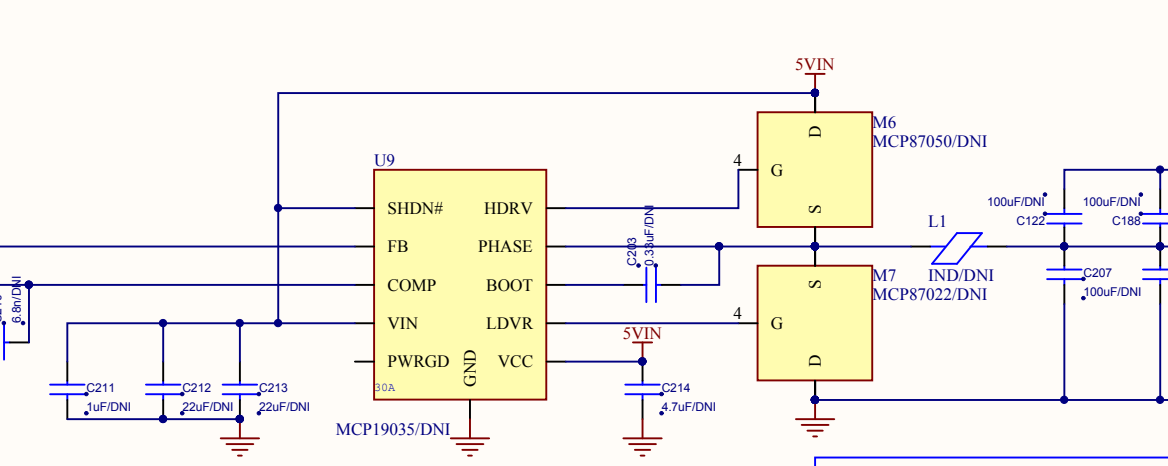
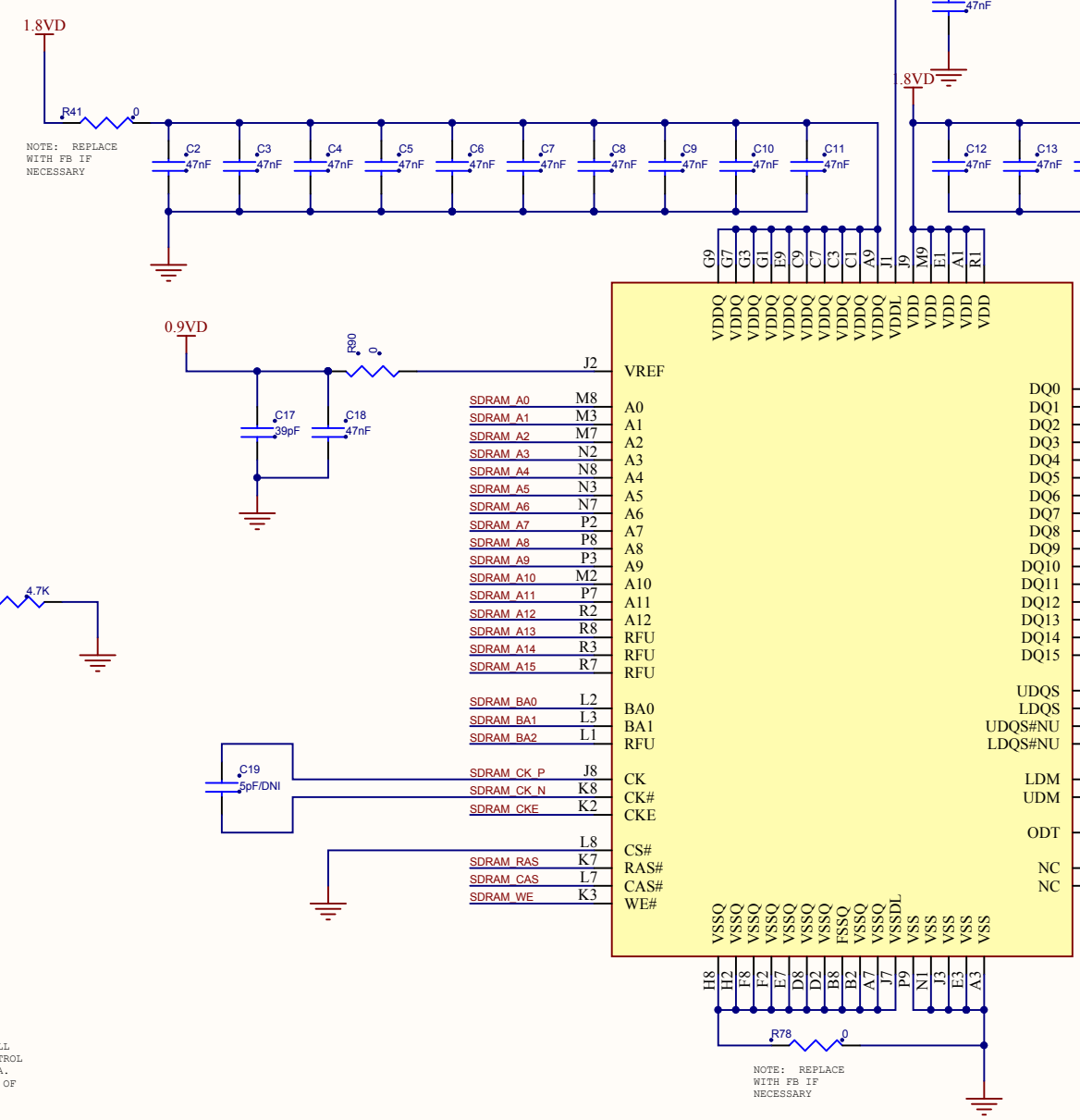
NOTE: PLACE TERMINATION AT LOAD



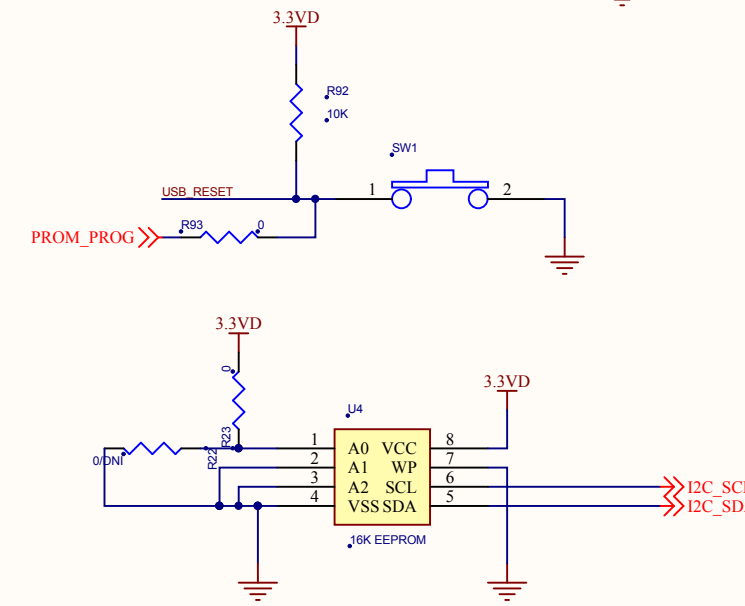
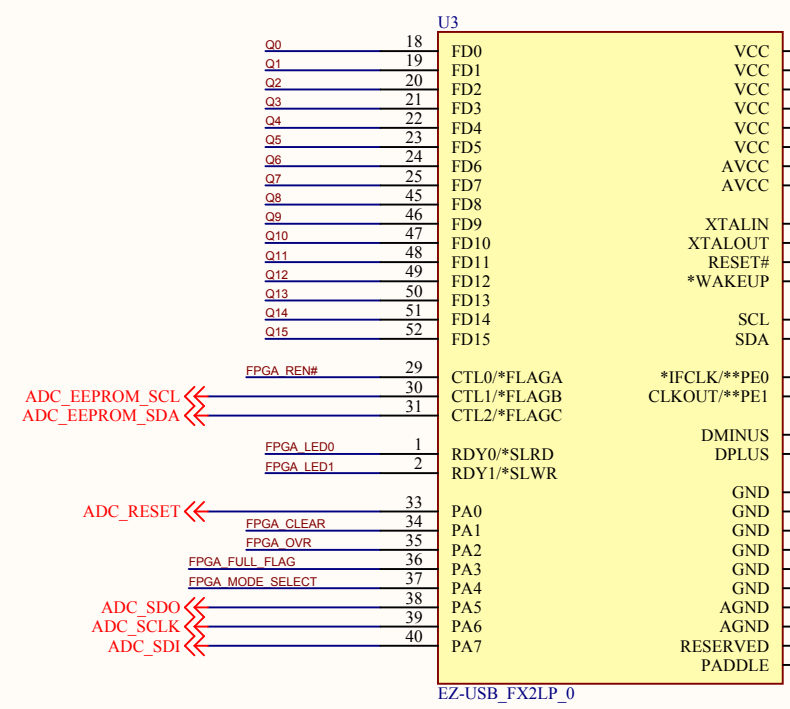
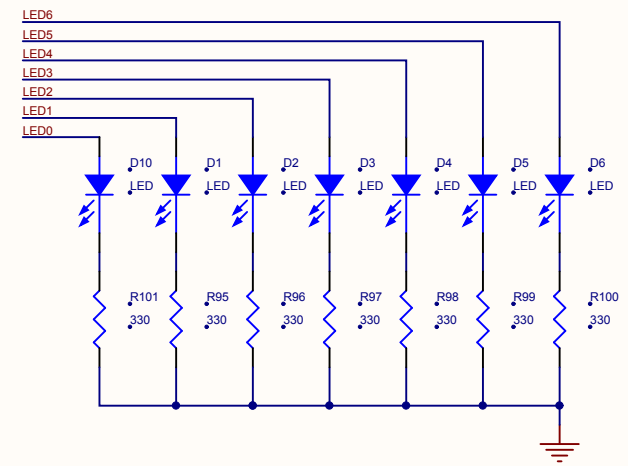
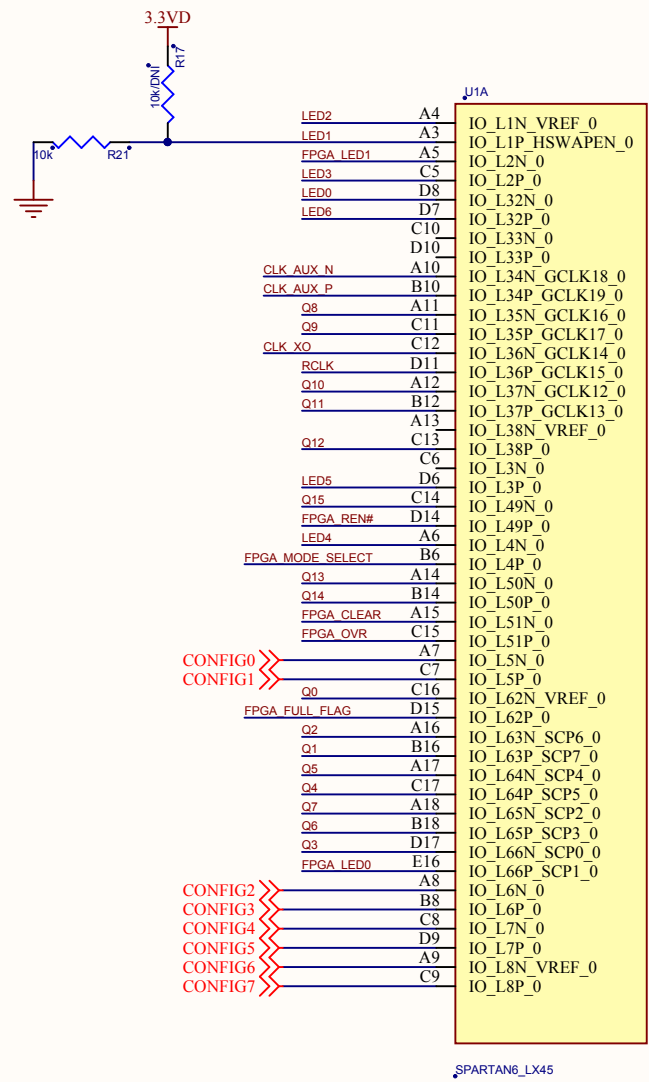
NOTE: PLACE TERMINATION AT LOAD

NOTE: ALL TRACES ROUTED AT 50 OHM SINGLE-ENDED, ALL DIFFERENTIAL TRACES ROUTED AT 100 OHM DIFFERENTIAL. TRACE LENGTHS SHOULD BE MATCHED TO KEEP PROPAGATION DELAY BETWEEN ANY TWO TRACES TO LESS THAN 25ps.

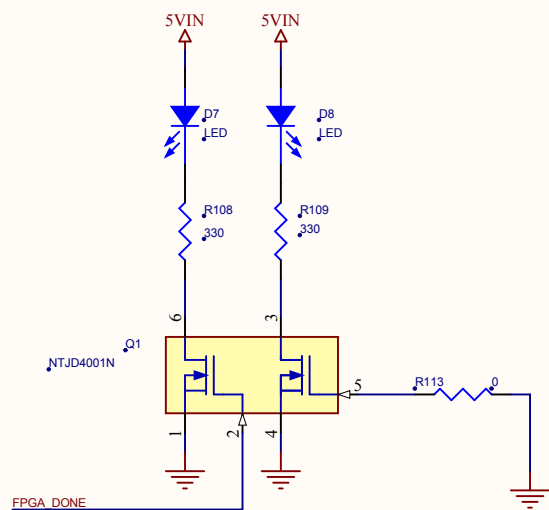
NOTE: SDRAM_LOOP PINS SHOULD BE ROUTED THE FULL DISTANCE TO THE SDRAM AND BACK TO FPGA JUST LIKE ALL OTHER SDRAM PINS TO SERVE AS TIMING ADJUSTMENT CONTROL FOR THE FPGA. IE. DO NOT CONNECT THEM AT THE FPGA. SIGNAL SHOULD BE ROUTED IN THE MIDDLE OF THE GROUP OF DQ ROUTES.



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D13 NC
E10 NC
E12 NC
E14 NC
E8 NC
F10 NC
F12 NC
F13 NC
F14 NC
F15 NC
F8 NC
F9 NC
G11 NC
G13 NC
G8 NC
G9 NC
H10 NC
H11 NC
H12 NC
H13 NC
H14 NC
P16 NC
R17 NC
P15 NC
D12 NC

A1 GND
A22 GND
AA13 GND
AA17 GND
AA5 GND
AA9 GND
AB1 GND
AB22 GND
B13 GND
B17 GND
B5 GND
B9 GND
D18 GND
D4 GND
E11 GND
E15 GND
E2 GND
E21 GND
E7 GND
G18 GND
G5 GND
H7 GND
J11 GND
J13 GND
J15 GND
J2 GND

J21 GND
J9 GND
K10 GND
K12 GND
K14 GND
L11 GND
L13 GND
L18 GND
L5 GND
L9 GND
M10 GND
M12 GND
M14 GND
M11 GND
N13 GND
N17 GND
N2 GND
N21 GND
N9 GND
P10 GND
P12 GND
P14 GND
R18 GND
R5 GND
U2 GND
U21 GND
U7 GND
V10 GND
V14 GND
V4 GND
W16 GND
W19 GND
W7 GND

V12
T9
VCCO_2
T13
VCCO_2
AA7
AA3
VCCO_2
AA19
AA15
VCCO_2
AA11

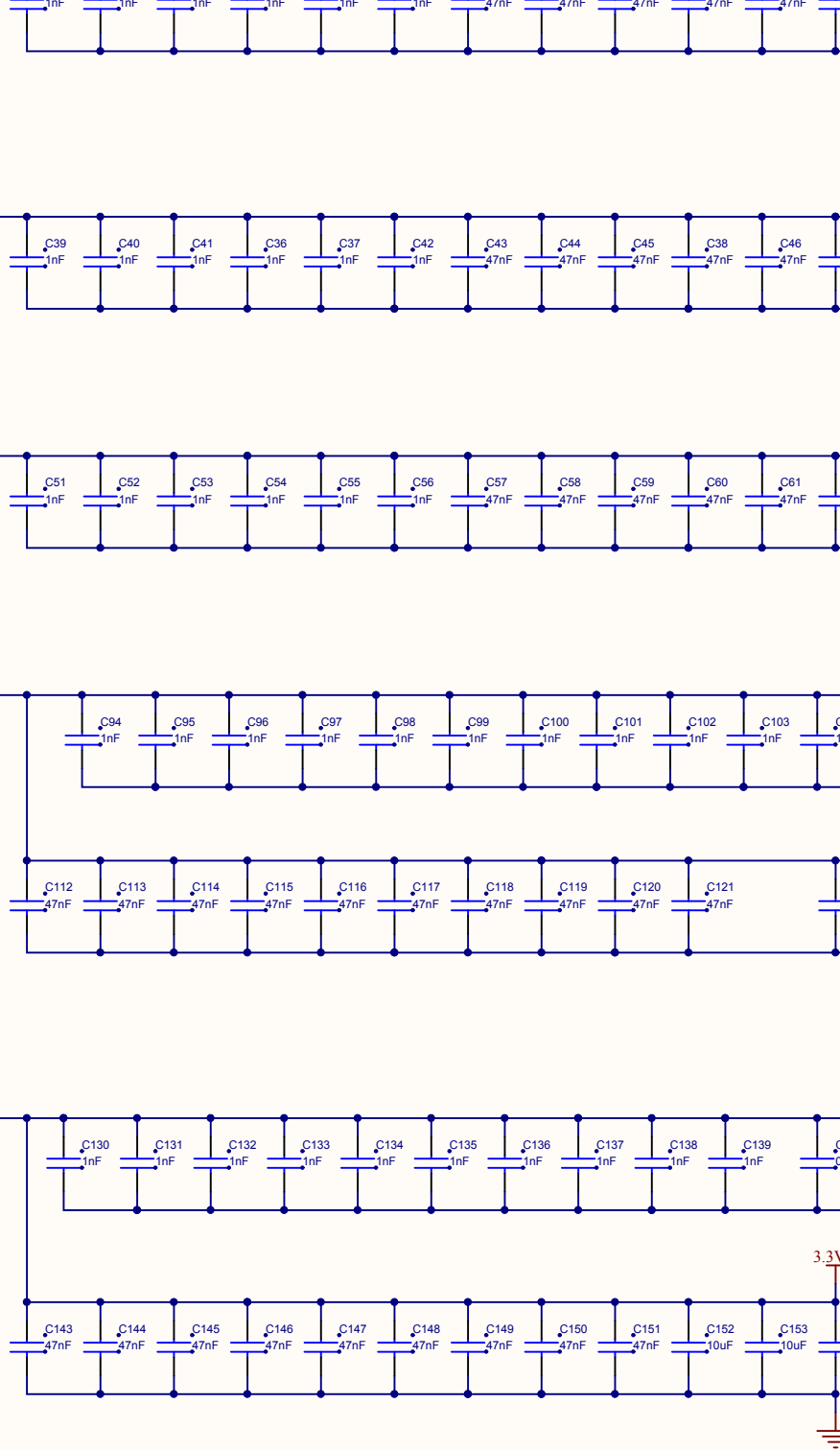
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U18
R21
N18
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L21
L16
VCCO_1
J18
VCCO_1
G21
E19
VCCO_1
C21

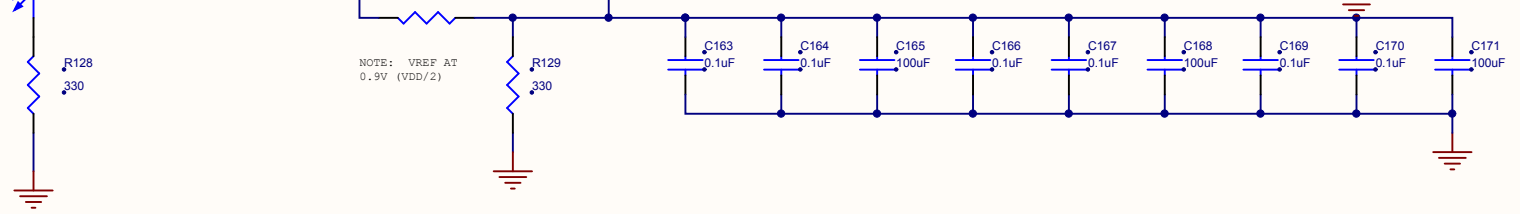
G14
G10
VCCO_0
E9
VCCO_0
E17
VCCO_0
E13
VCCO_0
B7
VCCO_0
B19
VCCO_0
B15
VCCO_0
B11

R14
P9
VCCINT
P13
VCCINT
P11
VCCINT
N14
VCCINT
N12
VCCINT
N10
VCCINT
M9
VCCINT
M13
VCCINT
M11
VCCINT
L14
VCCINT
L12
VCCINT
L10
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VCCINT
J8
VCCINT
J14
VCCINT
J12
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J10

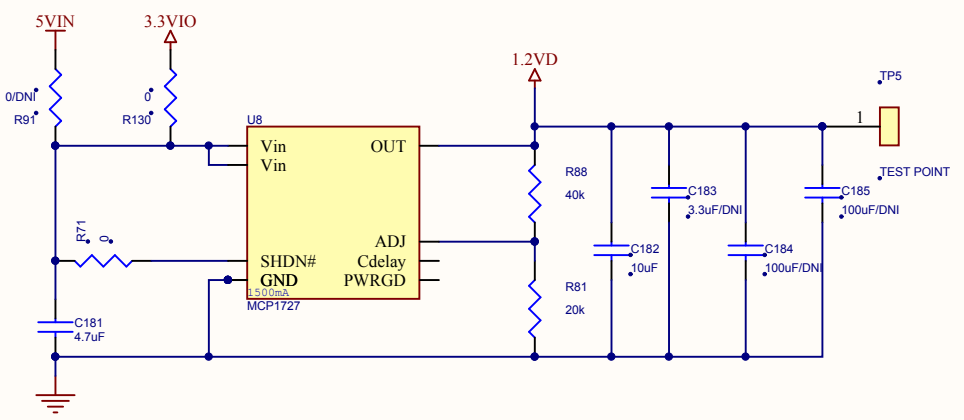
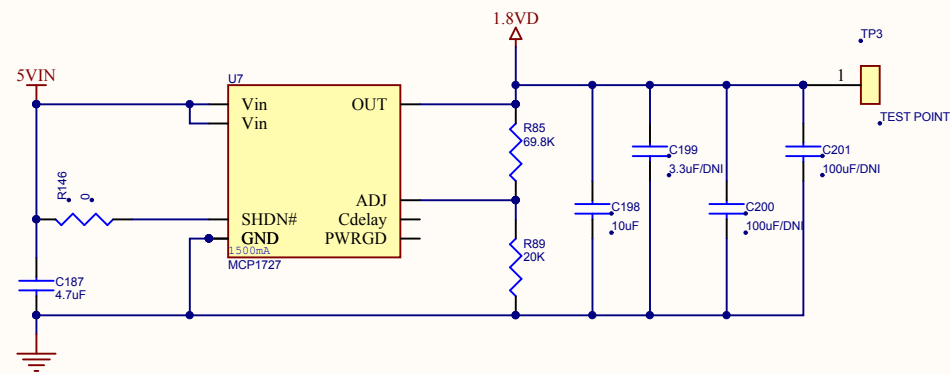
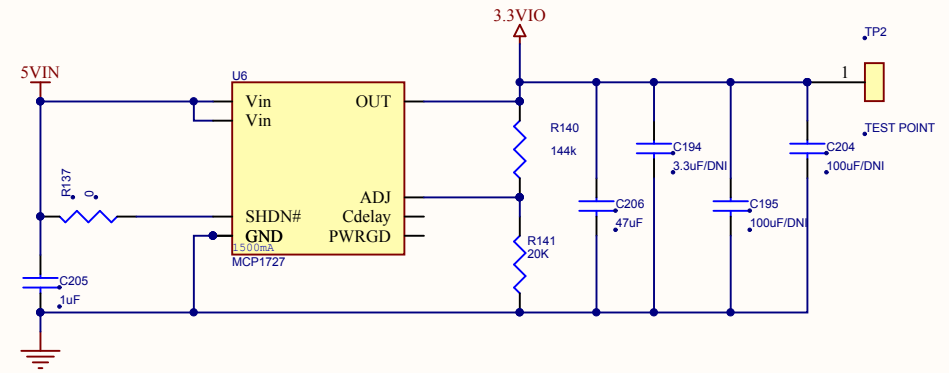
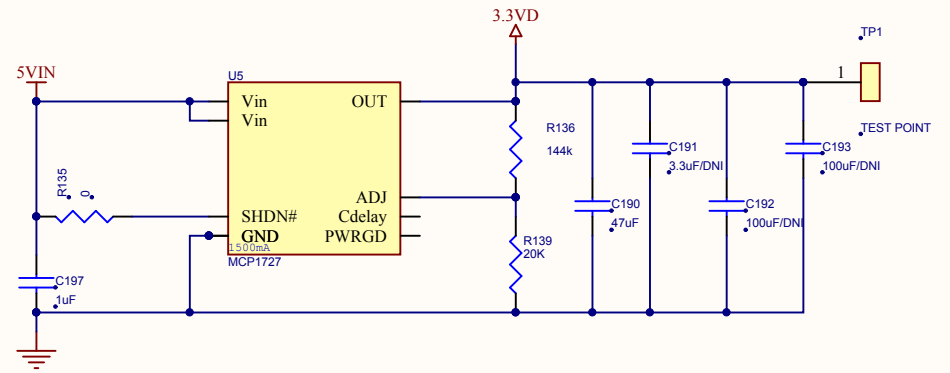
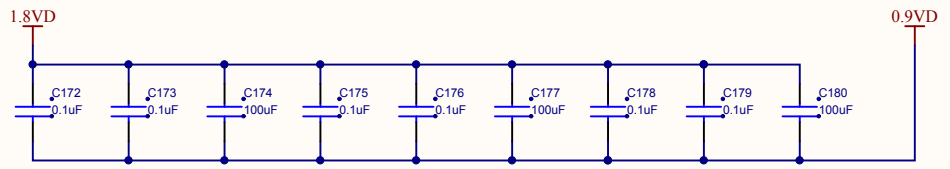
F11
VCCAUX
D16
VCCAUX
V6
VCCAUX
U11
VCCAUX
R6
VCCAUX
R12
VCCAUX
R10
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N8
VCCAUX
M15
VCCAUX
L8
VCCAUX
K15
VCCAUX
H9
VCCAUX
H15
VCCAUX
G12

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NOTE: USE IF SUPPLYING 3.3V TO EXTERNAL POWER CONNECTOR. MUST ALSO REMOVE OR SHUTDOWN 3.3V REGULATOR.



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