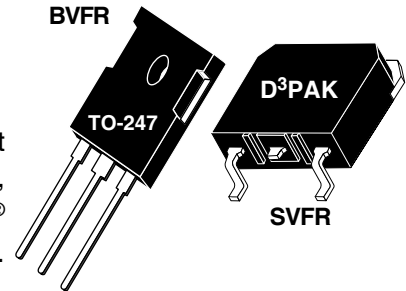
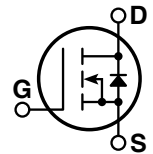


**POWER MOS V® FREDFET**

Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V® also achieves faster switching speeds through optimized gate layout.



- Avalanche Energy Rated
- Lower Leakage
- Faster Switching
- **FAST RECOVERY BODY DIODE**
- TO-247 or Surface Mount D³PAK Package



**MAXIMUM RATINGS**

 All Ratings:  $T_C = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	APT1001RBVFR_SVFR	UNIT
$V_{DSS}$	Drain-Source Voltage	1000	Volts
$I_D$	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	11	Amps
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	44	
$V_{GS}$	Gate-Source Voltage Continuous	$\pm 30$	Volts
$V_{GSM}$	Gate-Source Voltage Transient	$\pm 40$	
$P_D$	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	278	Watts
	Linear Derating Factor	2.22	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$T_L$	Lead Temperature: 0.063" from Case for 10 Sec.	300	
$I_{AR}$	Avalanche Current <sup>①</sup> (Repetitive and Non-Repetitive)	11	Amps
$E_{AR}$	Repetitive Avalanche Energy <sup>①</sup>	30	mJ
$E_{AS}$	Single Pulse Avalanche Energy <sup>④</sup>	1210	

**STATIC ELECTRICAL CHARACTERISTICS**

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-Source Breakdown Voltage ( $V_{GS} = 0V, I_D = 250\mu\text{A}$ )	1000			Volts
$R_{DS(on)}$	Drain-Source On-State Resistance <sup>②</sup> ( $V_{GS} = 10V, I_D = 5.5A$ )			1.00	Ohms
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{DS} = 1000V, V_{GS} = 0V$ )			250	$\mu\text{A}$
	Zero Gate Voltage Drain Current ( $V_{DS} = 800V, V_{GS} = 0V, T_C = 125^\circ\text{C}$ )			1000	
$I_{GSS}$	Gate-Source Leakage Current ( $V_{GS} = \pm 30V, V_{DS} = 0V$ )			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage ( $V_{DS} = V_{GS}, I_D = 1mA$ )	2		4	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

**DYNAMIC CHARACTERISTICS**

**APT1001RBVFR\_SVFR**

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
$C_{iss}$	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1\text{ MHz}$		3050		pF
$C_{oss}$	Output Capacitance			280		
$C_{rss}$	Reverse Transfer Capacitance			135		
$Q_g$	Total Gate Charge ③	$V_{GS} = 10V$ $V_{DD} = 500V$ $I_D = 11A @ 25^\circ C$		150		nC
$Q_{gs}$	Gate-Source Charge			16		
$Q_{gd}$	Gate-Drain ("Miller") Charge			70		
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$ $V_{DD} = 500V$ $I_D = 11A @ 25^\circ C$ $R_G = 1.6\Omega$		12		ns
$t_r$	Rise Time			11		
$t_{d(off)}$	Turn-off Delay Time			55		
$t_f$	Fall Time			12		

**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS**

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
$I_S$	Continuous Source Current (Body Diode)			11	Amps
$I_{SM}$	Pulsed Source Current ① (Body Diode)			44	Amps
$V_{SD}$	Diode Forward Voltage ② ( $V_{GS} = 0V, I_S = -11A$ )			1.3	Volts
$dv/dt$	Peak Diode Recovery $dv/dt$ ⑤			18	V/ns
$t_{rr}$	Reverse Recovery Time ( $I_S = -11A, di/dt = 100A/\mu s$ )	$T_j = 25^\circ C$		200	ns
		$T_j = 125^\circ C$		350	
$Q_{rr}$	Reverse Recovery Charge ( $I_S = -11A, di/dt = 100A/\mu s$ )	$T_j = 25^\circ C$		0.7	$\mu C$
		$T_j = 125^\circ C$		1.5	
$I_{RRM}$	Peak Recovery Current ( $I_S = -11A, di/dt = 100A/\mu s$ )	$T_j = 25^\circ C$		11	Amps
		$T_j = 125^\circ C$		16	

**THERMAL CHARACTERISTICS**

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.45	$^\circ C/W$
$R_{\theta JA}$	Junction to Ambient			40	

- ① Repetitive Rating: Pulse width limited by maximum junction temperature
- ② Pulse Test: Pulse width < 380  $\mu s$ , Duty Cycle < 2%
- ③ See MIL-STD-750 Method 3471

- ④ Starting  $T_j = +25^\circ C, L = 20.0mH, R_G = 25\Omega, \text{Peak } I_L = 11A$
- ⑤  $dv/dt$  numbers reflect the limitations of the test circuit rather than the device itself.  $I_S \leq -I_D 11A, di/dt \leq 700A/\mu s, v_R \leq 1000V, T_j \leq 150^\circ C$

APT Reserves the right to change, without notice, the specifications and information contained herein.

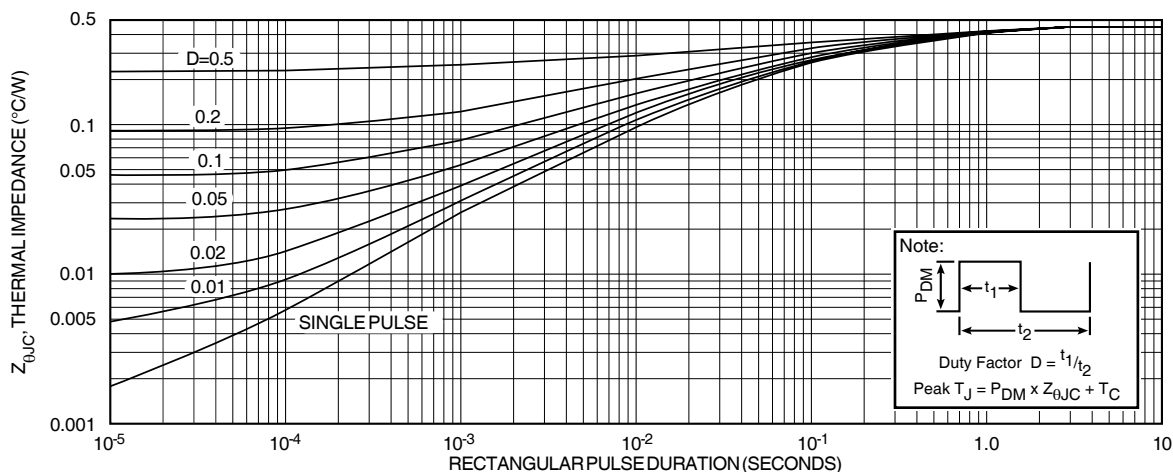


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Typical Performance Curves

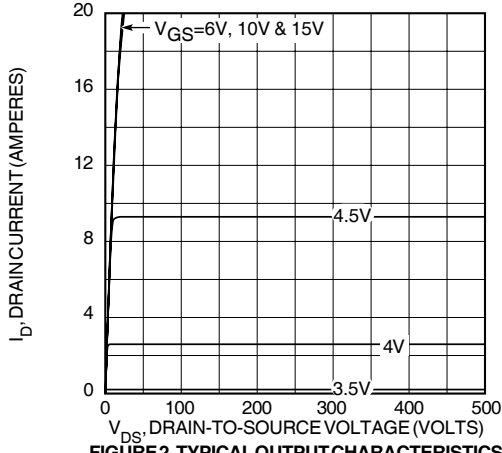


FIGURE 2, TYPICAL OUTPUT CHARACTERISTICS

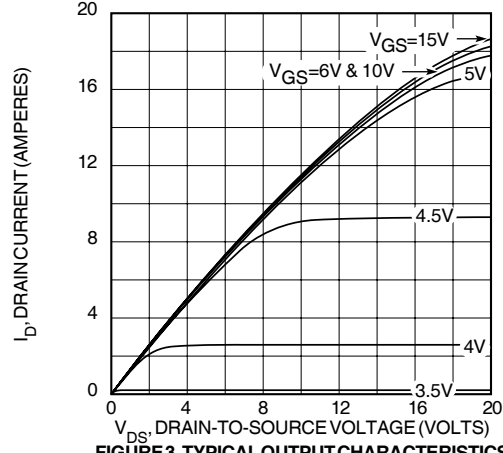


FIGURE 3, TYPICAL OUTPUT CHARACTERISTICS

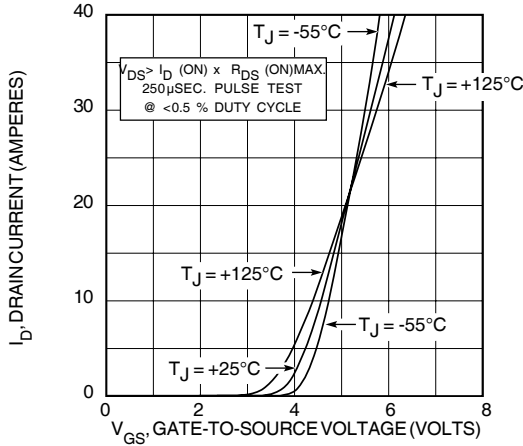


FIGURE 4, TYPICAL TRANSFER CHARACTERISTICS

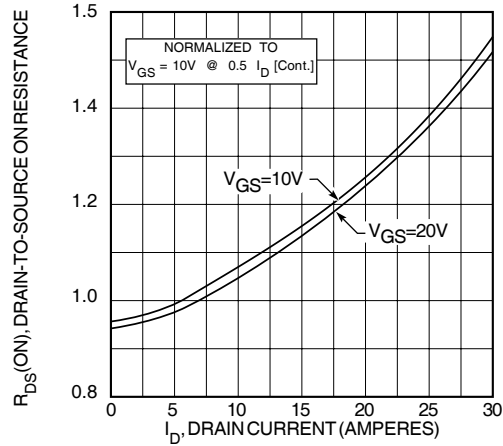


FIGURE 5,  $R_{DS(ON)}$  vs DRAIN CURRENT

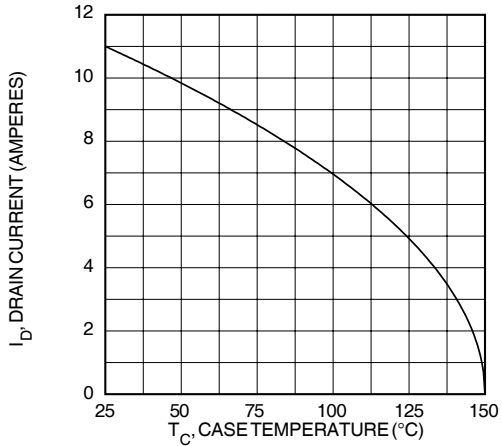


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

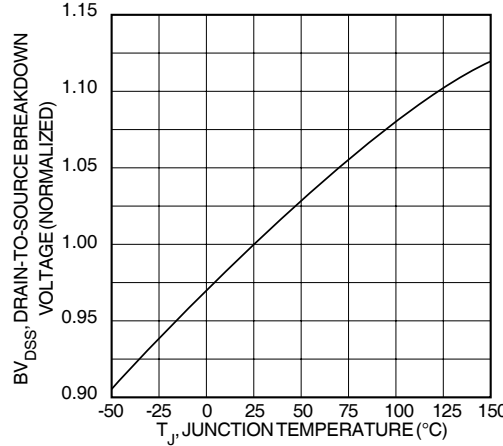


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

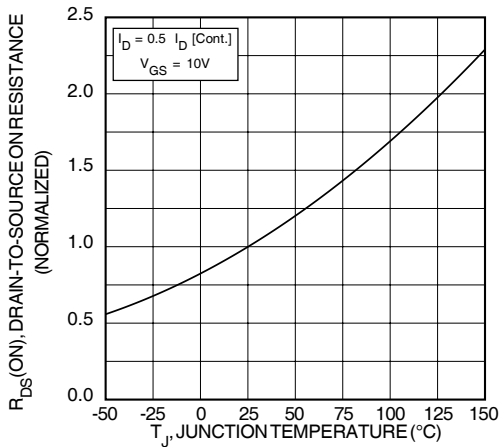


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

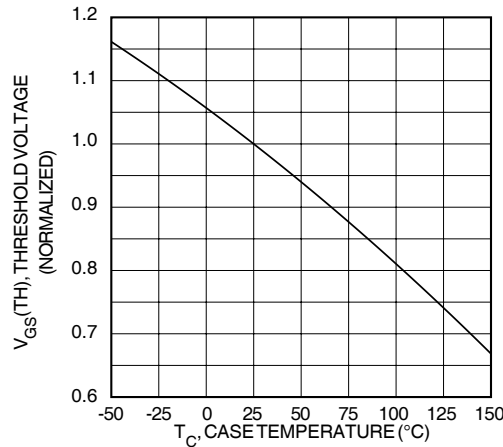


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

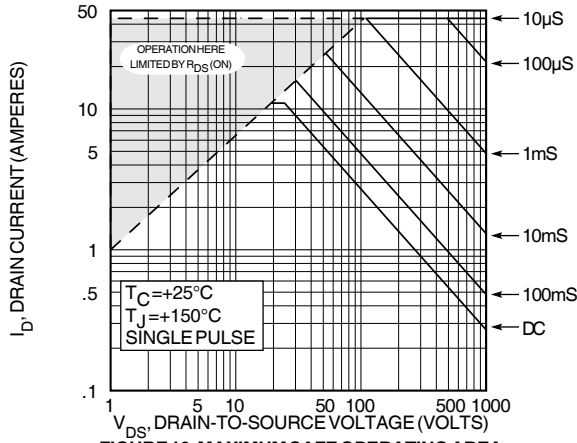


FIGURE 10, MAXIMUM SAFE OPERATING AREA

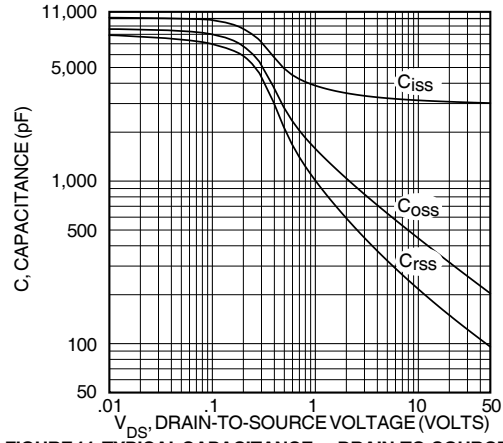


FIGURE 11, TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

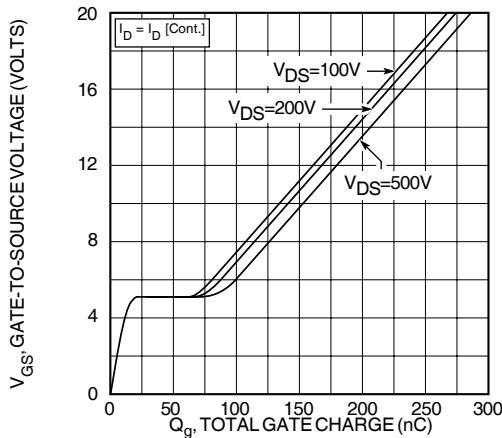


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

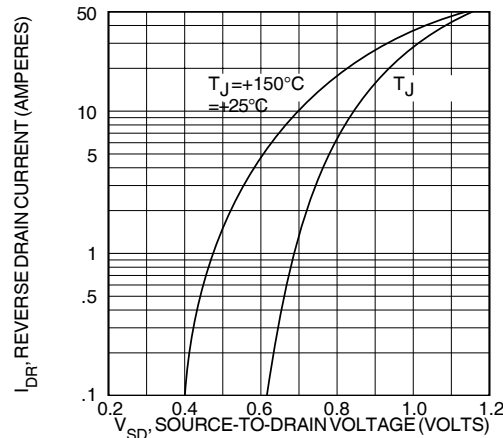
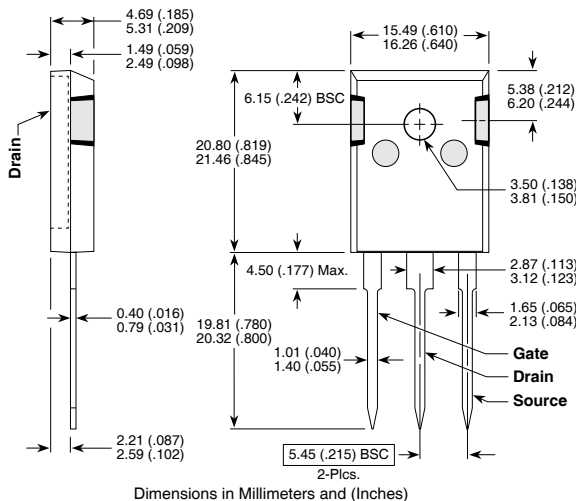


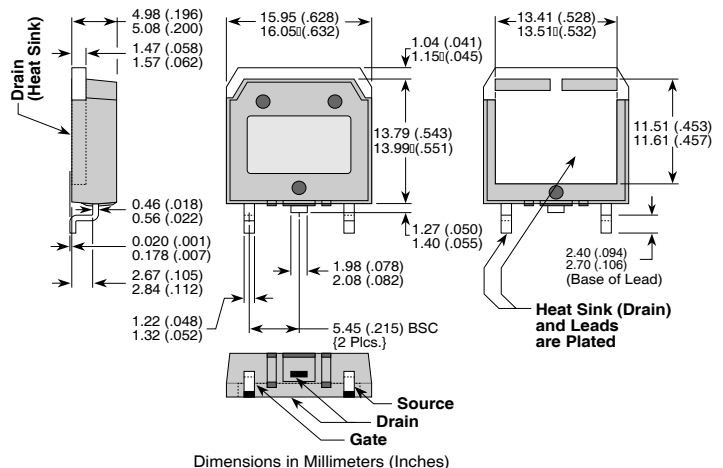
FIGURE 13, TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

TO-247 Package Outline (BVFR)



Dimensions in Millimeters and (Inches)

D<sup>3</sup>PAK Package Outline (SVFR)



Dimensions in Millimeters (Inches)

APT's products are covered by one or more of U.S. patents 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522

5,262,336 6,503,786 5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058 and foreign patents. US and Foreign patents pending. All Rights Reserved.

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