## N-Channel FREDFET

POWER MOS 8® is a high speed, high voltage N-channel switch-mode power MOSFET. This 'FREDFET' version has a drain-source (body) diode that has been optimized for high reliability in ZVS phase shifted bridge and other circuits through reduced t_{rr}, soft recovery, and high recovery dv/dt capability. Low gate charge, high gain, and a greatly reduced ratio of C_{rss}/C_{iss} result in excellent niose immunity and low switching loss. The intrinsic gate resistance and capacitance of the poly-silicon gate structure help control di/dt during switching, resulting in low EMI and reliable paralleling, even when switching at very high frequency.

ISOTOP®
APT17F120J
Single die FREDFET

"UL Recognized"
file # E145592
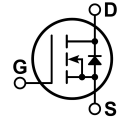
FEATURES

- **Fast switching with low EMI**
- **Low t_{rr} for high reliability**
- **Ultra low C_{rss} for improved noise immunity**
- **Low gate charge**
- **Avalanche energy rated**
- **RoHS compliant**

TYPICAL APPLICATIONS

- **ZVS phase shifted and other full full bridge**
- **Half bridge**
- **PFC and other boost converter**
- **Buck converter**
- **Single and two switch forward**
- **Flyback**

Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
I_D	Continuous Drain Current @ T_C = 25°C	18	A
	Continuous Drain Current @ T_C = 100°C	12	
I_{DM}	Pulsed Drain Current [1]	104	
V_{GS}	Gate-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy [2]	2165	mJ
I_{AR}	Avalanche Current, Repetitive or Non-Repetitive	14	A

Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
P_D	Total Power Dissipation @ T_C = 25°C			545	W
$R_{\theta JC}$	Junction to Case Thermal Resistance			0.23	°C/W
$R_{\theta CS}$	Case to Sink Thermal Resistance, Flat, Greased Surface		0.15		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55		150	°C
$V_{Isolation}$	RMS Voltage (50-60hHz Sinusoidal Wavefomr from Terminals to Mounting Base for 1 Min.)	2500			V
W_T	Package Weight		1.03		oz
			29.2		g
Torque	Terminals and Mounting Screws.			10	in·lbf
				1.1	N·m

050-8167 Rev B 8-2011

Static Characteristics $\quad T_J = 25°C$ unless otherwise specified $\qquad$ APT17F120J

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
$V_{BR(DSS)}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V$, $I_D = 250\mu A$		1200			V
$\Delta V_{BR(DSS)}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	Reference to 25°C, $I_D = 250\mu A$			1.41		V/°C
$R_{DS(on)}$	Drain-Source On Resistance ③	$V_{GS} = 10V$, $I_D = 14A$			0.55	0.58	Ω
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 2.5mA$		2.5	4	5	V
$\Delta V_{GS(th)}/\Delta T_J$	Threshold Voltage Temperature Coefficient				-10		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 1200V$	$T_J = 25°C$			250	μA
		$V_{GS} = 0V$	$T_J = 125°C$			1000	
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm30V$				±100	nA

Dynamic Characteristics $\quad T_J = 25°C$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g_{fs}	Forward Transconductance	$V_{DS} = 50V$, $I_D = 14A$		31		S
C_{iss}	Input Capacitance	$V_{GS} = 0V$, $V_{DS} = 25V$ $f = 1MHz$		9670		pF
C_{rss}	Reverse Transfer Capacitance			115		
C_{oss}	Output Capacitance			715		
$C_{o(cr)}$ ④	Effective Output Capacitance, Charge Related	$V_{GS} = 0V$, $V_{DS} = 0V$ to $800V$		275		
$C_{o(er)}$ ⑤	Effective Output Capacitance, Energy Related			140		
Q_g	Total Gate Charge	$V_{GS} = 0$ to $10V$, $I_D = 14A$, $V_{DS} = 600V$		300		nC
Q_{gs}	Gate-Source Charge			50		
Q_{gd}	Gate-Drain Charge			140		
$t_{d(on)}$	Turn-On Delay Time	**Resistive Switching** $V_{DD} = 800V$, $I_D = 14A$ $R_G = 2.2\Omega$⑥, $V_{GG} = 15V$		50		ns
t_r	Current Rise Time			31		
$t_{d(off)}$	Turn-Off Delay Time			170		
t_f	Current Fall Time			48		

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions			Min	Typ	Max	Unit
I_S	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode (body diode)					18	A
I_{SM}	Pulsed Source Current (Body Diode)①						104	
V_{SD}	Diode Forward Voltage	$I_{SD} = 14A$, $T_J = 25°C$, $V_{GS} = 0V$					1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 14A$③ $di_{SD}/dt = 100A/\mu s$	$T_J = 25°C$				330	ns
			$T_J = 125°C$				660	
Q_{rr}	Reverse Recovery Charge		$T_J = 25°C$			1.72		μC
			$T_J = 125°C$			4.67		
I_{rrm}	Reverse Recovery Current		$T_J = 25°C$			11		A
			$T_J = 125°C$			16		
dv/dt	Peak Recovery dv/dt	$I_{SD} \leq 14A$, $di/dt \leq 1000A/\mu s$, $V_{DD} = 100V$, $T_J = 125°C$					25	V/ns

① Repetitive Rating: Pulse width and case temperature limited by maximum junction temperature.

② Starting at $T_J = 25°C$, $L = 22.1mH$, $R_G = 25\Omega$, $I_{AS} = 14A$.

③ Pulse test: Pulse Width < 380μs, duty cycle < 2%.

④ $C_{o(cr)}$ is defined as a fixed capacitance with the same stored charge as C_{OSS} with $V_{DS} = 67\%$ of $V_{(BR)DSS}$.

⑤ $C_{o(er)}$ is defined as a fixed capacitance with the same stored energy as C_{OSS} with $V_{DS} = 67\%$ of $V_{(BR)DSS}$. To calculate $C_{o(er)}$ for any value of V_{DS} less than $V_{(BR)DSS,}$ use this equation: $C_{o(er)} = -8.27E\text{-}7/V_{DS}{}^2 + 1.01E\text{-}7/V_{DS} + 1.43E\text{-}10$.

⑥ R_G is external gate resistance, not including internal gate resistance or gate driver impedance. (MIC4452)

Microsemi reserves the right to change, without notice, the specifications and information contained herein.
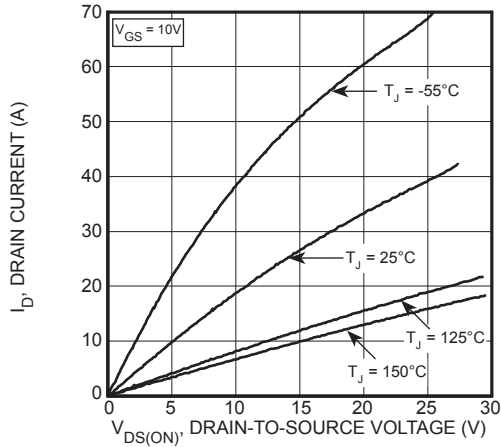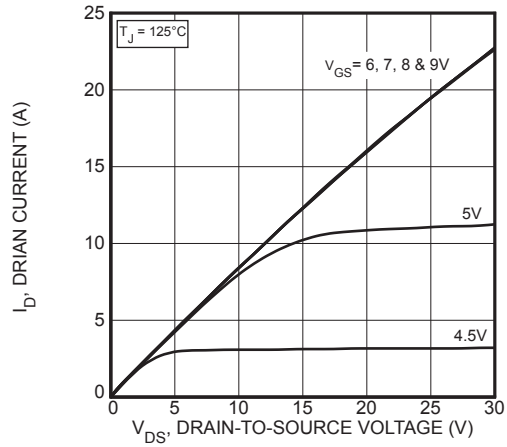
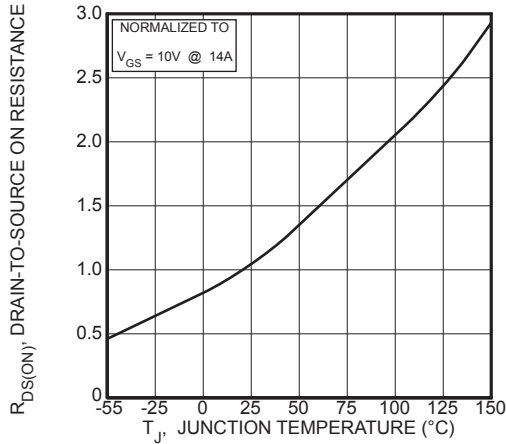**Figure 1, Output Characteristics**

Figure 2, Output Characteristics
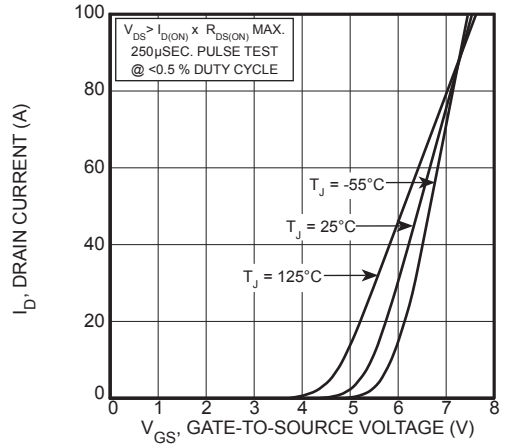
Figure 3, R$_{DS(ON)}$ vs Junction Temperature

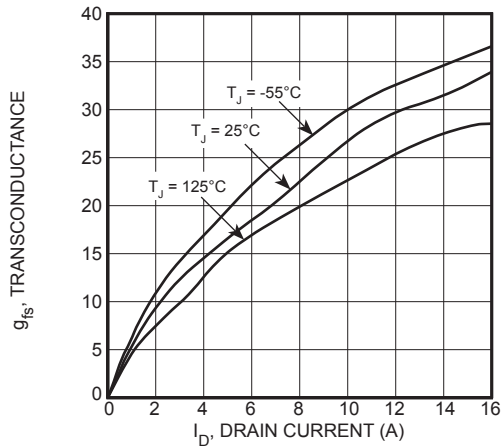**Figure 4, Transfer Characteristics**

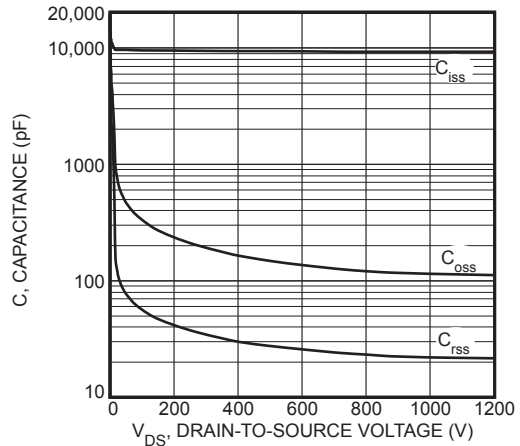**Figure 5, Gain vs Drain Current**

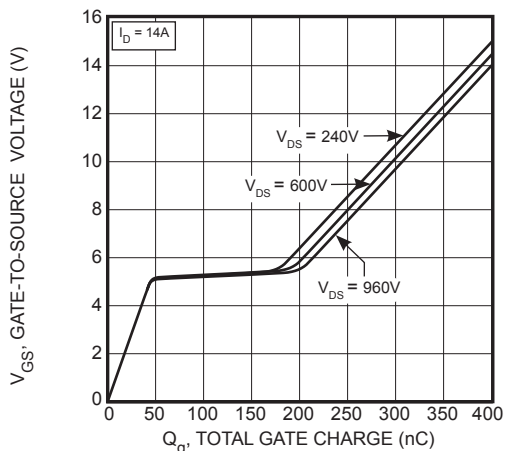**Figure 6, Capacitance vs Drain-to-Source Voltage**
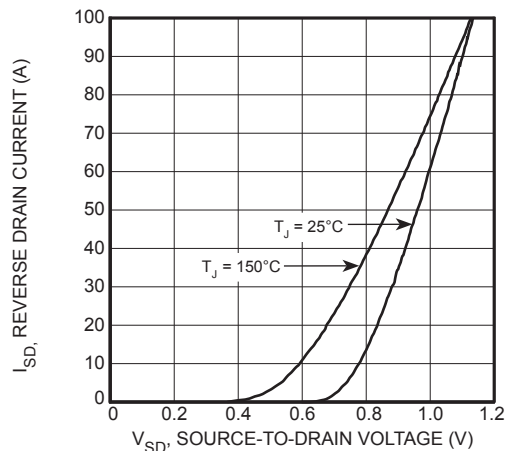
Figure 7, Gate Charge vs Gate-to-Source Voltage
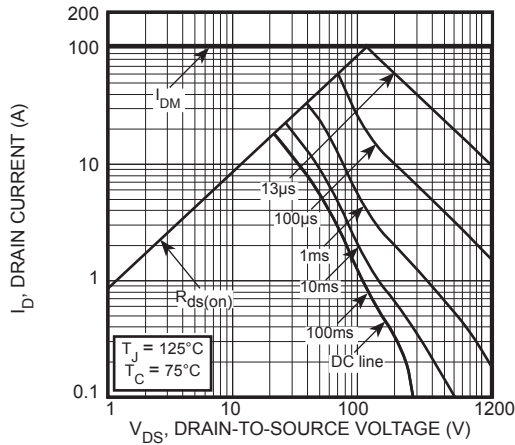
Figure 8, Reverse Drain Current vs Source-to-Drain Voltage
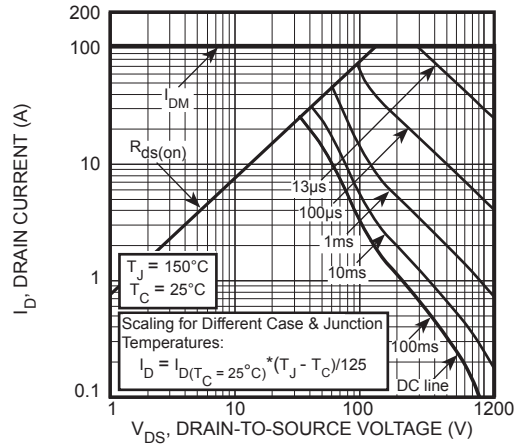
Figure 9, Forward Safe Operating Area

I_D, DRAIN CURRENT (A)

V_{DS}, DRAIN-TO-SOURCE VOLTAGE (V)

I_{DM}

$R_{ds(on)}$

13µs
100µs
1ms
10ms
100ms
DC line

$T_J = 125°C$
$T_C = 75°C$

Figure 10, Maximum Forward Safe Operating Area

I_D, DRAIN CURRENT (A)

V_{DS}, DRAIN-TO-SOURCE VOLTAGE (V)

I_{DM}

$R_{ds(on)}$

13µs
100µs
1ms
10ms
100ms
DC line

$T_J = 150°C$
$T_C = 25°C$

Scaling for Different Case & Junction Temperatures:

$$I_D = I_{D(T_C = 25°C)} * (T_J - T_C)/125$$

$Z_{\theta JC}$, THERMAL IMPEDANCE (°C/W)

D = 0.9
0.7
0.5
0.3
0.1
0.05

SINGLE PULSE

Note:

P_{DM}
t_1
t_2

t_1 = Pulse Duration
Duty Factor D = t_1/t_2
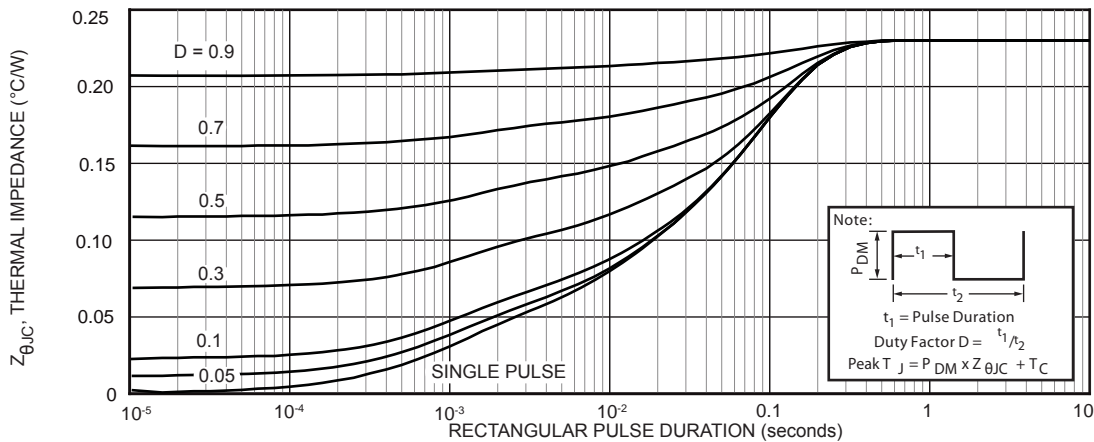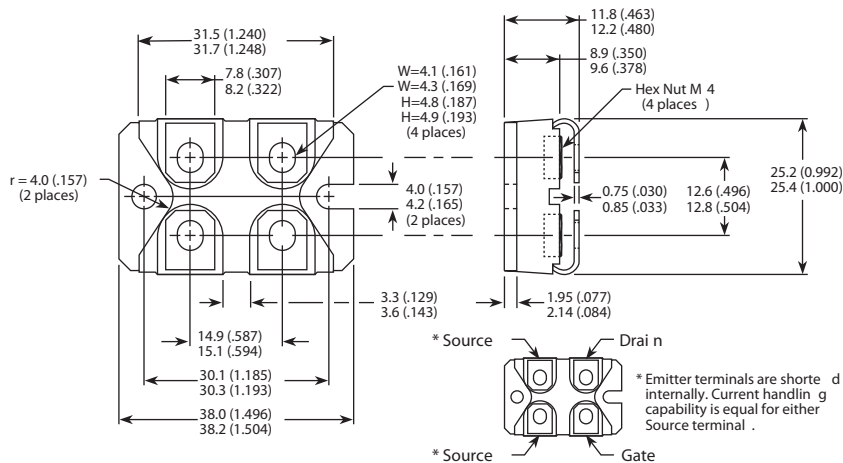Peak $T_J = P_{DM}$ x $Z_{\theta JC}$ + T_C

RECTANGULAR PULSE DURATION (seconds)

Figure 11. Maximum Effective Transient Thermal Impedance Junction-to-Case vs Pulse Duration

SOT-227 (ISOTOP®) Package Outline

31.5 (1.240)
31.7 (1.248)

7.8 (.307)
8.2 (.322)

W=4.1 (.161)
W=4.3 (.169)
H=4.8 (.187)
H=4.9 (.193)
(4 places)

r = 4.0 (.157)
(2 places)

4.0 (.157)
4.2 (.165)
(2 places)

3.3 (.129)
3.6 (.143)

14.9 (.587)
15.1 (.594)

30.1 (1.185)
30.3 (1.193)

38.0 (1.496)
38.2 (1.504)

11.8 (.463)
12.2 (.480)

8.9 (.350)
9.6 (.378)

Hex Nut M 4
(4 places)

0.75 (.030)   12.6 (.496)
0.85 (.033)   12.8 (.504)

25.2 (0.992)
25.4 (1.000)

1.95 (.077)
2.14 (.084)

* Source   Drai n

* Emitter terminals are shorte d
internally. Current handlin g
capability is equal for either
Source terminal .

* Source   Gate

Dimensions in Millimeters and (Inches)

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