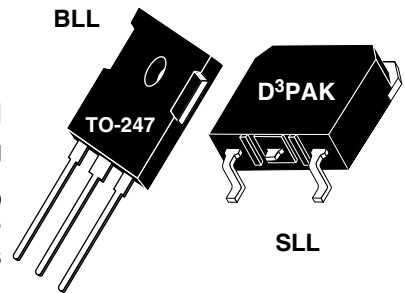
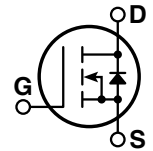


POWER MOS 7® MOSFET

Power MOS 7® is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7® by significantly lowering $R_{DS(ON)}$ and Q_g . Power MOS 7® combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.



- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge, Q_g
- Increased Power Dissipation
- Easier To Drive
- TO-247 or Surface Mount D³PAK Package




MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT5024BLL_SLL(G)	UNIT
V_{DSS}	Drain-Source Voltage	500	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	22	Amps
I_{DM}	Pulsed Drain Current ^①	88	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	265	Watts
	Linear Derating Factor	2.12	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	22	Amps
E_{AR}	Repetitive Avalanche Energy ^①	30	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	960	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu\text{A}$)	500			Volts
$I_{D(on)}$	On State Drain Current ^② ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	22			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, I_D = 11A$)			0.24	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = 500V, V_{GS} = 0V$)			100	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 400V, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			500	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1mA$)	3		5	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

DYNAMIC CHARACTERISTICS

APT5024BLL_SLL(G)

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C _{iss}	Input Capacitance	V _{GS} = 0V V _{DS} = 25V f = 1 MHz		1900		pF
C _{oss}	Output Capacitance			417		
C _{rss}	Reverse Transfer Capacitance			27		
Q _g	Total Gate Charge ③	V _{GS} = 10V V _{DD} = 250V I _D = 22A @ 25°C		43		nC
Q _{gs}	Gate-Source Charge			12		
Q _{gd}	Gate-Drain ("Miller") Charge			24		
t _{d(on)}	Turn-on Delay Time	RESISTIVE SWITCHING V _{GS} = 15V V _{DD} = 250V I _D = 22A @ 25°C R _G = 1.6Ω		8		ns
t _r	Rise Time			6		
t _{d(off)}	Turn-off Delay Time			18		
t _f	Fall Time			2		
E _{on}	Turn-on Switching Energy ⑥	INDUCTIVE SWITCHING @ 25°C V _{DD} = 333V, V _{GS} = 15V I _D = 22A, R _G = 5Ω		167		μJ
E _{off}	Turn-off Switching Energy			86		
E _{on}	Turn-on Switching Energy ⑥	INDUCTIVE SWITCHING @ 125°C V _{DD} = 333V V _{GS} = 15V I _D = 22A, R _G = 5Ω		262		
E _{off}	Turn-off Switching Energy			99		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I _S	Continuous Source Current (Body Diode)			22	Amps
I _{SM}	Pulsed Source Current ① (Body Diode)			88	
V _{SD}	Diode Forward Voltage ② (V _{GS} = 0V, I _S = -I _D 22A)			1.3	Volts
t _{rr}	Reverse Recovery Time (I _S = -I _D 22A, di _S /dt = 100A/μs)		516		ns
Q _{rr}	Reverse Recovery Charge (I _S = -I _D 22A, di _S /dt = 100A/μs)		7		μC
dv/dt	Peak Diode Recovery dv/dt ⑤			8	V/ns

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
R _{θJC}	Junction to Case			0.47	°C/W
R _{θJA}	Junction to Ambient			40	

- ① Repetitive Rating: Pulse width limited by maximum junction temperature
- ② Pulse Test: Pulse width < 380 μs, Duty Cycle < 2%
- ③ See MIL-STD-750 Method 3471
- ④ Starting T_J = +25°C, L = 3.97mH, R_G = 25Ω, Peak I_L = 22A
- ⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. I_S ≤ -I_D22A di_S/dt ≤ 700A/μs V_R ≤ V_{DSS} T_J ≤ 150°C
- ⑥ E_{on} includes diode reverse recovery. See figures 18, 20.

APT Reserves the right to change, without notice, the specifications and information contained herein.

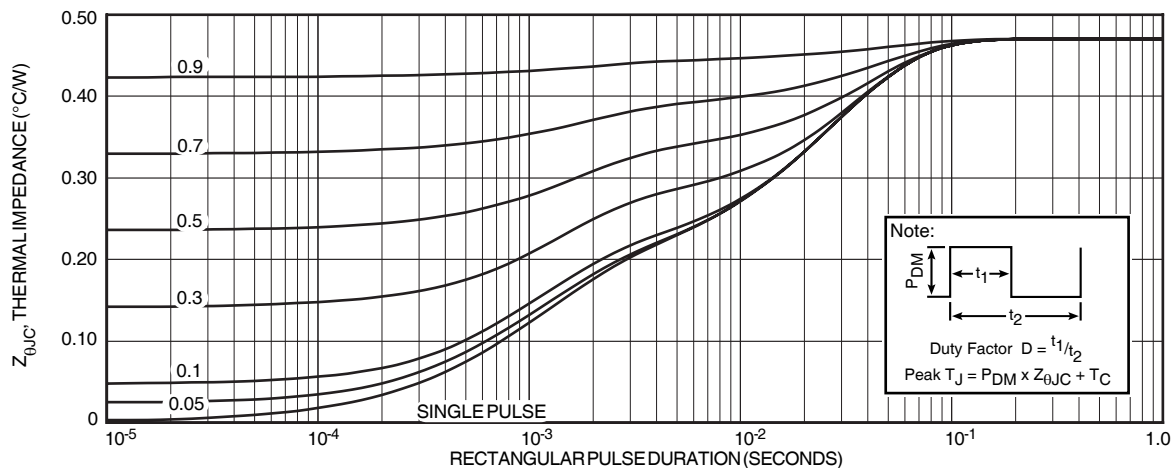


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Typical Performance Curves

APT5024BLL_SLL(G)

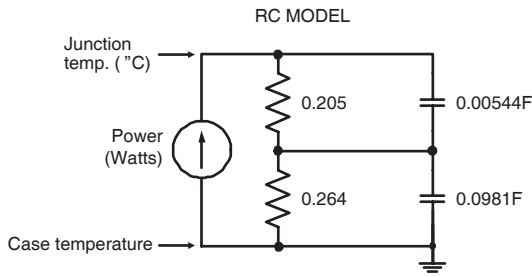


FIGURE 2, TRANSIENT THERMAL IMPEDANCE MODEL

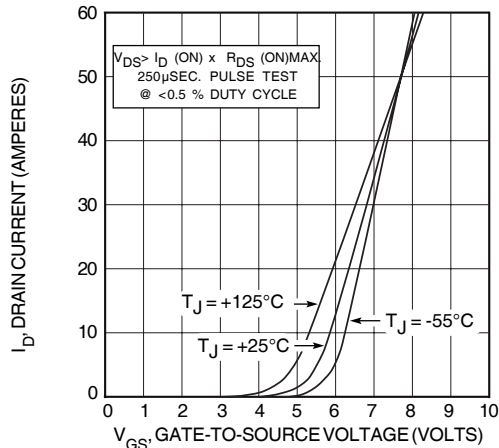


FIGURE 4, TRANSFER CHARACTERISTICS

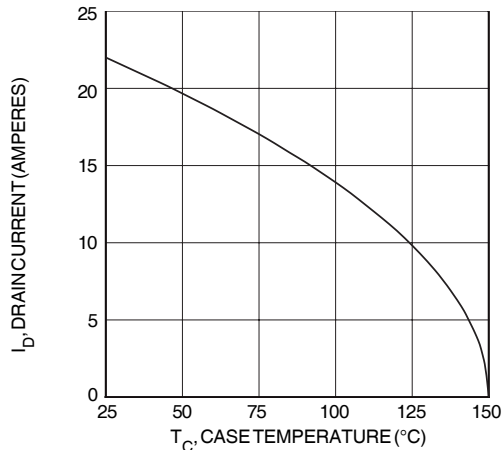


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

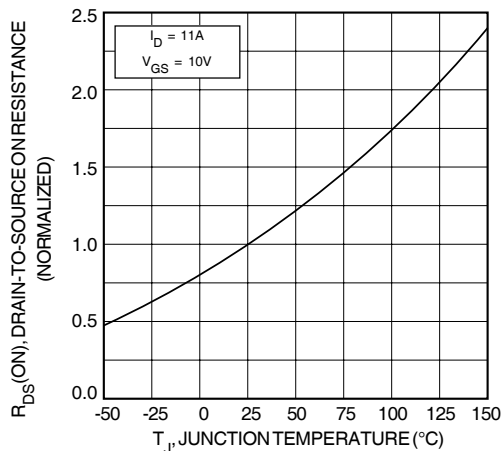


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

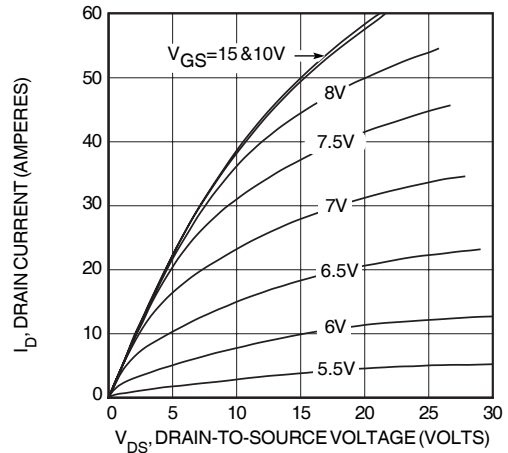


FIGURE 3, LOW VOLTAGE OUTPUT CHARACTERISTICS

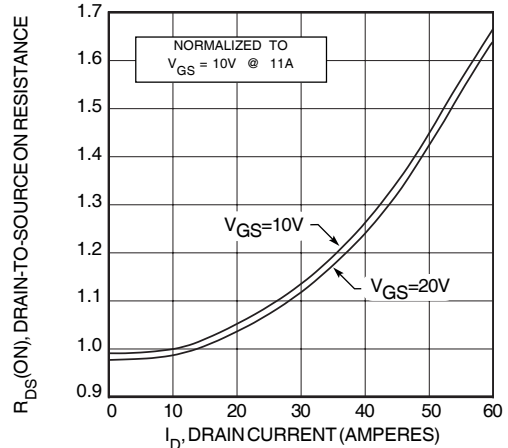


FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT

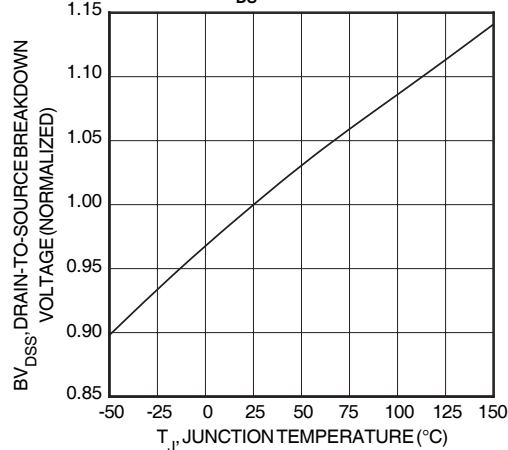


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

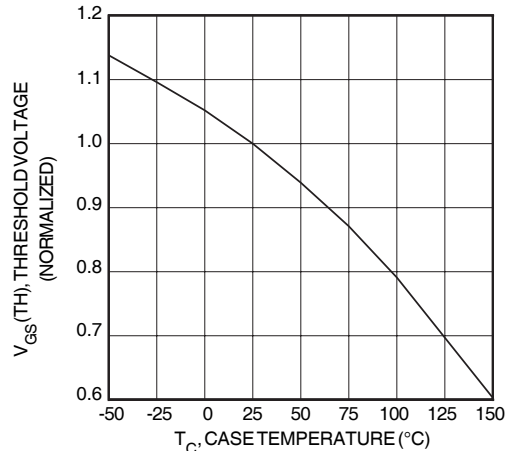


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

Typical Performance Curves

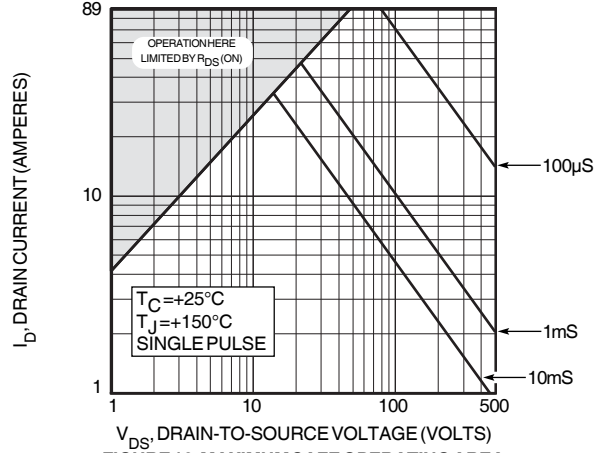


FIGURE 10, MAXIMUM SAFE OPERATING AREA

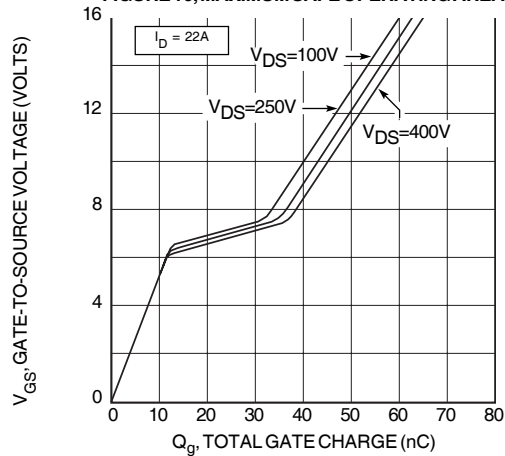


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

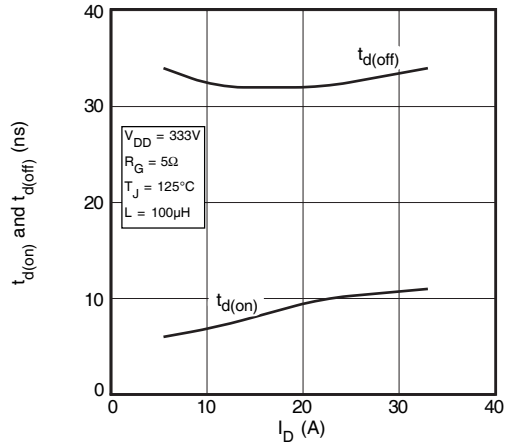


FIGURE 14, DELAY TIMES vs CURRENT

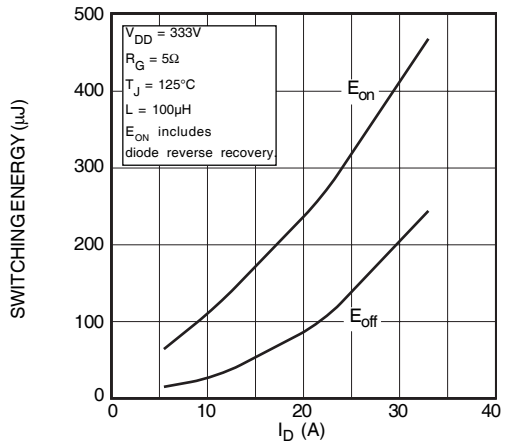


FIGURE 16, SWITCHING ENERGY vs CURRENT

APT5024BLL_SLL(G)

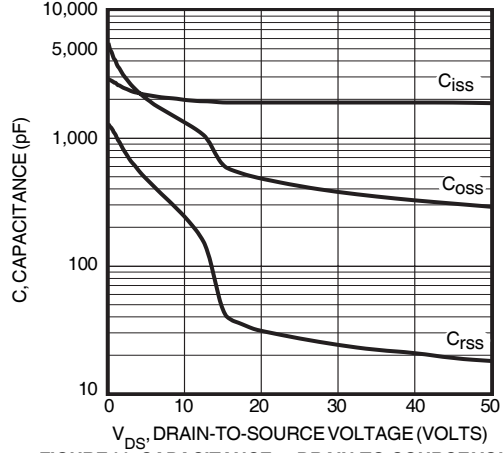


FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

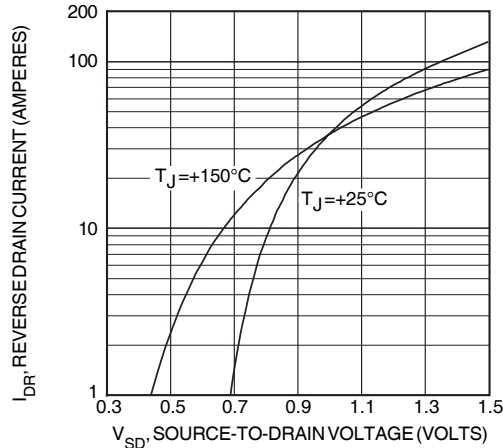


FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

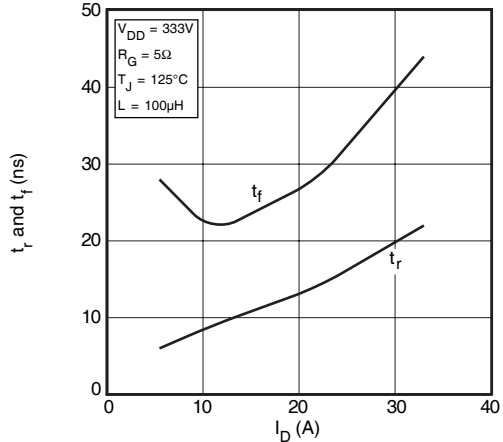


FIGURE 15, RISE AND FALL TIMES vs CURRENT

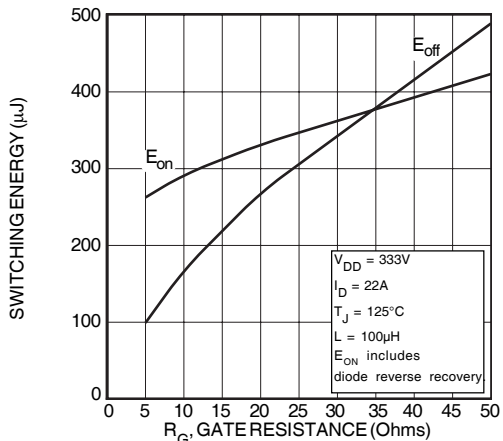


FIGURE 17, SWITCHING ENERGY vs. GATE RESISTANCE

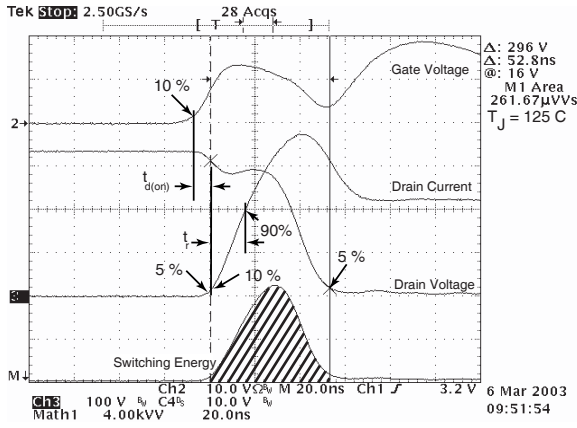


Figure 18, Turn-on Switching Waveforms and Definitions

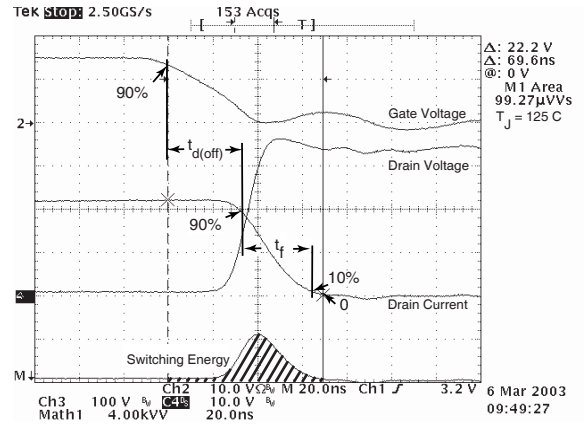


Figure 19, Turn-off Switching Waveforms and Definitions

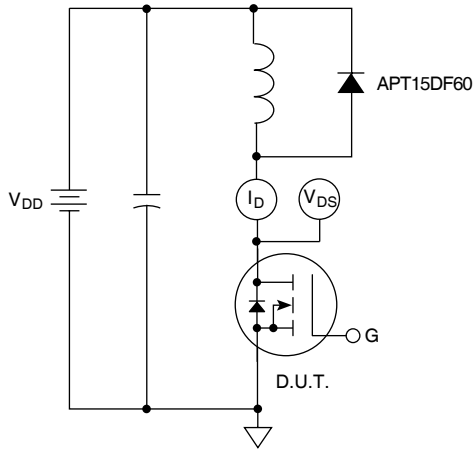
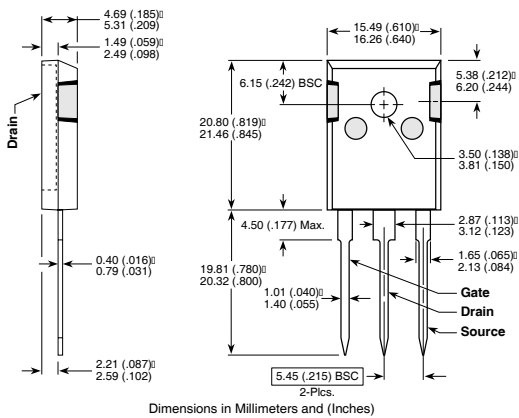


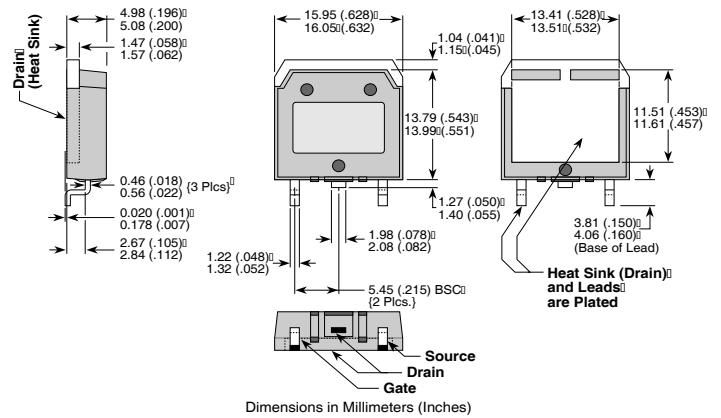
Figure 20, Inductive Switching Test Circuit

TO-247 Package Outline



Dimensions in Millimeters and (Inches)

D³PAK Package Outline



Dimensions in Millimeters (Inches)

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[DMN1006UCA6-7](#) [DMN16M9UCA6-7](#)