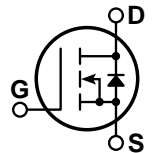
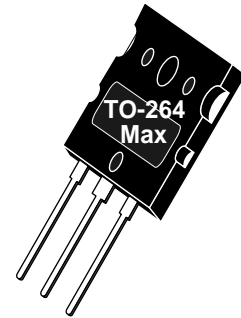


POWER MOS 7® MOSFET

Power MOS 7® is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7® by significantly lowering $R_{DS(ON)}$ and Q_g . Power MOS 7® combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.



- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge, Q_g
- Increased Power Dissipation
- Easier To Drive
- Popular TO-264 MAX Package


MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT50M50L2LL	UNIT
V_{DSS}	Drain-Source Voltage	500	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	89	Amps
I_{DM}	Pulsed Drain Current ^①	356	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	893	Watts
	Linear Derating Factor	7.14	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	89	Amps
E_{AR}	Repetitive Avalanche Energy ^①	50	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	3200	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu\text{A}$)	500			Volts
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, 44.5A$)			0.050	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = 500V, V_{GS} = 0V$)			100	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 400V, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			500	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 5mA$)	3		5	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

DYNAMIC CHARACTERISTICS

APT50M50L2LL

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C _{iss}	Input Capacitance	V _{GS} = 0V V _{DS} = 25V f = 1 MHz		10550		pF
C _{oss}	Output Capacitance			2060		
C _{rss}	Reverse Transfer Capacitance			105		
Q _g	Total Gate Charge ③	V _{GS} = 10V V _{DD} = 250V I _D = 89A @ 25°C		200		nC
Q _{gs}	Gate-Source Charge			50		
Q _{gd}	Gate-Drain ("Miller") Charge			105		
t _{d(on)}	Turn-on Delay Time	RESISTIVE SWITCHING V _{GS} = 15V V _{DD} = 250V I _D = 89A @ 25°C R _G = 0.6Ω		24		ns
t _r	Rise Time			22		
t _{d(off)}	Turn-off Delay Time			56		
t _f	Fall Time			8		
E _{on}	Turn-on Switching Energy ⑥	INDUCTIVE SWITCHING @ 25°C V _{DD} = 333V, V _{GS} = 15V I _D = 89A, R _G = 3Ω		1490		μJ
E _{off}	Turn-off Switching Energy			1650		
E _{on}	Turn-on Switching Energy ⑥	INDUCTIVE SWITCHING @ 125°C V _{DD} = 333V, V _{GS} = 15V I _D = 89A, R _G = 3Ω		2105		
E _{off}	Turn-off Switching Energy			1835		

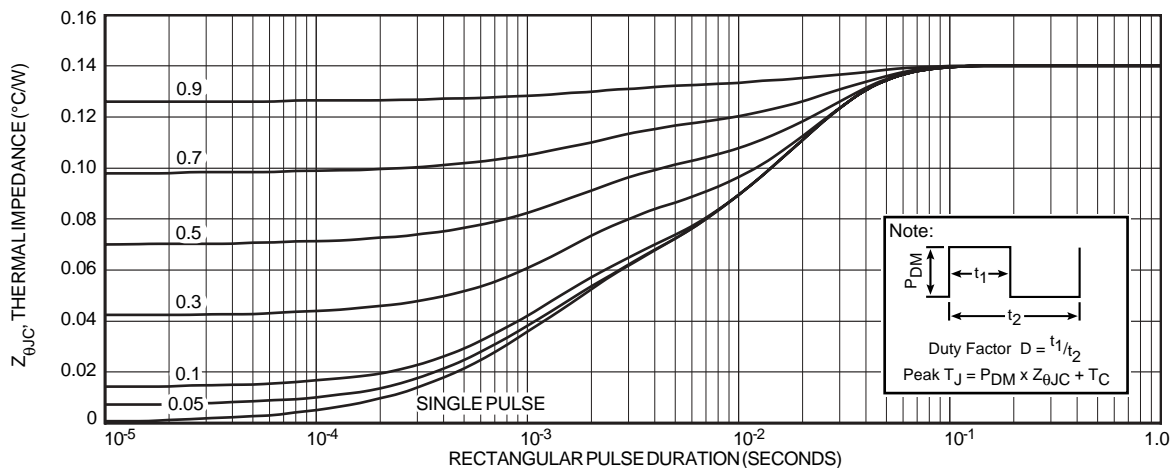
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I _S	Continuous Source Current (Body Diode)			89	Amps
I _{SM}	Pulsed Source Current ① (Body Diode)			356	
V _{SD}	Diode Forward Voltage ② (V _{GS} = 0V, I _S = -89A)			1.3	Volts
t _{rr}	Reverse Recovery Time (I _S = -89A, di _S /dt = 100A/μs)		680		ns
Q _{rr}	Reverse Recovery Charge (I _S = -89A, di _S /dt = 100A/μs)		17.0		μC
dv/dt	Peak Diode Recovery dv/dt ⑤			8	V/ns

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
R _{θJC}	Junction to Case			0.14	°C/W
R _{θJA}	Junction to Ambient			40	

- ① Repetitive Rating: Pulse width limited by maximum junction temperature
 - ② Pulse Test: Pulse width < 380 μs, Duty Cycle < 2%
 - ③ See MIL-STD-750 Method 3471
 - ④ Starting T_J = +25°C, L = 0.81mH, R_G = 25Ω, Peak I_L = 89A
 - ⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. I_S ≤ -89A di/dt ≤ 700A/μs V_R ≤ 500V T_J ≤ 150°C
 - ⑥ E_{on} includes diode reverse recovery. See figures 18, 20.
- APT Reserves the right to change, without notice, the specifications and information contained herein.**



Typical Performance Curves

APT50M50L2LL

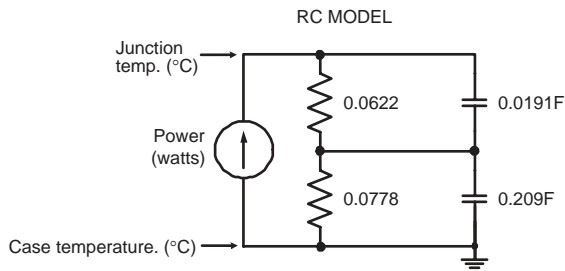


FIGURE 2, TRANSIENT THERMAL IMPEDANCE MODEL

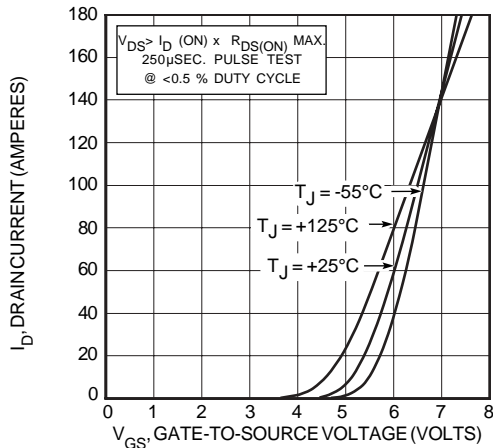


FIGURE 4, TRANSFER CHARACTERISTICS

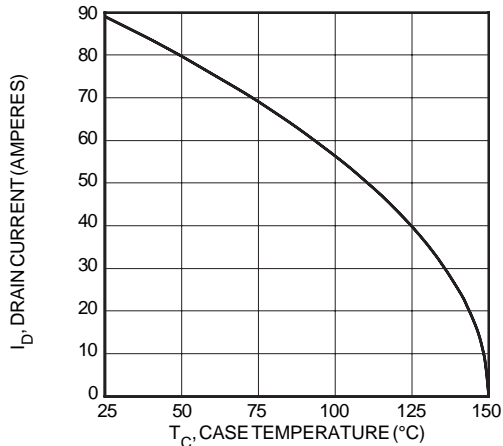


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

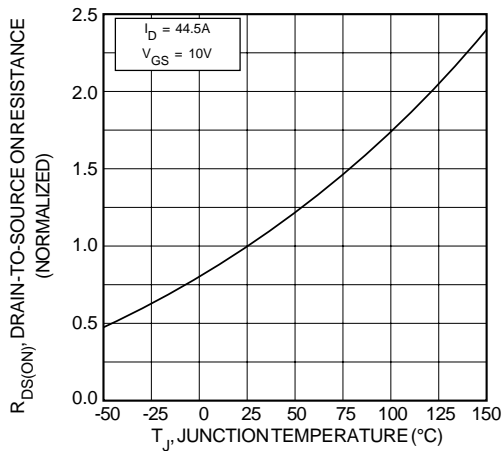


FIGURE 8, $R_{DS(ON)}$ vs. TEMPERATURE

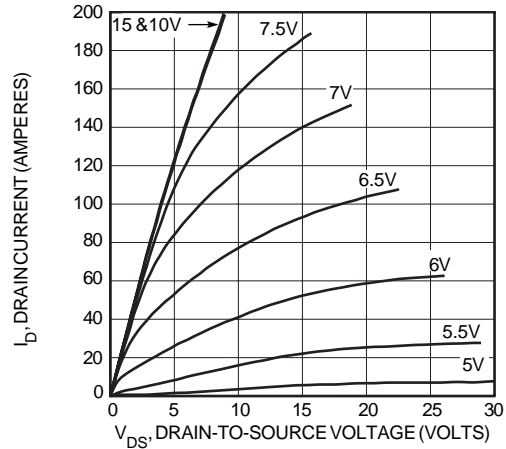


FIGURE 3, LOW VOLTAGE OUTPUT CHARACTERISTICS

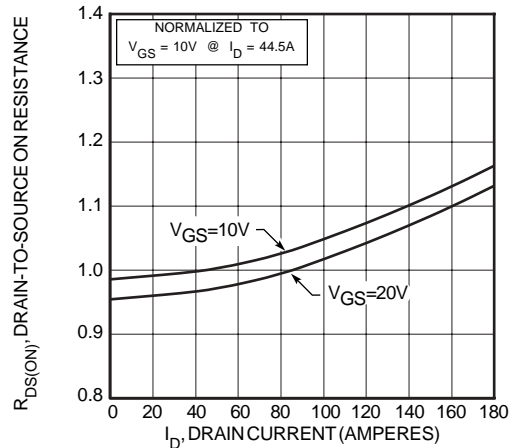


FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT

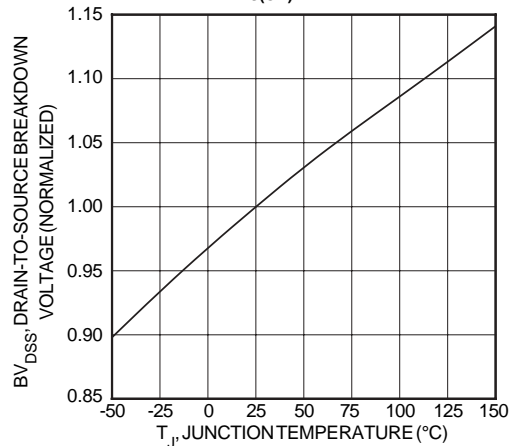


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

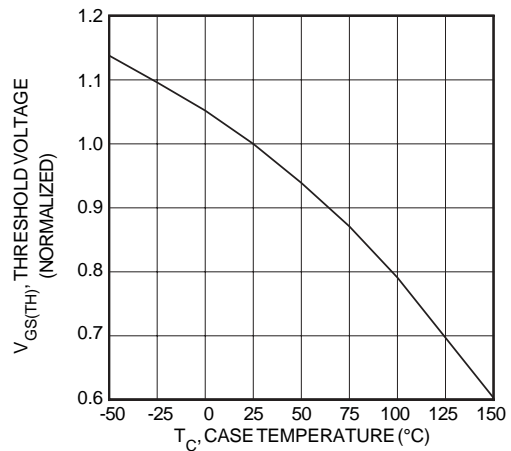


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

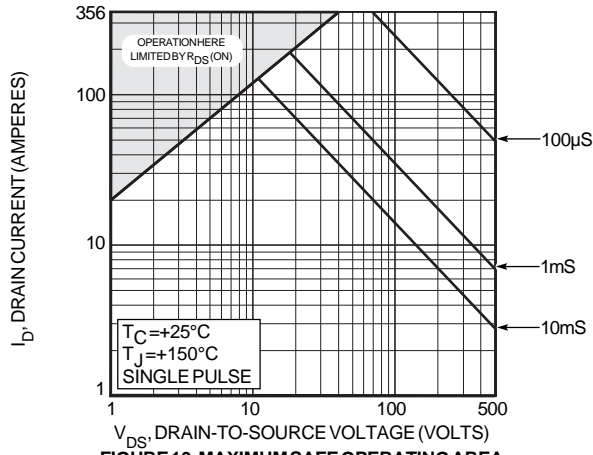


FIGURE 10, MAXIMUM SAFE OPERATING AREA

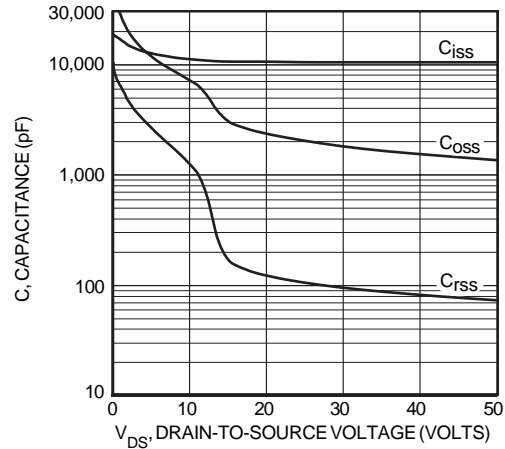


FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

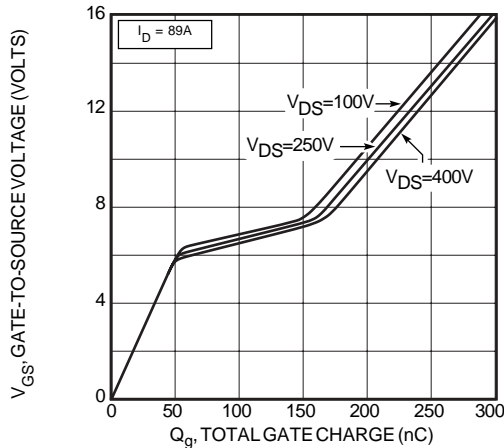


FIGURE 12, GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

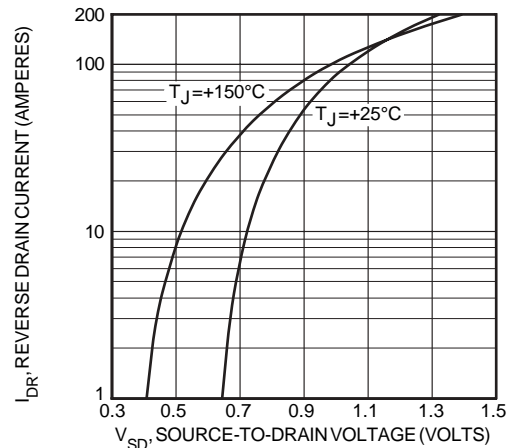


FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

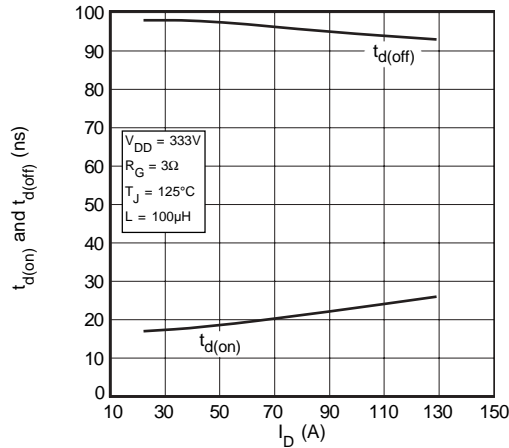


FIGURE 14, DELAY TIMES vs CURRENT

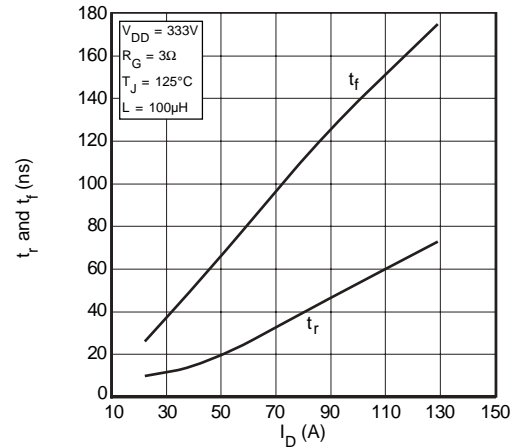


FIGURE 15, RISE AND FALL TIMES vs CURRENT

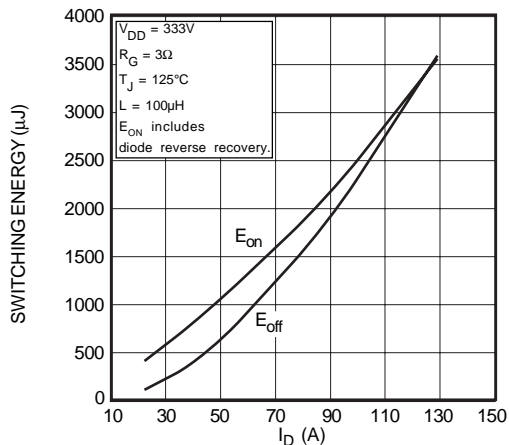


FIGURE 16, SWITCHING ENERGY vs CURRENT

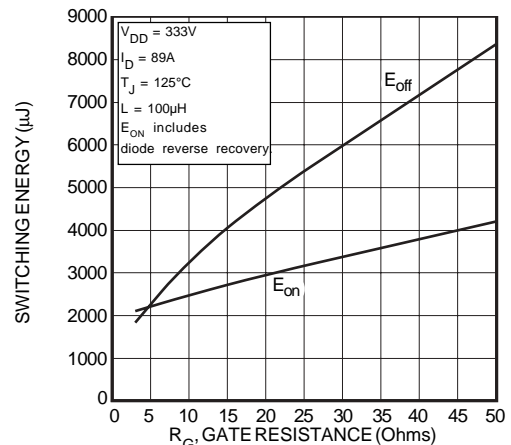


FIGURE 17, SWITCHING ENERGY vs. GATE RESISTANCE

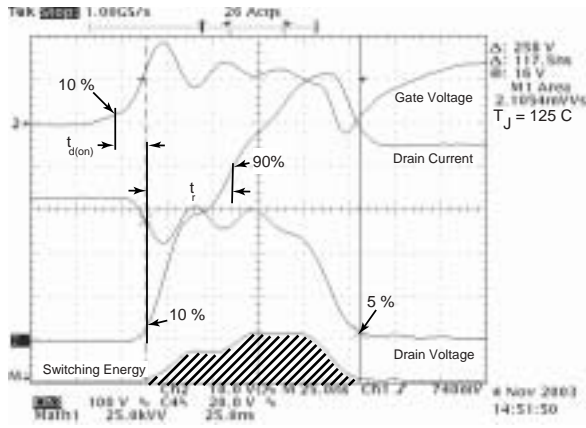


Figure 18, Turn-on Switching Waveforms and Definitions

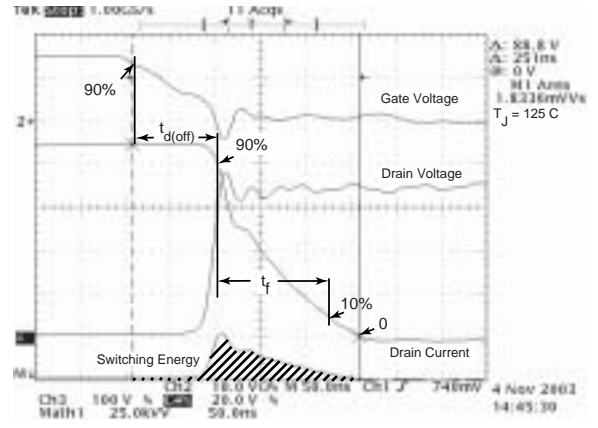


Figure 19, Turn-off Switching Waveforms and Definitions

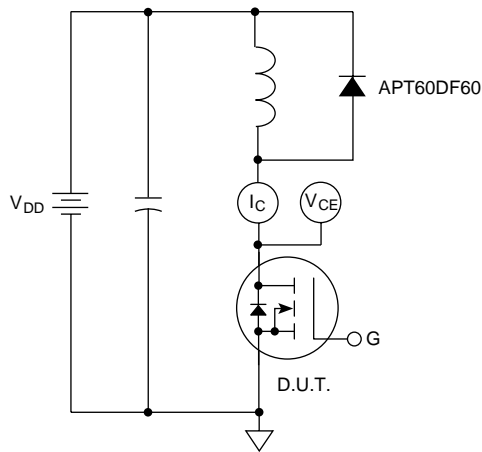
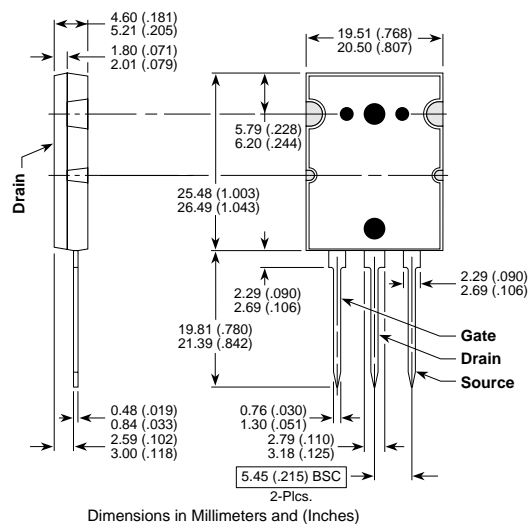


Figure 20, Inductive Switching Test Circuit

TO-264 MAX™(L2) Package Outline



Dimensions in Millimeters and (Inches)

APT's products are covered by one or more of U.S. patents 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522 5,262,336 6,503,786 5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058 and foreign patents. US and Foreign patents pending. All Rights Reserved.

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[NTE6400A](#) [NTE2910](#) [NTE2916](#) [NTE2956](#) [NTE2911](#) [DMN2080UCB4-7](#) [TK10A80W,S4X\(S](#) [SSM6P69NU,LF](#) [DMP22D4UFO-7B](#)
[DMN1006UCA6-7](#) [DMN16M9UCA6-7](#)