AT34C04

I²C-Compatible 4-Kbit Serial EEPROM with Reversible Software Write Protection

DATASHEET

Features

- Single 1.7V to 3.6V V_{CC} Supply
- JEDEC JC42.4 (EE1004-v) Serial Presence Detect (SPD) Compliant
- 2-wire Serial Interface: I²C Fast-Mode Plus (FM+)™ Compatible
  - 100kHz, 400kHz, and 1MHz Compatibility
  - Bus Timeout Supported
- Advanced Software Data Protection Features
  - Individually reversible software write protection on all four 128-byte quadrants
  - Software procedure to verify each quadrant's write protection status
- 16-byte Page Write Mode
  - Partial Page Writes Allowed
- Self-timed Write Cycle (5ms Maximum)
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- High-reliability
  - Endurance: 1,000,000 Write Cycles
  - Data Retention: 100 Years
- Low Operating Current
  - Write ~1.5mA (Typical)
  - Read ~ 0.2mA (Typical)
- Green Packaging Options (Pb/Halide-free/RoHS Compliant)
  - 8-lead JEDEC SOIC, 8-lead TSSOP, and 8-pad UDFN

Description

The Atmel® AT34C04 is a 1.7V rated minimum operating voltage Serial EEPROM device containing 4096-bits of Serially Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 512-bytes of eight bits each. The Serial EEPROM operation is tailored specifically for DRAM memory modules with Serial Presence Detect (SPD) to store a module's vital product data such as the module's size, speed, voltage, data width, and timing parameters.

The AT34C04 is protocol compatible with the legacy JEDEC EE1002 specification (2-Kbit) devices enabling the AT34C04 to be utilized in legacy applications without any software changes. The device is designed to respond to specific software commands that allow users to identify and set which half of the memory the internal address counter is located. This special page addressing method to select the upper or lower half of the Serial EEPROM is what facilitates legacy compatibility. However, there is one exception to the legacy compatibility as the AT34C04 does not support the Permanent Write Protection feature.

Additionally, the AT34C04 incorporates a Reversible Software Write Protection (RSWP) feature enabling the capability to selectively write protect any or all of the four 128-byte quadrants. Once the RSWP is set, it can only be reversed by sending a specific software command sequence.

The AT34C04 supports the industry standard 2-wire I²C Fast-Mode Plus (FM+) serial interface allowing device communication to operate at up to 1MHz. A bus timeout feature is supported to help prevent system lock-ups. The AT34C04 is available in space saving SOIC, TSSOP, and UDFN packages.

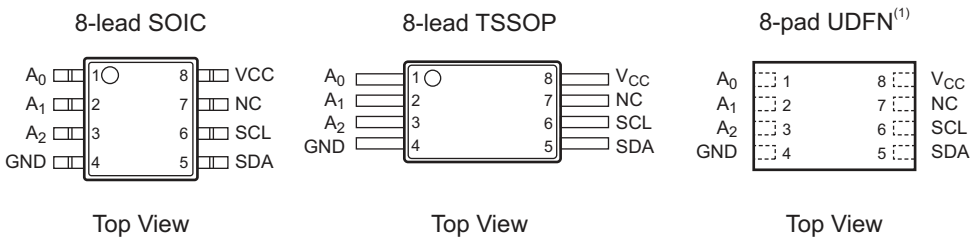
Table of Contents

1. Pin Descriptions and Pinouts

Table 1-1. Pin Descriptions

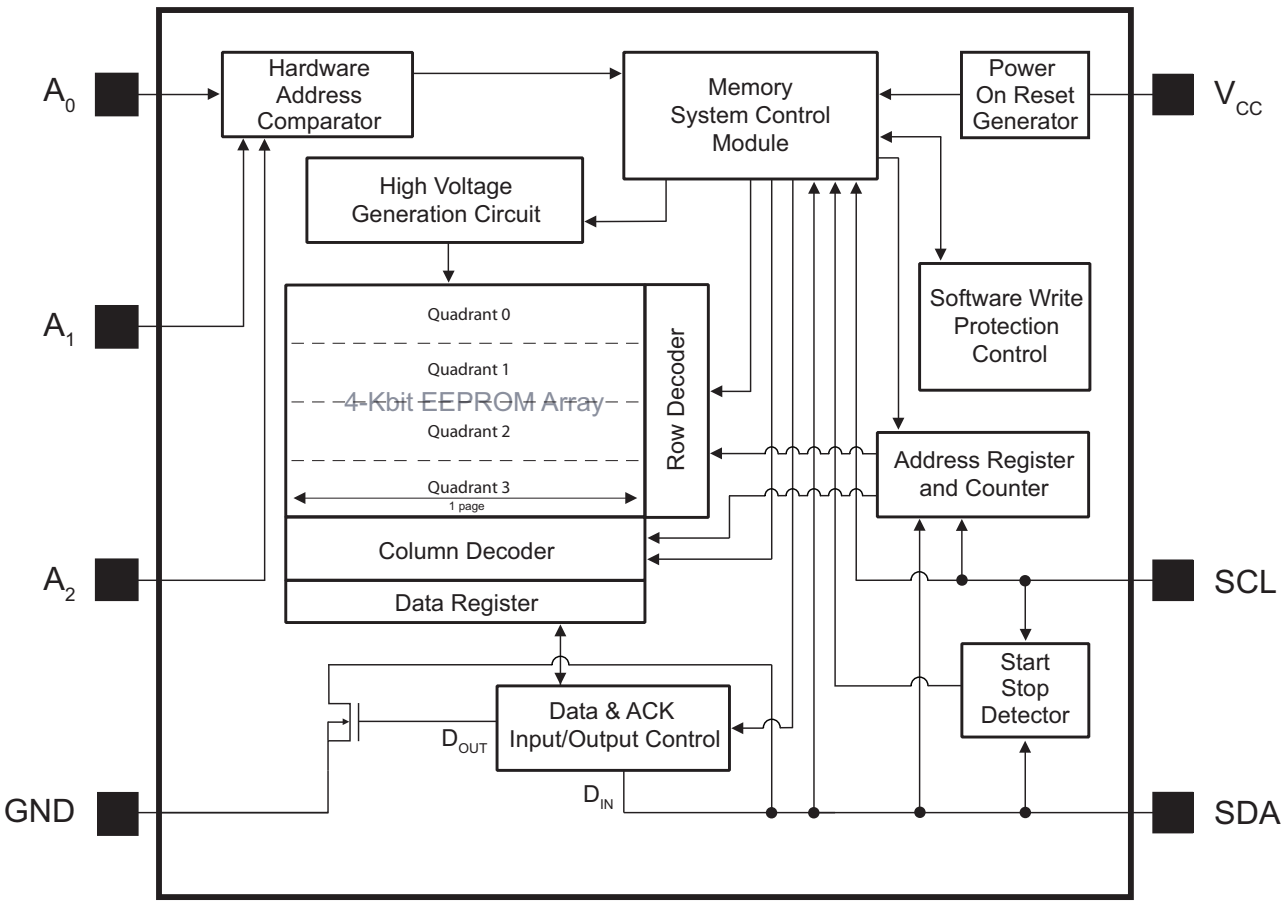
Symbol	Name and Function	Asserted State	Type
NC	**No Connect:** The NC pin is not bonded to a die pad. This pin can be connected to GND or left floating.	—	—
A_0, A_1, A_2	**Device Address Inputs:** The A_0, A_1, and A_2 pins are used to select the device address and corresponds to the three Least-Significant Bits (LSBs) of the I^2C FM+ seven bit slave address. These pins can be directly connected to V_{CC} or GND in any combination, allowing up to eight devices on the same bus. The A_0 pin is also an overvoltage tolerant pin, allowing up to 10V to support the Reversible Software Write Protection (RSWP) feature (see Section 7.).	—	Input
GND	**Ground:** The ground reference for the power supply. GND should be connected to the system ground.	—	Power
SDA	**Serial Data:** The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device. The SDA pin must be pulled-high using an external pull-up resistor (not to exceed 8KΩ in value) and may be wire-ORed with any number of other open-drain or open-collector pins from other devices on the same bus.	—	Input/ Output
SCL	**Serial Clock:** The SCL pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is always clocked out on the falling edge of SCL. The SCL pin must either be forced high when the serial bus is idle or pulled-high using an external pull-up resistor.	—	Input
V_{CC}	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	—	Power

Figure 1-1. Pinouts



Note: 1. The metal pad on the bottom of the UDFN package is not internally connected to a voltage potential. This pad can be a “no connect” or connected to GND.

2. Block Diagram



3. Device Communication

The AT34C04 operates as a slave device and utilizes a simple 2-wire digital serial interface, compatible with the I^2C Fast-Mode Plus (I^2C FM+) protocol, to communicate with a host controller, commonly referred to as the bus Master. The Master initiates and controls all Read and Write operations to the slave devices on the serial bus, and both the Master and the slave devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: the Serial Clock (SCL) and the Serial Data (SDA). The SCL pin is used to receive the clock signal from the Master, while the bidirectional SDA pin is used to receive command and data information from the Master, as well as, to send data back to the Master. Data is always latched into the AT34C04 on the rising edge of SCL and is always output from the device on the falling edge of SCL. Both the SCL and SDA pin incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

All command and data information is transferred with the Most-Significant Bit (MSB) first. During the bus communication, one data bit is transmitted every clock cycle, and after eight bits (one byte) of data has been transferred, the receiving device must respond with either an acknowledge (ACK) or a no-acknowledge (NACK) response bit during a ninth clock cycle (ACK/NACK clock cycle) generated by the Master. Therefore, nine clock cycles are required for every one byte of data transferred. There are no unused clock cycles during any Read or Write operation so there must not be any interruptions or breaks in the data stream during each data byte transfer and ACK or NACK clock cycle.

During data transfers, data on the SDA pin must only change while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. Start and Stop conditions are used to initiate and end all serial bus communication between the Master and the slave devices.The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the Master.

In order for the serial bus to be idle, both the SCL and SDA pins must be in the Logic 1 state at the same time.

3.1 Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is stable in the Logic 1 state. The Master uses a Start condition to initiate any data transfer sequence, therefore the Start condition must precede any command. The AT34C04 will continuously monitor the SDA and SCL pins for a Start condition, and the device will not respond unless one is given. Please refer to Figure 3-1 on page 6 for more details.

3.2 Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in the Logic 1 state. The Master uses the Stop condition to end a data transfer sequence to the AT34C04 which will subsequently return to the idle state. The Master can also utilize a repeated Start condition instead of a Stop condition to end the current data transfer if the Master will perform another operation. Please refer to Figure 3-1 on page 6 for more details.

3.3 Acknowledge (ACK)

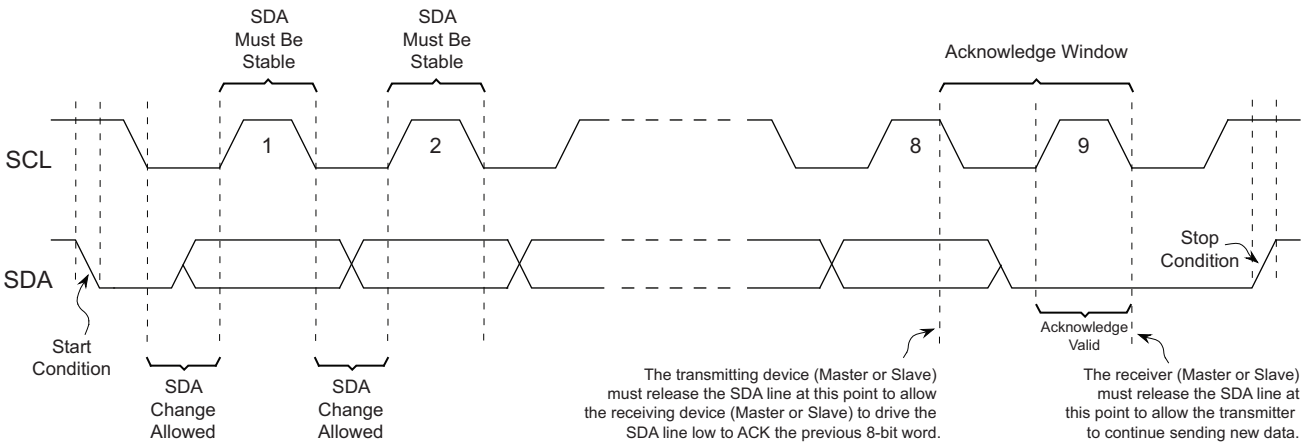
After every byte of data is received, the AT34C04 must acknowledge to the Master that it has successfully received the data byte by responding with an ACK. This is accomplished by the Master first releasing the SDA line and providing the ACK/NACK clock cycle (a ninth clock cycle for every byte). During the ACK/NACK clock cycle, the AT34C04 must output a Logic 0 (ACK) for the entire clock cycle such that the SDA line must be stable in the Logic 0 state during the entire high period of the clock cycle. Please refer to Figure 3-1 on page 6 for more details.

3.4 No-Acknowledge (NACK)

When the AT34C04 is transmitting data to the Master, the Master can indicate that it is done receiving data and wants to end the operation by sending a NACK response to the AT34C04 instead of an ACK response. This is accomplished by the Master outputting a Logic 1 during the ACK/NACK clock cycle, at which point the AT34C04 will release the SDA line so that the Master can then generate a Stop condition.

In addition, the AT34C04 can use a NACK to respond to the Master instead of an ACK for certain invalid operation cases such as an attempt to Write to a read-only register.

Figure 3-1. Start, Stop, and ACK



3.5 Standby Mode

The AT34C04 incorporates a low-power Standby mode which is enabled:

- Upon power-up *or*
- After the receipt of a Stop condition and the completion of any internal operations.

3.6 Device Reset and Initialization

The AT34C04 incorporates an internal Power-On Reset (POR) circuit to help prevent inadvertent operations during power-up and power down cycles. On a cold power-up, the supply voltage must rise monotonically between $V_{POR(max)}$ and $V_{CC(min)}$ without any ring back to ensure a proper power-up (see Figure 3-2). Once the supply voltage has passed the $V_{POR(min)}$ threshold, the device internal reset process is initiated. Completion of the internal reset process occurs within the t_{INIT} time listed in Table 3-1.

Before selecting the device and issuing protocol, a valid and stable supply voltage must be applied and no protocol should be issued to the device for the time specified by the t_{INIT} parameter. The supply voltage must remain stable and valid until the end of the protocol transmission, and for a Write instruction, until the end of the internal write cycle.

Figure 3-2. Power-up Timing

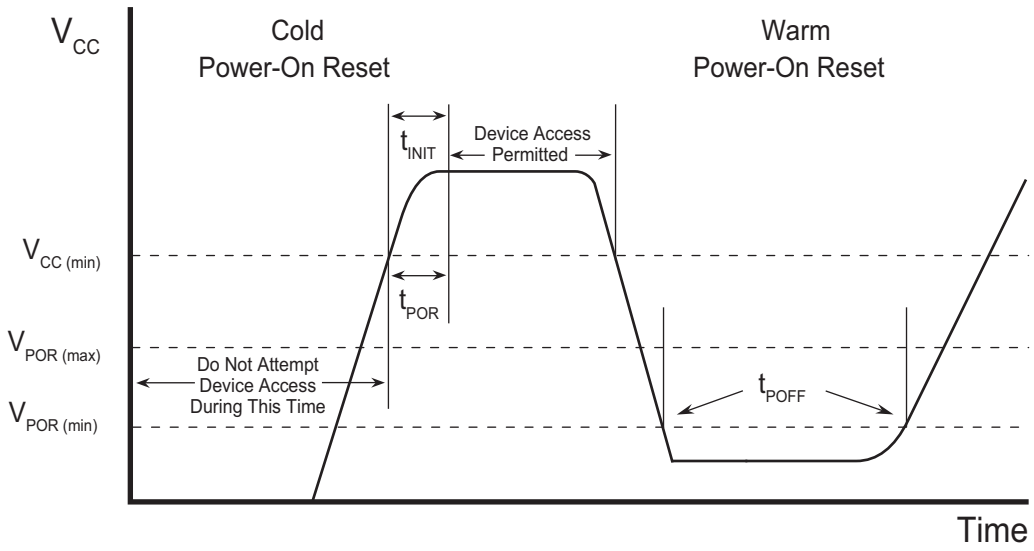


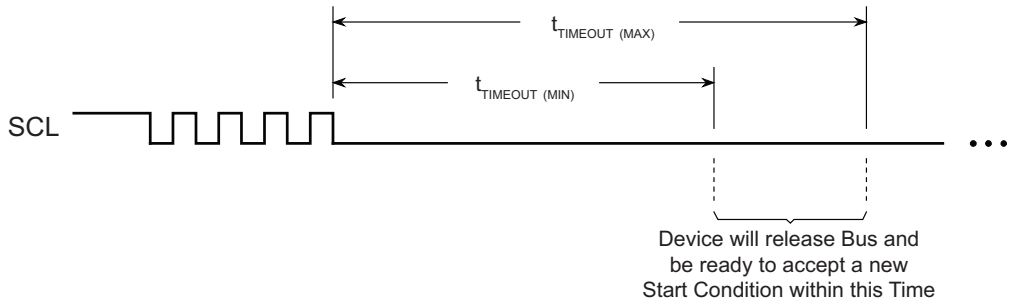
Table 3-1. Power-up Conditions

Symbol	Parameter	Min	Max	Units
t_{POR}	Power-On Reset Time		10.0	ms
V_{POR}	Power-On Reset Voltage Range	1.0	1.6	V
t_{INIT}	Time from Power-On to First Command	10.0		ms
t_{POFF}	Warm Power Cycle Off Time	1.0		ms

3.7 Timeout Function

The AT34C04 supports the industry standard bus Timeout feature to help prevent potential system bus hang-ups. The device resets its serial interface and will stop driving the bus (will let SDA float high) if the SCL pin is held low for more than the minimum Timeout (t_{OUT}) specification. The AT34C04 will be ready to accept a new Start condition before the maximum t_{OUT} has elapsed (see Figure 3-3). This feature does require a minimum SCL clock speed of 10kHz to avoid any timeout issues.

Figure 3-3. Timeout

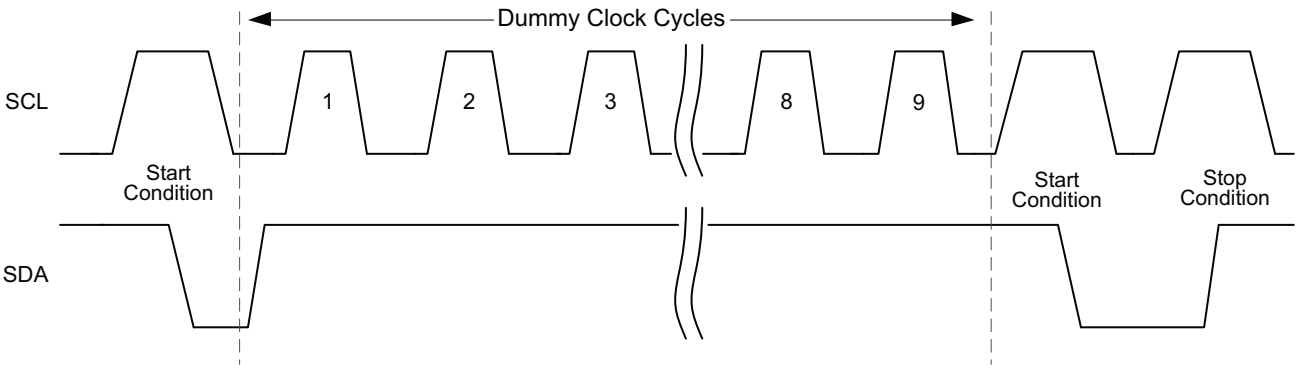


3.8 2-wire Software Reset

After an interruption in protocol, power loss, or system reset, any 2-wire part can be reset by following these steps:

1. Create a Start condition.
2. Clock nine cycles.
3. Create another Start condition followed by Stop condition as shown in Figure 3-4.

Figure 3-4. 2-wire Software Reset



4. Device Addressing

The AT34C04 requires a 7-bit device address and a Read/Write select bit following a Start condition from the Master to initiate communication with the Serial EEPROM. The device address byte is comprised of a 4-bit device type identifier followed by three device address bits (A2, A1, and A0) and a R/$\overline{W}$ bit and is clocked by the Master on the SDA pin with the most significant bit first (see Table 4-1).

The AT34C04 will respond to two unique device type identifiers. The device type identifier of `'1010'(Ah)` is necessary to select the device for reading or writing. The device type identifier of `'0110'`(6h) has multiple purposes. First, it is used to access the page address function which determines what the internal address counter is set to. For more information on accessing the page address function, please refer to Section 6.1.1. The device type identifier of `'0110'`(6h) is also used to access the software write protection feature of the device. Information on the software write protection functionality can be found in Section 7.

Table 4-1. AT34C04 Device Address Byte

Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Device Type Identifier				Device Address			Read/Write
EEPROM Read/Write	1	0	1	0	A2	A1	A0	R/$\overline{W}$
Write Protection and Page Address Functions	0	1	1	0	A2	A1	A0	R/$\overline{W}$

The software device address bits (A2, A1, and A0) must match their corresponding hard-wired device address inputs (A_2, A_1 and A_0) allowing up to eight devices on the bus at the same time (see Table 4-2). The eighth bit of the address byte is the R/$\overline{W}$ operation selection bit. A read operation is selected if this bit is a Logic 1, and a Write operation is selected if this bit is a Logic 0. Upon a compare of the device address byte, the AT34C04 will output an ACK during the ninth clock cycle; if a compare is not true, the device will output a NACK during the ninth clock cycle and return the device to the low-power Standby Mode.

Table 4-2. Device Address Combinations

Software Device Address Bits	Hard-wired Device Address Inputs		
A2, A1, A0	A_2	A_1	A_0
0 0 0	GND	GND	GND
0 0 1	GND	GND	V_{CC}
0 1 0	GND	V_{CC}	GND
0 1 1	GND	V_{CC}	V_{CC}
1 0 0	V_{CC}	GND	GND
1 0 1	V_{CC}	GND	V_{CC}
1 1 0	V_{CC}	V_{CC}	GND
1 1 1	V_{CC}	V_{CC}	V_{CC}

5. Electrical Specifications

5.1 Absolute Maximum Ratings*

Temperature under Bias	-40°C to +125°C
Storage Temperature	-65°C to +150°C
Supply voltage with respect to ground	-0.5V to +4.3V
All other input voltages with respect to ground	-0.5V to V_{CC} + 0.5V
All input voltages with respect to ground	-0.5V to V_{CC} + 0.5V

*Notice: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these ratings or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Voltage extremes referenced in the "Absolute Maximum Ratings" are intended to accommodate short duration undershoot/overshoot conditions and does not imply or guarantee functional device operation at these levels for any extended period of time.

5.2 DC Characteristics

Table 5-1. DC Characteristics

Applicable over recommended operating range: T_A = –20°C to +125°C, V_{CC} = 1.7V to 3.6V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC}	Supply Voltage			1.7		3.6	V
I_{CC1}	Supply Current	V_{CC} = 3.6V	Read at 100kHz		0.4	1.0	mA
I_{CC2}	Supply Current	V_{CC} = 3.6V	Write at 100kHz		1.5	3.0	mA
I_{SB}	Standby Current	V_{CC} = 1.7V	V_{IN} = V_{CC} or V_{SS}		1.6	3.0	µA
		V_{CC} = 3.6V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			0.1	2.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}			0.1	2.0	µA
V_{IL}	Input Low Level(1)			-0.5		0.3 * V_{CC}	V
V_{IH}	Input High Level(1)			0.7 * V_{CC}		V_{CC} + 0.5	V
V_{OL1}	Low-Level Output Voltage Open-Drain	V_{CC} > 2V	I_{OL} = 3mA			0.4	V
V_{OL2}		V_{CC} ≤ 2V	I_{OL} = 2mA			0.2 * V_{CC}	V
I_{OL}	Low-Level Output Current	V_{OL} = 0.4V	Freq ≤ 400kHz	3.0			mA
		V_{OL} = 0.6V	Freq ≤ 400kHz	6.0			mA
		V_{OL} = 0.4V	Freq > 400kHz	20.0			mA
V_{HV}	A_0 Pin High Voltage	V_{HV} - V_{CC} ≥ 4.8V		7		10	V
V_{HYST1}	Input Hysteresis (SDA, SCL)	V_{CC} < 2V		0.10 * V_{CC}			V
V_{HYST2}	Input Hysteresis (SDA, SCL)	V_{CC} ≥ 2V		0.05 * V_{CC}			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

5.3 AC Characteristics

Table 5-2. AC Characteristics

Applicable over recommended operating range: T_A = –20°C to +125°C, V_{CC} = 1.7V to 3.6V, CL = 1 TTL Gate and 100µF (unless otherwise noted).

Symbol	Parameter	V_{CC} < 2.2V		V_{CC} ≥ 2.2V				Units
		100kHz		400kHz		1000kHz		
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL	10[2]	100	10[2]	400	10[2]	1,000	kHz
t_{LOW}	Clock Pulse Width Low	4,700		1,300		500		ns
t_{HIGH}	Clock Pulse Width High	4,000		600		260		ns
t_I	Noise Suppression Time		50		50		50	ns
t_{BUF}	Time the bus must be free before a new transmission can start[1]	4,700		1,300		500		ns
$t_{HD.STA}$	Start Hold Time	4,000		600		260		ns
$t_{SU.STA}$	Start Set-up Time	4,700		600		260		ns
$t_{HD.DI}$	Data In Hold Time	0.0		0.0		0.0		ns
$t_{SU.DAT}$	Data In Set-up Time	250		100		50		ns
t_R	Inputs Rise Time[1]		1,000	20	300		120	ns
t_F	Inputs Fall Time[1]		300	20	300		120	ns
$t_{SU.STO}$	Stop Set-up Time	4,000		600		260		ns
$t_{HD.DAT}$	Data Out Hold Time	200	3,450	200	900	0	350	ns
t_{WR}	Write Cycle Time		5		5		5	ms
t_{OUT}	Timeout Time	25	35	25	35	25	35	ms
Endurance	25°C, Page Mode[1]	1,000,000						Write Cycles

Notes: 1. This parameter is ensured by characterization only.
2. The minimum frequency is specified at 10kHz to avoid activating the timeout feature.

Figure 5-1. Bus Timing

SCL: Serial Clock, SDA: Serial Data I/O

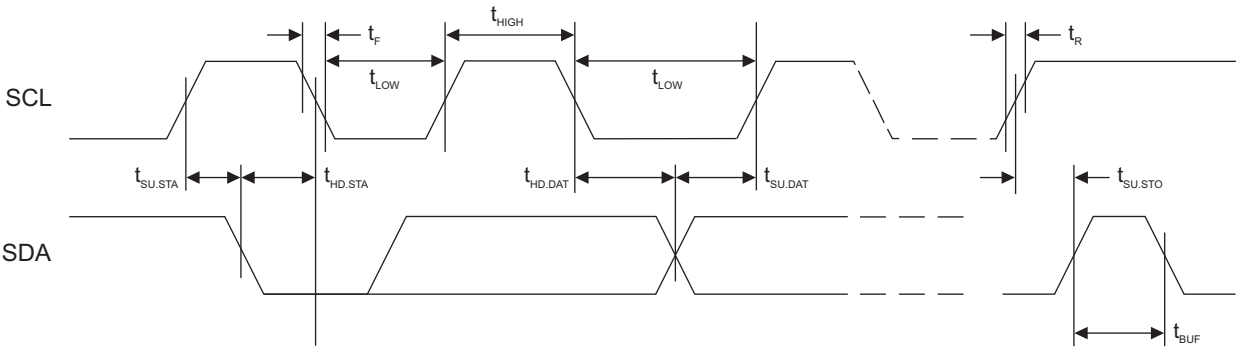


Table 5-3. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1 MHz, V_{CC} = 1.7V - 3.6V.

Symbol	Test condition	Max	Units	Conditions
$C_{I/O}$	Input/output capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is ensured by characterization only.

6. Read and Write Operations

6.1 Memory Organization

To provide the greatest flexibility and backwards compatibility with the previous generations of SPD devices, the AT34C04 memory organization is organized into two independent 2-Kbit memory arrays. Each 2-Kbit (256-byte) section is internally organized into two independent quadrants of 128 bytes with each quadrant comprised of eight pages of 16 bytes. Including both memory sections, there are four 128-byte quadrants totaling 512 bytes. The memory array organization details are shown in Section 2. on page 4 and Table 6-1.

6.1.1 Set Page Address and Read Page Address Commands

The AT34C04 incorporates an innovative memory addressing technique that utilizes a Set Page Address (SPA) and Read Page Address (RPA) commands to select and verify the desired half of the memory enabled to perform Write and Read operations. Due to the requirement for A_0 pin to be driven to V_{HV}, the SPA and the RPA commands are fully supported in a single DIMM (isolated DIMM) end application or a single DIMM programming station only.

Example: If SPA = 0, then the first-half or lower 256 bytes of the Serial EEPROM is selected allowing access to Quadrant 0 and Quadrant 1. Alternately, if SPA = 1, then the second-half or upper 256 bytes of the Serial EEPROM is selected allowing access to Quadrant 2 and Quadrant 3.

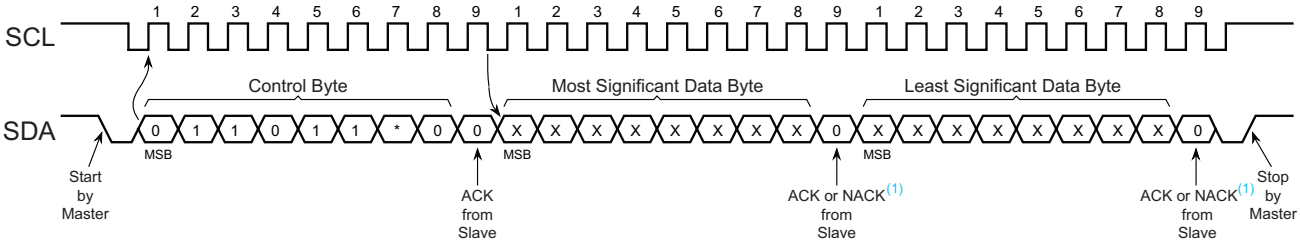
Table 6-1. SPA Setting and Memory Organization

Block	Set Page Address (SPA)	Memory Address Locations
Quadrant 0	0	00h to 7Fh
Quadrant 1		80h to FFh
Quadrant 2	1	00h to 7Fh
Quadrant 3		80h to FFh

Setting the Set Page Address (SPA) value selects the desired half of the EEPROM for performing Write or Read operations. This is done by sending the SPA as seen in Figure 6-1. The SPA command sequence requires the Master to transmit a Start condition followed by sending a control byte of `'011011*0'` where the `'*'` in the bit 7 position will dictate which half of the EEPROM is being addressed. A `'0'` in this position (or 6Ch) is required to set the page address to the first half of the memory and a `'1'` (or 6Eh) is necessary to set the page address to the second half of the memory. After receiving the control byte, the AT34C04 should return an ACK and the Master should follow by sending two data bytes of don't care values.

The JEDEC EE1004v specification allows for either an ACK or NACK response for each of the two data bytes. The AT34C04 responds with an ACK. An alternate part number is available for applications which expect a NACK response. For details, refer to Section 9. The protocol is completed by the Master sending a Stop condition to end the operation.

Figure 6-1. Set Page Address (SPA)



Bit * = 0: Indicates the page address is located in the first half of the memory.

Bit * = 1: Indicates the page address is located in the second half of the memory.

Note: 1. The AT34C04 will ACK the data bytes. An alternate part number is available if a NACK response is needed. For details, refer to Section 9.

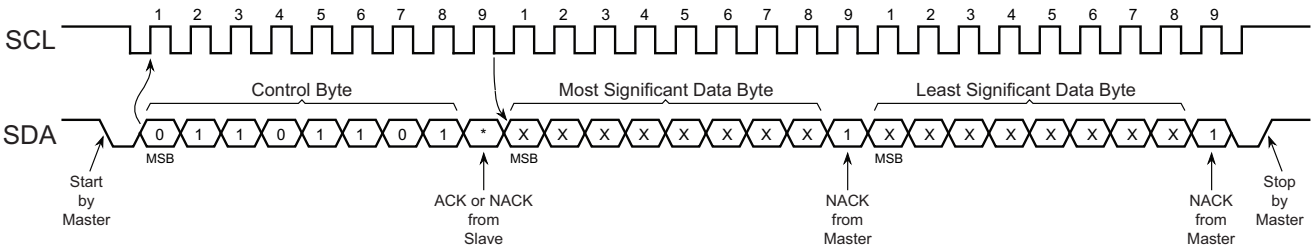
Reading the state of the SPA can be accomplished via the Read Page Address (RPA) command. The Master can issue the RPA command to determine if the AT34C04's internal address counter is located in the first 2-Kbit section or the second 2-Kbit memory section based upon the device's ACK or NACK response to the RPA command.

The RPA command sequence requires the Master to transmit a Start bit followed by a control byte of '01101101' (6Dh). If the device's current address counter (page address) is located in the first half of the memory, the AT34C04 responds with an ACK to the RPA command. Alternatively, a NACK response to the RPA command indicates the page address is located in the second half of the memory (see Figure 6-2). Following the control byte and the device's ACK or NACK response, the AT34C04 should transmit two data bytes of don't care values. The Master should NACK on these two data bytes followed by the Master sending a Stop condition to end the operation.

After power-up, the SPA is set to zero indicating internal address counter is located in the first half of the memory. Performing a software reset (see 2-wire Software Reset on page 8) will also set the SPA to zero.

The AT34C04 incorporates a Reversible Software Write Protect (RSWP) feature that allows the ability to selectively write protect data stored in any or all of the four 128-byte quadrants. See Section 7. "Write Protection" on page 20 for more information on the RSWP feature.

Figure 6-2. Read Page Address (RPA)



Bit * = 0: ACK indicates the device's internal address counter is located in the first half of the memory.

Bit * = 1: NACK indicates the device's internal address counter is located in the second half of the memory.

6.2 Read Operations

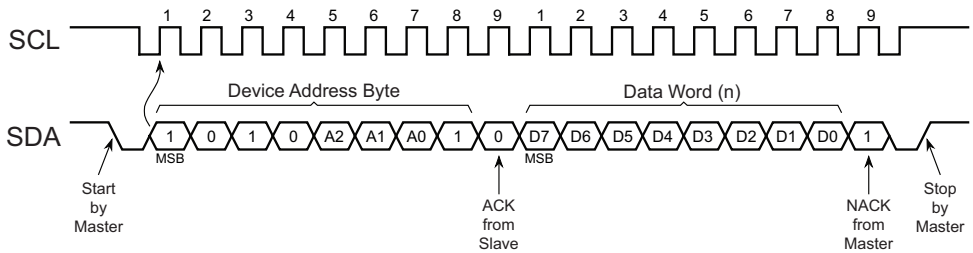
All Read operations are initiated by the Master transmitting a Start bit, a device type identifier of '1010' (Ah), three software address bits (A2, A1, A0) that match their corresponding hard-wired address pins (A_2, A_1, A_0), and the R/$\overline{W}$ select bit with a Logic 1 state. In the following clock cycle, the device should respond with an ACK. The subsequent protocol depends on the type of Read operation desired. There are three Read operations: Current Address Read, Random Address Read, and Sequential Read.

CAUTION: All Read operations should be preceded by the SPA and/or RPA commands to ensure the desired half of the memory is selected. The reason this is important, for example, during a Sequential Read operation on the last byte in the first half of the memory (address FFh) with SPA=0 (indicating first half is selected), the internal address counter will roll-over to address 00h in the first half of memory as opposed to the first byte in the second half of the memory. For more information on the SPA and RPA commands, see Section 6.1.1 on page 13.

6.2.1 Current Address Read

Following a Start condition, the Master only transmits the device address byte with the R/$\overline{W}$ select bit set to a Logic 1 (see Figure 6-3). The AT34C04 should respond with an ACK and then serially transmits the data word addressed by the internal address counter. The internal data word address counter maintains the last address accessed during the last Read or Write operation, incremented by one. This address stays valid between operations as long as power to the device is maintained. The address roll-over during a Read is from the last byte of the last page to the first byte of the first page of the addressed 2-Kbit (depends on the current SPA setting). To end the command, the Master does not respond with an ACK but does generate a following Stop condition.

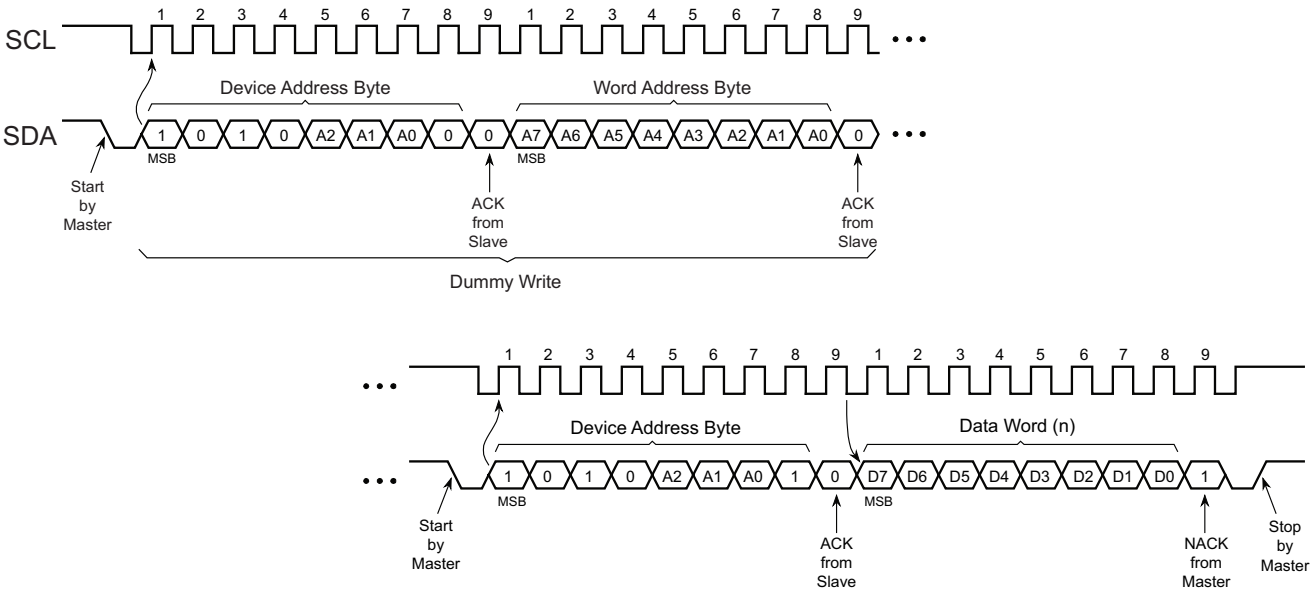
Figure 6-3. Current Address Read



6.2.2 Random Read

A Random Read operation allows the Master to access any memory location in a random manner and requires a dummy write sequence to preload the starting data word address. To perform a Random Read, the device address byte and the word address byte are transmitted to the AT34C04 as part of the dummy write sequence (see Figure 6-4). Once the device address byte and data word address are clocked in and acknowledged by the AT34C04, the Master must generate another Start condition. The Master initiates a Current Address Read by sending another device address byte with the R/$\overline{W}$ select bit to a Logic 1. The AT34C04 acknowledges the device address byte, increments its internal address counter and serially clocks out the first data word. The device will continue to transmit sequential data words as long as the Master continues to ACK each data word. To end the sequence, the Master responds with a NACK and a Stop condition.

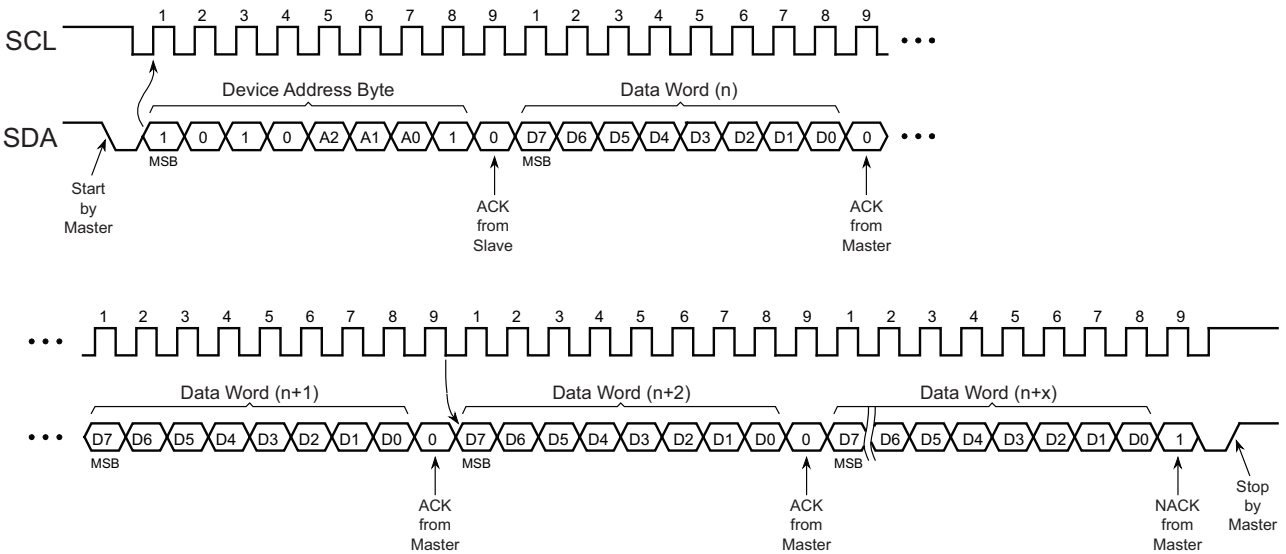
Figure 6-4. Random Read



6.2.3 Sequential Read

A Sequential Read operation is initiated in the same way as a Random Read operation, except after the AT34C04 transmits the first data word, the Master responds with an ACK (instead of a NACK followed by a Stop condition). As long as the AT34C04 receives an ACK, it will continue to increment the data word address and serially clock out the sequential data words (see Figure 6-5). When the internal address counter is at the last byte of the last page, the data word address will roll-over to the beginning of the selected 2-Kbit array (depending on the SPA setting) starting at address zero, and the Sequential Read operation will continue. The Sequential Read operation is terminated when the Master responds with a NACK followed by a Stop condition.

Figure 6-5. Sequential Read



6.3 Write Operations

The AT34C04 supports single Byte Write and Page Write operations up to the maximum page size of 16 bytes in one operation. The only difference between a Byte Write and a Page Write operation is the amount of data bytes sent to the device. Regardless of whether a Byte Write or Page Write operation is performed, the internally self-timed write cycle will take the same amount of time to write the data to the addressed memory location(s).

CAUTION: All Byte Write and Page Write operations should be preceded by the SPA and or RPA commands to ensure the internal address counter is located in the desired half of the memory.

If a Byte Write or Page Write operation is attempted to a protected quadrant, the AT34C04 will respond (ACK or NACK) to the write operation according to Table 6-2.

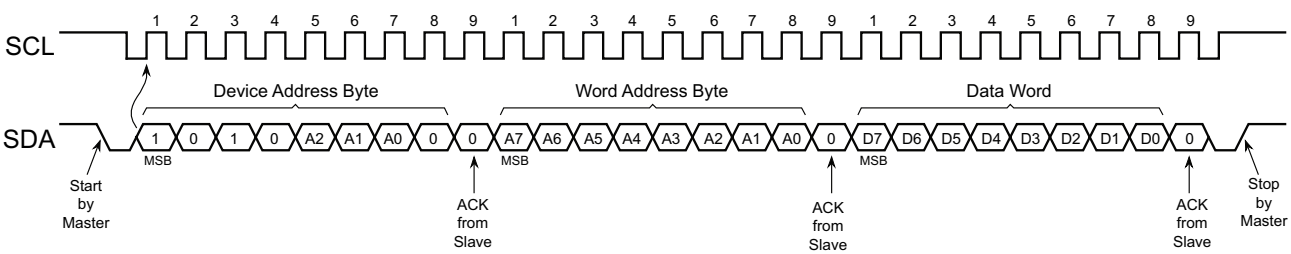
Table 6-2. Acknowledge Status When Writing Data or Defining Write Protection

Quadrant Status	Instruction	ACK	Word Address	ACK	Data Word	ACK	Write Cycle
Write Protected with Set RSWP	Set RSWP	NACK	Don't Care	NACK	Don't Care	NACK	No
	Clear RSWP	ACK	Don't Care	ACK	Don't Care	ACK	Yes
	Byte Write or Page Write to Protected Quadrant	ACK	Word Address	ACK	Data	NACK	No
Not Protected	Set RSWP or Clear RSWP	ACK	Don't Care	ACK	Don't Care	ACK	Yes
	Byte Write or Page Write	ACK	Word Address	ACK	Data	ACK	Yes

6.3.1 Byte Write

Following the Start condition from the Master, the device type identifier (`'1010'`), the device address bits and the R/$\overline{W}$ select bit (set to a Logic 0) are clocked onto the bus by the Master. This indicates to the addressed device that the Master will follow by transmitting a byte with the word address. The AT34C04 will respond with an ACK during the ninth clock cycle. Then the next byte transmitted by the Master is the 8-bit word address of the byte location to be written into the Serial EEPROM. After receiving an ACK from the AT34C04, the Master transmits the data word to be programmed followed by an ACK from the AT34C04. The Master ends the Write sequence with a Stop condition during the 10th clock cycle to initiate the internally self-timed write cycle. A Stop condition issued during any other clock cycle during the Write operation will not trigger the internally self-timed write cycle. Once the write cycle begins, the pre-loaded data word will be programmed in the amount of time not to exceed the t_{WR} specification. The t_{WR} time is defined in more detail in Section 6.3.4 on page 19. During this time, the Master should wait a fixed amount of time set to the t_{WR} specification, or for time sensitive applications, an ACK polling routine can be implemented. All inputs are ignored by the device during the write cycle and the device will not respond until the write cycle is complete (see Figure 6-9). The Serial EEPROM will increment its internal address counter each time a byte is written.

Figure 6-6. Byte Write

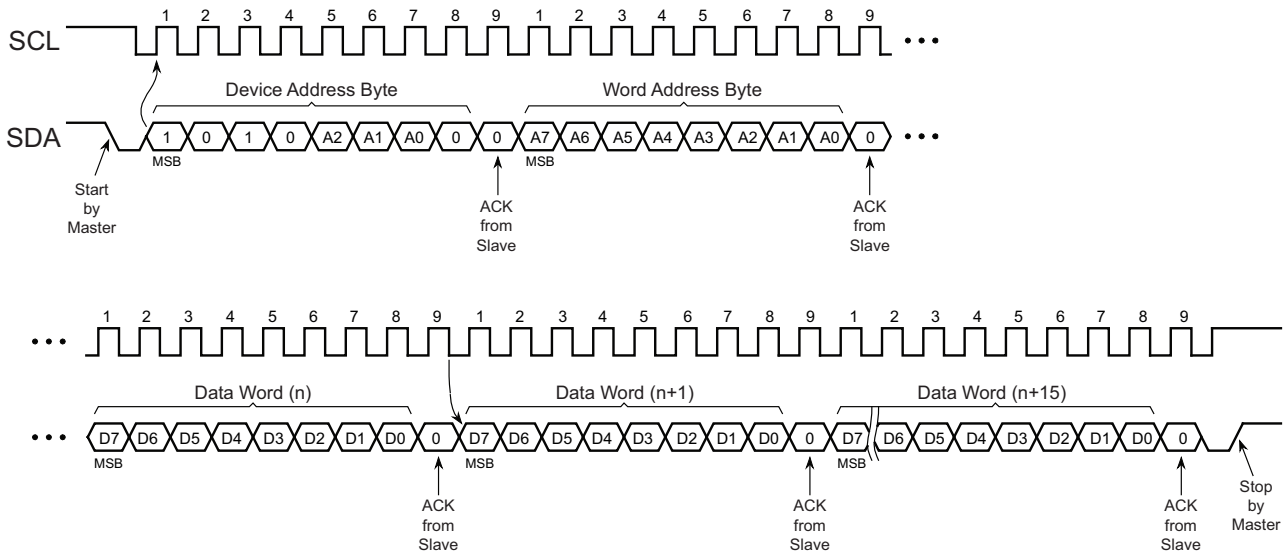


6.3.2 Page Write

The 4-Kbit Serial EEPROM is capable of writing up to 16 data bytes at a time executing the Page Write protocol sequence. A partial or full Page Write operation is initiated the same as a Byte Write operation except that the Master does not send a Stop condition after the first data word is clocked in. Instead, after the device has acknowledged receipt of the first data word, the Master can transmit up to fifteen more data words. The device will respond with an ACK after each data word is received. The Master must terminate the Page Write sequence with a Stop condition during the 10th clock cycle (see Figure 6-7) to start the write cycle. A Stop condition issued at any other clock cycle will not initiate the internally self-timed write cycle and the Write sequence will have to be repeated again.

Once the write cycle begins, the data words should be programmed in the amount of time not exceed the t_{WR} parameter (see Figure 6-9). During this time, the Master should wait a fixed amount of time set to the specified t_{WR} parameter, or for time sensitive applications, an Acknowledge polling routine can be implemented as described in Section 6.3.3. The t_{WR} time is defined in more detail in Section 6.3.4 on page 19. The lower four bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the internally generated word address reaches the page boundary, then the following data word is placed at the beginning of the same page. If more than sixteen data words are transmitted to the device, the data word address will roll-over and the previous data will be overwritten. The address roll-over during a Write sequence is from the last byte of the current page to the first byte of the same page.

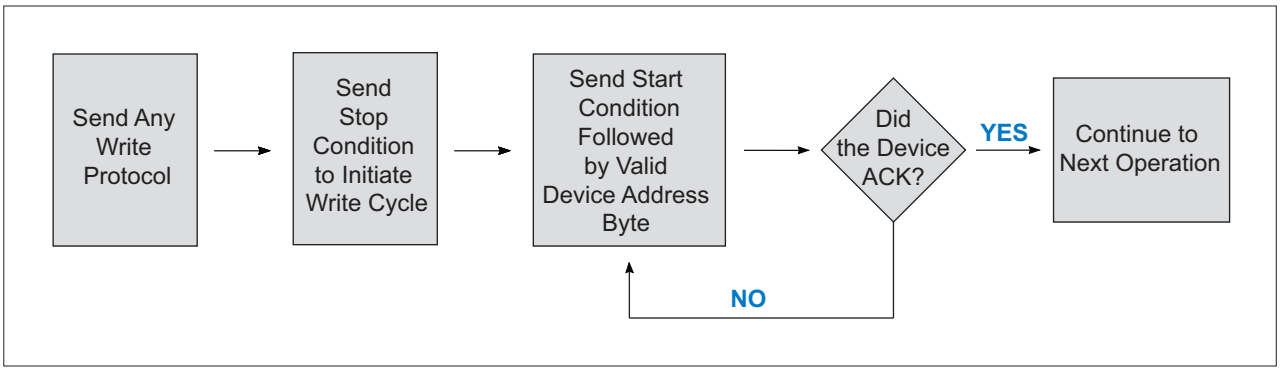
Figure 6-7. Page Write



6.3.3 Acknowledge (ACK) Polling

An ACK polling routine can be implemented to optimize time sensitive applications that would not prefer waiting the fixed maximum write cycle time and would prefer to know immediately when the Serial EEPROM write cycle has completed to start a subsequent operation. Once the internally self timed write cycle has started (the Stop condition during the 10th clock cycle at the end of the Write sequence), the device inputs are disabled and ACK polling can be initiated (see Figure 6-8). An ACK polling routine involves sending a valid Start condition followed by the device address byte. While the write cycle is in progress, the device will not respond with an ACK indicating the device is busy writing data. Once complete, the device will ACK and the next device operation can be started.

Figure 6-8. Acknowledge Polling Flow Chart

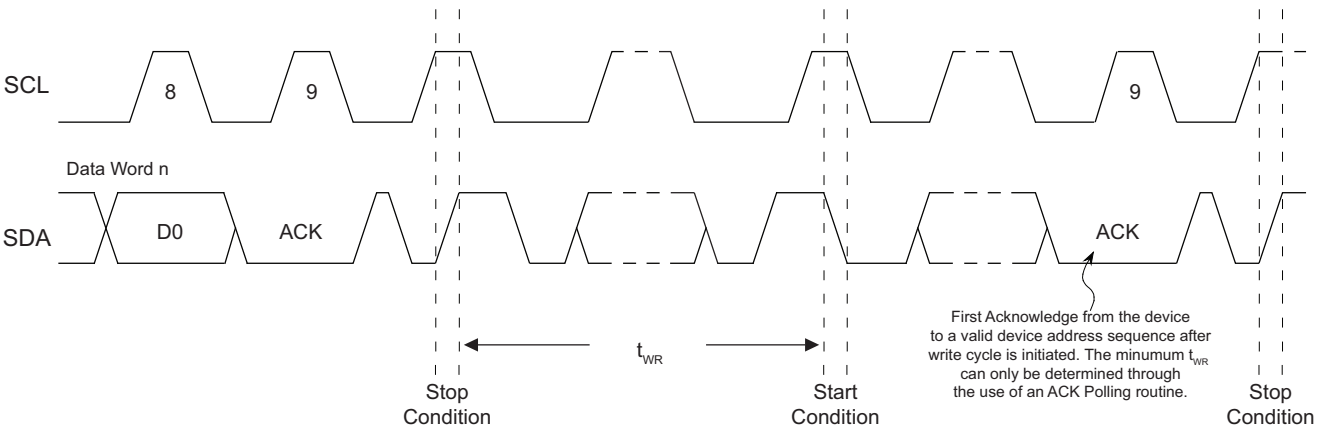


6.3.4 Write Cycle Timing

The length of the self timed write cycle, or t_{WR}, is defined as the amount of time from a valid Stop condition that begins the internal write sequence to the Start condition of the first device address byte sent to the AT34C04 that it subsequently responds to with an ACK. Figure 6-9 has been included to show this measurement.

Figure 6-9. Write Cycle Timing

SCL: Serial Clock, SDA: Serial Data I/O



7. Write Protection

The AT34C04 incorporates a Reversible Software Write Protection (RSWP) feature that allows the ability to selectively write protect data stored in each of the four independent 128-byte EEPROM quadrants. Table 7-1 identifies the memory quadrant identifier with its associated quadrant, SPA and memory address locations.

The AT34C04 has three RSWP software commands:

- Set RSWP command for setting the RSWP.
- Clear RSWP command for resetting all of the quadrants to an unprotected state.
- Read RSWP command for checking the RSWP status.

Table 7-1. Memory Organization

Block	SPA	Address Locations	Memory Quadrant Identifier
Quadrant 0	0	00h to 7Fh	001
Quadrant 1	0	80h to FFh	100
Quadrant 2	1	00h to 7Fh	101
Quadrant 3	1	80h to FFh	000

7.1 Set RSWP

Setting the RSWP is enabled by sending the Set RSWP command, similar to a normal Write command to the device which programs the write protection to the target quadrant. The Set RSWP sequence requires sending a control byte of `'0110MMM0'` (where `'M'` represents the memory quadrant identifier for the target quadrant to be write-protected) with the R/$\overline{W}$ bit set to a Logic 0. In conjunction with sending the protocol, the A_0 pin must be connected to V_{HV} for the duration of the RSWP sequence (see Figure 7-1). The Set RSWP command acts on a single quadrant only as specified in the Set RSWP command and can only be reversed by issuing the Clear RSWP command and will unprotect all quadrants in one operation (see Table 7-2).

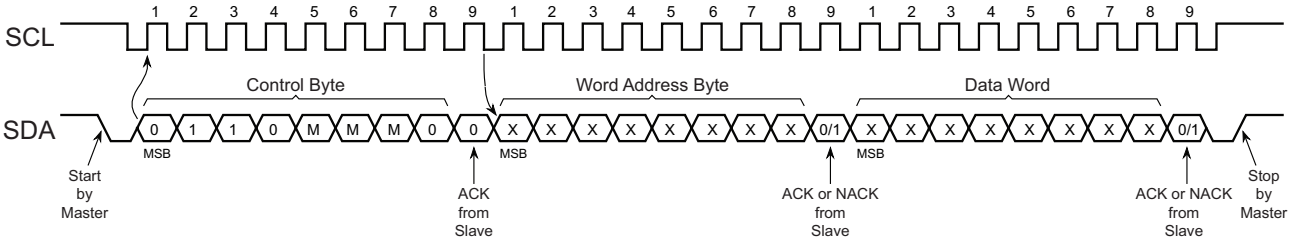
Example: If Quadrant 0 and Quadrant 3 are to be write-protected, two separate Set RSWP commands would be required; however, only one Clear RSWP command is needed to clear and unprotect both quadrants.

Table 7-2. Set RSWP and Clear RSWP

Function	Pin			Control Byte							
				Device Type Identifier				Memory Quadrant Identifier			R/$\overline{W}$
	A_2	A_1	A_0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Set RSWP, Quadrant 0	X	X	V_{HV}	0	1	1	0	0	0	1	0
Set RSWP, Quadrant 1	X	X						1	0	0	0
Set RSWP, Quadrant 2	X	X						1	0	1	0
Set RSWP, Quadrant 3	X	X						0	0	0	0
Clear RSWP	X	X						0	1	1	0

Notes:
1. X = Don't care but recommended to be hard-wired to V_{CC} or GND.
2. See Table 5-1 for V_{HV} value.
3. Due to the requirement for the A_0 pin to be driven to V_{HV}, the RSWP set and RSWP clear commands are fully supported in a single DIMM (isolated DIMM) end application or a single DIMM programming station only.

Figure 7-1. Set RSWP and Clear RSWP



M = Memory Quadrant Identifier

X = Don't care

7.2 Clear RSWP

Similar to the Set RSWP command, the reversible write protection on all quadrants can be reversed or unprotected by transmitting the Clear RSWP command. The Clear RSWP sequence requires the Master to send a Start condition followed by sending a control byte of '01100110' (66h) with the R/$\overline{W}$ bit set to a Logic 0. The AT34C04 should respond with an ACK. The Master transmits a word address byte and data bytes with don't care values. The AT34C04 will respond with either an ACK or NACK to both the word address and data word. In conjunction with sending the protocol, the A_0 pin must be connected to V_{HV} for the duration of the Clear RSWP command (see Figure 7-1). To end the Clear RSWP sequence, the Master sends a Stop condition.

CAUTION: The write protection of individual quadrants cannot be reversed separately, and executing the Clear RSWP command will clear the write protection on all four quadrants leaving all quadrants with no software write protection.

7.3 Read RSWP

The Read RSWP command allows the ability to check a quadrant's write protection status. To find out if the software write protection has been set to a specific quadrant, the same procedure that was used to set the quadrant's write protection can be utilized except that the R/$\overline{W}$ select bit is set to a Logic 1, and the A_0 pin is not required to have V_{HV} (see Table 7-4).

The Read RSWP sequence requires sending a control byte of '0110MMM1' (where the 'M' represents the memory quadrant identifier for the quadrant to be read) with the R/$\overline{W}$ bit set to a Logic 1 (see Figure 7-2).

If the RSWP has not been set, then the AT34C04 responds to the control byte with an ACK. If the RSWP has been set, the AT34C04 responds with a NACK. In either case, both Word Address and Data Word bytes will not be acknowledged. The operation is completed by the Master creating a Stop Condition. A summary of the response is shown in Table 7-3.

Table 7-3. Acknowledge When Reading Protection Status

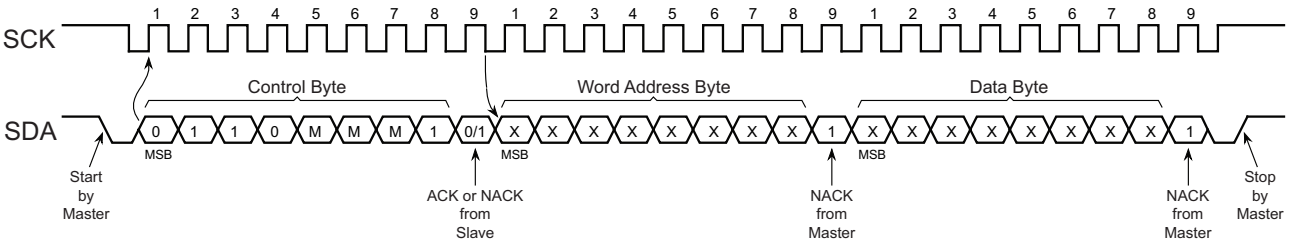
Quadrant Status	Instruction Sent	Instruction Response	Word Address Sent	Word Address Response	Data Word Sent	Data Word Response
Write Protected	Read RSWP	NACK	Don't Care	NACK	Don't Care	NACK
Not Protected	Read RSWP	ACK	Don't Care	NACK	Don't Care	NACK

Table 7-4. Read RSWP

Function	Pin			Control Byte							
				Device Type Identifier				Memory Quadrant Identifier			R/$\overline{W}$
	A_2	A_1	A_0	B7	B6	B5	B4	B3	B2	B1	B0
Read RSWP, Quadrant 0	X	X	0, 1 or V_{HV}	0	1	1	0	0	0	1	1
Read RSWP, Quadrant 1	X	X						1	0	0	1
Read RSWP, Quadrant 2	X	X						1	0	1	1
Read RSWP, Quadrant 3	X	X						0	0	0	1

Note: 1. X = Don't care but recommend to be hard-wired to V_{CC} or GND.

Figure 7-2. Read RSWP



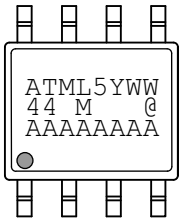
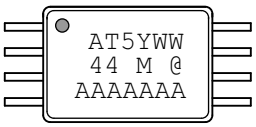
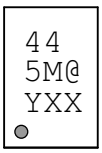
M = Memory Quadrant Identifier

X = Don't care

8. Part Marking Detail

8.1 Part Markings

AT34C04: Package Marking Information

8-lead SOIC	8-lead TSSOP	8-lead UDFN
		2.0 x 3.0 mm Body 

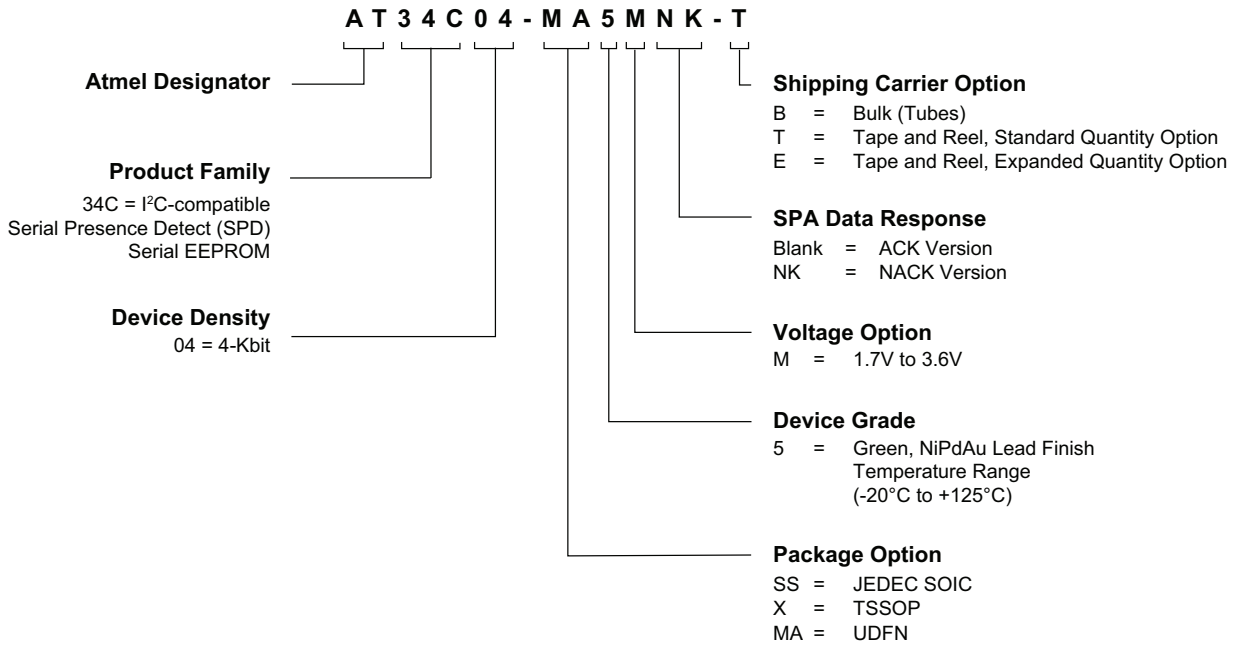
Note 1: ● designates pin 1
Note 2: Package drawings are not to scale

Catalog Number Truncation			
AT34C04		Truncation Code ##: 44	
Date Codes			**Voltages**
Y = Year	M = Month	WW = Work Week of Assembly	M: 1.7V min
2: 2012 6: 2016 3: 2013 7: 2017 4: 2014 8: 2018 5: 2015 9: 2019	A: January B: February ... L: December	02: Week 2 04: Week 4 ... 52: Week 52	
Country of Assembly	**Lot Number**		**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number		5: Industrial (C) (-20°C to 125°C)/NiPdAu
Trace Code			**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

8/16/12

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE	DRAWING NO.	REV.
	34C04SM, AT34C04 Package Marking Information	34C04SM	B

9. Ordering Code Detail



10. Ordering Information

Additional package types that are not listed below may be available for order. Please contact Atmel for availability details.

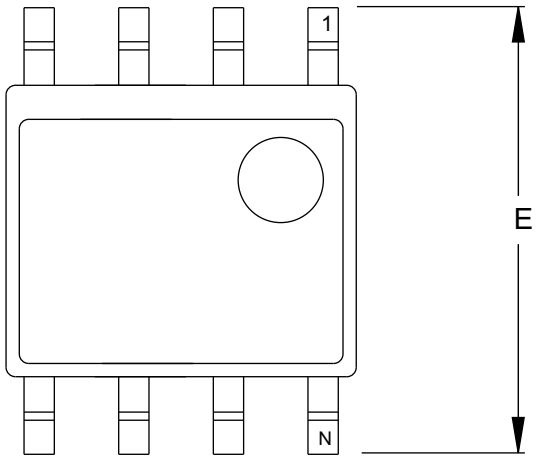
Atmel Ordering Code	Lead Finish	Package	Delivery Information		Operational Range
			Form	Quantity	
AT34C04-SS5M-B	NiPdAu (Lead-free/Halogen-free)	8S1	Bulk (Tubes)	100 per Tube	-20°C to 125°C
AT34C04-SS5M-T			Tape and Reel	4,000 per Reel	
AT34C04-X5M-B		8X	Bulk (Tubes)	100 per Tube	
AT34C04-X5M-T			Tape and Reel	5,000 per Reel	
AT34C04-MA5M-T(1)		8MA2	Tape and Reel	5,000 per Reel	
AT34C04-MA5M-E(1)			Tape and Reel	15,000 per Reel	
AT34C04-MA5MNK-T(1)			Tape and Reel	5,000 per Reel	

Note: 1. The “NK” designates that the device will NACK the SPA command data bytes. Refer to Section 6.1.1 for additional information.

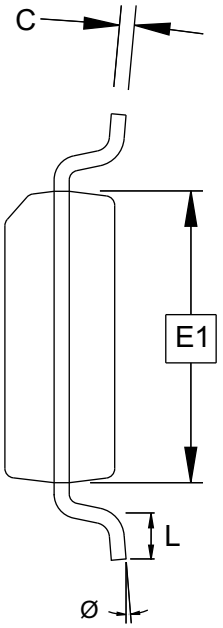
	Package Type
8S1	8-lead, 0.150” wide body, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 4.4mm body, Plastic Thin Shrink Small Outline (TSSOP)
8MA2	8-pad, 2.0 x 3.0mm body, 0.5mm pitch, Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead (UDFN)

11. Package Information

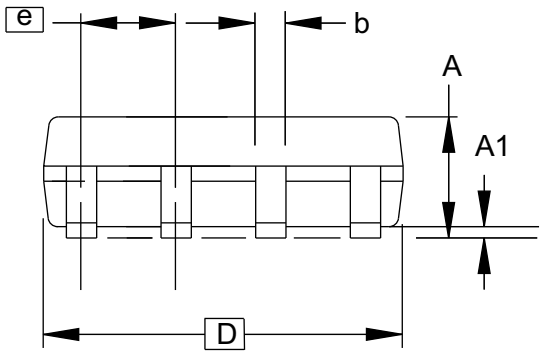
11.1 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

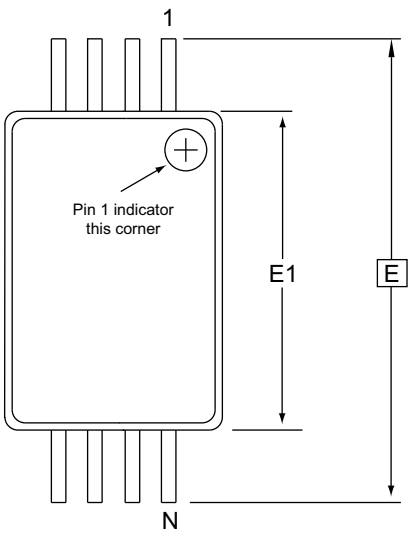
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.90 BSC			
E	6.00 BSC			
E1	3.90 BSC			
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

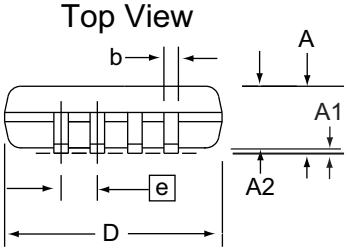
3/6/2015

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** H

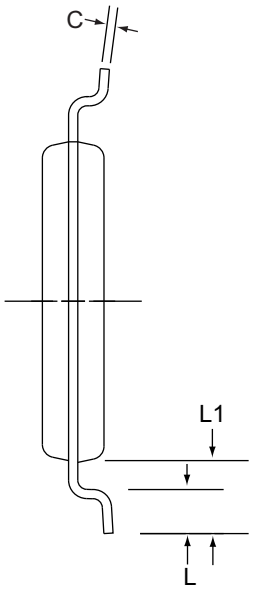
11.2 8X — 8-lead TSSOP



Top View



Side View



End View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

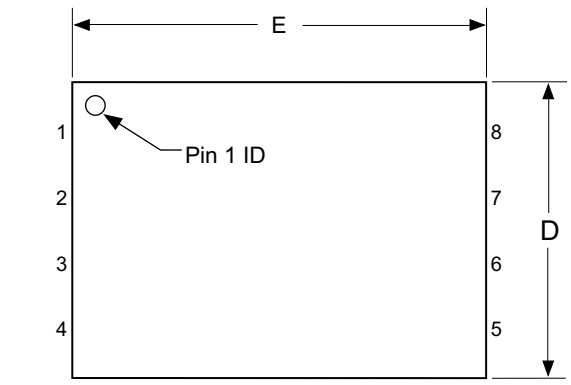
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	0.25	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

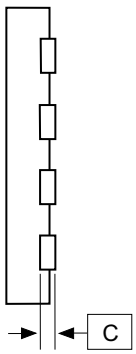
2/27/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	**GPC** TNR	**DRAWING NO.** 8X	**REV.** E

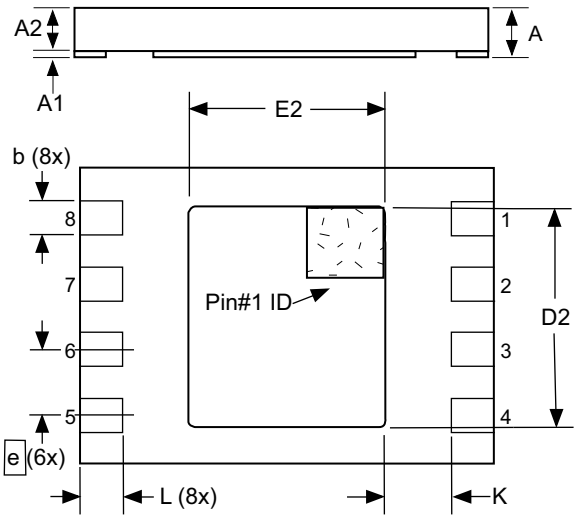
11.3 8MA2 — 8-pad UDFN



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Notes:
1. This drawing is for general information only. Refer to Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. The Pin #1 ID is a laser-marked feature on Top View.
3. Dimensions b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
4. The Pin #1 ID on the Bottom View is an orientation feature on the thermal pad.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.50	0.55	0.60	
A1	0.0	0.02	0.05	
A2	-	-	0.55	
D	1.90	2.00	2.10	
D2	1.40	1.50	1.60	
E	2.90	3.00	3.10	
E2	1.20	1.30	1.40	
b	0.18	0.25	0.30	3
C	1.52 REF			
L	0.30	0.35	0.40	
e	0.50 BSC			
K	0.20	-	-	

11/26/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8MA2, 8-pad 2 x 3 x 0.6mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No-Lead Package (UDFN)	**GPC** YNZ	**DRAWING NO.** 8MA2	**REV.** G

12. Revision History

Doc. Rev.	Date	Comments
8827G	01/2017	Added AT34C04-MA5MNK-T Part Number Correct Set Page Address figure and section Changed Ordering Code Detail and Ordering Information sections
8827F	10/2015	Correct Set Page Address figure and section.
8827E	01/2015	Add the UDFN extended quantity product offering. Update 8X and 8MA2 package outline drawings and the ordering information section.
8827D	12/2013	Remove Preliminary datasheet status.
8827C	07/2013	Remove part number, AT34C04-MA5M-B. Update electrical specifications. Update footers and disclaimer page.
8827B	12/2012	Increase V_{POR} maximum from 1.5V to 1.6V. Decrease t_I 100kHz maximum from 100ns to 50ns. Minor changes to DC and AC characteristic tables. Update datasheet status from advance to preliminary.
8827A	09/2012	Initial document release.

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