# AT91SAM7S-EK Evaluation Board

## User Guide

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# Section 1

# Overview

## 1.1 Scope

The AT91SAM7S-EK evaluation board enables the evaluation of and code development for applications running on an AT91SAM7Sxx device.

This document describes the evaluation board fitted with an AT91SAM7S256.

This guide focuses on the AT91SAM7S-EK board as an evaluation platform for the AT91SAM7S family.

## 1.2 Deliverables

### 1.2.1 Standard Version AT91SAM7S-EK VAR

The AT91SAM7S-EK package contains the following items:

- An AT91SAM7S-EK board
- One A/B-type USB cable
- One DVD-ROM containing summary and full datasheets, datasheets with electrical and mechanical characteristics, application notes and getting started documents for all development boards and AT91 microcontrollers. An AT91 software package with C and assembly listings is also provided. This allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly.

## 1.3 AT91SAM7S-EK Evaluation Board

The board is generally equipped with an AT91SAM7S256 (64-pin PQFP package) together with the following:

- USB device port interface
- Two serial communication ports
- JTAG/ICE debug interface
- Four buffered analog inputs
- Four general-purpose LEDs and pushbuttons
- Expansion connector
- Prototyping area

***Note:*** The user can also evaluate the AT91SAM7S32 with this board. A 48-pin TQFP footprint has been provided for this purpose. To do so, the user must unsolder the AT91SAM7S256 microcontroller (IC4) and fit the AT91SAM7S32 on the 48-pin TQFP footprint (IC5).

# Section 2

# Setting Up the AT91SAM7S-EK Board

## 2.1 Electrostatic Warning

The AT91SAM7S-EK evaluation board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

## 2.2 Requirements

In order to set up the AT91SAM7S-EK evaluation board, the following items are needed:

- The AT91SAM7S-EK evaluation board itself.
- Optional DC power supply capable of supplying 7V to 12V at 0.5 A.

***Note:*** The AT91SAM7S-EK is not delivered with the JTAG/ICE interface required to start evaluating the device.

## 2.3 Powering Up the Board

AT91SAM7S-EK is self-powered by the USB port. If the USB port is not used, the card can be supplied by an external DC power supply via the 2.1 mm socket (J1). The polarity of the power supply is not critical.

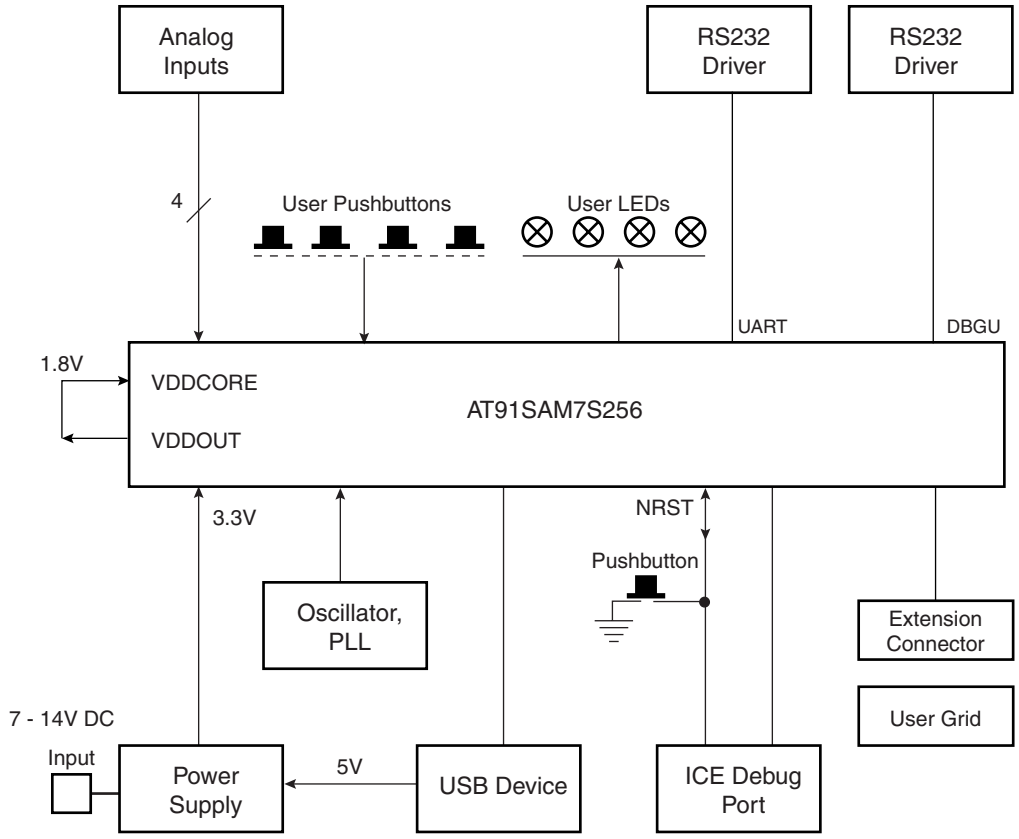
The regulator allows the input voltage range to be from 7V to 12V.

## 2.4 Getting Started

The AT91SAM7S-EK evaluation board is delivered with a DVD-ROM containing all necessary information and step-by-step procedures for working with the most common development toolchains. Please refer to this DVD-ROM, or to the AT91 web site, http://www.atmel.com/products/AT91/, for the most up-to-date information on getting started with the AT91SAM7S-EK.

## 2.5 AT91SAM7S-EK Block Diagram

***Figure 2-1.*** Block Diagram for AT91SAM7S-EK Board



# Section 3

# Board Description

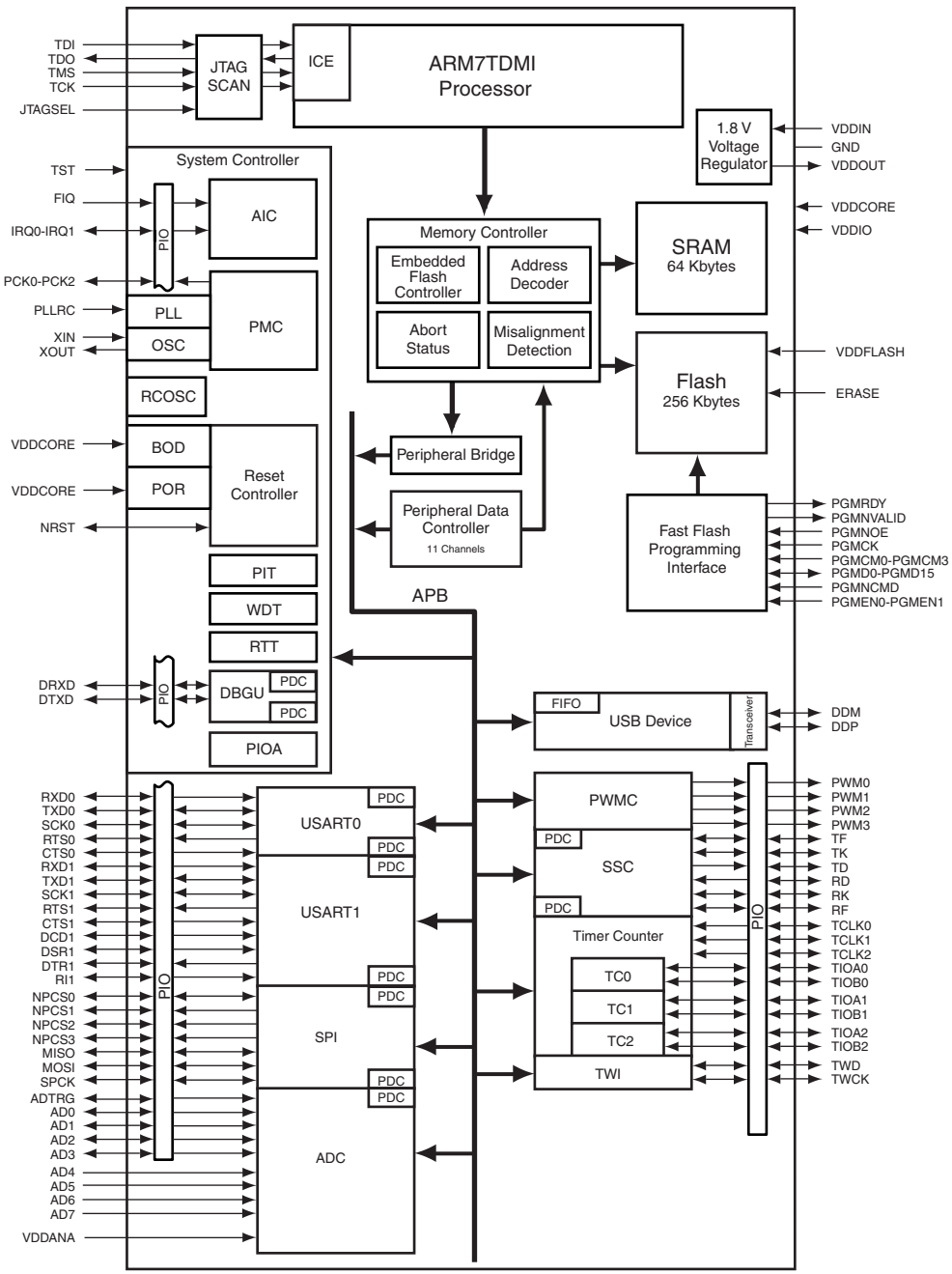
## 3.1 AT91SAM7S256 Microcontroller

- Incorporates the ARM7TDMI® ARM® Thumb® Processor
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - EmbeddedICE™ In-circuit Emulation, Debug Communication Channel Support
- 256 Kbytes of Internal High-speed Flash, Organized in 1024 Pages of 256 Bytes
  - Single Cycle Access at Up to 30 MHz in Worst Case Conditions, Prefetch Buffer Optimizing Thumb Instruction Execution at Maximum Speed
  - Page Programming Time: 4 ms, Including Page Auto-erase, Full Erase Time: 10 ms
  - 10,000 Write Cycles, 10-year Data Retention Capability, Sector Lock Capabilities, Flash Security Bit
  - Fast Flash Programming Interface for High Volume Production
- 64 Kbytes of Internal High-speed SRAM, Single-cycle Access at Maximum Speed
- Memory Controller (MC)
  - Embedded Flash Controller, Abort Status and Misalignment Detection
- Reset Controller (RSTC)
  - Based on Power-on Reset and Low-power Factory-calibrated Brown-out Detector
  - Provides External Reset Signal Shaping and Reset Source Status
- Clock Generator (CKGR)
  - Low-power RC Oscillator, 3 to 20 MHz On-chip Oscillator and one PLL
- Power Management Controller (PMC)
  - Software Power Optimization Capabilities, Including Slow Clock Mode (Down to 500 Hz) and Idle Mode
  - Three Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Two External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire UART and Support for Debug Communication Channel interrupt, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
  - 20-bit Programmable Counter plus 12-bit Interval Counter
- Windowed Watchdog (WDT)

  - 12-bit key-protected Programmable Counter
  - Provides Reset or Interrupt Signals to the System
  - Counter May Be Stopped While the Processor is in Debug State or in Idle Mode
- Real-time Timer (RTT)
  - 32-bit Free-running Counter with Alarm
  - Runs Off the Internal RC Oscillator
- One Parallel Input/Output Controller (PIOA)
  - Thirty-Two Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up resistor and Synchronous Output
- Eleven Peripheral Data Controller (PDC) Channels
- One USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, 328-byte Configurable Integrated FIFOs
- One Synchronous Serial Controller (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Two Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
  - Manchester Encoder/Decoder
  - Full Modem Line Support on USART1
- One Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counter (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- One Four-channel 16-bit PWM Controller (PWMC)
- One Two-wire Interface (TWI)
  - Master Mode Support Only, All Two-wire Atmel EEPROMs Supported
- One 8-channel 10-bit Analog-to-Digital Converter, Four Channels Multiplexed with Digital I/Os
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- 5V-tolerant I/Os, including Four High-current Drive I/O lines, Up to 16 mA Each
- Power Supplies
  - Embedded 1.8V Regulator, Drawing up to 100 mA for the Core and External Components
  - 1.8V or 3.3V VDDIO I/O Lines Power Supply, Independent 3.3V VDDFLASH Flash Power Supply
  - 1.8V VDDCORE Core Power Supply with Brown-out Detector
  - 3.3V VDDANA Analog Voltage Supply
- Fully Static Operation: Up to 55 MHz at 1.65V and 85° C Worst Case Conditions
- Available in a 64-lead TQFP Package

## 3.2 AT91SAM7S256 Block Diagram

*Figure 3-1.* AT91SAM7S256 Block Diagram




## 3.3 Memory

- 256 Kbytes of internal high-speed Flash
- 64 Kbytes of internal high-speed SRAM

## 3.4 Clock Circuitry

- 18.432 MHz standard crystal for the embedded oscillator

## 3.5 Reset Circuitry

- Internal bi-directional reset controller with brown out detector
- External reset pushbutton

## 3.6 Power Supply Circuitry

- USB powered. The dynamic power consumption on VDDCORE is less than 50 mA at full speed when running out of the Flash. The total current drawn by all the I/O lines cannot exceed 200 mA.
- External power can be applied via the 2.1 mm connector to the regulator in either polarity because of the diode-rectifying circuit (CR3 to CR6). The minimum voltage required is 7V. The board has a voltage regulator providing +3.3V. The regulator allows the input voltage to be from 7V to 14V (REG1).
- The two power supplies are separated from each other by the diodes CR1 and CR2.
- On-chip embedded VDDCORE 1.8V regulator

## 3.7 Remote Communication

- Two serial interface via RS-232 DB9 male sockets
  - DBGU COM Port
  - UART COM Port with RTS/CTS handshake control possibility (USART 0)
- USB V2.0 full-speed compliant, 12 Mbits per second (UDP)

## 3.8 Analog Interface

- Four analog inputs (0V to 3.3V) via J7, J8, J9, J10 footprints

## 3.9 User Interface

- Four pushbuttons via general PIO lines
- Four LEDs via high current PIO lines

## 3.10 Debug Interface

- 20-pin JTAG/ICE interface connector
- DBGU COM port

## 3.11 Expansion Connector

One expansion connector (J5) gives access to all the microcontroller's signals.

All I/Os of the AT91SAM7S256 are routed to this connector. This allows the developer to check the integrity of the components and to extend the features of the board by adding external hardware components or boards.

## 3.12 Wrapping User Area

This allows the developer to fit additional components for prototyping use.

# Section 4

# Configuration Straps

## 4.1 Configuration Strap

Table 4-1 gives details on configuration straps on the AT91SAM7S-EK evaluation board and their default settings.

***Table 4-1.*** Configuration Straps

| Designation | Default Setting | Feature |
|---|---|---|
| JP1 | Closed | Enables the use of the remote DP pull-up (USB) |
| JP2 | Closed | Enables the use of the VBUS detect (USB) |
| JP3 | Opened | Disable external VCC on the expansion connector J5 (pin 1, 2) |
| JP4 | Closed | The System Reset signal (NRST) is connected to the ICE/JTAG socket (J4, pin 15). |
| JP5 | Opened | Do not use: Factory test mode |
| JP6 | Closed | Enables the use of the CTS signal (UART) |
| JP7 | Closed | Enables the use of the TXD signal (UART) |
| JP8 | Closed | Enables the use of the RTS signal (UART) |
| JP9 | Closed | Enables the use of the RXD signal (UART) |
| JP10 | Closed | |
| JP11 | Closed | Enables the use of the RXD signal (DBGU) |
| JP12 | Closed | Enables the use of the TXD signal (DBGU) |
| JP13(1) | Closed | VDDFLASH Jumper |
| JP14(1) | Closed | VDDIO Jumper |
| JP15 | Closed | Enables the use of the User LED (DS1) |
| JP16 | Closed | Enables the use of the User LED (DS2) |
| JP17 | Closed | Enables the use of the User LED (DS3) |
| JP18 | Closed | Enables the use of the User LED (DS4) |
| JP19 | Opened | Select ICE mode or JTAG mode (Closed) |
| JP20(1) | Closed | ADVREFP Jumper |
| JP21(1) | Closed | VDDPLL Jumper |

***Table 4-1.*** Configuration Straps

| Designation | Default Setting | Feature |
|---|---|---|
| JP22[1] | Closed | VDDIN Jumper |
| JP23[1] | Closed | VDDCORE Jumper |
| JP24 | Closed | Enables the use of the EXT_AD0 (Analog Input 0) |
| JP25 | Closed | Enables the use of the EXT_AD1 (Analog Input 1) |
| JP26 | Closed | Enables the use of the EXT_AD4 (Analog Input 4) |
| JP27 | Closed | Enables the use of the EXT_AD5 (Analog Input 5) |
| JP28 | Opened | Erases all internal Flash memory when the board is powered. To do so, the user must close J28 for at least 10 ms. |
| TP1 | N.A | GND Test point |
| TP3 | N.A | GND Test point |
| TP5 | N.A | GND Test point |
| TP6 | N.A | GND Test point |

Note: 1. These jumpers are dedicated to power consumption measurement use. The user has to open the jumper and insert an anmeter.
If these jumpers are not populated (previous revisions of the kit), the related straps are wired on board. In this case and in order to use the power consumption measurement feature, the user has to open the strap by cutting it before soldering a jumper and inserting an anmeter.

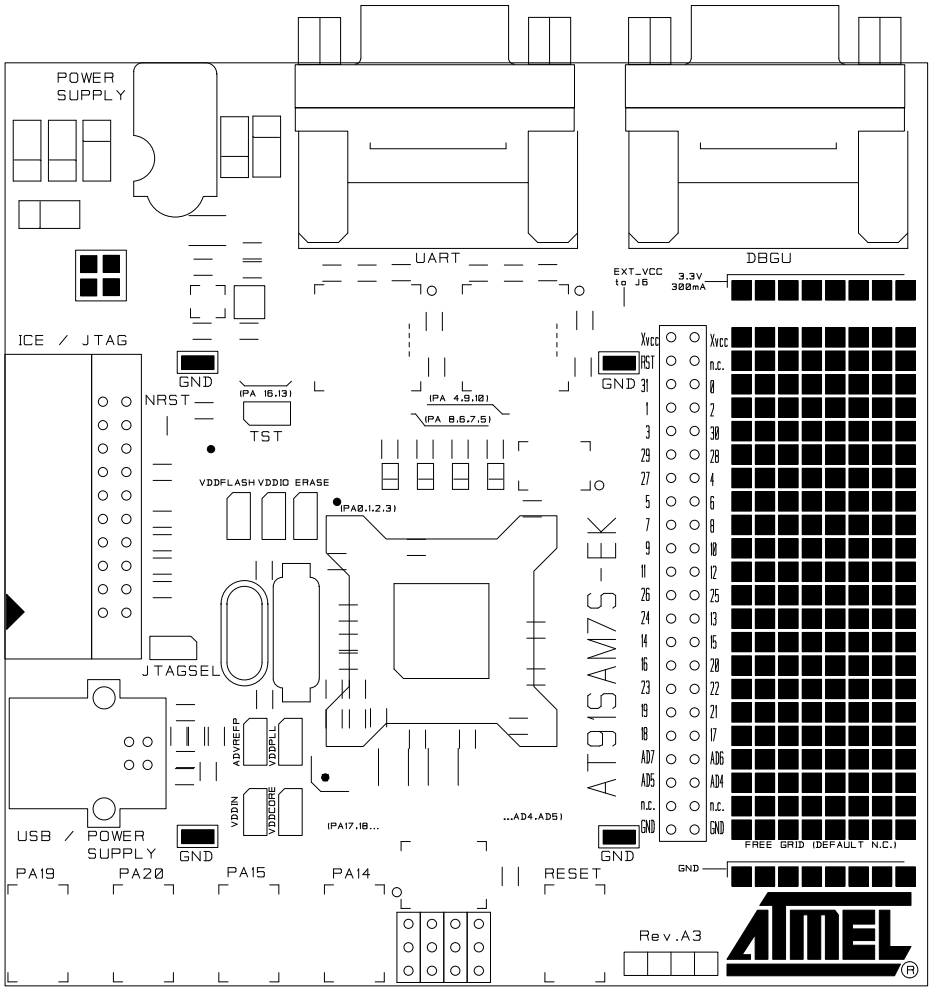
# Section 5

# Schematics

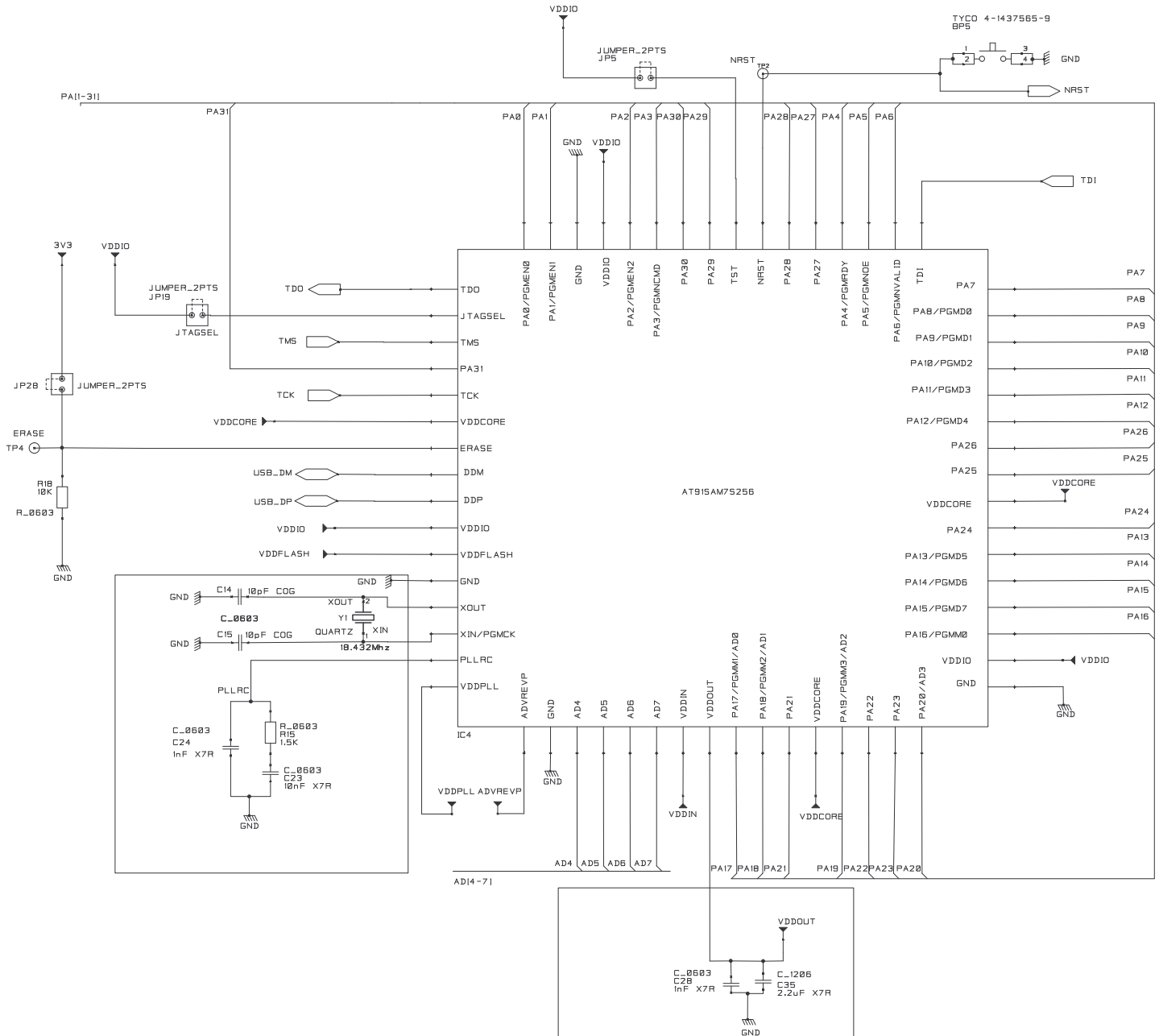
## 5.1 Schematics

This section contains the following schematics:

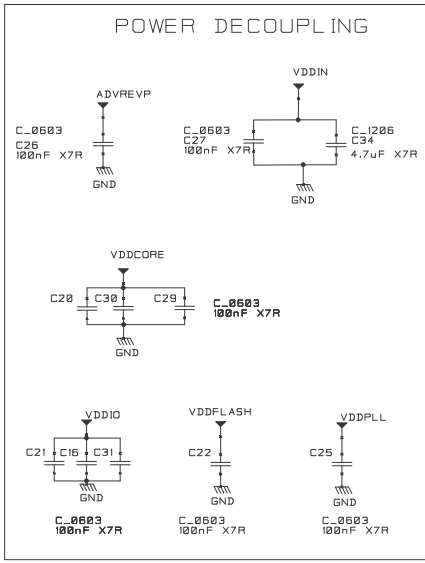
- Board Layout And Silkscreen Printing - Top View
- 64-pin SAM7 Microcontroller (dual footprint)
- 48-pin SAM7 Microcontroller
- Power Supply
- ICE/EXT Connectors
- Device Interface
- PIO
- User PAD Grid




| | | |
|---|---|---|
| | | |
| A3 | 4 AUG 04 | |
| A2 | 9 JUNE04 | |
| A | 15APR04 | Initial version |

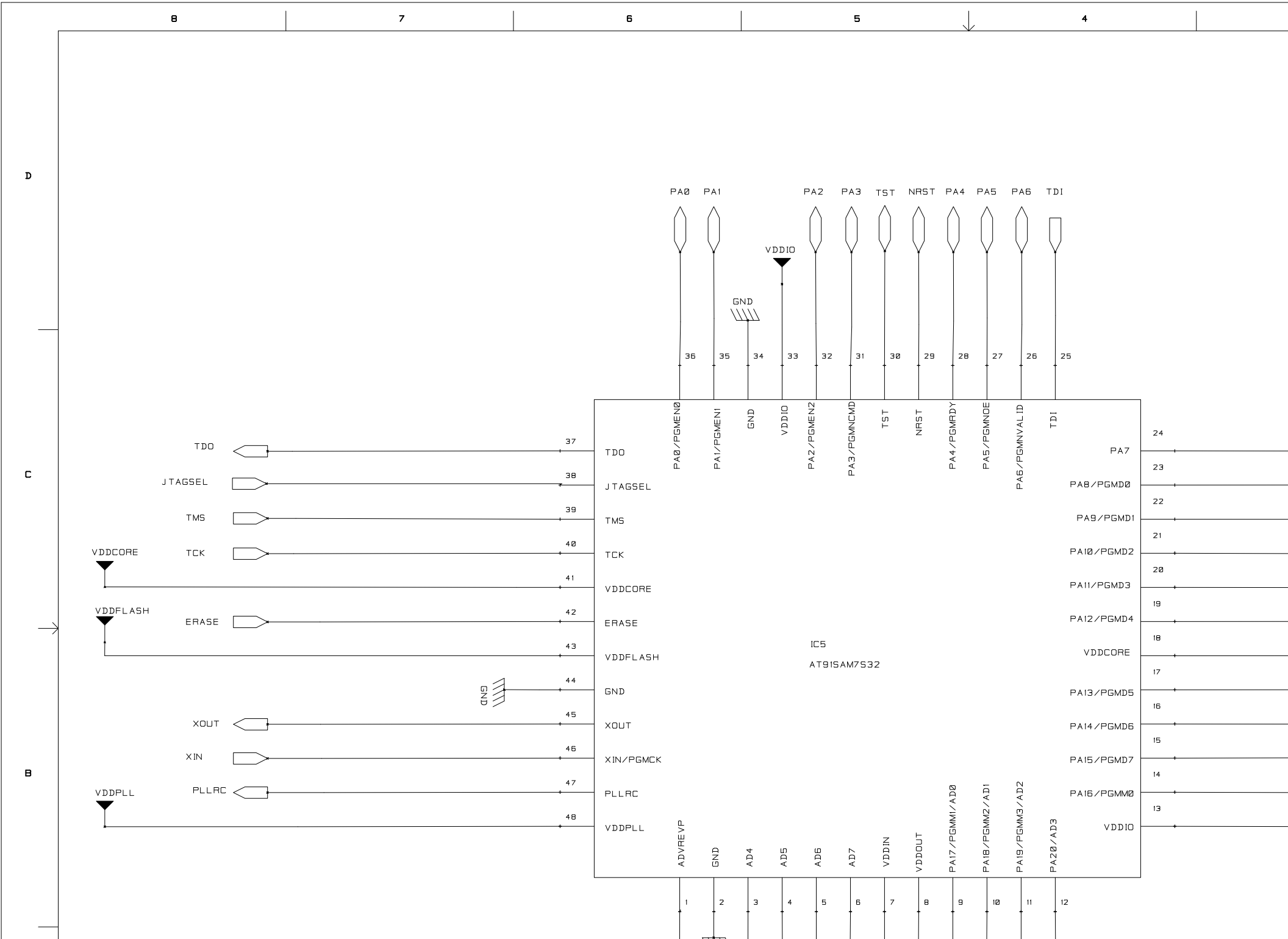



## POWER DECOUPLING



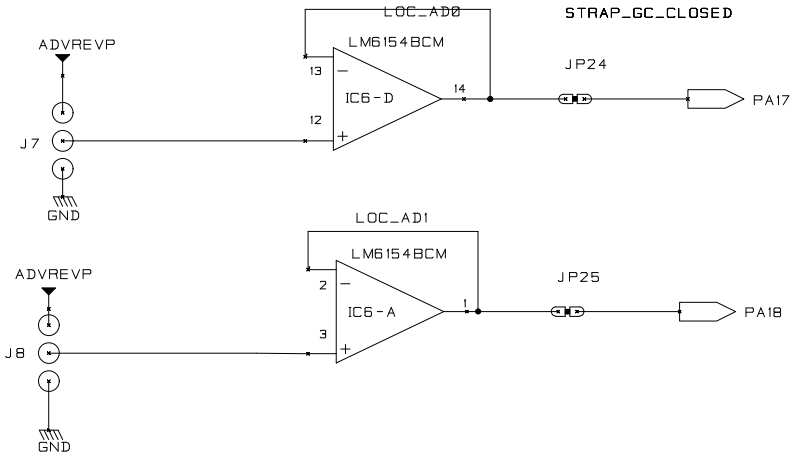

AT91SAM7S-EK

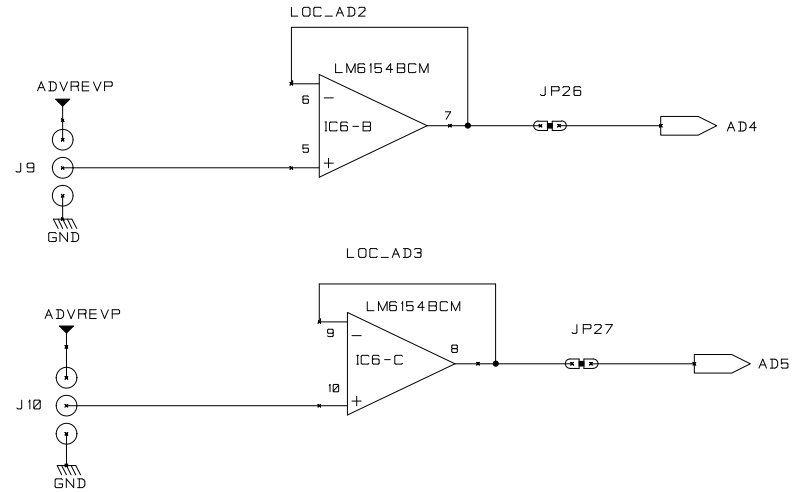
| | Title. | Ind. | Date |
|---|---|---|---|
| ATMEL | AT91SAM7S-EK | A4 | NOV05 |
| | AT91SAM7S-EK | A3 | 04AOU0 |
| AT91SAM7S-EK | AT91SAM7S-EK | A2 | 17MA04 |
| | AT91SAM7S-EK | A | 19AVRIL |
| 64 PINS SAM7 | Scale. 1:1 | Page 1 | |

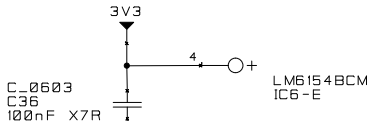

8
7
6
5
4
D
C
B
PA0
PA1
PA2
PA3
TST
NRST
PA4
PA5
PA6
TDI
VDDIO
GND
36
35
34
33
32
31
30
29
28
27
26
25
PA0/PGMEN0
PA1/PGMEN1
GND
VDDIO
PA2/PGMEN2
PA3/PGMNCMD
TST
NRST
PA4/PGMRDY
PA5/PGMNOE
PA6/PGMNVALID
TDI
TDO
JTAGSEL
TMS
TCK
VDDCORE
ERASE
VDDFLASH
GND
XOUT
XIN
PLLRC
VDDPLL
37
38
39
40
41
42
43
44
45
46
47
48
TDO
JTAGSEL
TMS
TCK
VDDCORE
ERASE
VDDFLASH
GND
XOUT
XIN/PGMCK
PLLRC
VDDPLL
IC5
AT91SAM7S32
24
23
22
21
20
19
18
17
16
15
14
13
PA7
PA8/PGMD0
PA9/PGMD1
PA10/PGMD2
PA11/PGMD3
PA12/PGMD4
VDDCORE
PA13/PGMD5
PA14/PGMD6
PA15/PGMD7
PA16/PGMM0
VDDIO
1
2
3
4
5
6
7
8
9
10
11
12
ADVREVP
GND
AD4
AD5
AD6
AD7
VDDIN
VDDOUT
PA17/PGMM1/AD0
PA18/PGMM2/AD1
PA19/PGMM3/AD2
PA20/AD3

## ANALOG INPUTS

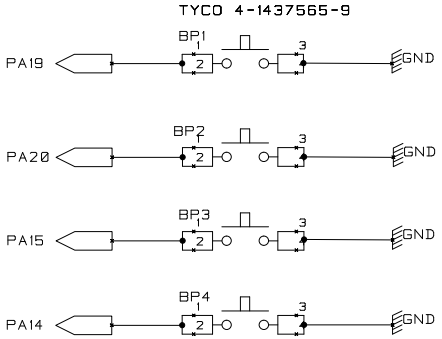
BARRETTE 3PTS 2.54MM



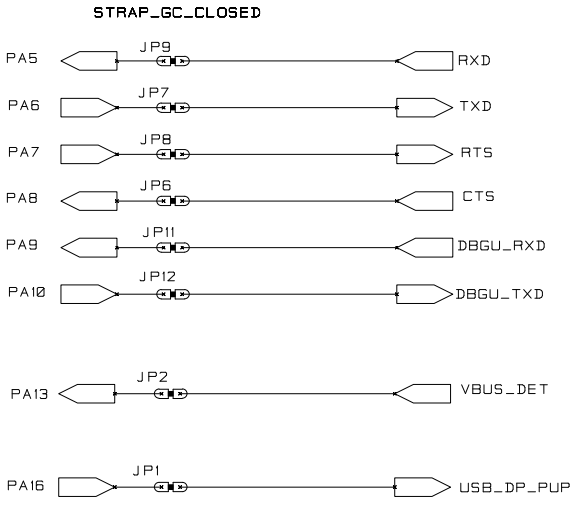




## USER PUSH-BUTTONS



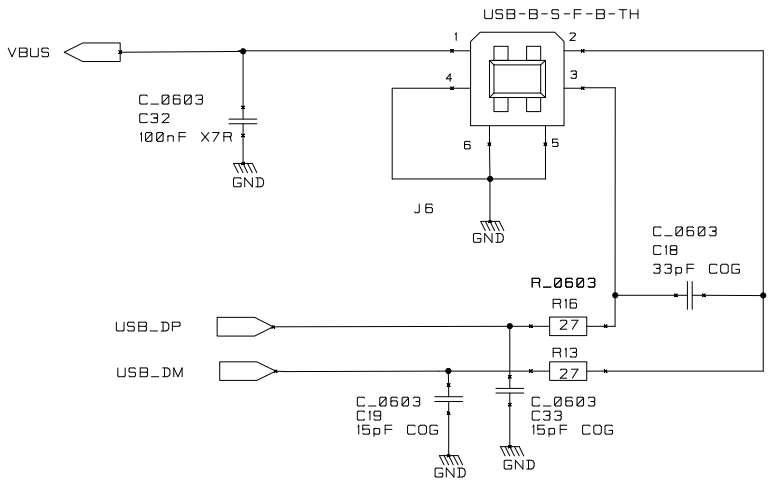

## PIO STRAPS



8 7 6 5 4

D C B

## USB




## COM/SERIAL PORT.

DB

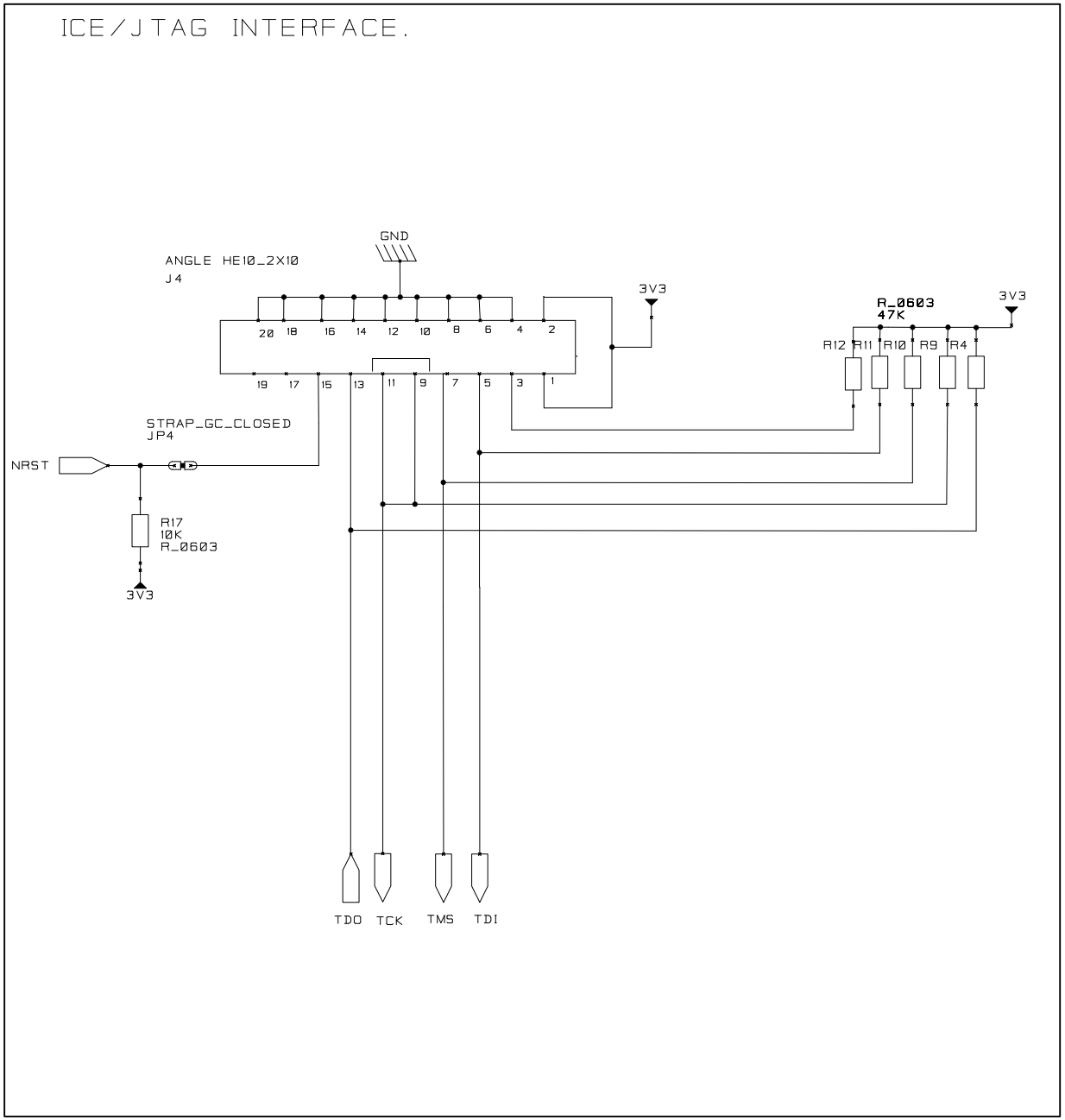
DE

RTS

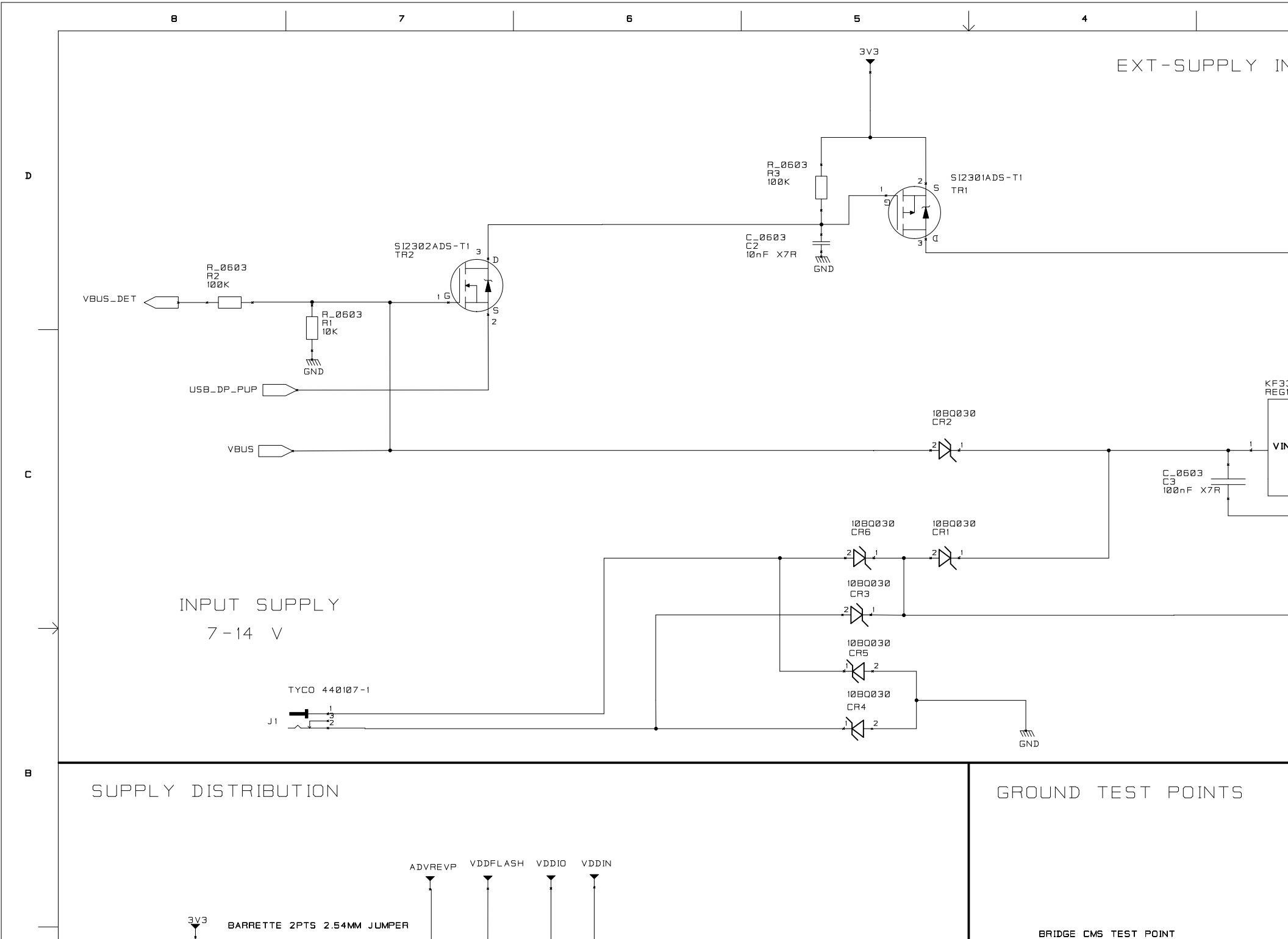
TXD

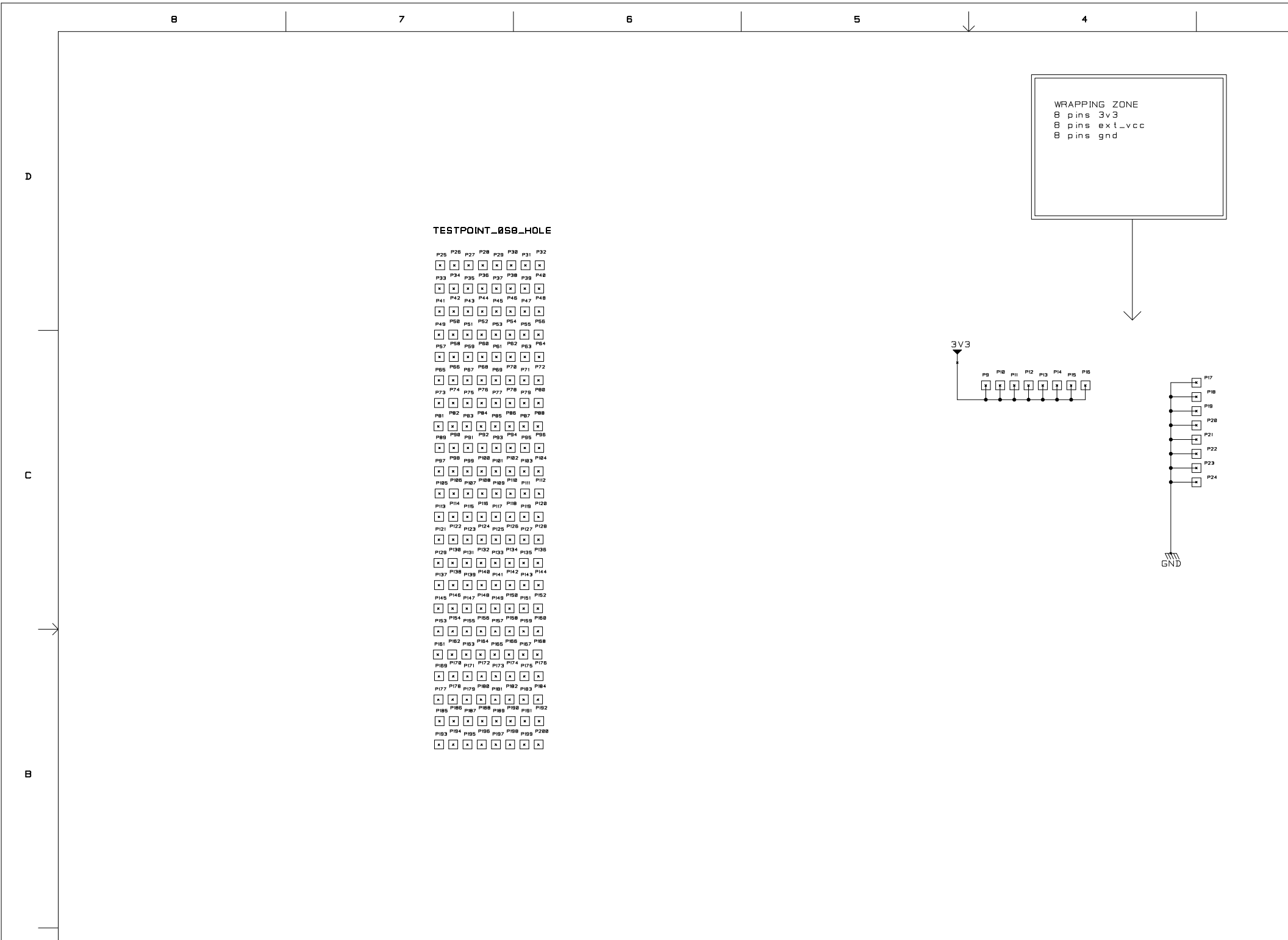
RXD

CTS


ICE/JTAG INTERFACE.
GND
ANGLE HE10_2X10
J4
20 18 16 14 12 10 8 6 4 2
19 17 15 13 11 9 7 5 3 1
3V3
R_0603
47K
3V3
R12 R11 R10 R9 R4
STRAP_GC_CLOSED
JP4
NRST
R17
10K
R_0603
3V3
TDO TCK TMS TDI

I/O


EXT-SUPPLY IN
3V3
R_0603
R3
100K
SI2301ADS-T1
TR1
C_0603
C2
10nF X7R
GND
SI2302ADS-T1
TR2
R_0603
R2
100K
VBUS_DET
R_0603
R1
10K
GND
USB_DP_PUP
VBUS
10BQ030
CR2
C_0603
C3
100nF X7R
10BQ030
CR6
10BQ030
CR1
10BQ030
CR3
10BQ030
CR5
10BQ030
CR4
INPUT SUPPLY
7-14 V
TYCO 440107-1
J1
GND
SUPPLY DISTRIBUTION
ADVREVP
VDDFLASH
VDDIO
VDDIN
3V3
BARRETTE 2PTS 2.54MM JUMPER
GROUND TEST POINTS
BRIDGE CMS TEST POINT


8
7
6
5
4
D
C
B
TESTPOINT_0S8_HOLE
P25 P26 P27 P28 P29 P30 P31 P32
P33 P34 P35 P36 P37 P38 P39 P40
P41 P42 P43 P44 P45 P46 P47 P48
P49 P50 P51 P52 P53 P54 P55 P56
P57 P58 P59 P60 P61 P62 P63 P64
P65 P66 P67 P68 P69 P70 P71 P72
P73 P74 P75 P76 P77 P78 P79 P80
P81 P82 P83 P84 P85 P86 P87 P88
P89 P90 P91 P92 P93 P94 P95 P96
P97 P98 P99 P100 P101 P102 P103 P104
P105 P106 P107 P108 P109 P110 P111 P112
P113 P114 P115 P116 P117 P118 P119 P120
P121 P122 P123 P124 P125 P126 P127 P128
P129 P130 P131 P132 P133 P134 P135 P136
P137 P138 P139 P140 P141 P142 P143 P144
P145 P146 P147 P148 P149 P150 P151 P152
P153 P154 P155 P156 P157 P158 P159 P160
P161 P162 P163 P164 P165 P166 P167 P168
P169 P170 P171 P172 P173 P174 P175 P176
P177 P178 P179 P180 P181 P182 P183 P184
P185 P186 P187 P188 P189 P190 P191 P192
P193 P194 P195 P196 P197 P198 P199 P200
WRAPPING ZONE
8 pins 3v3
8 pins ext_vcc
8 pins gnd
3V3
P9 P10 P11 P12 P13 P14 P15 P16
P17 P18 P19 P20 P21 P22 P23 P24
GND

# Section 6

# Revision History

## 6.1 Revision History

*Table 6-1.*

| Document | Comments | Change Request Ref. |
|---|---|---|
| 6112A | First issue. | |
| 6112B | New schematics. | 1457 |
| 6112C | Corrected features for JP26 and JP27 in Table 4-1, "Configuration Straps".<br>Corrected device label in 64-pin SAM7 schematic. | 3849<br>2734 |

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