AT91SAM9263-EK Evaluation Board Rev. B

User Guide

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Section 1

Overview

1.1 Scope

The AT91SAM9263-EK evaluation kit enables the evaluation of and code development for applications running on an AT91SAM9263.

This guide focuses on the AT91SAM9263-EK board Rev. B as an evaluation platform.

1.2 How to Identify the Kit BOM Revision

Table 1-1. AT91SAM9263-EK History

Kit BOM Revision	Schematics Revision	PCB Revision	NAND Flash Device Mounted on Board	AT91SAM9623 Silicon Revision	Boot from DataFlash® Card	Boot from on-board NAND Flash
001..003	A	A	MN21B = Samsung® K9F2G08U0M-PCB0	A	yes	no
004..006	B	B	MN21B = Samsung K9F2G08U0M-PCB0	A	yes	no
007	B	B	MN21B = Micron® MT29F2G08AACWP	B	yes	yes
008..on	C	B	MN21B = Micron MT29F2G08AACWP	B	yes	yes

The BOM (bill of material) revision level is tagged on the kit box as shown below in Figure 1-1.

Figure 1-1. AT91SAM9263-E Kit BOM

1.3 How to Identify the PCB Revision

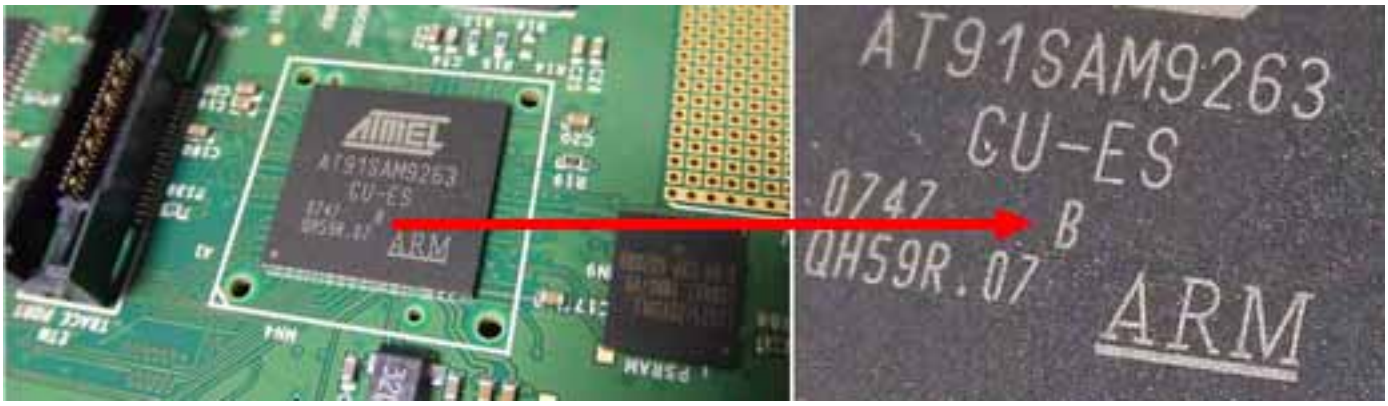
The PCB revision can be clearly identified by looking at the board copper marking on the bottom side. The last character of the series indicates the revision. Thus, If the series of characters ends with the letter “B” (e.g. 63PC0608021B), your board is Rev. B.

For technical information on Revision A boards, refer to the corresponding User Guide, Atmel literature number 6279, available on the Atmel web site.

1.4 How to Identify the SAM9263 Silicon Revision

The AT91SAM9263 MRL B (Marketing Revision Level B) parts are identified with a letter “B” on top of the package as shown below:

Figure 1-2. AT91SAM92639263 MRL B



1.5 NAND Flash Access Issue

On the AT91SAM9263-EK with Kit BOM revision 007, the user can experience access errors when reading or writing the NAND Flash device (MN21B).

This problem is due to disturbances on the chip select line. It can be fixed by the following:

- replacing the resistor R139 (0 Ohms) by a 2.2 µH inductor
- replacing the resistor R33 (470 K Ohms) by a 100 pF capacitor

This fix has been implemented on the AT91SAM9263-EK with Kit BOM revisions 008 and onward.

Alternatively, tying the NAND Flash chip select line to the ground fixes the problem.

This can be achieved simply by connecting pin 2 of J29 together with pin 30 of J23. However, this simpler solution prevents some Flash modes from being operational because the accesses are then controlled only through NANDOE and NANDWE. But, this does at least allow to boot WinCE and Linux on the board from the NAND Flash.

1.6 Deliverables

The AT91SAM9263-EK package contains the following items:

- an AT91SAM9263-EK board Rev. B
- one A/B-type USB cable
- one serial RS232 cable
- one RJ45 crossed Ethernet cable
- one CD-ROM that allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly.

1.7 AT91SAM9263-EK Evaluation Board Rev. B

The board is equipped with an AT91SAM9263 (324-ball LFBGA package) together with the following:

- 64 Mbytes of SDRAM memory
- 4 Mbytes of PSRAM memory on EBI1
- 256 Mbytes of NAND Flash memory
- One NOR Flash memory (footprint only)
- One 1.8” Hard disk connectors
- One TWI serial memory
- One USB device port interface
- Two USB Host port interfaces
- One RS232 serial communication port
- One DBGU serial communication port
- One serial CAN 2.0B communication port
- One JTAG/ICE debug interface
- One Ethernet 100-base TX with three status LEDs
- One AC97 Audio DAC
- One 3.5" 1/4 VGA TFT LCD Module with TouchScreen and backlight
- One ISI connector (camera interface)
- One Power LED and two general-purpose LEDs
- Two user input push buttons
- One Wakeup input push button
- One reset push button
- One DataFlash®/SD/SDIO/MMC card slot
- One SD/SDIO/MMC card slot
- One Lithium Coin Cell Battery Retainer for 12 mm cell size

Section 2

Setting Up the AT91SAM9263-EK Board Rev. B

2.1 Electrostatic Warning

The AT91SAM9263-EK evaluation board Rev. B is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

In order to set up the AT91SAM9263-EK evaluation board Rev. B, the following items are needed:

- the AT91SAM9263-EK evaluation board Rev. B itself
- AC/DC power adapter (12V at 1A), 2.1 mm by 5.5 mm

2.3 Layout

See Figures 2-1 and 2-2.

Figure 2-1. AT91SAM9263-EK Layout - Top View

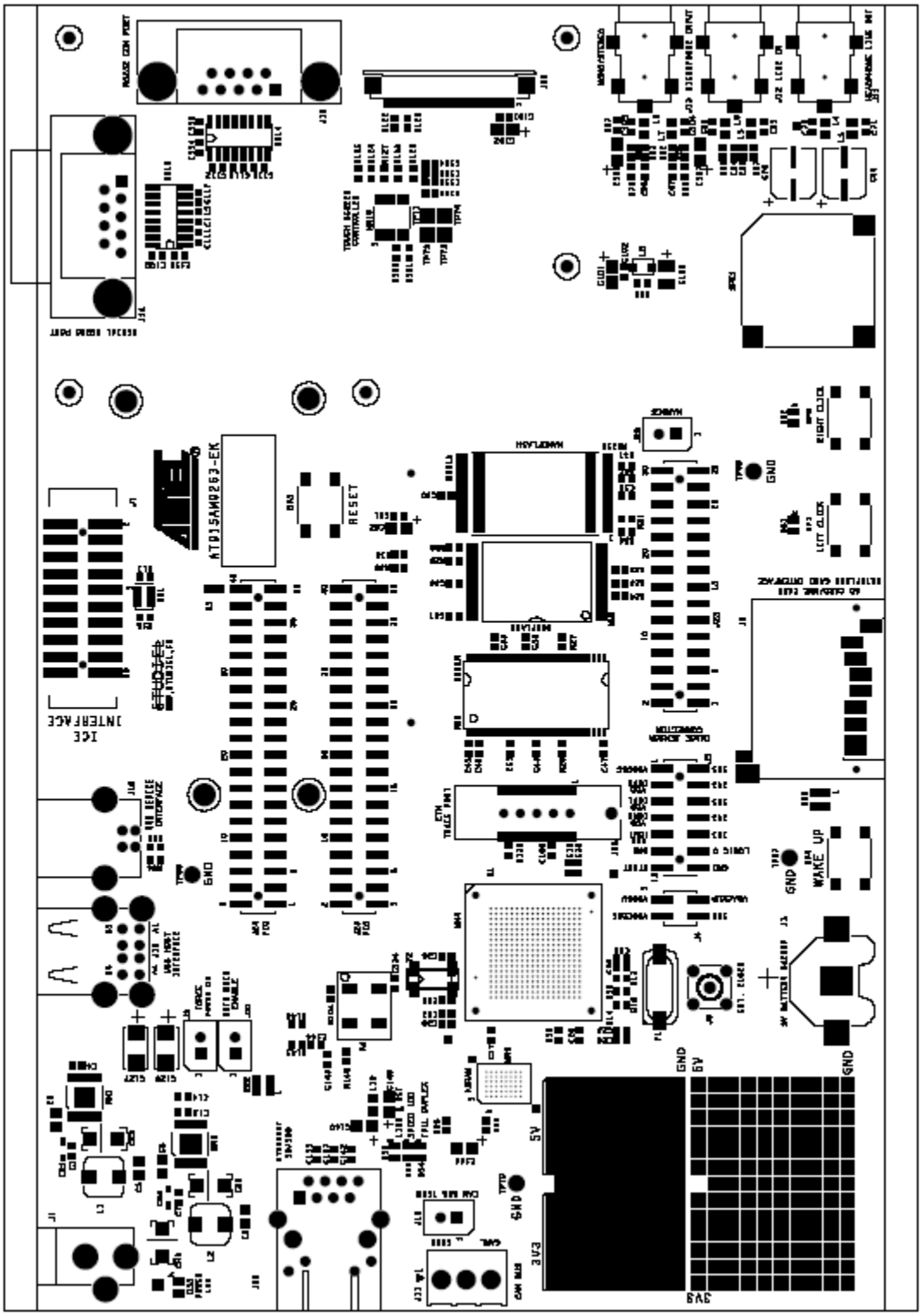
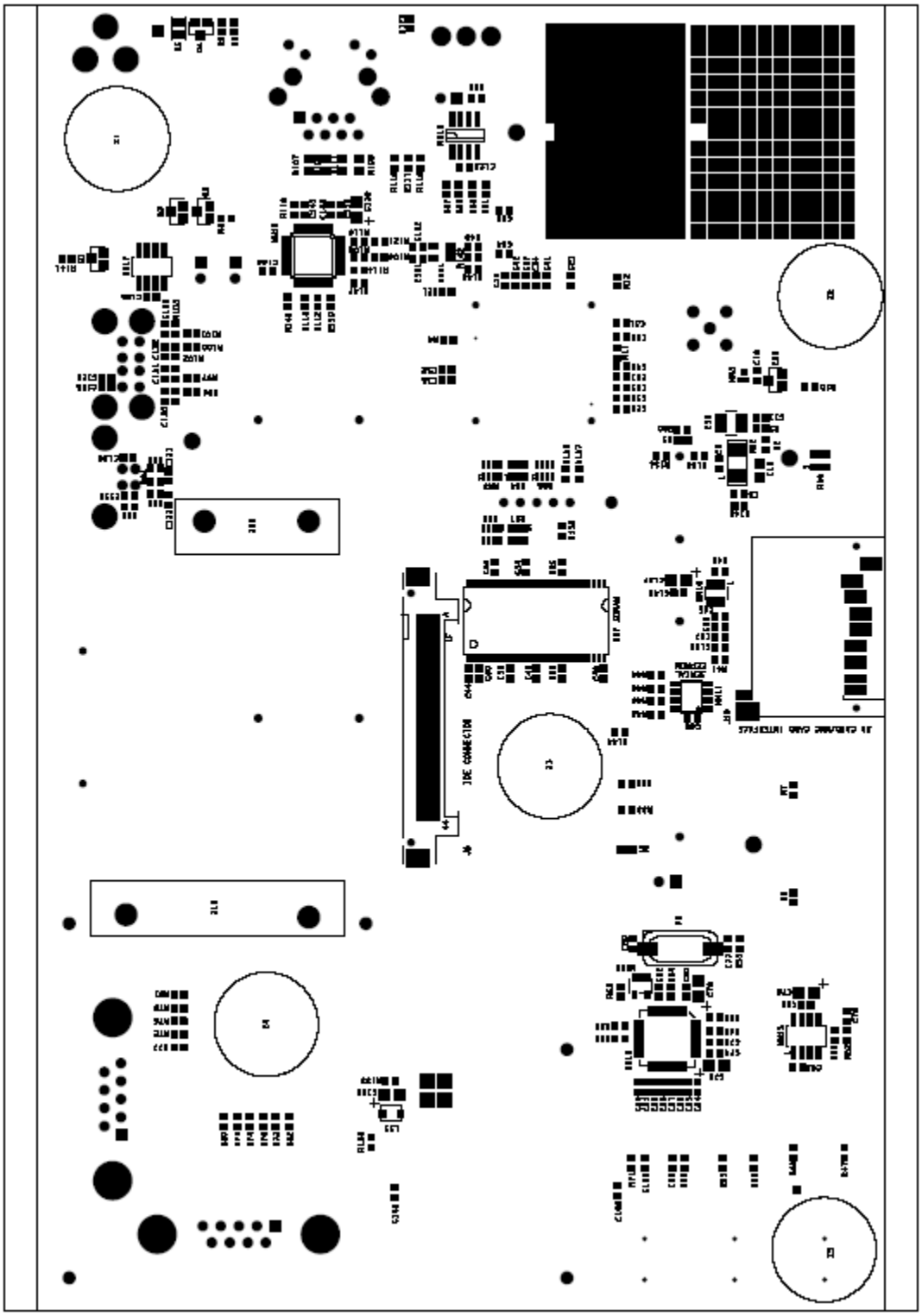


Figure 2-2. AT91SAM9263-EK Layout - Bottom View



2.4 Powering Up the Board

The AT91SAM9263-EK requires 12V DC. DC power is supplied to the board via the 2.1 mm by 5.5 mm socket J1. Coaxial plug center positive standard.

2.5 Backup Power Supply

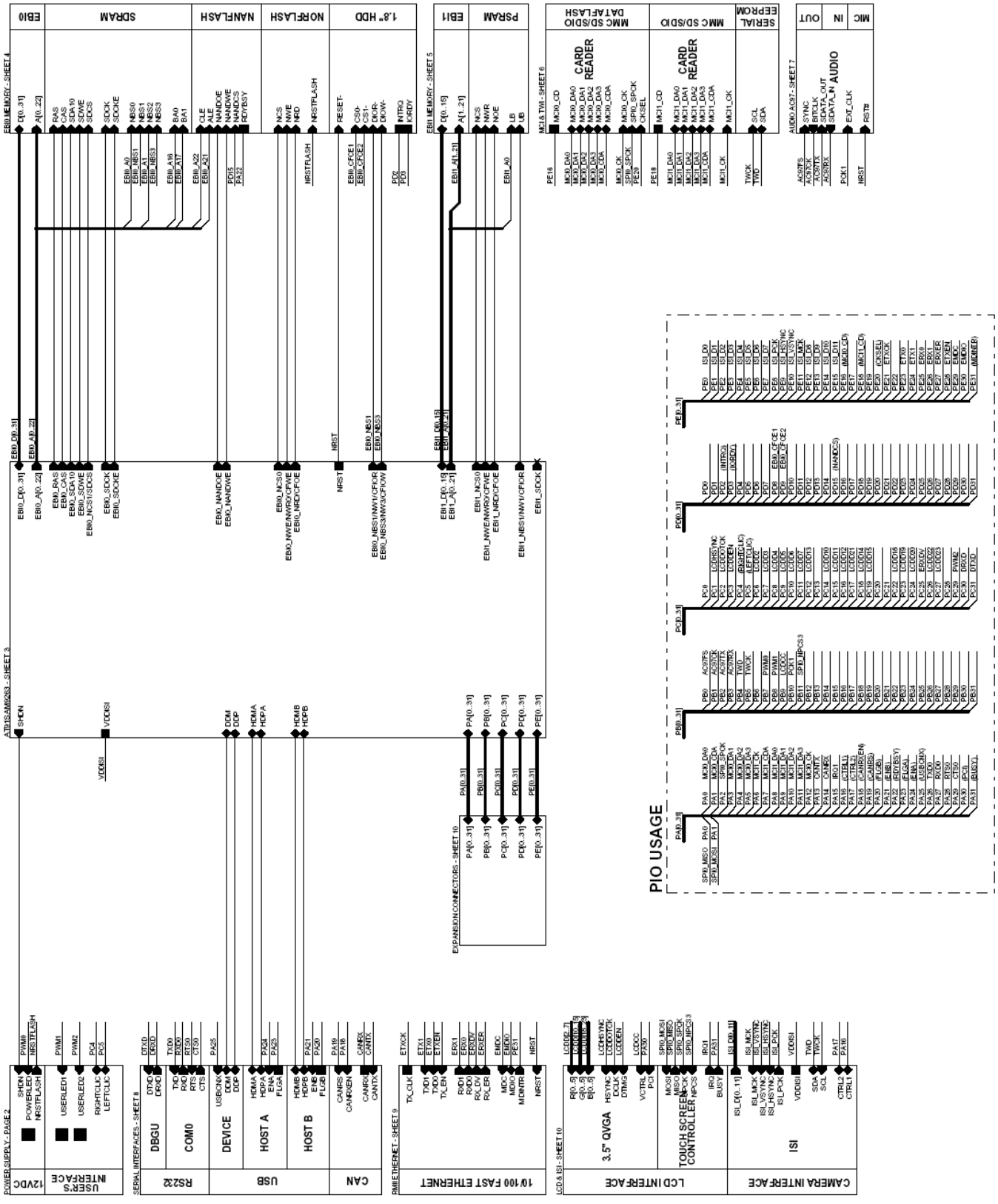
The user has the possibility to plug a battery (3V Lithium Battery CR1225 or equivalent) in order to permanently power the backup part of the device.

2.6 Getting Started

The AT91SAM9263-EK evaluation board Rev. B is delivered with a CD-ROM that allows the user to begin evaluation of the AT91 ARM Thumb 32-bit microcontroller quickly. Please refer to the AT91 web site, http://www.atmel.com/products/AT91/, for the most up-to-date information on getting started with the AT91SAM9263-EK.

2.7 AT91SAM9263-EK Block Diagram

Figure 2-3. AT91SAM9263-EK Block Diagram



Section 3

Board Description

3.1 AT91SAM9263 Microcontroller

- Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
  - DSP Instruction Extensions, Jazelle® Technology for Java® Acceleration
  - 16 Kbyte Data Cache, 16 Kbyte Instruction Cache, Write Buffer
  - 200 MIPS at 180 MHz
  - Memory Management Unit
  - EmbeddedICE™, Debug Communication Channel Support
  - Mid-level Implementation Embedded Trace Macrocell™
- Bus Matrix
  - Nine 32-bit-layer Matrix, Allowing a Total of 28.8 Gbps of On-chip Bus Bandwidth
  - Boot Mode Select Option, Remap Command
- Embedded Memories
  - One 128 Kbyte Internal ROM, Single-cycle Access at Maximum Bus Matrix Speed
  - One 80 Kbyte Internal SRAM, Single-cycle Access at Maximum Processor Bus Matrix Speed
  - One 16 Kbyte Internal SRAM, Single-cycle Access at Maximum Bus Matrix Speed
- Dual External Bus Interface (EBI0 and EBI1)
  - EBI0 Supports SDRAM, Static Memory, ECC-enabled NAND Flash and CompactFlash®
  - EBI1 Supports SDRAM, Static Memory and ECC-enabled NAND Flash
- DMA Controller (DMAC)
  - Acts as one Bus Matrix Master
  - Embeds 2 Unidirectional Channels with Programmable Priority, Address Generation, Channel Buffering and Control
- Twenty Peripheral DMA Controller Channels (PDC)
- LCD Controller
  - Supports Passive or Active Displays
  - Up to 24 bits per Pixel in TFT Mode, Up to 16 bits per Pixel in STN Color Mode
  - Up to 16M Colors in TFT Mode, Resolution Up to 2048x2048, Supports Virtual Screen Buffers
- 2D Graphics Accelerator
  - Line Draw, Block Transfer, Polygon Fill, Clipping, Commands Queuing
- Image Sensor Interface
  - ITU-R BT. 601/656 External Interface, Programmable Frame Capture Rate
  - 12-bit Data Interface for Support of High Sensibility Sensors
  - SAV and EAV Synchronization, Preview Path with Scaler, YCbCr Format

- USB 2.0 Full Speed (12 Mbits per second) Host Double Port
  - Dual On-chip Transceivers
  - Integrated FIFOs and Dedicated DMA Channels
- USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, 2,432-byte Configurable Integrated DPRAM
- Ethernet MAC 10/100 Base-T
  - Media Independent Interface or Reduced Media Independent Interface
  - 28-byte FIFOs and Dedicated DMA Channels for Receive and Transmit
- Fully-featured System Controller, including
  - Reset Controller, Shutdown Controller
  - Twenty 32-bit Battery Backup Registers for a Total of 80 Bytes
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Double Real-time Timer
- Reset Controller (RSTC)
  - Based on Two Power-on Reset Cells, Reset Source Identification and Reset Output Control
- Shutdown Controller (SHDWC)
  - Programmable Shutdown Pin Control and Wake-up Circuitry
- Clock Generator (CKGR)
  - 32768Hz Low-power Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
  - 3 to 20 MHz On-chip Oscillator and Two Up to 240 MHz PLLs
- Power Management Controller (PMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Four Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Two External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire UART and Support for Debug Communication Channel, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
  - 20-bit Interval Timer plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock
- Two Real-time Timers (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler
- Five 32-bit Parallel Input/Output Controllers (PIOA, PIOB, PIOC, PIOD and PIOE)
  - 160 Programmable I/O Lines Multiplexed with Up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- One Part 2.0A and Part 2.0B-compliant CAN Controller

  - 16 Fully-programmable Message Object Mailboxes, 16-bit Time Stamp Counter
- Two Multimedia Card Interface (MCI)
  - SDCard/SDIO and MultiMediaCard™ Compliant
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC
  - Two SDCard Slots Support on eAch Controller
- Two Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- One AC97 Controller (AC97C)
  - 6-channel Single AC97 Analog Front End Interface, Slot Assigner
- Three Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation, Manchester Encoding/Decoding
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
- Two Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
  - Synchronous Communications at Up to 90Mbits/sec
- One Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- One Four-channel 16-bit PWM Controller (PWMC)
- One Two-wire Interface (TWI)
  - Master Mode Support, All Two-wire Atmel® EEPROMs Supported
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies
  - 1.08V to 1.32V for VDDCORE and VDDBU
  - 3.0V to 3.6V for VDDOSC, VDDPLL and VDDIOP0 (Peripheral I/Os)
  - 1.65V to 3.6V for VDDIOP1 (Peripheral I/Os)
  - Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOM0/VDDIOM1 (Memory I/Os)
- Available in a 324-ball BGA Green Package

3.2 AT91SAM9263 Block Diagram

Figure 3-1. AT91SAM9263 Block Diagram

3.3 Memory

- 16 Kbytes of Internal data cache
- 16 Kbytes of Internal instruction cache
- 128 Kbytes of Internal ROM
- 80 Kbytes of Internal single-cycle access high-speed SRAM
- 16 Kbytes of Internal single-cycle access high-speed SRAM
- 8 Mbytes of Atmel NOR Flash (not populated)
- 64 Mbytes of SDRAM memory
- 4 Mbytes of PSRAM (EBI1)
- 256 Mbytes of NAND Flash memory
- Atmel TWI serial EEPROM

3.4 Clock Circuitry

- 16.36766 MHz standard crystal for the embedded oscillator
- 32.768 kHz standard crystal for the slow clock oscillator

3.5 Reset Circuitry

- Internal reset controller with bi-directional reset pin
- External reset pushbutton

3.6 Shutdown Controller

- Programmable shutdown and Wake-Up
- Wake-up push button

3.7 Power Supply Circuitry

- For dynamic power consumption, the AT91SAM9263 consumes a maximum of 50 mA on VDDCORE at maximum speed in typical conditions (1.2V, 25°C), processor running full-performance algorithm.
- On-board 1.2V high efficiency step-down Charge Pump regulator with shutdown control
- On-board 3.3V switching regulator with shutdown control
- On-board 5V switching regulator with shutdown control

3.8 Remote Communication

- One RS232 serial communication port
- One serial CAN 2.0B communication port via 3-position printed circuit terminal block
- One USB V2.0 Full-speed Compliant, 12 Mbits per second (UDP)
- Two USB Host ports V2.0 Full-speed Compliant, 12 Mbits per second (UHP)
- One RMII Ethernet 100-base TX with three status LEDs

3.9 Audio Stereo Interface

- One AC'97 2.3 compliant Codec (20-bit PCM DAC)
- One 32-ohm Stereo Headset line-out
- One stereo line input
- One stereo electret microphone input
- One mono 8-ohm amplified speaker

3.10 User Interface

- Two user input push buttons
- Two user green LEDs
- One yellow power LED (can be also software controlled)
- One 3.5" ¼ VGA display LCD with Touch Panel and white LED backlight
- One ISI connector (camera interface)

3.11 Debug Interface

- 20-pin JTAG/ICE interface connector
- One Serial interface (DBGU COM Port) via RS-232 DB9 male socket

3.12 Expansion Slot

- One DataFlash/SD/SDIO/MMC card slot
- One SD/SDIO/MMC card slot
- All unused I/Os of the AT91SAM9263 are routed to peripheral extension connectors (J24 and J25). This allows the developer to add external hardware components or boards.

3.13 PIO Usage

Table 3-1. PIO Controller A

I/O Line	Peripheral A	Peripheral B	Peripheral Usage		Powered by
PA0	MCI0_DA0	SPI0_MISO	SD/MMC/DATAFLASH SOCKET (J9) & TOUCH SCEEN CONTROLLER	MCI0_DA0 or SPI0_MISO	VDDIOP0
PA1	MCI0_CDA	SPI0_MOSI	SD/MMC/DATAFLASH SOCKET (J9) & TOUCH SCEEN CONTROLLER	MCI0_CDA or SPI0_MOSI	VDDIOP0
PA2		SPI0_SPCK	SD/MMC/DATAFLASH SOCKET (J9) & TOUCH SCEEN CONTROLLER	SPI0_SPCK	VDDIOP0
PA3	MCI0_DA1	SPI0_NPCS1	SD/MMC/DATAFLASH SOCKET (J9)		VDDIOP0
PA4	MCI0_DA2	SPI0_NPCS2	SD/MMC/DATAFLASH SOCKET (J9)		VDDIOP0
PA5	MCI0_DA3	SPI0_NPCS0	SD/MMC/DATAFLASH SOCKET (J9)		VDDIOP0
PA6	MCI1_CK	PCK2	SD/MMC SOCKET (J10)	MCI1_CK	VDDIOP0
PA7	MCI1_CDA		SD/MMC SOCKET (J10)	MCI1_CDA	VDDIOP0
PA8	MCI1_DA0		SD/MMC SOCKET (J10)	MCI1_DA0	VDDIOP0
PA9	MCI1_DA1		SD/MMC SOCKET (J10)	MCI1_DA1	VDDIOP0
PA10	MCI1_DA2		SD/MMC SOCKET (J10)	MCI1_DA2	VDDIOP0
PA11	MCI1_DA3		SD/MMC SOCKET (J10)	MCI1_DA3	VDDIOP0
PA12	MCI0_CK		SD/MMC/DATAFLASH SOCKET (J9)	MCI0_CK	VDDIOP0
PA13	CANTX	PCK0	CAN BUS INTERFACE (J17)	CANTX	VDDIOP0
PA14	CANRX	IRQ0	CAN BUS INTERFACE (J17)	CANRX	VDDIOP0
PA15	TCLK2	IRQ1	TOUCH SCREEN CONTROLLER (MN19)	IRQ1	VDDIOP0
PA16	MCI0_CDB	EBI1_D16	IMAGE SENSORS CONNECTORS (J23)	PA16 as CTRL1	VDDIOM1
PA17	MCI0_DB0	EBI1_D17	IMAGE SENSORS CONNECTORS (J23)	PA17 as CTRL2	VDDIOM1
PA18	MCI0_DB1	EBI1_D18	CAN INTERFACE (RXEN)	PA18 as RXEN	VDDIOM1
PA19	MCI0_DB2	EBI1_D19	CAN INTERFACE (RS)	PA19 as RS	VDDIOM1
PA20	MCI0_DB3	EBI1_D20	USB HOST B POWER MONITOR (MN17)	PA20 as FLGB	VDDIOM1
PA21	MCI1_CDB	EBI1_D21	USB HOST B POWER CONTROL (MN17)	PA21 as ENB	VDDIOM1
PA22	MCI1_DB0	EBI1_D22	NAND FLASH (MN12B)	PA22 as RDY/BSY	VDDIOM1
PA23	MCI1_DB1	EBI1_D23	USB HOST B POWER MONITOR (MN17)	PA23 as FLGA	VDDIOM1
PA24	MCI1_DB2	EBI1_D24	USB HOST B POWER CONTROL (MN17)	PA24 as ENA	VDDIOM1
PA25	MCI1_DB3	EBI1_D25	USB DEVICE INTERFACE	PA25 as USB_CNX	VDDIOM1
PA26	TXD0	EBI1_D26	RS232 COM PORT (J15)	TXD0	VDDIOM1
PA27	RXD0	EBI1_D27	RS232 COM PORT (J15)	RXD0	VDDIOM1
PA28	RTS0	EBI1_D28	RS232 COM PORT (J15)	RTS0	VDDIOM1
PA29	CTS0	EBI1_D29	RS232 COM PORT (J15)	CTS0	VDDIOM1
PA30	SCK0	EBI1_D30	LCD PANEL (Power Control In)	PA30 as PCI	VDDIOM1
PA31	DMARQ0	EBI_D31	TOUCH SCREEN CONTROLLER (MN19)	PA31 as BUSY	VDDIOM1

Table 3-2. PIO Controller B

I/O Line	Peripheral A	Peripheral B	Peripheral Usage		Powered by
PB0	AC97FS	TF0	AC97 CODEC (MN12)	AC97FS	VDDIOP0
PB1	AC97CK	TK0	AC97 CODEC (MN12)	AC97CK	VDDIOP0
PB2	AC97TX	TD0	AC97 CODEC (MN12)	AC97TX	VDDIOP0
PB3	AC97RX	RD0	AC97 CODEC (MN12)	AC97RX	VDDIOP0
PB4	TWD	RK0	TWI EEPROM (MN11)	TWD / SDA	VDDIOP0
PB5	TWCK	RF0	TWI EEPROM (MN11)	TWCK / SCL	VDDIOP0
PB6	TF1	DMARQ1			VDDIOP0
PB7	TK1	PWM0	POWER LED CONTROL (DS3)	PB7 or PWM0	VDDIOP0
PB8	TD1	PWM1	USER'S LED1 CONTROL (DS1)	PB8 or PWM1	VDDIOP0
PB9	RD1	LCDCC	LCD PANEL (backlight control)	LCDCC	VDDIOP0
PB10	RK1	PCK1	AC97 CODEC (MN12) Optional clock source	PCK1	VDDIOP0
PB11	RF1	SPI0_NPCS3	TOUCH SCREEN CONTROLLER (MN19)	SPI0_NPCS3	VDDIOP0
PB12	SPI1_MISO				VDDIOP0
PB13	SPI1_MOSI				VDDIOP0
PB14	SPI1_SPCK				VDDIOP0
PB15	SPI1_NPCS0				VDDIOP0
PB16	SPI1_NPCS1	PCK1			VDDIOP0
PB17	SPI1_NPCS2	TIOA2			VDDIOP0
PB18	SPI1_NPCS3	TIOB2			VDDIOP0
PB19					VDDIOP0
PB20					VDDIOP0
PB21					VDDIOP0
PB22					VDDIOP0
PB23					VDDIOP0
PB24		DMARQ3			VDDIOP0
PB25					VDDIOP0
PB26					VDDIOP0
PB27		PWM2			VDDIOP0
PB28		TCLK0			VDDIOP0
PB29		PWM3			VDDIOP0
PB30					VDDIOP0
PB31					VDDIOP0

Table 3-3. PIO Controller C

I/O Line	Peripheral A	Peripheral B	Peripheral Usage			Powered by
PC0	LCDVSYNC					VDDIOP0
PC1	LCDHSYNC		LCD PANEL	LCDHSYNC		VDDIOP0
PC2	LCDDOTCK		LCD PANEL	LCDDOTCK		VDDIOP0
PC3	LCDDEN	PWM1	LCD PANEL	LCDDEN		VDDIOP0
PC4	LCDD0	LCDD3	USER'S PUSH BUTTON (BP2)	PC4 as RIGHT CLICK		VDDIOP0
PC5	LCDD1	LCDD4	USER'S PUSH BUTTON (BP1)	PC5 as LEFT CLICK		VDDIOP0
PC6	LCDD2	LCDD5	LCD PANEL	LCDD2	RED	VDDIOP0
PC7	LCDD3	LCDD6	LCD PANEL	LCDD3	RED	VDDIOP0
PC8	LCDD4	LCDD7	LCD PANEL	LCDD4	RED	VDDIOP0
PC9	LCDD5	LCDD10	LCD PANEL	LCDD5	RED	VDDIOP0
PC10	LCDD6	LCDD11	LCD PANEL	LCDD6	RED	VDDIOP0
PC11	LCDD7	LCDD12	LCD PANEL	LCDD7	RED	VDDIOP0
PC12	LCDD8	LCDD13	LCD PANEL	LCDD13	GREEN	VDDIOP0
PC13	LCDD9	LCDD14				VDDIOP0
PC14	LCDD10	LCDD15	LCD PANEL	LCDD10	GREEN	VDDIOP0
PC15	LCDD11	LCDD19	LCD PANEL	LCDD11	GREEN	VDDIOP0
PC16	LCDD12	LCDD20	LCD PANEL	LCDD12	GREEN	VDDIOP0
PC17	LCDD13	LCDD21	LCD PANEL	LCDD21	BLUE	VDDIOP0
PC18	LCDD14	LCDD22	LCD PANEL	LCDD14	GREEN	VDDIOP0
PC19	LCDD15	LCDD23	LCD PANEL	LCDD15	GREEN	VDDIOP0
PC20	LCDD16	ETX2				VDDIOP0
PC21	LCDD17	ETX3				VDDIOP0
PC22	LCDD18	ERX2	LCD PANEL	LCDD18	BLUE	VDDIOP0
PC23	LCDD19	ERX3	LCD PANEL	LCDD19	BLUE	VDDIOP0
PC24	LCDD20	ETXER	LCD PANEL	LCDD20	BLUE	VDDIOP0
PC25	LCDD21	ERXDV	ETHERNET RMII (MN18)	ERXDV		VDDIOP0
PC26	LCDD22	ECOL	LCD PANEL	LCDD22	BLUE	VDDIOP0
PC27	LCDD23	ERXCK	LCD PANEL	LCDD23	BLUE	VDDIOP0
PC28	PWM0	TCLK1				VDDIOP0
PC29	PCK0	PWM2	USER'S LED2 CONTROL (DS2)	PC29 or PWM2		VDDIOP0
PC30	DRXD		SERIAL DEBUG PORT (J14)	DRXD		VDDIOP0
PC31	DTXD		SERIAL DEBUG PORT (J14)	DTXD		VDDIOP0

Table 3-4. PIO Controller D

I/O Line	Peripheral A	Peripheral B	Peripheral Usage		Powered by
PD0	TXD1	SPI0_NPCS2			VDDIOP0
PD1	RXD1	SPI0_NPCS3			VDDIOP0
PD2	TXD2	SPI1_NPCS2	HDD CONNECTORS (J8)	PD2 as IRQ	VDDIOP0
PD3	RXD2	SPI1_NPCS3	HDD CONNECTORS (J8)	PD3 as IOREADY	VDDIOP0
PD4	FIQ	DMARQ2			VDDIOP0
PD5	EBI0_NWAIT	RTS2			VDDIOM0
PD6	EBI0_NCS4/CFCS0	CTS2			VDDIOM0
PD7	EBI0_NCS5/CFCS1	RTS1			VDDIOM0
PD8	EBI0_CFCE1	CTS1	HDD CONNECTORS (J8)	EBI0_CFCE1	VDDIOM0
PD9	EBI0_CFCE2	SCK2	HDD CONNECTORS (J8)	EBI0_CFCE2	VDDIOM0
PD10		SCK1			VDDIOM0
PD11	EBI0_NCS2	TSYNC			VDDIOM0
PD12	EBI0_A23	TCLK			VDDIOM0
PD13	EBI0_A24	TPS0			VDDIOM0
PD14	EBI0_A25_CFRNW	TPS1			VDDIOM0
PD15	EBI0_NCS3/NANDCS	TPS2	NAND FLASH (MN12B)	EBI0_NCS3/NANDCS	VDDIOM0
PD16	EBI0_D16	TPK0	EBI0 SDRAM DATA BUS	D16	VDDIOM0
PD17	EBI0_D17	TPK1	EBI0 SDRAM DATA BUS	D17	VDDIOM0
PD18	EBI0_D18	TPK2	EBI0 SDRAM DATA BUS	D18	VDDIOM0
PD19	EBI0_D19	TPK3	EBI0 SDRAM DATA BUS	D19	VDDIOM0
PD20	EBI0_D20	TPK4	EBI0 SDRAM DATA BUS	D20	VDDIOM0
PD21	EBI0_D21	TPK5	EBI0 SDRAM DATA BUS	D21	VDDIOM0
PD22	EBI0_D22	TPK6	EBI0 SDRAM DATA BUS	D22	VDDIOM0
PD23	EBI0_D23	TPK7	EBI0 SDRAM DATA BUS	D23	VDDIOM0
PD24	EBI0_D24	TPK8	EBI0 SDRAM DATA BUS	D24	VDDIOM0
PD25	EBI0_D25	TPK9	EBI0 SDRAM DATA BUS	D25	VDDIOM0
PD26	EBI0_D26	TPK10	EBI0 SDRAM DATA BUS	D26	VDDIOM0
PD27	EBI0_D27	TPK11	EBI0 SDRAM DATA BUS	D27	VDDIOM0
PD28	EBI0_D28	TPK12	EBI0 SDRAM DATA BUS	D28	VDDIOM0
PD29	EBI0_D29	TPK13	EBI0 SDRAM DATA BUS	D29	VDDIOM0
PD30	EBI0_D30	TPK14	EBI0 SDRAM DATA BUS	D30	VDDIOM0
PD31	EBI0_D31	TPK15	EBI0 SDRAM DATA BUS	D31	VDDIOM0

Table 3-5. PIO Controller E

I/O Line	Peripheral A	Peripheral B	Peripheral Usage		Powered by
PE0	ISI_D0		IMAGE SENSORS CONNECTORS (J23)	ISI_D0	VDDIOP1
PE1	ISI_D1		IMAGE SENSORS CONNECTORS (J23)	ISI_D1	VDDIOP1
PE2	ISI_D2		IMAGE SENSORS CONNECTORS (J23)	ISI_D2	VDDIOP1
PE3	ISI_D3		IMAGE SENSORS CONNECTORS (J23)	ISI_D3	VDDIOP1
PE4	ISI_D4		IMAGE SENSORS CONNECTORS (J23)	ISI_D4	VDDIOP1
PE5	ISI_D5		IMAGE SENSORS CONNECTORS (J23)	ISI_D5	VDDIOP1
PE6	ISI_D6		IMAGE SENSORS CONNECTORS (J23)	ISI_D6	VDDIOP1
PE7	ISI_D7		IMAGE SENSORS CONNECTORS (J23)	ISI_D7	VDDIOP1
PE8	ISI_PCK	TIOA1	IMAGE SENSORS CONNECTORS (J23)	ISI_PCK	VDDIOP1
PE9	ISI_HSYNC	TIOB1	IMAGE SENSORS CONNECTORS (J23)	ISI_HSYNC	VDDIOP1
PE10	ISI_VSYNC	PWM3	IMAGE SENSORS CONNECTORS (J23)	ISI_VSYNC	VDDIOP1
PE11	ISI_MCK	PCK3	IMAGE SENSORS CONNECTORS (J23)	ISI_MCK	VDDIOP1
PE12		ISI_D8	IMAGE SENSORS CONNECTORS (J23)	ISI_D8	VDDIOP1
PE13		ISI_D9	IMAGE SENSORS CONNECTORS (J23)	ISI_D9	VDDIOP1
PE14		ISI_D10	IMAGE SENSORS CONNECTORS (J23)	ISI_D10	VDDIOP1
PE15		ISI_D11	IMAGE SENSORS CONNECTORS (J23)	ISI_D11	VDDIOP1
PE16			SD/MMC/DATAFLASH SOCKET (J9)	PE16 as CD (Card Detect)	VDDIOP1
PE17					VDDIOP1
PE18		TIOA0	SD/MMC SOCKET (J10)	PE18 as CD (Card Detect)	VDDIOP1
PE19		TIOB0			VDDIOP1
PE20		EBI1_NWAIT	SD/MMC/DATAFLASH SOCKET (J9)	PE20 as CKSEL (Clock Select)	VDDIOM1
PE21	ETXCK	EBI1_NANDWE	ETHERNET RMII (MN18)	ETXCK	VDDIOM1
PE22	ECRS	EBI1_NCS2/NANDCS			VDDIOM1
PE23	ETX0	EB1_NANDOE	ETHERNET RMII (MN18)	ETX0	VDDIOM1
PE24	ETX1	EBI1_NWR3/NBS3	ETHERNET RMII (MN18)	ETX1	VDDIOM1
PE25	ERX0	EBI1_NCS1/SDCS	ETHERNET RMII (MN18)	ERX0	VDDIOM1
PE26	ERX1			ERX1	VDDIOM1
PE27	ERXER	EBI1_SDCKE	ETHERNET RMII (MN18)	ERXER	VDDIOM1
PE28	ETXEN	EBI1_RAS	ETHERNET RMII (MN18)	ETXEN	VDDIOM1
PE29	EMDC	EBI1_CAS	ETHERNET RMII (MN18)	EMDC	VDDIOM1
PE30	EMDIO	EBI1_SDWE	ETHERNET RMII (MN18)	EMDIO	VDDIOM1
PE31	EF100	EBI1_SDA10	ETHERNET RMII (MN18)	PE31 as IRQ	VDDIOM1

Section 4

Configuration

4.1 Configuration Jumpers and Straps

Table 4-1. Configuration Jumpers and Straps

Designation	Default Setting	Feature
J2	Closed	Forces power on. To use the software shutdown control, J2 must be opened and the battery backup inserted in its socket.
J4-1	Closed	VDDBU jumper (1)
J4-2	Closed	VDDCORE jumper (1)
J5-1	Closed	VDDOSC jumper (1)
J5-2	Closed	VDDIOP0 jumper(1)
J5-3	Closed	VDDIOP1 jumper(1)
J5-4	Closed	VDDIOM0 jumper (1)
J5.5	Closed	VDDIOM1 jumper (1)
J5-6	Opened	Enables Boot on the internal ROM. Close to boot from NCS0.
	Closed	Enables Boot on the NCS0
J5-7	Opened	NTRST Ground
J16	Closed	Enables 120 ohms CAN bus resistance termination
J21	Closed	Enables Ethernet Auto MDIX control
J29	Closed	NAND FLash chip select
S1	Opened	Selects ICE or JTAG mode. (closed)
S2	Opened	Disables NAND FLASH write protect
S3	Opened	Disables 5V power supply on J24, J25 expansion connectors
R17	IN	Enables the ICE NTRST input
R18	IN	Enables the ICE NRST input
R13	IN	Enables the use of the Y1 crystal. If an external clock has to be used, R13 and R15 must be unsoldered and R16/J16 fitted.
R15	IN	
R30	IN	Enables the use of the MN7 SDRAM device. Needs to be removed when ETM is used.(2)
R45	IN	Enables the use of the SERIAL EEPROM SCL (PB5)
R46	IN	Enables the use of the SERIAL EEPROM SDA (PB4)
R75	IN	Enables the use of the DBGU TXD signal (PC31)

Table 4-1. Configuration Jumpers and Straps (Continued)

Designation	Default Setting	Feature
R79	IN	Enables the use of the DBGU RXD signal (PC30)
R84	IN	Enables the use of the USB CNX detection (PA25)
R76	IN	Enables the use of the RS232 COM PORT TXD signal (PA26)
R78	IN	Enables the use of the RS232 COM PORT RTS signal (PA28)
R80	IN	Enables the use of the RS232 COM PORT RXD signal (PA27)
R82	IN	Enables the use of the RS232 COM PORT CTS signal (PA29)
R87	IN	Enables the use of the CAN BUS driver RS control signal (PA26)
R89	IN	Enables the use of the CAN BUS driver CANTXRT RTS signal (PA28)
R91	IN	Enables the use of the RS232 COM PORT RXD signal (PA27)
R93	IN	Enables the use of the RS232 COM PORT CTS signal (PA29)
R112	IN	Enables the use of interrupt ETHERNET PHY (PE31)
R126	IN	Enables the use of TOUCH SCEEN CONTROLLER (PB11_SPI0_NPCS3)
R127	IN	Enables the use of TOUCH SCEEN CONTROLLER BUSY signal (PA31)
R128	IN	Enables the use of TOUCH SCEEN CONTROLLER PENIRQ (PA15_IRQ1)
TP67	N.A	GND Test point
TP68	N.A	GND Test point
TP69	N.A	GND Test point
TP70	N.A	GND Test point
TP71	N.A	0 to 3.3V analog user's input
TP72	N.A	0 to 3.3V analog user's input
TP73	N.A	AGND of TP71
TP74	N.A	AGND of TP72

Note: 1. These jumpers are provided for power consumption measurement use. By default, they are closed. To use this feature, the user has to open the strap and insert an ammeter.

2. AT91SAM9263 ETM signals [TPK0 - TPK15] are multiplexed with EBI0 signals [EBI0_D16 - EBI0_D31]. AT91SAM9263-EK EBI0 signals [EBI0_D16 - EBI0_D31] are connected to an SDRAM device (part MN7).
Having this SDRAM device enabled adds capacitance to the data line [EBI0_D16 - EBI0_D31], which leads to ETM data corruption.

You need to remove the resistor R30 to release the EBI0_NCS1_SDCS signal and put the SDRAM IOs [EBI0_D16 - EBI0_D31] in High-Z. Having these signals in High-Z removes the added capacitance; the ETM signals are no longer corrupted.

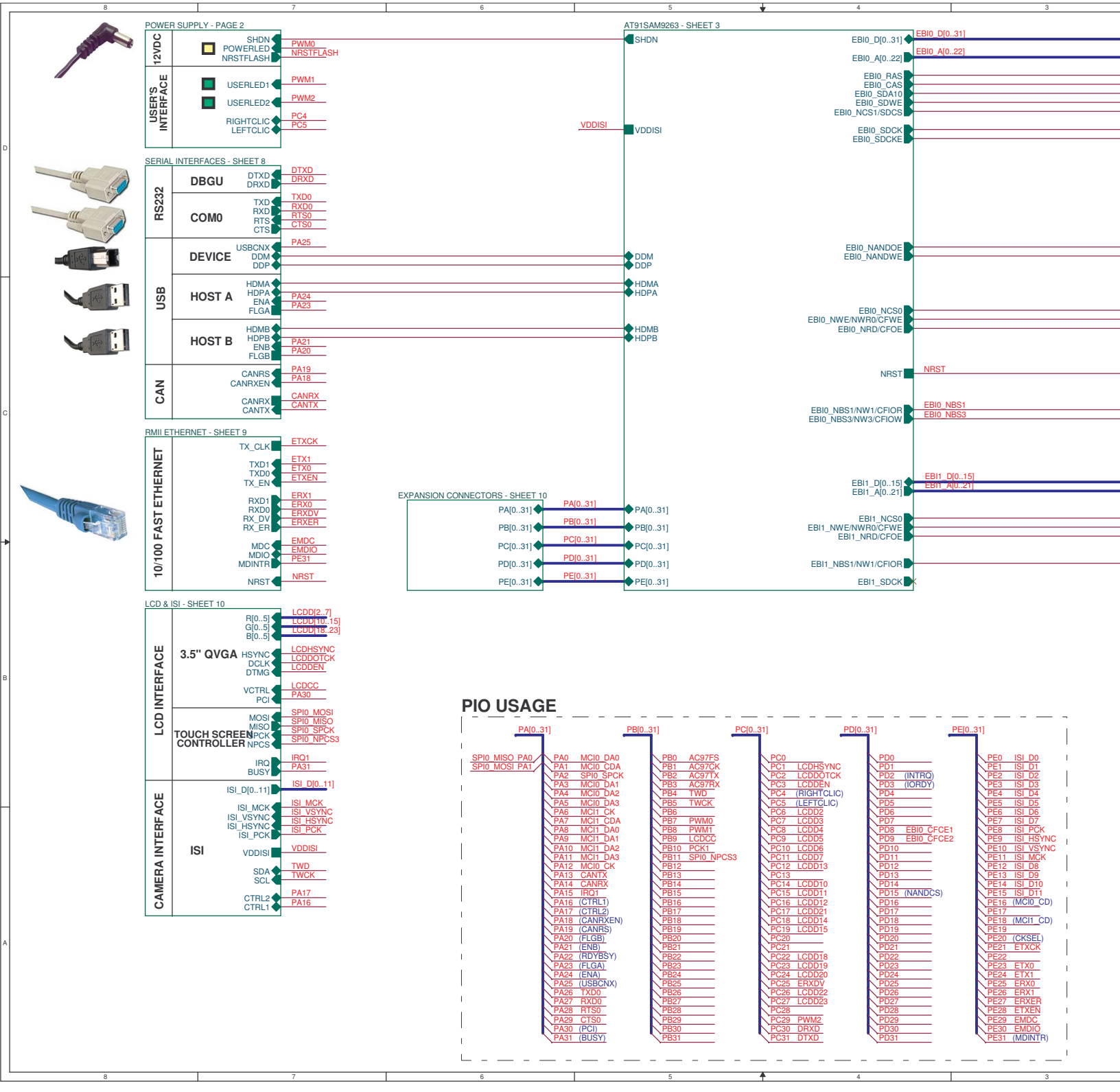
Section 5

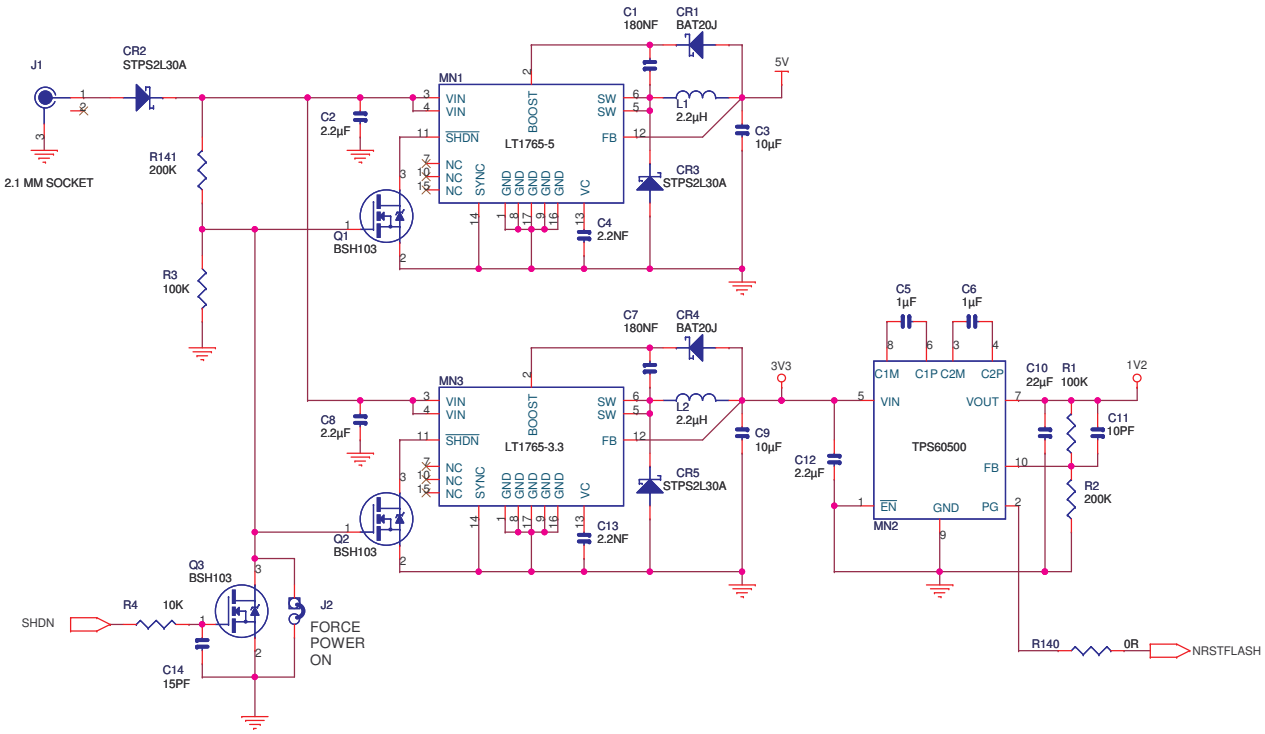
Schematics

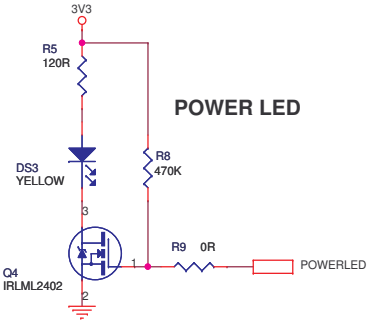
5.1 Schematics

This section contains the following schematics:

- AT91SAM9263-EK Diagram
- Power Supply
- AT91SAM9263
- EBI0 Memory
- EBI1 Memory
- Serial Memory
- Audio AC97
- Serial Interfaces
- Ethernet
- LCD and ISI
- Expansion

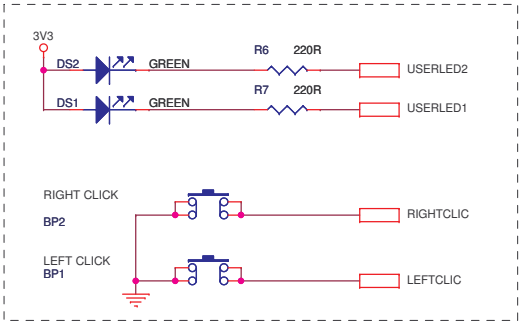

POWER SUPPLY - PAGE 2
12VDC
SHDN
POWERLED
NRSTFLASH
PWM0
NRSTFLASH
USER'S INTERFACE
USERLED1
USERLED2
PWM1
PWM2
RIGHTCLIC
LEFTCLIC
PC4
PC5
SERIAL INTERFACES - SHEET 8
RS232
DBGU
DTXD
DRXD
COM0
TXD
RXD
RTS
CTS
TXD0
RXD0
RTS0
CTS0
USB
DEVICE
USBCNX
DDM
DDP
PA25
HOST A
HDMA
HDPA
ENA
FLGA
PA24
PA23
HOST B
HDMB
HDPB
ENB
FLGB
PA21
PA20
CAN
CANRS
CANRXEN
CANRX
CANTX
PA19
PA18
CANRX
CANTX
RMII ETHERNET - SHEET 9
10/100 FAST ETHERNET
TX_CLK
TXD1
TXD0
TX_EN
RXD1
RXD0
RX_DV
RX_ER
MDC
MDIO
MDINTR
NRST
ETXCK
ETX1
ETX0
ETXEN
ERX1
ERX0
ERXDV
ERXER
EMDC
EMDIO
PE31
NRST
LCD & ISI - SHEET 10
LCD INTERFACE
3.5" QVGA
R[0..5]
G[0..5]
B[0..5]
HSYNC
DCLK
DTMG
VCTRL
PCI
LCDD[2..7]
LCDD[10..15]
LCDD[18..23]
LCDHSYNC
LCDDOTCK
LCDDEN
LCDCC
PA30
TOUCH SCREEN CONTROLLER
MOSI
MISO
SPCK
NPCS
SPI0_MOSI
SPI0_MISO
SPI0_SPCK
SPI0_NPCS3
IRQ
BUSY
IRQ1
PA31
CAMERA INTERFACE
ISI
ISI_D[0..11]
ISI_MCK
ISI_VSYNC
ISI_HSYNC
ISI_PCK
VDDISI
SDA
SCL
CTRL2
CTRL1
ISI_D[0..11]
ISI_MCK
ISI_VSYNC
ISI_HSYNC
ISI_PCK
VDDISI
TWD
TWCK
PA17
PA16
AT91SAM9263 - SHEET 3
SHDN
VDDISI
DDM
DDP
HDMA
HDPA
HDMB
HDPB
PA[0..31]
PB[0..31]
PC[0..31]
PD[0..31]
PE[0..31]
EBI0_D[0..31]
EBI0_A[0..22]
EBI0_RAS
EBI0_CAS
EBI0_SDA10
EBI0_SDWE
EBI0_NCS1/SDCS
EBI0_SDCK
EBI0_SDCKE
EBI0_NANDOE
EBI0_NANDWE
EBI0_NCS0
EBI0_NWE/NWR0/CFWE
EBI0_NRD/CFOE
NRST
EBI0_NBS1/NW1/CFIOR
EBI0_NBS3/NW3/CFIOW
EBI1_D[0..15]
EBI1_A[0..21]
EBI1_NCS0
EBI1_NWE/NWR0/CFWE
EBI1_NRD/CFOE
EBI1_NBS1/NW1/CFIOR
EBI1_SDCK
EXPANSION CONNECTORS - SHEET 10
PA[0..31]
PB[0..31]
PC[0..31]
PD[0..31]
PE[0..31]
PIO USAGE
PA[0..31]
SPI0_MISO PA0
SPI0_MOSI PA1
PA0 MCI0_DA0
PA1 MCI0_CDA
PA2 SPI0_SPCK
PA3 MCI0_DA1
PA4 MCI0_DA2
PA5 MCI0_DA3
PA6 MCI1_CK
PA7 MCI1_CDA
PA8 MCI1_DA0
PA9 MCI1_DA1
PA10 MCI1_DA2
PA11 MCI1_DA3
PA12 MCI0_CK
PA13 CANTX
PA14 CANRX
PA15 IRQ1
PA16 (CTRL1)
PA17 (CTRL2)
PA18 (CANRXEN)
PA19 (CANRS)
PA20 (FLGB)
PA21 (ENB)
PA22 (RDYBSY)
PA23 (FLGA)
PA24 (ENA)
PA25 (USBCNX)
PA26 TXD0
PA27 RXD0
PA28 RTS0
PA29 CTS0
PA30 (PCI)
PA31 (BUSY)
PB[0..31]
PB0 AC97FS
PB1 AC97CK
PB2 AC97TX
PB3 AC97RX
PB4 TWD
PB5 TWCK
PB6
PB7 PWM0
PB8 PWM1
PB9 LCDCC
PB10 PCK1
PB11 SPI0_NPCS3
PB12
PB13
PB14
PB15
PB16
PB17
PB18
PB19
PB20
PB21
PB22
PB23
PB24
PB25
PB26
PB27
PB28
PB29
PB30
PB31
PC[0..31]
PC0
PC1 LCDHSYNC
PC2 LCDDOTCK
PC3 LCDDEN
PC4 (RIGHTCLIC)
PC5 (LEFTCLIC)
PC6 LCDD2
PC7 LCDD3
PC8 LCDD4
PC9 LCDD5
PC10 LCDD6
PC11 LCDD7
PC12 LCDD13
PC13
PC14 LCDD10
PC15 LCDD11
PC16 LCDD12
PC17 LCDD21
PC18 LCDD14
PC19 LCDD15
PC20
PC21
PC22 LCDD18
PC23 LCDD19
PC24 LCDD20
PC25 ERXDV
PC26 LCDD22
PC27 LCDD23
PC28
PC29 PWM2
PC30 DRXD
PC31 DTXD
PD[0..31]
PD0
PD1
PD2 (INTRQ)
PD3 (IORDY)
PD4
PD5
PD6
PD7
PD8 EBI0_CFCE1
PD9 EBI0_CFCE2
PD10
PD11
PD12
PD13
PD14
PD15 (NANDCS)
PD16
PD17
PD18
PD19
PD20
PD21
PD22
PD23
PD24
PD25
PD26
PD27
PD28
PD29
PD30
PD31
PE[0..31]
PE0 ISI_D0
PE1 ISI_D1
PE2 ISI_D2
PE3 ISI_D3
PE4 ISI_D4
PE5 ISI_D5
PE6 ISI_D6
PE7 ISI_D7
PE8 ISI_PCK
PE9 ISI_HSYNC
PE10 ISI_VSYNC
PE11 ISI_MCK
PE12 ISI_D8
PE13 ISI_D9
PE14 ISI_D10
PE15 ISI_D11
PE16 (MCI0_CD)
PE17
PE18 (MCI1_CD)
PE19
PE20 (CKSEL)
PE21 ETXCK
PE22
PE23 ETX0
PE24 ETX1
PE25 ERX0
PE26 ERX1
PE27 ERXER
PE28 ETXEN
PE29 EMDC
PE30 EMDIO
PE31 (MDINTR)

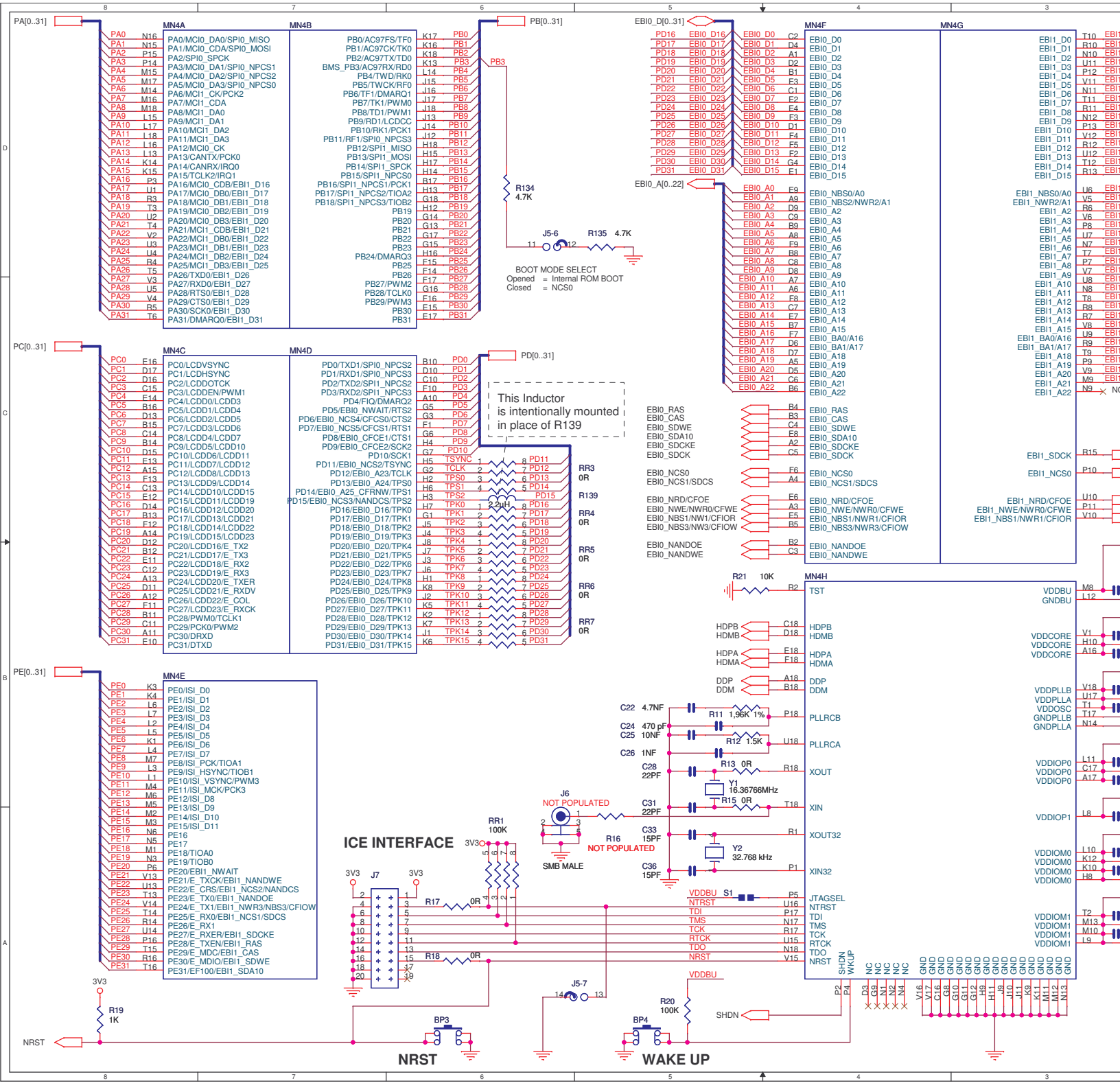


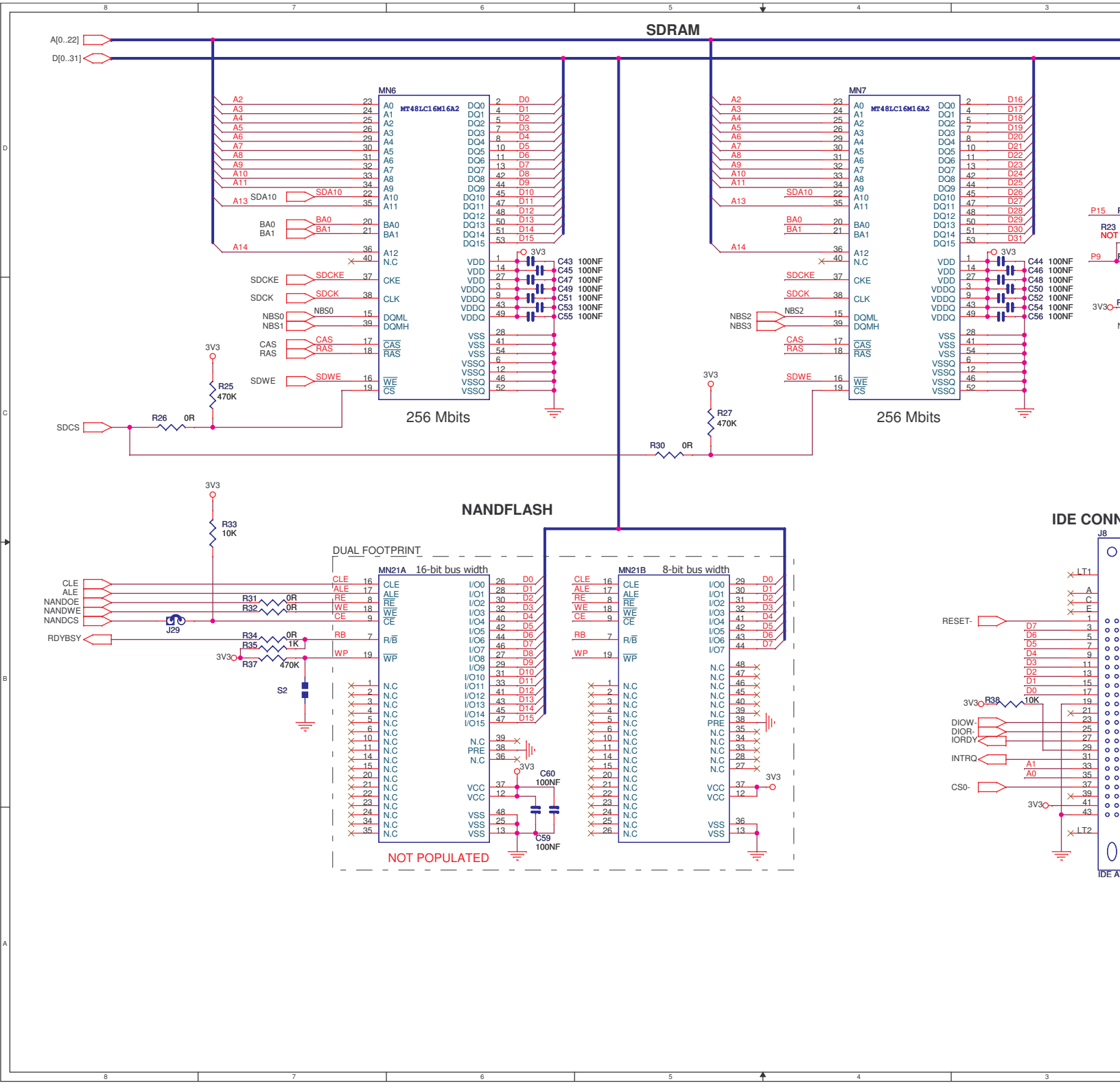


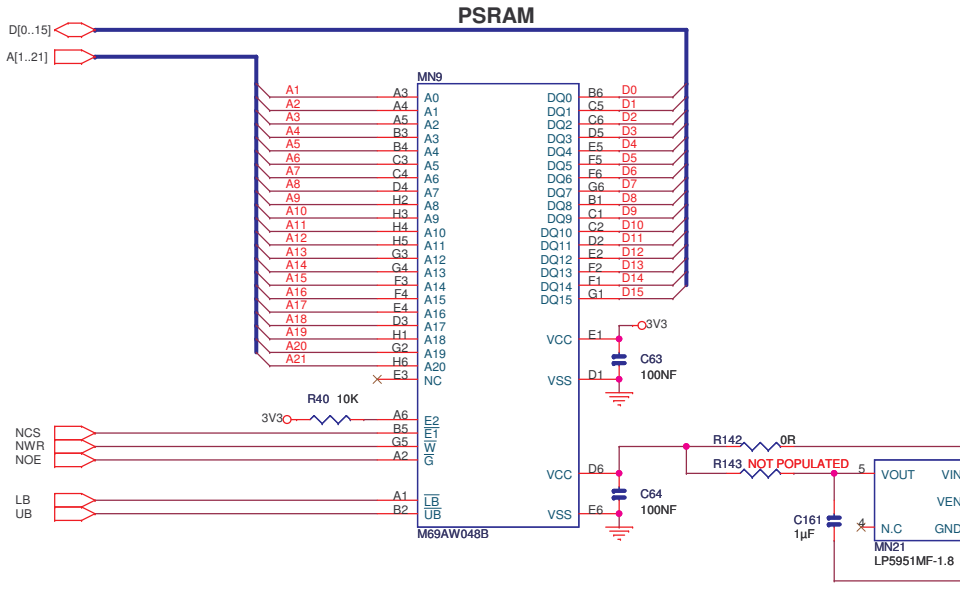
POWER LED

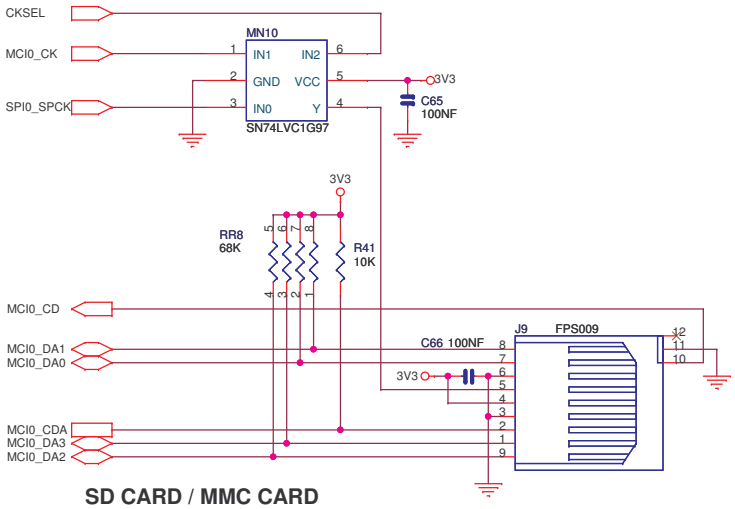
USER INTERFACE



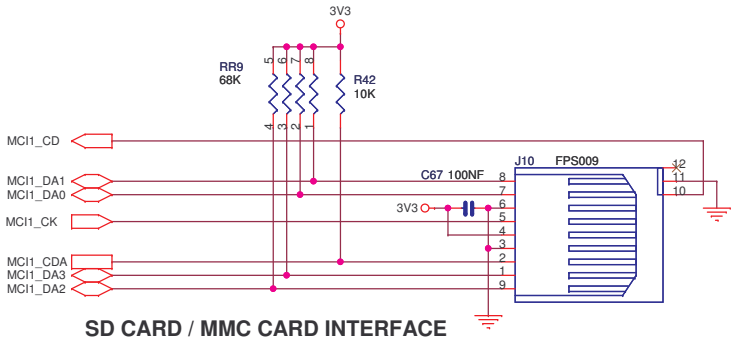

PA[0..31]
MN4A
MN4B
PB[0..31]
PB3
R134
4.7K
J5-6
R135 4.7K
BOOT MODE SELECT
Opened = Internal ROM BOOT
Closed = NCS0
EBI0_D[0..31]
EBI0_A[0..22]
MN4F
MN4G
PC[0..31]
MN4C
MN4D
PD[0..31]
This Inductor
is intentionally mounted
in place of R139
RR3
0R
R139
2.2uH
RR4
0R
RR5
0R
RR6
0R
RR7
0R
EBI0_RAS
EBI0_CAS
EBI0_SDWE
EBI0_SDA10
EBI0_SDCKE
EBI0_SDCK
EBI0_NCS0
EBI0_NCS1/SDCS
EBI0_NRD/CFOE
EBI0_NWE/NWR0/CFWE
EBI0_NBS1/NW1/CFIOR
EBI0_NBS3/NW3/CFIOW
EBI0_NANDOE
EBI0_NANDWE
EBI1_SDCK
EBI1_NCS0
EBI1_NRD/CFOE
EBI1_NWE/NWR0/CFWE
EBI1_NBS1/NWR1/CFIOR
PE[0..31]
MN4E
MN4H
R21 10K
TST
HDPB
HDMB
HDPA
HDMA
DDP
DDM
C22 4.7NF
C24 470 pF
C25 10NF
C26 1NF
R11 1.96K 1%
R12 1.5K
R13 0R
R15 0R
PLLRCB
PLLRCA
XOUT
XIN
XOUT32
XIN32
Y1
16.36766MHz
Y2
32.768 kHz
C28 22PF
C31 22PF
C33 15PF
C36 15PF
J6
NOT POPULATED
R16
NOT POPULATED
SMB MALE
RR1
100K
ICE INTERFACE
3V3
J7
R17 0R
R18 0R
JTAGSEL
NTRST
TDI
TMS
TCK
RTCK
TDO
NRST
S1
VDDBU
SHDN
WKUP
J5-7
R19
1K
R20
100K
BP3
BP4
NRST
WAKE UP
VDDBU
GNDBU
VDDCORE
VDDPLLB
VDDPLLA
VDDOSC
GNDPLLB
GNDPLLA
VDDIOP0
VDDIOP1
VDDIOM0
VDDIOM1


SDRAM
A[0..22]
D[0..31]
MN6
MT48LC16M16A2
256 Mbits
MN7
MT48LC16M16A2
256 Mbits
3V3
R25 470K
R26 0R
SDCS
R27 470K
R30 0R
NANDFLASH
DUAL FOOTPRINT
MN21A 16-bit bus width
MN21B 8-bit bus width
R33 10K
R31 0R
R32 0R
R34 0R
R35 1K
R37 470K
J29
S2
C60 100NF
C59 100NF
NOT POPULATED
IDE CONN
J8
R38 10K
IDE A

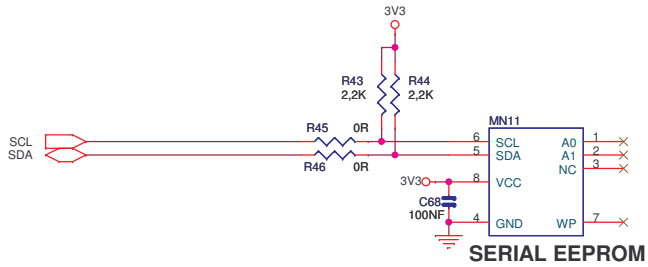

PSRAM
D[0..15]
A[1..21]
MN9
M69AW048B
R40 10K
3V3
NCS
NWR
NOE
LB
UB
C63
100NF
C64
100NF
R142 0R
R143 NOT POPULATED
C161
1µF
MN21
LP5951MF-1.8
VOUT
VIN
VEN
N.C
GND



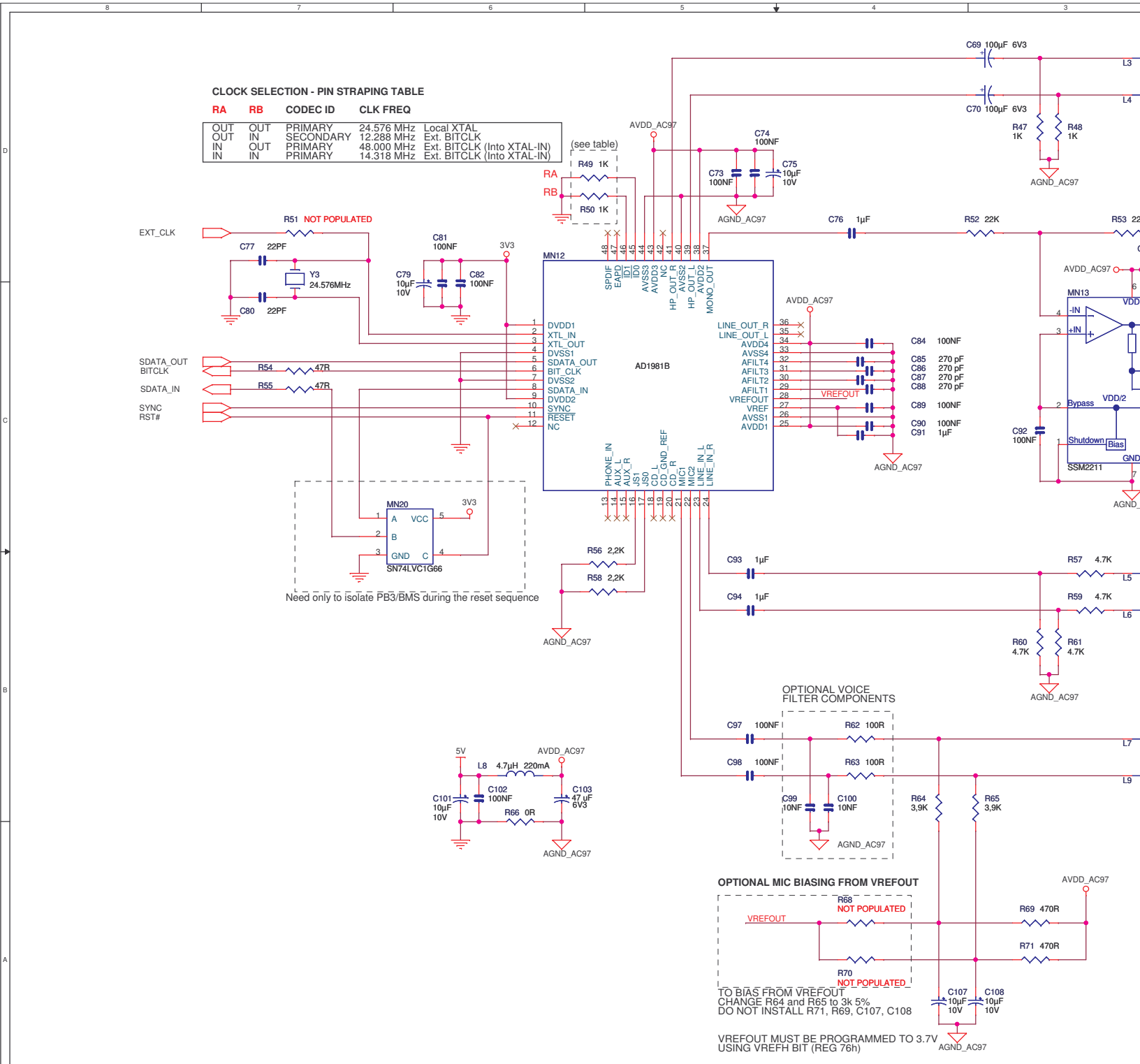
SD CARD / MMC CARD
DATAFLASH CARD INTERFACE



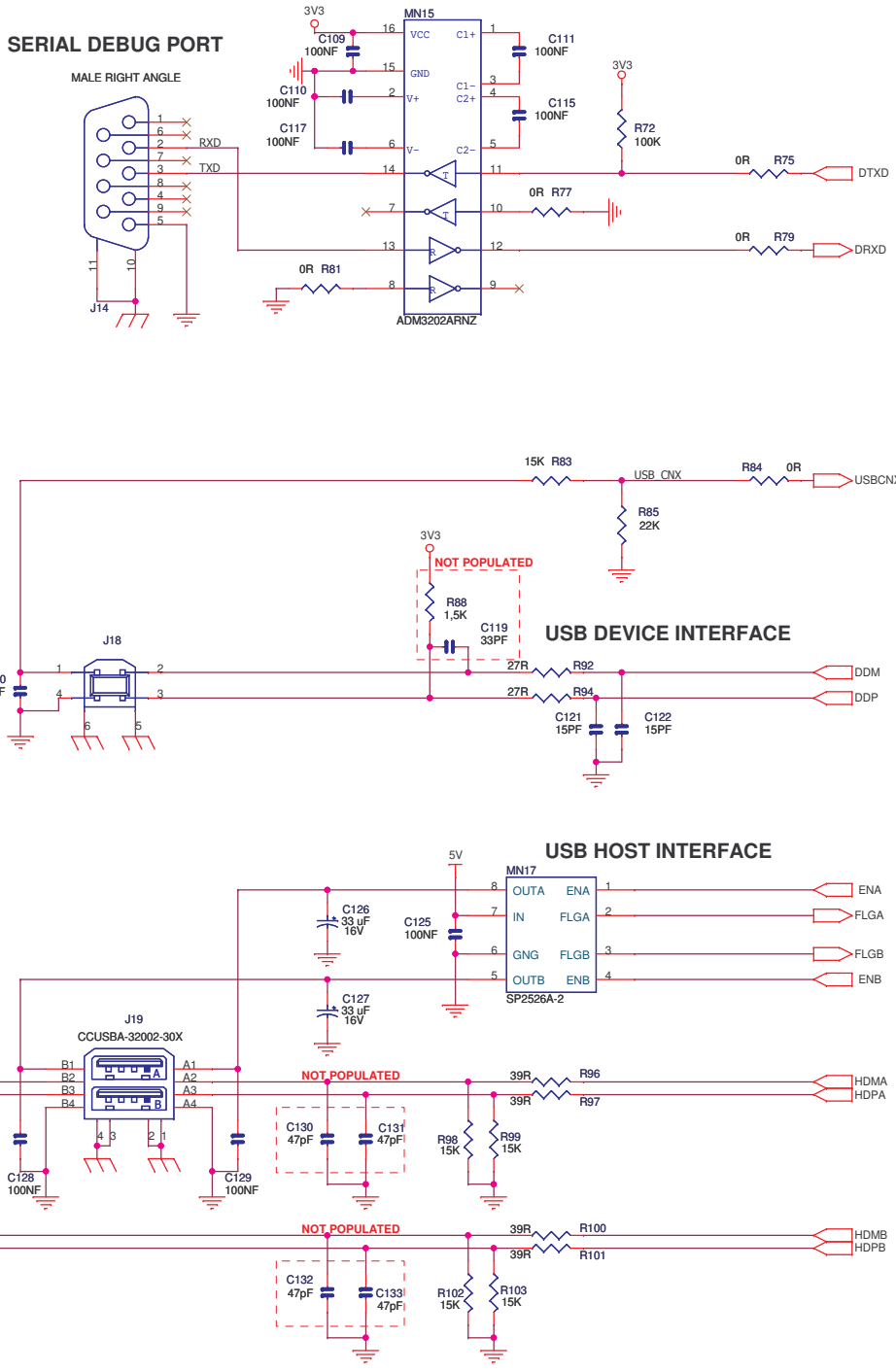
SD CARD / MMC CARD INTERFACE

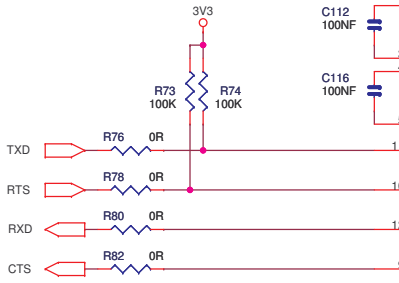


SERIAL EEPROM

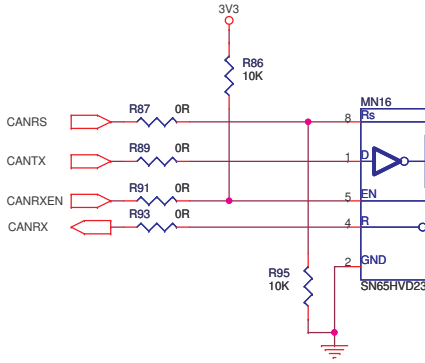

CLOCK SELECTION - PIN STRAPING TABLE
RA RB CODEC ID CLK FREQ
OUT OUT PRIMARY 24.576 MHz Local XTAL
OUT IN SECONDARY 12.288 MHz Ext. BITCLK
IN OUT PRIMARY 48.000 MHz Ext. BITCLK (Into XTAL-IN)
IN IN PRIMARY 14.318 MHz Ext. BITCLK (Into XTAL-IN)
(see table)
RA
RB
R49 1K
R50 1K
AVDD_AC97
AGND_AC97
C69 100µF 6V3
C70 100µF 6V3
C74 100NF
C73 100NF
C75 10µF 10V
R47 1K
R48 1K
L3
L4
EXT_CLK
R51 NOT POPULATED
C77 22PF
C80 22PF
Y3 24.576MHz
C81 100NF
C79 10µF 10V
C82 100NF
3V3
MN12
AD1981B
DVDD1
XTL_IN
XTL_OUT
DVSS1
SDATA_OUT
BIT_CLK
DVSS2
SDATA_IN
DVDD2
SYNC
RESET
NC
SPDIF
EAPD
TDI
TDO
AVSS3
AVDD3
NC
HP_OUT_R
AVSS2
HP_OUT_L
AVDD2
MONO_OUT
LINE_OUT_R
LINE_OUT_L
AVDD4
AVSS4
AFILT4
AFILT3
AFILT2
AFILT1
VREFOUT
VREF
AVSS1
AVDD1
PHONE_IN
AUX_L
AUX_R
JS1
JS0
CD_GND_REF
CD_R
MIC1
MIC2
LINE_IN_L
LINE_IN_R
SDATA_OUT
BITCLK
SDATA_IN
SYNC
RST#
R54 47R
R55 47R
C84 100NF
C85 270 pF
C86 270 pF
C87 270 pF
C88 270 pF
C89 100NF
C90 100NF
C91 1µF
C76 1µF
R52 22K
R53 22
MN13
-IN
+IN
VDD
Bypass
VDD/2
Shutdown
Bias
GND
SSM2211
C92 100NF
MN20
SN74LVC1G66
Need only to isolate PB3/BMS during the reset sequence
R56 2,2K
R58 2,2K
C93 1µF
C94 1µF
R57 4.7K
R59 4.7K
R60 4.7K
R61 4.7K
L5
L6
OPTIONAL VOICE FILTER COMPONENTS
C97 100NF
C98 100NF
R62 100R
R63 100R
C99 10NF
C100 10NF
R64 3,9K
R65 3,9K
L7
L9
5V
L8 4.7µH 220mA
C101 10µF 10V
C102 100NF
C103 47 uF 6V3
R66 0R
OPTIONAL MIC BIASING FROM VREFOUT
R68 NOT POPULATED
R69 470R
R71 470R
R70 NOT POPULATED
TO BIAS FROM VREFOUT
CHANGE R64 and R65 to 3k 5%
DO NOT INSTALL R71, R69, C107, C108
C107 10µF 10V
C108 10µF 10V
VREFOUT MUST BE PROGRAMMED TO 3.7V
USING VREFH BIT (REG 76h)

SERIAL DEBUG PORT





USB DEVICE INTERFACE



USB HOST INTERFACE

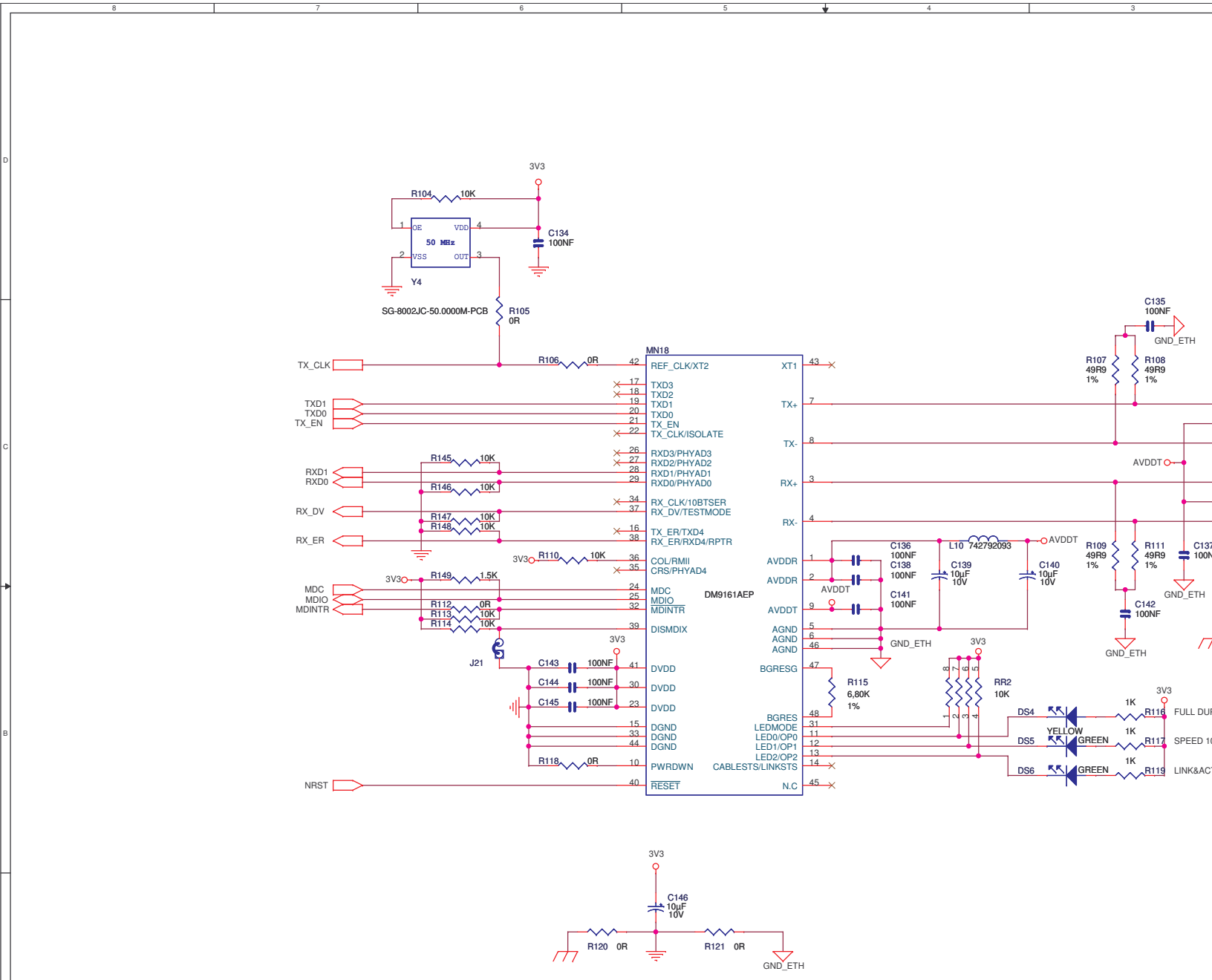
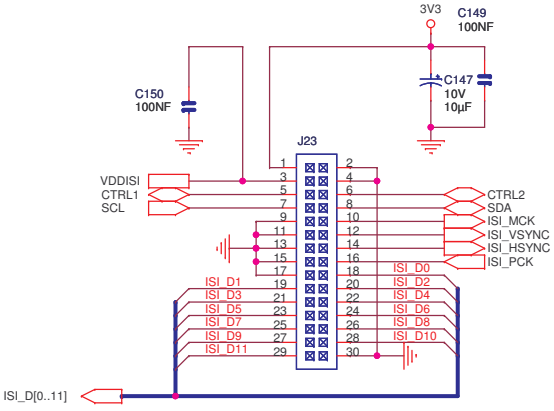
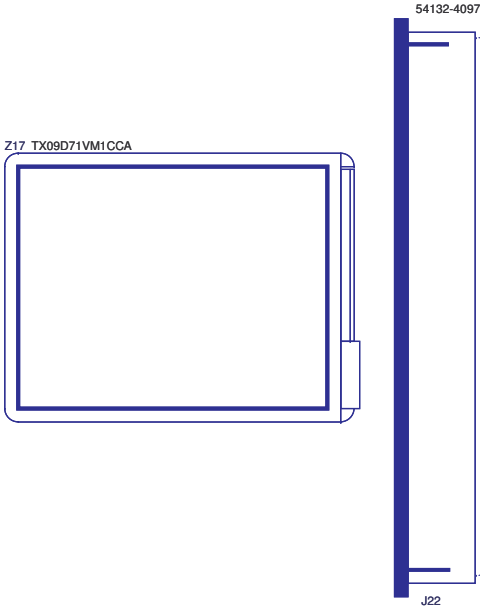

3V3
R104 10K
OE
VDD
50 MHz
VSS
OUT
C134 100NF
Y4
SG-8002JC-50.0000M-PCB
R105 0R
MN18
DM9161AEP
TX_CLK
R106 0R
REF_CLK/XT2
TXD1
TXD0
TX_EN
TXD3
TXD2
TXD1
TXD0
TX_EN
TX_CLK/ISOLATE
RXD1
RXD0
RXD3/PHYAD3
RXD2/PHYAD2
RXD1/PHYAD1
RXD0/PHYAD0
RX_DV
RX_CLK/10BTSER
RX_DV/TESTMODE
RX_ER
TX_ER/TXD4
RX_ER/RXD4/RPTR
COL/RMII
CRS/PHYAD4
MDC
MDIO
MDINTR
DISMDIX
J21
DVDD
DVDD
DVDD
DGND
DGND
DGND
PWRDWN
RESET
NRST
XT1
TX+
TX-
RX+
RX-
AVDDR
AVDDR
AVDDT
AGND
AGND
AGND
BGRESG
BGRES
LEDMODE
LED0/OP0
LED1/OP1
LED2/OP2
CABLESTS/LINKSTS
N.C
R145 10K
R146 10K
R147 10K
R148 10K
R110 10K
R149 1.5K
R112 0R
R113 10K
R114 10K
C143 100NF
C144 100NF
C145 100NF
R118 0R
R115 6,80K 1%
C135 100NF
GND_ETH
R107 49R9 1%
R108 49R9 1%
AVDDT
C136 100NF
C138 100NF
C141 100NF
L10 742792093
C139 10µF 10V
C140 10µF 10V
R109 49R9 1%
R111 49R9 1%
C142 100NF
RR2 10K
DS4
DS5
DS6
YELLOW
GREEN
GREEN
R116 1K
R117 1K
R119 1K
FULL DUP
SPEED 10
LINK&AC
C146 10µF 10V
R120 0R
R121 0R

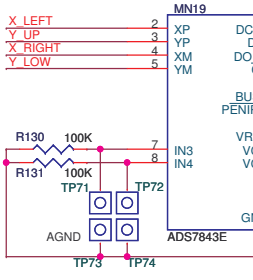
IMAGE SENSOR CONNECTOR



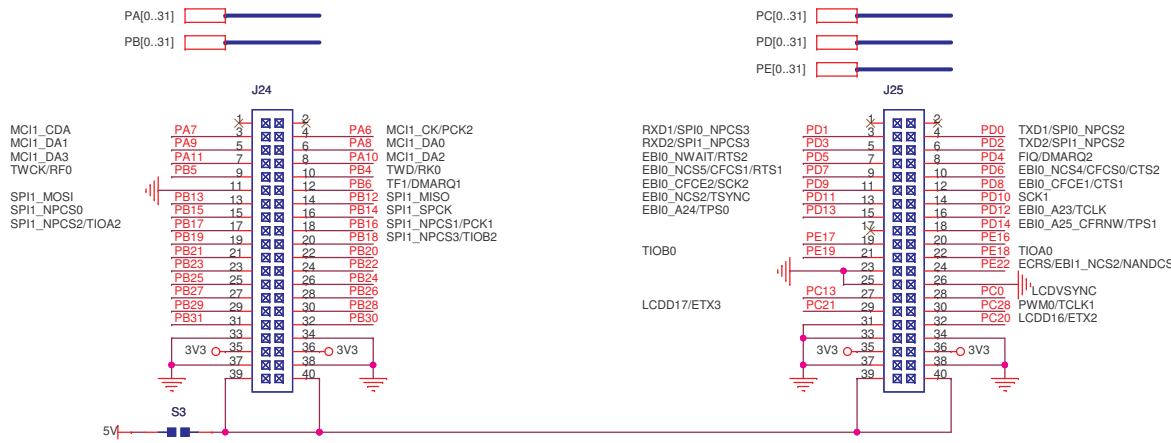
1/4 VGA TFT LCD DISPL



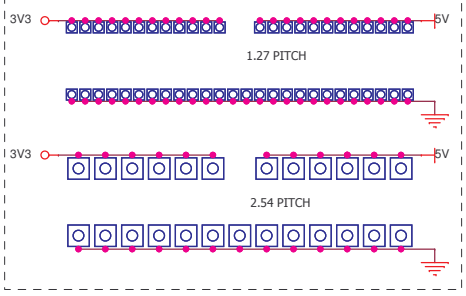
TOUCH SCREEN CONTROL



TWO USER'S ANALOG INPUTS
Full-Scale Input Span 0 to VREF



USER'S GRID AERA



Section 6

Warning

6.1 BMS Signal Sampling

The following behavior and its consequences are related to an AT91SAM9263 device issue described in the Errata section of the AT91SAM9263 datasheet (“BMS: BMS does not have correct state”). The text below is a reminder of this issue and a Workaround proposal at the board level.

Description

The BMS signal, which is multiplexed with the PB3/AC97RX PIO needs to be sampled at a High Level for the AT91SAM9263 microcontroller to boot out of the internal ROM.

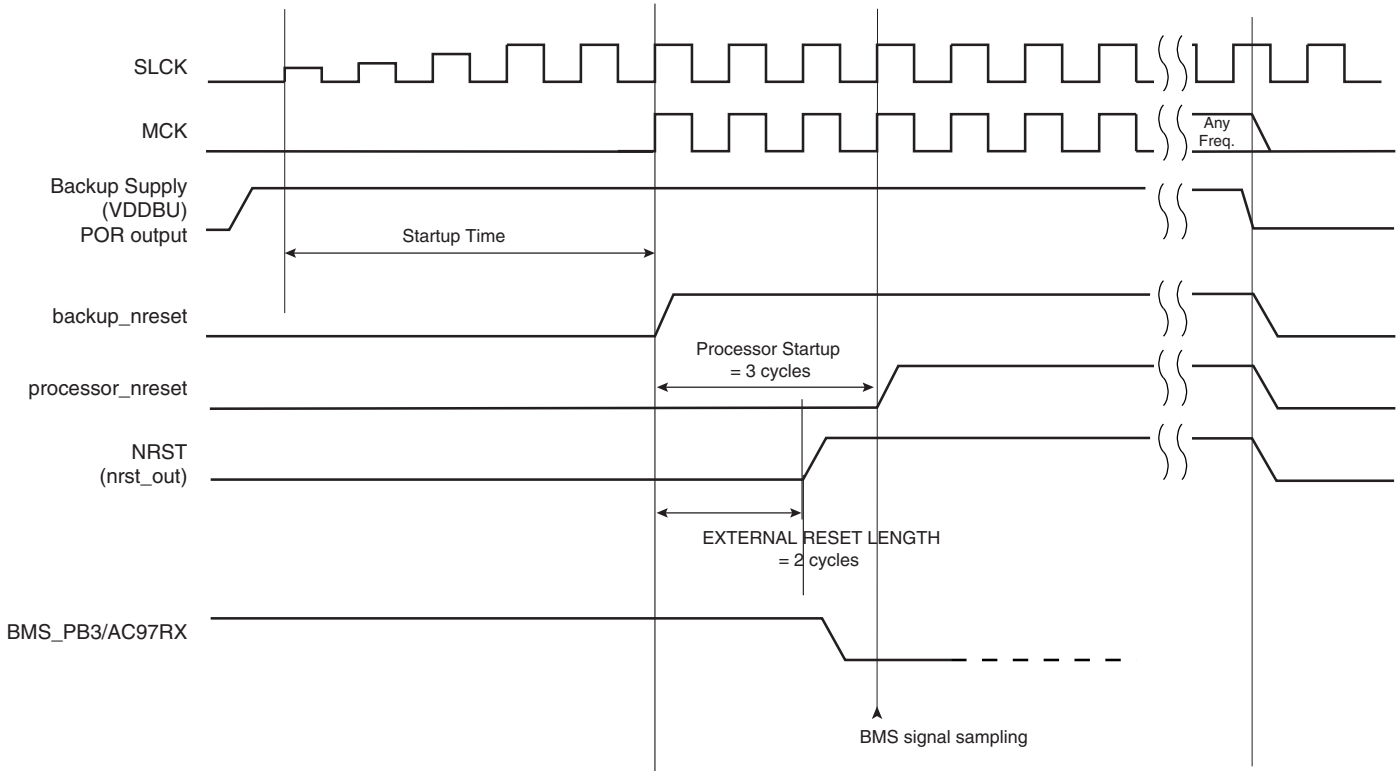
At power up, the on-board AC97 device negates its “SDATA_IN” output pin and due to this fact, the BMS_PB3/AC97RX pin needs to be isolated during the reset phase.

The MN20 gate, controlled by the NRST signal, achieves this, but with the default ERSTL value in the reset controller (refer to the RSTC section in the AT91SAM9263 datasheet for more details), when the VDDBU power supply is applied for more than 1.2 seconds before the VDDCORE power supply, the AT91SAM9263 microcontroller samples the BMS signal one Slow Clock (SLCK) cycle after the NRST signal rising (See Figure 6-1).

As a result, the BMS signal is sampled at a Low Level and the AT91SAM9263 boots out of the external EBI device connected to NCS0.

Warning

Figure 6-1. BMS Signal Sampling



Workaround:

At the first VDDBU power up or if this power supply has been shut down (J4-1 opened (VDDBU/VDDBACKUP Jumper) or the CR1225 battery cell (J3) removed or changed), the following power-up sequence has to be applied in order to boot out of the internal ROM:

1. Close J2 to force power on
2. Open J5 (Boot Mode Select Jumper)
3. Power on the board
4. Remove and replace J4-1 (VDDBU/VDDBACKUP Jumper)

Section 7

Revision History

7.1 Revision History

In the following table the most recent version of the document appears first.

Table 7-1.

Document	Comments	Change Request Ref.
6341D	PE17 and PE19 information removed from ‘Peripheral Usage’ column in Table 3-5, “PIO Controller E,” on page 3-11	6694
6341C	Section 1.5 ”NAND Flash Access Issue” on page 1-3 edited	6024
	Row R30 and note (2) added to Table 4-1 on page 4-1	6057
6341B	Section 1.2, ” How to Identify the Kit BOM Revision”, added to this user guide. Section 1.3, ” How to Identify the PCB Revision”, updated. Section 1.4, ” How to Identify the SAM9263 Silicon Revision”, added to this user guide Section 1.5, ” NAND Flash Access Issue”, added to this user guide.	5626
	Section 5.1, ” Schematics”, updated with rev C schematics. (“Audio AC97” schematic updated)	5626 5082
	Table 4-1, “Configuration Jumpers and Straps,” on page 4-1, added J5-7 and J29	5391
6341A	First issue.	

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
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