Features

- Core
  - ARM926EJ-S™ ARM® Thumb® Processor running up to 400 MHz @ 1.0V +/- 10%
  - 16 Kbytes Data Cache, 16 Kbytes Instruction Cache, Memory Management Unit
- Memories
  - One 128-Kbyte internal ROM embedding bootstrap routine
  - One 32-Kbyte internal SRAM, single-cycle access at system speed
  - 32-bit External Bus Interface supporting 8-bank DDR2/LPDDR, SDR/LPSDR, Static Memories
  - MLC/SLC NAND Controller, with up to 24-bit Programmable Multi-bit Error Correcting Code (PMECC)
- System running up to 133 MHz
  - Power-on Reset, Reset Controller, Shut Down Controller, Periodic Interval Timer, Watchdog Timer and Real Time Clock
  - Boot Mode Select Option, Remap Command
  - Internal Low Power 32 kHz RC and Fast 12 MHz RC Oscillators
  - Selectable 32768 Hz Low-power Oscillator, 16 MHz Oscillator, one PLL for the system and one PLL optimized for USB
  - Six 32-bit-layer AHB Bus Matrix
  - Dual Peripheral Bridge with dedicated programmable clock
  - One dual port 8-channel DMA Controller
  - Advanced Interrupt Controller and Debug Unit
  - Two Programmable External Clock Signals
- Low Power Mode
  - Shut Down Controller with four 32-bit battery backup registers
  - Clock Generator and Power Management Controller
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
- Peripherals
  - LCD Controller
  - USB Device Full Speed with dedicated On-Chip Transceiver
  - USB Host Full Speed with dedicated On-Chip Transceiver
  - One High speed SD card and SDIO Host Controller
  - Two Master/Slave Serial Peripheral Interfaces
  - Two Three-channel 32-bit Timer/Counters
  - One Synchronous Serial Controller
  - One Four-channel 16-bit PWM Controller
  - Two Two-wire Interfaces
  - Four USARTs plus two UARTs
  - One 12-channel 10-bit Analog-to-Digital Converter with up to 5-wire resistive Touch screen support
- Customizing
  - TRNG True Random Number Generator compliant with NIST Special Publication 800-22
  - 320 Fuse bits for device configuration, including JTAG disable and forced boot from the on-chip ROM
- I/O
  - Four 32-bit Parallel Input/Output Controllers
  - 105 Programmable I/O Lines Multiplexed with up to Three Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line, optional Schmitt Trigger input
  - Individually Programmable Open-drain, Pull-up and Pull-down Resistor, Synchronous Output
  - Package: 217-ball BGA, pitch 0.8 mm

AT91SAM ARM-based Embedded MPU

SAM9N12

Summary

11096AS–ATARM–4-Oct-11

1. Description

The ARM926EJ-S based SAM9N12 features the frequently requested combination of user interface functionality and high data rate connectivity, including LCD Controller, resistive touchscreen, multiple UARTs, SPI, I2C, full speed USB Host and Device and SDIO.

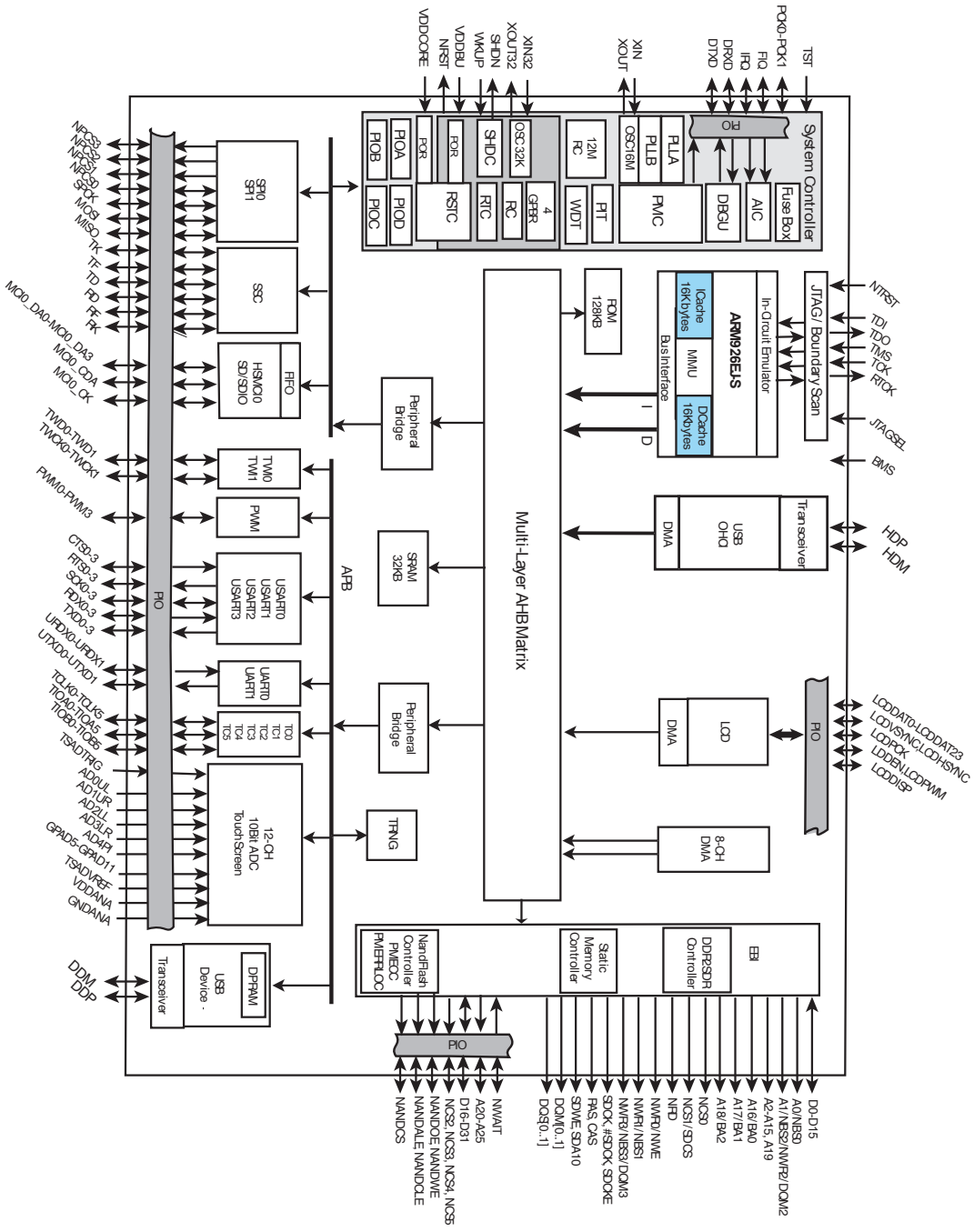
The SAM9N12 supports the latest generation of LPDDR/DDR2 and NAND Flash memory interfaces for program and data storage. An internal 125 MHz multi-layer bus architecture associated with 8 DMA channels, a distributed memory including a 32-Kbyte SRAM, sustains the high bandwidth required by the processor and the high speed peripherals.

The I/Os support 1.8V or 3.3V operation, which are independently configurable for the memory interface and peripheral I/Os. This feature completely eliminates the need for any external level shifters. In addition it supports 0.8 ball pitch package for low cost PCB manufacturing.

The SAM9N12 power management controller features efficient clock gating and a battery backup section minimizing power consumption in active and standby modes.

2. Block Diagram

Figure 2-1. SAM9N12 Block Diagram



3. Signal Description

Table 3-1 gives details on the signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level
Clocks, Oscillators and PLLs			
XIN	Main Oscillator Input	Input	
XOUT	Main Oscillator Output	Output	
XIN32	Slow Clock Oscillator Input	Input	
XOUT32	Slow Clock Oscillator Output	Output	
VBG	Bias Voltage Reference for USB	Analog	
PCK0 - PCK1	Programmable Clock Output	Output	
Shutdown, Wakeup Logic			
SHDN	Shut-Down Control	Output	
WKUP	Wake-Up Input	Input	
ICE and JTAG			
TCK	Test Clock	Input	
TDI	Test Data In	Input	
TDO	Test Data Out	Output	
TMS	Test Mode Select	Input	
JTAGSEL	JTAG Selection	Input	
RTCK	Return Test Clock	Output	
Reset/Test			
NRST	Microcontroller Reset	I/O	Low
NTRST	Test Reset Signal	Input	
BMS	Boot Mode Select	Input	
Debug Unit - DBGU			
DRXD	Debug Receive Data	Input	
DTXD	Debug Transmit Data	Output	
Advanced Interrupt Controller - AIC			
IRQ	External Interrupt Input	Input	
FIQ	Fast Interrupt Input	Input	
PIO Controller - PIOA - PIOB - PIOC - PIOD			
PA0 - PA31	Parallel IO Controller A	I/O	
PB0 - PB18	Parallel IO Controller B	I/O	
PC0 - PC31	Parallel IO Controller C	I/O	
PD0 - PD21	Parallel IO Controller D	I/O	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level
External Bus Interface - EBI			
D0 -D15	Data Bus	I/O	
D16 -D31	Data Bus	I/O	
A0 - A25	Address Bus	Output	
NWAIT	External Wait Signal	Input	Low
Static Memory Controller - SMC			
NCS0 - NCS5	Chip Select Lines	Output	Low
NWR0 - NWR3	Write Signal	Output	Low
NRD	Read Signal	Output	Low
NWE	Write Enable	Output	Low
NBS0 - NBS3	Byte Mask Signal	Output	Low
NAND Flash Support			
NFD0-NFD15	NAND Flash I/O	I/O	
NANDCS	NAND Flash Chip Select	Output	Low
NANDOE	NAND Flash Output Enable	Output	Low
NANDWE	NAND Flash Write Enable	Output	Low
DDR2/SDRAM/LPDDR Controller			
SDCK,#SDCK	DDR2/SDRAM differential clock	Output	
SDCKE	DDR2/SDRAM Clock Enable	Output	High
SDCS	DDR2/SDRAM Controller Chip Select	Output	Low
BA[0..2]	Bank Select	Output	Low
SDWE	DDR2/SDRAM Write Enable	Output	Low
RAS - CAS	Row and Column Signal	Output	Low
SDA10	SDRAM Address 10 Line	Output	
DQS[0..1]	Data Strobe	I/O	
DQM[0..3]	Write Data Mask	Output	
High Speed Multimedia Card Interface - HSMCI			
MCI_CK	Multimedia Card Clock	I/O	
MCI_CDA	Multimedia Card Slot Command	I/O	
MCI_DA0 - MCI_DA7	Multimedia Card Slot Data	I/O	
Universal Synchronous Asynchronous Receiver Transmitter- USARTx			
SCKx	USARTx Serial Clock	I/O	
TXDx	USARTx Transmit Data	Output	
RXDx	USARTx Receive Data	Input	
RTSx	USARTx Request To Send	Output	
CTSx	USARTx Clear To Send	Input	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level
Universal Asynchronous Receiver Transmitter - UARTx			
UTXDx	UARTx Transmit Data	Output	
URXDx	UARTx Receive Data	Input	
Synchronous Serial Controller - SSC			
TD	SSC Transmit Data	Output	
RD	SSC Receive Data	Input	
TK	SSC Transmit Clock	I/O	
RK	SSC Receive Clock	I/O	
TF	SSC Transmit Frame Sync	I/O	
RF	SSC Receive Frame Sync	I/O	
Timer Counter - TCx x=0..5			
TCLKx	TC Channel x External Clock Input	Input	
TIOAx	TC Channel x I/O Line A	I/O	
TIOBx	TC Channel x I/O Line B	I/O	
Serial Peripheral Interface - SPIx			
SPIx_MISO	Master In Slave Out	I/O	
SPIx_MOSI	Master Out Slave In	I/O	
SPIx_SPCK	SPI Serial Clock	I/O	
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low
SPIx_NPCS1- SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low
Two-wire Interface -TWIx			
TWDx	Two-wire Serial Data	I/O	
TWCKx	Two-wire Serial Clock	I/O	
Pulse Width Modulation Controller- PWM			
PWM0 - PWM3	Pulse Width Modulation Output	Output	
USB Device Full Speed Port - UDP			
DDP	USB Device Data +	Analog	
DDM	USB Device Data -	Analog	
USB Host Full Speed Port - UHP			
HDP	USB Host Data +	Analog	
HDM	USB Host Data -	Analog	
LCD Controller - LCDC			
LCDDAT 0-23	LCD Data Bus	Output	
LCDVSYNC	LCD Vertical Synchronization	Output	
LCDHSYNC	LCD Horizontal Synchronization	Output	
LCDPCK	LCD Pixel Clock	Output	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level
LCDDEN	LCD Data Enable	Output	
LCDPWM	LCD Contrast Control	Output	
LCDDISP	LCD Display Enable	Output	
Analog-to-Digital Converter - ADC			
$AD0_{XP\_UL}$	Top/Upper Left Channel	Analog	
$AD1_{XM\_UR}$	Bottom/Upper Right Channel	Analog	
$AD2_{YP\_LL}$	Right/Lower Left Channel	Analog	
$AD3_{YM\_SENSE}$	Left/Sense Channel	Analog	
$AD4_{LR}$	Lower Right Channel	Analog	
AD5-AD11	7 Analog Inputs	Analog	
ADTRG	ADC Trigger	Input	
ADVREF	ADC Reference	Analog	

Table 3-2. SAM9N12 I/O Type Description

I/O Type	Signal Name	Voltage Range	Analog	Pull-up	Pull-up Value (Ohm)	Pull-down	Pull-down Value (Ohm)	Schmitt Trigger
GPIO	all PIO lines except following	1.65-3.6V		switchable	50-100K	switchable	50-100K	switchable
GPIO_CLK	MCICK, SPI0SPCK, SPI1SPCK	1.65-3.6V		switchable	50-100K	switchable	50-100K	switchable
GPIO_CLK2	LCDDOTCK	1.65-3.6V		switchable	50-100K	switchable	50-100K	switchable
GPIO_ANA	ADx, GPADx	3.0-3.6V	I	switchable	50-100K			switchable
EBI	all Data lines (Input/output) except the following	1.65-1.95V, 3.0-3.6V		switchable	50-100K	switchable	50-100K	
EBI_O	all Address and control lines (output only) except the following	1.65-1.95V, 3.0-3.6V		Reset State	50-100K	Reset State	50-100K	
EBI_CLK	SDCK, #SDCK	1.65-1.95V, 3.0-3.6V						
RSTJTAG	NRST, NTRST, BMS, TCK, TDI, TMS, TDO, RTCK	3.0-3.6V		Reset State	100K	Reset State	100K	Reset State
SYSC	WKUP, SHDN, JTAGSEL, SHDN	1.65-3.6V		Reset State	100k	Reset State	15K	Reset State
VBG	VBG	0.9-1.1V	I					
USBFS	HDP, HDM, DDP, DDM	3.0-3.6V	I/O					
CLOCK	XIN, XOUT, XIN32, XOUT32	1.65-3.6V	I/O					

When “Reset State” is stated, the configuration is defined by the “Reset State” column of the Pin Description table.

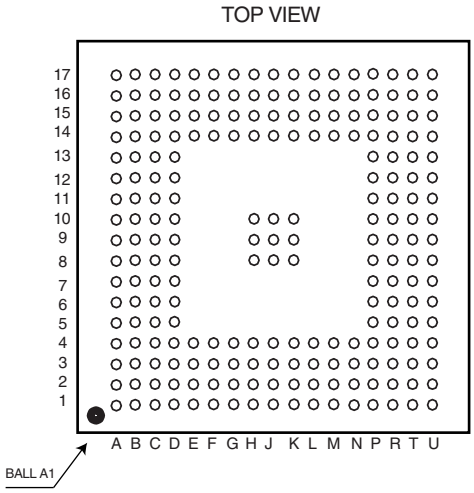
4. Package and Pinout

The SAM9N12 is available in 217-ball BGA.

4.1 Mechanical Overview of the 217-ball BGA Package

Figure 4-1 shows the orientation of the 217-ball BGA Package.

Figure 4-1. Orientation of the 217-ball BGA Package



4.2 217-ball BGA Package Pinout

Table 4-1. BGA217 Pin Description

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
T3	VDDIOP0	GPIO	PA0	I/O			TXD0	O	SPI1_NPCS1	O			PIO, I, PU, ST
U2	VDDIOP0	GPIO	PA1	I/O			RXD0	I	SPI0_NPCS2	O			PIO, I, PU, ST
U3	VDDIOP0	GPIO	PA2	I/O			RTS0	O					PIO, I, PU, ST
P4	VDDIOP0	GPIO	PA3	I/O			CTS0	I					PIO, I, PU, ST
T4	VDDIOP0	GPIO	PA4	I/O			SCK0	I/O					PIO, I, PU, ST
U4	VDDIOP0	GPIO	PA5	I/O			TXD1	O					PIO, I, PU, ST
P5	VDDIOP0	GPIO	PA6	I/O			RXD1	I					PIO, I, PU, ST
R4	VDDIOP0	GPIO	PA7	I/O			TXD2	O	SPI0_NPCS1	O			PIO, I, PU, ST
U6	VDDIOP0	GPIO	PA8	I/O			RXD2	I	SPI1_NPCS0	I/O			PIO, I, PU, ST
R5	VDDIOP0	GPIO	PA9	I/O			DRXD	I					PIO, I, PU, ST
R6	VDDIOP0	GPIO	PA10	I/O			DTXD	O					PIO, I, PU, ST
T5	VDDIOP0	GPIO	PA11	I/O			SPI0_MISO	I/O	MCDA4	I/O			PIO, I, PU, ST
T6	VDDIOP0	GPIO	PA12	I/O			SPI0_MOSI	I/O	MCDA5	I/O			PIO, I, PU, ST
U5	VDDIOP0	GPIO_CLK	PA13	I/O			SPI0_SPCK	I/O	MCDA6	I/O			PIO, I, PU, ST
U7	VDDIOP0	GPIO	PA14	I/O			SPI0_NPCS0	I/O	MCDA7	I/O			PIO, I, PU, ST
T7	VDDIOP0	GPIO	PA15	I/O			MCDA0	I/O					PIO, I, PU, ST

Table 4-1. BGA217 Pin Description (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
R7	VDDIOP0	GPIO	PA16	I/O			MCCDA	I/O					PIO, I, PU, ST
U8	VDDIOP0	GPIO_CLK	PA17	I/O			MCCK	I/O					PIO, I, PU, ST
P8	VDDIOP0	GPIO	PA18	I/O			MCDA1	I/O					PIO, I, PU, ST
T8	VDDIOP0	GPIO	PA19	I/O			MCDA2	I/O					PIO, I, PU, ST
R8	VDDIOP0	GPIO	PA20	I/O			MCDA3	I/O					PIO, I, PU, ST
U9	VDDIOP0	GPIO	PA21	I/O			TIOA0	I/O	SPI1_MISO	I/O			PIO, I, PU, ST
U10	VDDIOP0	GPIO	PA22	I/O			TIOA1	I/O	SPI1_MOSI	I/O			PIO, I, PU, ST
T9	VDDIOP0	GPIO_CLK	PA23	I/O			TIOA2	I/O	SPI1_SPCK	I/O			PIO, I, PU, ST
U11	VDDIOP0	GPIO	PA24	I/O			TCLK0	I	TK	I/O			PIO, I, PU, ST
T10	VDDIOP0	GPIO	PA25	I/O			TCLK1	I	TF	I/O			PIO, I, PU, ST
R9	VDDIOP0	GPIO	PA26	I/O			TCLK2	I	TD	O			PIO, I, PU, ST
U12	VDDIOP0	GPIO	PA27	I/O			TIOB0	I/O	RD	I			PIO, I, PU, ST
T11	VDDIOP0	GPIO	PA28	I/O			TIOB1	I/O	RK	I/O			PIO, I, PU, ST
U13	VDDIOP0	GPIO	PA29	I/O			TIOB2	I/O	RF	I/O			PIO, I, PU, ST
R10	VDDIOP0	GPIO	PA30	I/O			TWD0	I/O	SPI1_NPCS3	O			PIO, I, PU, ST
T12	VDDIOP0	GPIO	PA31	I/O			TWCK0	O	SPI1_NPCS2	O			PIO, I, PU, ST
E4	VDDANA	GPIO	PB0	I/O					RTS2	O			PIO, I, PU, ST
F3	VDDANA	GPIO	PB1	I/O					CTS2	I			PIO, I, PU, ST
F4	VDDANA	GPIO	PB2	I/O					SCK2	I/O			PIO, I, PU, ST
F2	VDDANA	GPIO	PB3	I/O					SPI0_NPCS3	O			PIO, I, PU, ST
G4	VDDANA	GPIO_CLK	PB4	I/O									PIO, I, PU, ST
G3	VDDANA	GPIO	PB5	I/O									PIO, I, PU, ST
D2	VDDANA	GPIO_ANA	PB6	I/O	AD7	I							PIO, I, PU, ST
E2	VDDANA	GPIO_ANA	PB7	I/O	AD8	I							PIO, I, PU, ST
D1	VDDANA	GPIO_ANA	PB8	I/O	AD9	I							PIO, I, PU, ST
F1	VDDANA	GPIO_ANA	PB9	I/O	AD10	I			PCK1	O			PIO, I, PU, ST
E1	VDDANA	GPIO_ANA	PB10	I/O	AD11	I			PCK0	O			PIO, I, PU, ST
A1	VDDANA	GPIO_ANA	PB11	I/O	AD0	I			PWM0	O			PIO, I, PU, ST
C3	VDDANA	GPIO_ANA	PB12	I/O	AD1	I			PWM1	O			PIO, I, PU, ST
B1	VDDANA	GPIO_ANA	PB13	I/O	AD2	I			PWM2	O			PIO, I, PU, ST
C2	VDDANA	GPIO_ANA	PB14	I/O	AD3	I			PWM3	O			PIO, I, PU, ST
D3	VDDANA	GPIO_ANA	PB15	I/O	AD4	I							PIO, I, PU, ST
C1	VDDANA	GPIO_ANA	PB16	I/O	AD5	I				I			PIO, I, PU, ST
E3	VDDANA	GPIO_ANA	PB17	I/O	AD6	I				I			PIO, I, PU, ST
D4	VDDANA	GPIO	PB18	I/O			IRQ	I	ADTRG	I			PIO, I, PU, ST
G2	VDDIOP1	GPIO	PC0	I/O			LCDDAT0	O			TWD1	I/O	PIO, I, PU, ST
G1	VDDIOP1	GPIO	PC1	I/O			LCDDAT1	O			TWCK1	O	PIO, I, PU, ST
H4	VDDIOP1	GPIO	PC2	I/O			LCDDAT2	O			TIOA3	I/O	PIO, I, PU, ST

Table 4-1. BGA217 Pin Description (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
J1	VDDIOP1	GPIO	PC3	I/O			LCDDAT3	O			TIOB3	I/O	PIO, I, PU, ST
H3	VDDIOP1	GPIO	PC4	I/O			LCDDAT4	O			TCLK3	I	PIO, I, PU, ST
J3	VDDIOP1	GPIO	PC5	I/O			LCDDAT5	O			TIOA4	I/O	PIO, I, PU, ST
H2	VDDIOP1	GPIO	PC6	I/O			LCDDAT6	O			TIOB4	I/O	PIO, I, PU, ST
H1	VDDIOP1	GPIO	PC7	I/O			LCDDAT7	O			TCLK4	I	PIO, I, PU, ST
K2	VDDIOP1	GPIO	PC8	I/O			LCDDAT8	O			UTXD0	O	PIO, I, PU, ST
J2	VDDIOP1	GPIO	PC9	I/O			LCDDAT9	O			URXD0	I	PIO, I, PU, ST
L1	VDDIOP1	GPIO	PC10	I/O			LCDDAT10	O			PWM0	O	PIO, I, PU, ST
K1	VDDIOP1	GPIO	PC11	I/O			LCDDAT11	O			PWM1	O	PIO, I, PU, ST
L2	VDDIOP1	GPIO	PC12	I/O			LCDDAT12	O			TIOA5	I/O	PIO, I, PU, ST
K3	VDDIOP1	GPIO	PC13	I/O			LCDDAT13	O			TIOB5	I/O	PIO, I, PU, ST
M1	VDDIOP1	GPIO	PC14	I/O			LCDDAT14	O			TCLK5	I	PIO, I, PU, ST
M2	VDDIOP1	GPIO_CLK	PC15	I/O			LCDDAT15	O			PCK0	O	PIO, I, PU, ST
K4	VDDIOP1	GPIO	PC16	I/O			LCDDAT16	O			UTXD1	O	PIO, I, PU, ST
M3	VDDIOP1	GPIO	PC17	I/O			LCDDAT17	O			URXD1	I	PIO, I, PU, ST
N1	VDDIOP1	GPIO	PC18	I/O			LCDDAT18	O			PWM0	O	PIO, I, PU, ST
N2	VDDIOP1	GPIO	PC19	I/O			LCDDAT19	O			PWM1	O	PIO, I, PU, ST
N3	VDDIOP1	GPIO	PC20	I/O			LCDDAT20	O			PWM2	O	PIO, I, PU, ST
P1	VDDIOP1	GPIO	PC21	I/O			LCDDAT21	O			PWM3	O	PIO, I, PU, ST
P2	VDDIOP1	GPIO	PC22	I/O			LCDDAT22	O	TXD3	O			PIO, I, PU, ST
P3	VDDIOP1	GPIO	PC23	I/O			LCDDAT23	O	RXD3	I			PIO, I, PU, ST
R1	VDDIOP1	GPIO	PC24	I/O			LCDDISP	O	RTS3	O			PIO, I, PU, ST
R3	VDDIOP1	GPIO	PC25	I/O					CTS3	I			PIO, I, PU, ST
R2	VDDIOP1	GPIO	PC26	I/O			LCDPWM	O	SCK3	I/O			PIO, I, PU, ST
T1	VDDIOP1	GPIO	PC27	I/O			LCDVSYNC	O			RTS1	O	PIO, I, PU, ST
M4	VDDIOP1	GPIO	PC28	I/O			LCDHSYNC	O			CTS1	I	PIO, I, PU, ST
N4	VDDIOP1	GPIO_CLK	PC29	I/O			LCDDEN	O			SCK1	I/O	PIO, I, PU, ST
T2	VDDIOP1	GPIO_CLK2	PC30	I/O			LCDPCK	O					PIO, I, PU, ST
U1	VDDIOP1	GPIO	PC31	I/O			FIQ	I			PCK1	O	PIO, I, PU, ST
P15	VDDNF	EBI	PD0	I/O			NANDOE	O					PIO, I, PU
N14	VDDNF	EBI	PD1	I/O			NANDWE	O					PIO, I, PU
M15	VDDNF	EBI	PD2	I/O			A21/NANDALE	O					A21,O, PD
M14	VDDNF	EBI	PD3	I/O			A22/NANDCLE	O					A22,O, PD
P16	VDDNF	EBI	PD4	I/O			NCS3	O					PIO, I, PU
M17	VDDNF	EBI	PD5	I/O			NWAIT	I					PIO, I, PU
L15	VDDNF	EBI	PD6	I/O			D16	O					PIO, I, PU
L16	VDDNF	EBI	PD7	I/O			D17	O					PIO, I, PU
L17	VDDNF	EBI	PD8	I/O			D18	O					PIO, I, PU

Table 4-1. BGA217 Pin Description (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
K17	VDDNF	EBI	PD9	I/O			D19	O					PIO, I, PU
K16	VDDNF	EBI	PD10	I/O			D20	O					PIO, I, PU
K15	VDDNF	EBI	PD11	I/O			D21	O					PIO, I, PU
J17	VDDNF	EBI	PD12	I/O			D22	O					PIO, I, PU
J16	VDDNF	EBI	PD13	I/O			D23	O					PIO, I, PU
H17	VDDNF	EBI	PD14	I/O			D24	O					PIO, I, PU
J15	VDDNF	EBI	PD15	I/O			D25	O	A20	O			A20, O, PD
G17	VDDNF	EBI	PD16	I/O			D26	O	A23	O			A23, O, PD
H16	VDDNF	EBI	PD17	I/O			D27	O	A24	O			A24, O, PD
H15	VDDNF	EBI	PD18	I/O			D28	O	A25	O			A25, O, PD
F17	VDDNF	EBI	PD19	I/O			D29	O	NCS2	O			PIO, I, PU
G16	VDDNF	EBI	PD20	I/O			D30	O	NCS4	O			PIO, I, PU
E17	VDDNF	EBI	PD21	I/O			D31	O	NCS5	O			PIO, I, PU
H8 H9 H10	VDDIOM	POWER	VDDIOM	I									I
J14 K14 L14	VDDNF	POWER	VDDNF	I									I
J8 J9 J10 K9 K10	GNDIOM	GND	GNDIOM	I									I
P9 P12	VDDIOP0	POWER	VDDIOP0	I									I
L3 L4	VDDIOP1	POWER	VDDIOP1	I									I
P6 P7 P13	GNDIOP	GND	GNDIOP	I									I
D6	VDDBU	POWER	VDDBU	I									I
D5 B3	GNDBU	GND	GNDBU	I									I
C4	VDDANA	POWER	VDDANA	I									I
B2	GNDANA	GND	GNDANA	I									I
T16	VDDPLL	POWER	VDDPLL	I									I
P14	GNDPLL	GND	GNDPLL	I									I
R14	VDDOSC	POWER	VDDOSC	I									I
R15	VDDUSB	POWER	VDDUSB	I									I
N16	VDDFUSE	POWER	VDDFUSE	I									I
M16	GNDFUSE	GND	GNDFUSE										I
T17	GNDUSB	GND	GNDUSB	I									I

Table 4-1. BGA217 Pin Description (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
C8 G15 J4 P10	VDDCORE	POWER	VDDCORE	I									I
D8 H14 K8 P11	GNDCORE	GND	GNDCORE	I									I
B14	VDDIOM	EBI	D0	I/O									O, PD
A14	VDDIOM	EBI	D1	I/O									O, PD
C14	VDDIOM	EBI	D2	I/O									O, PD
D13	VDDIOM	EBI	D3	I/O									O, PD
C13	VDDIOM	EBI	D4	I/O									O, PD
B13	VDDIOM	EBI	D5	I/O									O, PD
A13	VDDIOM	EBI	D6	I/O									O, PD
C12	VDDIOM	EBI	D7	I/O									O, PD
D12	VDDIOM	EBI	D8	I/O									O, PD
B12	VDDIOM	EBI	D9	I/O									O, PD
C11	VDDIOM	EBI	D10	I/O									O, PD
D11	VDDIOM	EBI	D11	I/O									O, PD
A12	VDDIOM	EBI	D12	I/O									O, PD
B11	VDDIOM	EBI	D13	I/O									O, PD
A11	VDDIOM	EBI	D14	I/O									O, PD
C10	VDDIOM	EBI	D15	I/O									O, PD
D17	VDDIOM	EBI_O	A0	O	NBS0	O							O, PD
C17	VDDIOM	EBI_O	A1	O	NBS2/ DQM2/ NWR2	O							O, PD
F16	VDDIOM	EBI_O	A2	O									O, PD
B17	VDDIOM	EBI_O	A3	O									O, PD
A17	VDDIOM	EBI_O	A4	O									O, PD
F15	VDDIOM	EBI_O	A5	O									O, PD
E16	VDDIOM	EBI_O	A6	O									O, PD
D16	VDDIOM	EBI_O	A7	O									O, PD
E15	VDDIOM	EBI_O	A8	O									O, PD
G14	VDDIOM	EBI_O	A9	O									O, PD
C16	VDDIOM	EBI_O	A10	O									O, PD
F14	VDDIOM	EBI_O	A11	O									O, PD
B16	VDDIOM	EBI_O	A12	O									O, PD
A16	VDDIOM	EBI_O	A13	O									O, PD
C15	VDDIOM	EBI_O	A14	O									O, PD
D15	VDDIOM	EBI_O	A15	O									O, PD

Table 4-1. BGA217 Pin Description (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
B15	VDDIOM	EBI_O	A16	O	BA0	O							O, PD
E14	VDDIOM	EBI_O	A17	O	BA1	O							O, PD
A15	VDDIOM	EBI_O	A18	O	BA2	O							O, PD
D14	VDDIOM	EBI_O	A19	O									O, PD
B7	VDDIOM	EBI_O	NCS0	O									O, PU
C5	VDDIOM	EBI_O	NCS1	O	SDCS	O							O, PU
C7	VDDIOM	EBI_O	NRD	O									O, PU
A6	VDDIOM	EBI_O	NWR0	O	NWRE	O							O, PU
C6	VDDIOM	EBI_O	NWR1	O	NBS1	O							O, PU
D7	VDDIOM	EBI_O	NWR3	O	NBS3/ DQM3	O							O, PU
A10	VDDIOM	EBI_CLK	SDCK	O									O
A9	VDDIOM	EBI_CLK	#SDCK	O									O
D10	VDDIOM	EBI_O	SDCKE	O									O, PU
B9	VDDIOM	EBI_O	RAS	O									O, PU
D9	VDDIOM	EBI_O	CAS	O									O, PU
B10	VDDIOM	EBI_O	SDWE	O									O, PU
B6	VDDIOM	EBI_O	SDA10	O									O, PU
C9	VDDIOM	EBI_O	DQM0	O									O, PU
A8	VDDIOM	EBI_O	DQM1	O									O, PU
B8	VDDIOM	EBI	DQS0	I/O									O, PD
A7	VDDIOM	EBI	DQS1	I/O									O, PD
A2	VDDANA	POWER	ADVREF	I									I
P17	VDDUSB	USBFS	HDP	I/O									O, PD
N17	VDDUSB	USBFS	HDM	I/O									O, PD
R17	VDDUSB	USBFS	DDP	I/O									O, PD
R16	VDDUSB	USBFS	DDM	I/O									O, PD
A5	VDDBU	SYSC	WKUP	I									I, ST
B5	VDDBU	SYSC	SHDN	O									O, PU
U15	VDDCORE	RSTJTAG	BMS	I									I, PD, ST
B4	VDDBU	SYSC	JTAGSEL	I									I, PD
R12	VDDIOP0	RSTJTAG	TCK	I									I, ST
R11	VDDIOP0	RSTJTAG	TDI	I									I, ST
U14	VDDIOP0	RSTJTAG	TDO	O									O
T13	VDDIOP0	RSTJTAG	TMS	I									I, ST
T14	VDDIOP0	RSTJTAG	RTCK	O									O
R13	VDDIOP0	RSTJTAG	NRST	I/O									I, PU, ST
T15	VDDIOP0	RSTJTAG	NTRST	I									I, PU, ST

Table 4-1. BGA217 Pin Description (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
A4	VDDBU	CLOCK	XIN32	I									I
A3	VDDBU	CLOCK	XOUT32	O									O
U17	VDDIOP0	CLOCK	XIN	I									I
U16	VDDIOP0	CLOCK	XOUT	O									O
N15	NC												

5. Power Considerations

5.1 Power Supplies

The SAM9N12 has several types of power supply pins:

Table 5-1. SAM9N12 Power Supplies

Name	Voltage Range, nominal	Associated Ground	Powers
VDDCORE	0.9-1.1V, 1.0V	GNDCORE	the core, including the processor, the embedded memories and the peripherals, the internal 12 MHz RC
VDDIOM	1.65-1.95V, 1.8V 3.0-3.6V, 3.3V	GNDIOM	the External Memory Interface I/O lines
VDDNF	1.65-1.95V, 1.8V 3.0-3.6V, 3.3V	GNDIOM	the NAND Flash I/O and control, D16-D32 and multiplexed SMC lines
VDDIOP0	1.65-3.6V	GNDIOP	a part of Peripherals I/O lines
VDDIOP1	1.65-3.6V	GNDIOP	a part of Peripherals I/O lines
VDDBU	1.65-3.6V	GNDBU	the Slow Clock oscillator, the internal 32-kbyte RC and a part of the System Controller
VDDUSB	3.0-3.6V, 3.3V	GNDUSB	the USB interface
VDDPLL	0.9-1.1V, 1.0V	GNDPLL	the PLL cells
VDDOSC	1.65-3.6V	GNDPLL	the Main Oscillator cells
VDDANA	3.0-3.6V, 3.3V	GNDANA	the Analog to Digital Converter
VDDFUSE	3.0-3.6V, 3.3V	GNDFUSE	Fuse box for programming

5.2 Programmable I/O Lines Power Supplies and Current Drive

5.2.1 External Bus interface

32 bits Wide Interface, Supporting:

- 16-bit DDR2/LPDDR, 32-bit SDRAM/LPSDR
- Static Memories
- NAND Flash with up to 24-bit ECC

Refer to EBI section, chapter Implementation examples for hardware connection details.

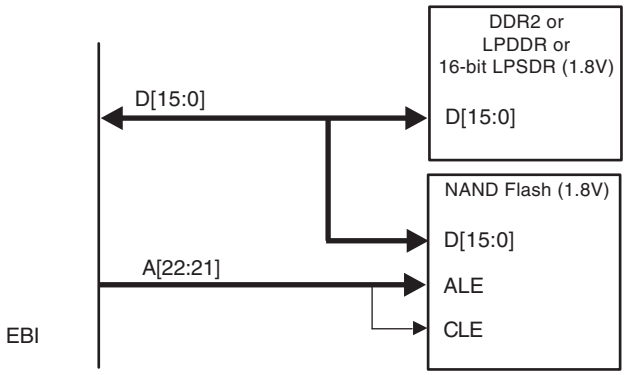
The EBI I/Os accept two drive levels, HIGH and LOW. This allows to avoid overshoots and give the best performances according to the bus load and external memories.

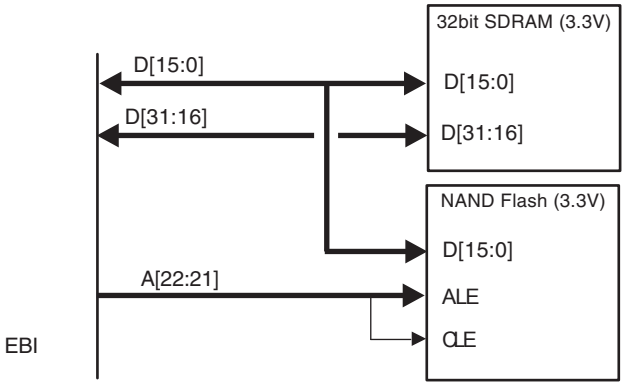
The voltage ranges and the slew rates are determined by programming EBI_DRIVE field in the Chip Configuration registers located in the Matrix User Interface.

At reset the selected current drive is HIGH.

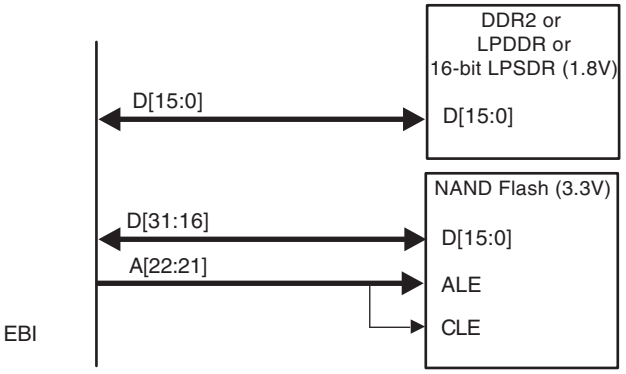
A switch NFD0_ON_D16 allows the user to select NAND Flash path on D0-D15 or D16-D31, depending on memory power supplies. This switch is located in the register EBICSA in the Bus Matrix user interface.

In the following example, the NAND Flash and the external RAM (DDR2 or LPDDR or 16-bit LPSDR) are in the same power supply range, (NFD0_ON_D16 = 0).





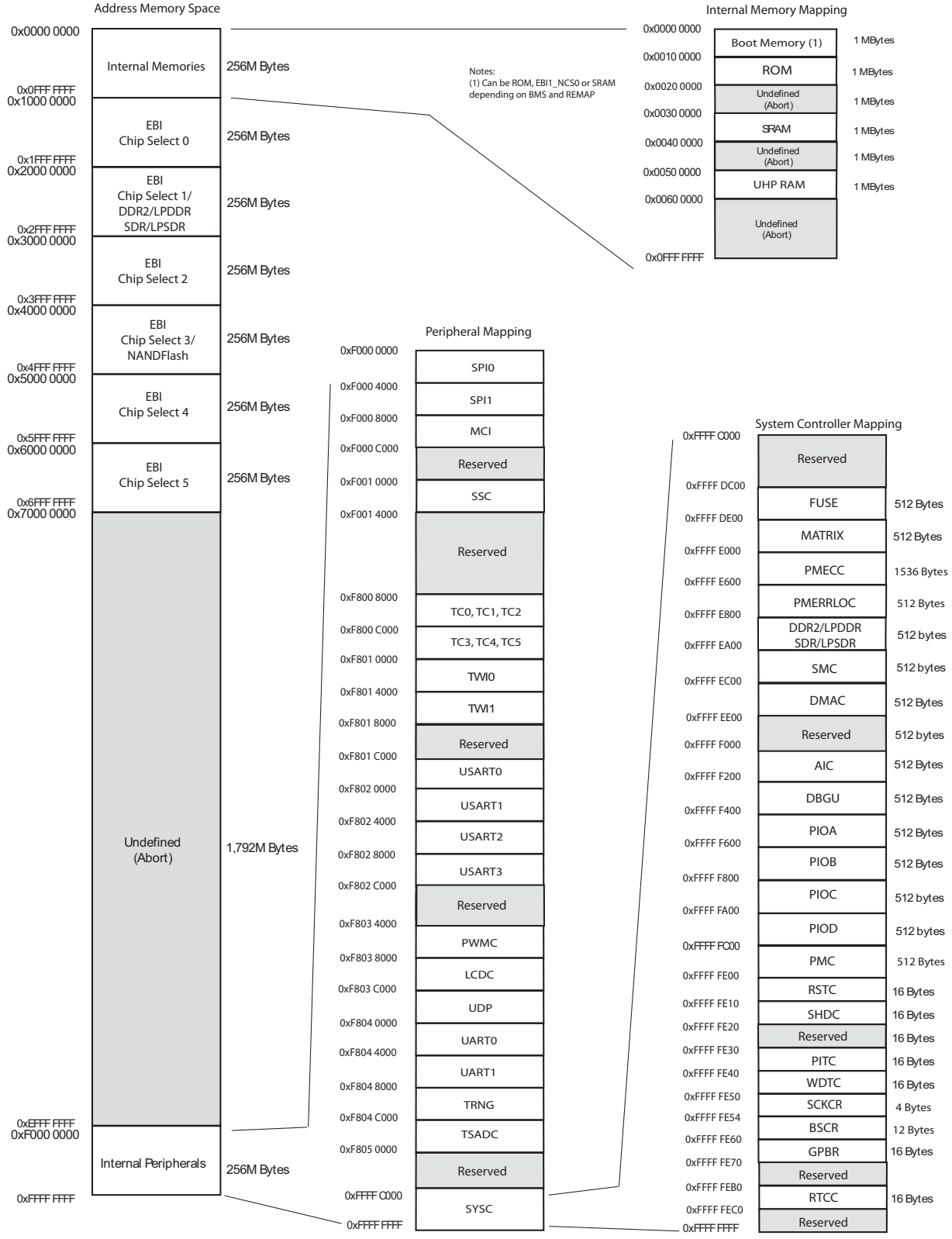
In the following example the NAND Flash and the external RAM (DDR2 or LPDDR or 16bit LPSDR) are NOT in the same power supply range (NFD0_ON_D16 = 1).



At reset NFD0_ON_D16 = 0 and NAND Flash is connected to D0-D15.

6. Memories

Figure 6-1. SAM9N12 Memory Mapping



6.1 Memory Mapping

A first level of address decoding is performed by the AHB Bus Matrix, i.e., the implementation of the Advanced High performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4 Gbytes of address space into 16 banks of 256 Mbytes. The banks 1 to 6 are directed to the EBI that associates these banks to the external chip selects EBI_NCS0 to EBI_NCS5. The bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1Mbyte of internal memory area. The bank 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

6.2 Embedded Memories

6.2.1 Internal SRAM

The SAM9N12 embeds a total of 32 Kbytes high-speed SRAM.

After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x0030 0000.

After Remap, the SRAM also becomes available at address 0x0.

6.2.2 Internal ROM

The SAM9N12 contains the bootloader and specific tables used to compute SLC and MLC NAND Flash ECC.

The ROM is mapped at address 0x0010 0000. It is also accessible at address 0x0 (BMS = 1) after the reset and before the Remap Command.

6.3 External Memories Overview

The SAM9N12 features a External Bus Interface to offer interface to a wide range of external memories and to any parallel peripheral.

6.3.1 External Bus Interface

- Integrates three External Memory Controllers:
  - Static Memory Controller
  - DDR2/SDRAM Controller
  - MLC NAND Flash ECC Controller
- Up to 26-bit Address Bus (up to 64MBytes linear per chip select)
- Up to 6 chips selects, Configurable Assignment:
  - Static Memory Controller on NCS0, NCS1, NCS2, NCS3, NCS4, NCS5
  - DDR2/SDRAM Controller (SDCS) or Static Memory Controller on NCS1
  - NAND Flash support on NCS3

6.3.2 Static Memory Controller

- 8- or 16-bit Data Bus
- Multiple Access Modes supported
  - Byte Write or Byte Select Lines
  - Asynchronous read in Page Mode supported (4- up to 16-byte page size)
- Multiple device adaptability
  - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time
- Slow Clock mode supported

6.3.3 DDR-SDRAM Controller

- Supports DDR2-SDRAM, Low-power DDR1-SDRAM or DDR2-SDRAM, SDR-SDRAM and Low-power SDR-SDRAM
- Numerous Configurations Supported
  - 2K, 4K, 8K, 16K Row Address Memory Parts
  - SDRAM with 4 Internal Banks
  - SDR-SDRAM with 16-bit or 32-bit Data Path
  - DDR-SDRAM with 16-bit Data Path
  - One Chip Select for SDRAM Device (256 Mbytes Address Space)
- Programming Facilities
  - Multibank Ping-pong Access (Up to 4 Banks or 8 Banks Opened at Same Time = Reduced Average Latency of Transactions)
  - Timing Parameters Specified by Software
  - Automatic Refresh Operation, Refresh Rate is Programmable

  - Automatic Update of DS, TCR and PASR Parameters (Low-power SDRAM Devices)
- Energy-saving Capabilities
  - Self-refresh, Power-down, Active Power-down and Deep Power-down Modes Supported
- SDRAM Power-up Initialization by Software
- CAS Latency of 2, 3 Supported
- Reset Function Supported (DDR2-SDRAM)
- ODT (On-die Termination) Not Supported
- Auto Precharge Command Not Used
- SDR-SDRAM with 16-bit Datapath and Eight Columns Not Supported
- DDR2-SDRAM with Eight Internal Banks Supported
- Linear and interleaved decoding supported
- Clock Frequency Change in Precharge Power-down Mode Not Supported
- OCD (Off-chip Driver) Mode Not Supported

6.3.4 Programmable Multi-bit Error Correcting Code (PMECC)

- Multibit Error Correcting Code.
- Algorithm based on binary shortened Bose, Chaudhuri and Hocquenghem (BCH) codes.
- Programmable Error Correcting Capability: 2, 4, 8, 16 and 24 bit of errors per block.
- Programmable block size: 512 bytes or 1024 bytes.
- Programmable number of block per page: 1, 2, 4 or 8 blocks of data per page.
- Programmable spare area size.
- Supports spare area ECC protection.
- Supports 8 kbytes page size using 1024 bytes/block and 4 kbytes page size using 512 bytes/block.
- Multibit Error detection is interrupt driven.

6.3.5 Programmable Multi-bit ECC Error Location (PMERRLOC)

- Provides hardware acceleration for determining roots of polynomials defined over a finite field
- Programmable finite Field GF(2^13) or GF(2^14)
- Finds roots of error-locator polynomial.
- Programmable number of roots.

7. System Controller

The System Controller is a set of peripherals that allows handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc.

The System Controller User Interface also embeds the registers that configure the Matrix and a set of registers for the chip configuration. The chip configuration registers configure the EBI chip select assignment and voltage range for external memories.

7.1 System Controller Mapping

The System Controller's peripherals are all mapped within the highest 16 Kbytes of address space, between addresses 0xFFFF E400 and 0xFFFF FFFF.

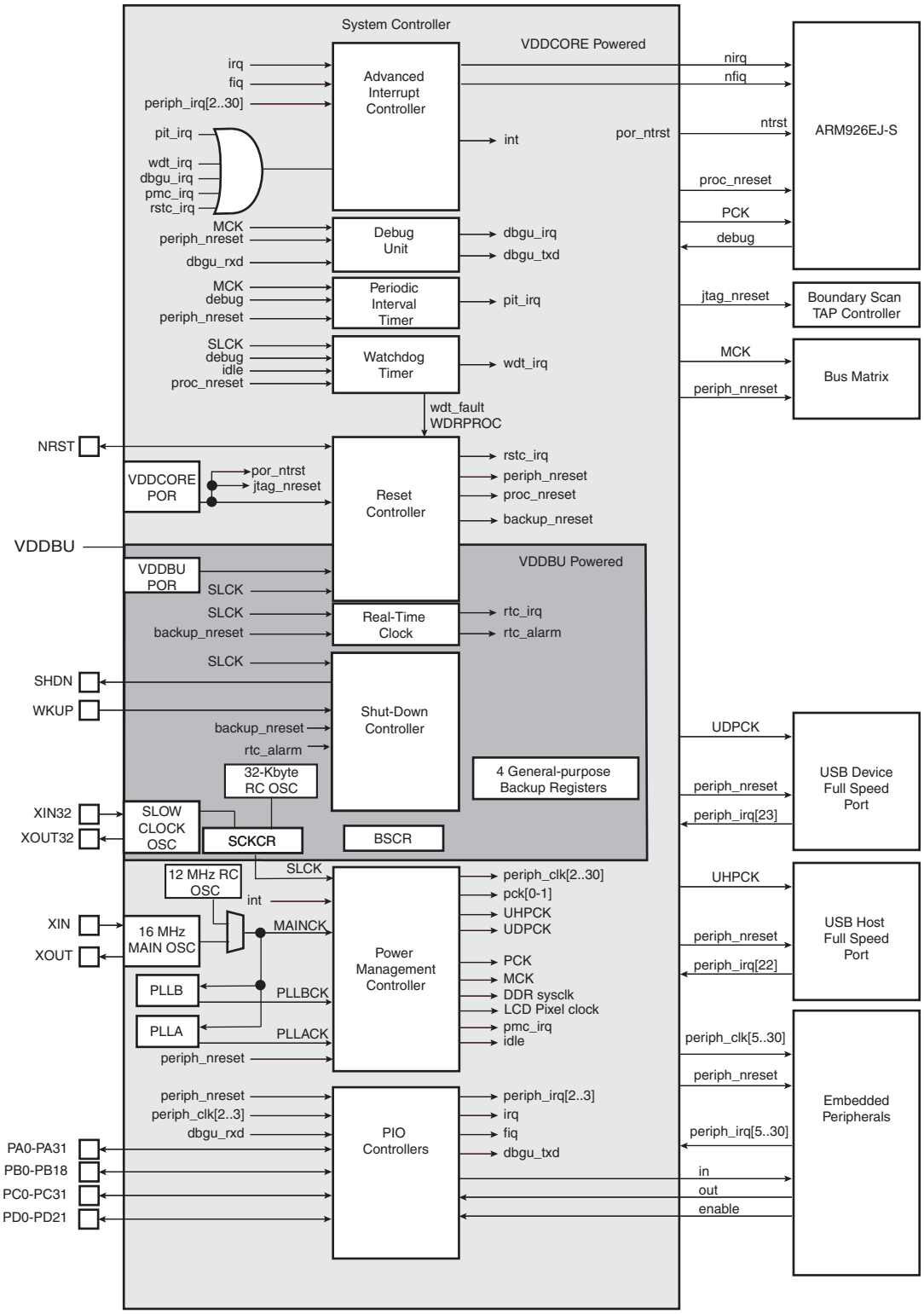
However, all the registers of the System Controller are mapped on the top of the address space. All the registers of the System Controller can be addressed from a single pointer by using the standard ARM instruction set, as the Load/Store instruction have an indexing mode of ±4 Kbytes.

Figure 7-1 shows the System Controller block diagram.

Figure 6-1 shows the mapping of the User Interfaces of the System Controller peripherals.

7.2 System Controller Block Diagram

Figure 7-1. SAM9N12 System Controller Block Diagram



7.3 Chip Identification

- Chip ID: 0x819A_05A1
- SAM9N12 Chip ID Extension: 6
- JTAG ID: 0x05B3_003F
- ARM926 TAP ID: 0x0792_603F

7.4 Backup Section

The SAM9N12 features a Backup Section that embeds:

- RC Oscillator
- Slow Clock Oscillator
- Real Time Counter (RTC)
- Shutdown Controller
- 4 backup registers
- Slow Clock Control Register (SCKCR)
- A part of the reset Controller (RSTC)
- This section is powered by the VDDBU rail.

7.5 Security Features

The SAM9N12 features:

- 320 OTP bits array
- Secure bootloader selectable by a dedicated fuse bit
- Bits in SFR register to forbid ROM and OTP read access

The OTP array enables the user to set security features and program device configuration

The secure bootloader allows:

- Keeping the firmware stored in Non-Volatile memory encrypted
- Decryption, in internal SRAM only, the firmware using the customer's crypto key burned in the fuse bits
- The encryption/decryption uses high strength hardware, AES256

8. Peripherals

8.1 Peripheral Mapping

As shown in Figure 6-1, the Peripherals are mapped in the upper 256M bytes of the address space between the addresses 0xFFF7 8000 and 0xFFFC FFFF.

Each User Peripheral is allocated 16K bytes of address space.

8.2 Peripheral Identifiers

Table 8-1 defines the Peripheral Identifiers of the SAM9N12. A peripheral identifier is required for the control of the peripheral interrupt with the Advanced Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 8-1. SAM9N12 Peripheral Identifiers

Instance ID	Instance name	Instance description	External interrupt	Wired-or interrupt
0	AIC	Advanced Interrupt Controller	FIQ	
1	SYS	System Controller Interrupt		DBGU, PMC, SYSC, PMECC, PMERRLOC
2	PIOA,PIOB	Parallel I/O Controller A and B		
3	PIOC,PIOD	Parallel I/O Controller C and D		
4	Reserved			
5	USART0	USART 0		
6	USART1	USART 1		
7	USART2	USART 2		
8	USART3	USART 3		
9	TWI0	Two-Wire Interface 0		
10	TWI1	Two-Wire Interface 1		
11	Reserved			
12	HSMCI	High Speed Multimedia Card Interface		
13	SPI0	Serial Peripheral Interface 0		
14	SPI1	Serial Peripheral Interface 1		
15	UART0	UART 0		
16	UART1	UART 1		
17	TC0,TC1	Timer Counter 0,1,2,3,4,5		
18	PWM	Pulse Width Modulation Controller		
19	ADC	ADC Controller		
20	DMAC	DMA Controller		
21	Reserved			
22	UHP	USB Host		
23	UDP	USB Device		
24	Reserved			
25	LCDC	LCD Controller		
26	Reserved			

Table 8-1. SAM9N12 Peripheral Identifiers (Continued)

Instance ID	Instance name	Instance description	External interrupt	Wired-or interrupt
27	Reserved			
28	SSC	Synchronous Serial Controller		
29	Reserved			
30	TRNG	True Random Number Generator		
31	AIC	Advanced Interrupt Controller	IRQ	

8.3 Peripheral Interrupts and Clock Control

8.3.1 System Interrupt

The System Interrupt in Source 1 is the wired-OR of the interrupt signals coming from:

- the DDR2/LPDDR Controller
- the Debug Unit
- the Periodic Interval Timer
- the Real-Time Clock
- the Watchdog Timer
- the Reset Controller
- the Power Management Controller

The clock of these peripherals cannot be deactivated and Peripheral ID 1 can only be used within the Advanced Interrupt Controller.

8.3.2 External Interrupts

All external interrupt signals, i.e., the Fast Interrupt signal FIQ or the Interrupt signal IRQ, use a dedicated Peripheral ID. However, there is no clock control associated with these peripheral IDs.

8.4 Peripheral Signal Multiplexing on I/O Lines

The SAM9N12 features 4 PIO controllers, PIOA, PIOB, PIOC and PIOD, which multiplex the I/O lines of the peripheral set.

Each PIO Controller controls 32 lines, 19 lines, 32 lines and 22 lines respectively for PIOA, PIOB, PIOC and PIOD. Each line can be assigned to one of three peripheral functions, A, B or C.

Refer to Section 4. “Package and Pinout” and the package pinout table, Table 4-1, depending on the package.

8.4.1 Reset State

The column “Reset State” (Table 4-1) indicates the reset state of the line with mnemonics.

- “PIO”/”signal”

Indicates whether the PIO Line resets in I/O mode or in peripheral mode. If “PIO” is mentioned, the PIO Line is maintained in a static state as soon as the reset is released. As a result, the bit corresponding to the PIO Line in the register PIO_PSR (Peripheral Status Register) resets low.

If a signal name is mentioned in the “Reset State” column, the PIO Line is assigned to this function and the corresponding bit in PIO_PSR resets high. This is the case on pins controlling memories, in particular the address lines, which require the pin to be driven as soon as the reset is released.

- 'I'/'O'

Indicates whether the signal is input or output state.

- "PU"/"PD"

Indicates whether Pull-up or Pull-down, or nothing is enabled.

- "ST"

Indicates if Schmitt Trigger is enabled.

Note: Example: The PB18 "Reset State" column shows "PIO, I, PU, ST". That means the line PIO18 is configured as an Input with Pull-Up and Schmitt Trigger enabled. PD14 reset state is "PIO, I, PU". That means PIO Input with Pull-Up. PD15 reset state is "A20, O, PD" which means output address line 20 with Pull-Down.

8.4.2 PIO Line Selection

Peripheral A, B or C is selected thanks to the PIO_ABCDSR1 and PIO_ABCDSR2 registers in the PIO Controller Interface.

Table 8-2. PIO Line Selection

Px value in PIO_ABCDSR2	Px value in PIO_ABCDSR1	A, B or C
0	0	A
0	1	B
1	0	C

8.5 Fuse Box Features

SAM9N12 embeds 320 One Time Programming (OTP) bits. When the OTP bit is set, it is seen as '1'. The user interface allows the user to perform the following operations:

8.5.1 Read

- 10 registers SR0-SR9 that reflect OTP bit state
- MSK field (write-once) allow user to mask registers SR1 to SR9
- All OTP bits are read as '1' when VDDFUSE is floating, all security features are set.

8.5.2 Write

- Done in one 32-bit DATA register
- SEL field to select the 32-bit word 0 to 9

Table 8-3. Special OTP Bit Description

Bit Number	Bit Name	Function
0	W	OTP bit writing is disabled if set OTP bits are not accessible in test mode
1	B	BMS sampling is disabled if set, system boots systematically out of the ROM code
2	J	JTAG is disabled if set
3-7	3-7	Reserved

9. Embedded Peripherals

9.1 Advanced Interrupt Controller (AIC)

- Controls the interrupt lines (nIRQ and nFIQ) of the ARM Processor
- Thirty-two individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals (PIT, RTT, PMC, DBGU, PMECC, etc.)
  - Programmable Edge-triggered or Level-sensitive Internal Sources
  - Programmable Positive/Negative Edge-triggered or High/Low Level-sensitive
- One External Sources plus the Fast Interrupt signal
- 8-level Priority Controller
  - Drives the Normal Interrupt of the processor
  - Handles priority of the interrupt sources 1 to 31
  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes Interrupt Service Routine Branch and Execution
  - One 32-bit Vector Register per interrupt source
  - Interrupt Vector Register reads the corresponding current Interrupt Vector
- Protect Mode
  - Easy debugging by preventing automatic operations when protect models are enabled
- Fast Forcing
  - Permits redirecting any normal interrupt source on the Fast Interrupt of the processor

9.2 Reset Controller (RSTC)

- Manages All Resets of the System, Including
  - External Devices Through the NRST Pin
  - Processor Reset
  - Peripheral Set Reset
- Based on 2 Embedded Power-on Reset Cells
- Reset Source Status
  - Status of the Last Reset
  - Either Power-up Reset, Software Reset, User Reset, Watchdog Reset
- External Reset Signal Shaping
- AMBA®-compliant Interface
  - Interfaces to the ARM® Advanced Peripheral Bus

9.3 Real-time Clock (RTC)

- Low power consumption
- Full asynchronous design
- Two hundred year calendar
- Programmable Periodic Interrupt
- Alarm and update parallel load
- Control of alarm and update Time/Calendar Data In

9.4 Periodic Interval Timer (PIT)

- 20-bit Programmable Counter plus 12-bit Interval Counter
- Reset-on-read Feature
- Both Counters Work on Master Clock/16
- AMBA-compliant Interface
  - Interfaces to the ARM® Advanced Peripheral Bus

9.5 Watchdog Timer (WDT)

- 12-bit Key-protected Programmable Counter
- Provides Reset or Interrupt Signals to the System
- Counter May Be Stopped While the Processor is in Debug State or in Idle Mode
- AMBA-compliant Interface
  - Interfaces to the ARM Advanced Peripheral Bus

9.6 Shut Down Controller (SHDWC)

- Shutdown and Wake-up Logic
  - Software Assertion of the SHDW Output Pin
  - Programmable De-assertion from the WKUP Input Pins
- AMBA-compliant Interface
  - Interfaces to the ARM Advanced Peripheral Bus

9.7 General-Purpose Backup Registers (GPBR)

- Four 32-bit backup general-purpose registers

9.8 Power Management Controller (PMC)

The Power Management Controller provides all the clock signals to the system.

PMC input clocks:

- PLLACK: From PLLA
- PLLBCK: From PLLB and dedicated to USB clock generation.
- SLCK: slow clock from external 32K oscillator or internal 32K RC
- MAINCK: Main Clock from external 16MHz oscillator or internal 12M RC

PMC output clocks:

- Processor Clock PCK.
- Master Clock MCK, in particular to the Matrix, the memory interfaces, the peripheral bridge. The divider can be 2, 3 or 4.
- Each peripheral embeds its own divider, programmable in the PMC User Interface.
- 250MHz DDR system clock

Note: DDR system clock is not available when Master Clock (MCK) equals Processor Clock (PCK).

- LCD pixel clock that can use DDR system clock or MCK, the choice is done in the LCD user interface.
- USB clocks (USB48M and USB12M) thanks to PLLBCK.
- Two programmable clock outputs: PCK0 and PCK1

This allows the software control of five flexible operating modes:

- Normal Mode, processor and peripherals running at a programmable frequency
- Idle Mode, processor stopped waiting for an interrupt
- Slow Clock Mode, processor and peripherals running at low frequency
- Standby Mode, mix of Idle and Backup Mode, peripheral running at low frequency, processor stopped waiting for an interrupt
- Backup Mode, Main Power Supplies off, VDDBU powered by a battery

9.9 PIO Controllers (PIO)

- Up to 32 Programmable I/O Lines
- Fully Programmable through Set/Clear Registers
- Multiplexing of Four Peripheral Functions per I/O Line
- For each I/O Line (Whether Assigned to a Peripheral or Used as General Purpose I/O)
  - Input Change Interrupt
  - Programmable Glitch Filter
  - Programmable Debouncing Filter
  - Multi-drive Option Enables Driving in Open Drain
  - Programmable Pull Up on Each I/O Line
  - Pin Data Status Register, Supplies Visibility of the Level on the Pin at Any Time
  - Additional Interrupt Modes on a Programmable Event: Rising Edge, Falling Edge, Low Level or High Level
  - Lock of the Configuration by the Connected Peripheral
- Synchronous Output, Provides Set and Clear of Several I/O lines in a Single Write
- Write Protect Registers
- Programmable I/O Delay
- Programmable Schmitt Trigger Inputs

9.10 Debug Unit (DBGU)

- System Peripheral to Facilitate Debug of Atmel® ARM®-based Systems
- Composed of Four Functions
  - Two-pin UART
  - Debug Communication Channel (DCC) Support
  - Chip ID Registers
  - ICE Access Prevention
- Two-pin UART
  - Implemented Features are USART Compatible
  - Independent Receiver and Transmitter with a Common Programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Interrupt Generation
  - Support for Two DMA Channels with Connection to Receiver and Transmitter
- Debug Communication Channel Support
  - Offers Visibility of COMMRX and COMMTX Signals from the ARM Processor
  - Interrupt Generation
- Chip ID Registers
  - Identification of the Device Revision, Sizes of the Embedded Memories, Set of Peripherals
- ICE Access Prevention
  - Enables Software to Prevent System Access Through the ARM Processor's ICE
  - Prevention is Made by Asserting the NTRST Line of the ARM Processor's ICE

9.11 Programmable Multibit ECC Controller (PMECC)

- Multibit Error Correcting Code.
- Algorithm based on binary shortened Bose, Chaudhuri and Hocquenghem (BCH) codes.
- Programmable Error Correcting Capability: 2, 4, 8, 12 and 24 bit of errors per sector.
- Programmable Sector Size: 512 bytes or 1024 bytes.
- Programmable Number of Sectors per page: 1, 2, 4 or 8 sectors of data per page.
- Programmable Spare Area Size.
- Supports Spare Area ECC Protection.
- Supports 8 kbytes page size using 1024 bytes per sector and 4 kbytes page size using 512 bytes per sector.
- Configurable through APB interface
- Multibit Error Detection is Interrupt Driven

9.12 Programmable Multibit ECC Error Location Controller (PMERRLOC)

- Provides Hardware Acceleration for determining roots of polynomials defined over a finite field
- Programmable Finite Field GF(2^13) or GF(2^14)
- Finds Roots of Error Locator Polynomial
- Programmable Number of Roots

9.13 AHB Static Memory Controller (AHB SMC)

- 6 Chip Selects Available
- 64-Mbyte Address Space per Chip Select
- 8-, 16- or 32-bit Data Bus
- Word, Halfword, Byte Transfers
- Byte Write or Byte Select Lines
- Programmable Setup, Pulse And Hold Time for Read Signals per Chip Select
- Programmable Setup, Pulse And Hold Time for Write Signals per Chip Select
- Programmable Data Float Time per Chip Select
- Compliant with LCD Module
- External Wait Request
- Automatic Switch to Slow Clock Mode
- Asynchronous Read in Page Mode Supported: Page Size Ranges from 4 to 32 Bytes

9.14 AHB DDR/SDR SDRAM Controller (DDRSDRC)

- AMBA Compliant Interface, interfaces Directly to the ARM® Advanced High performance Bus (AHB)
  - Four AHB Interfaces, Management of All Accesses Maximizes Memory Bandwidth and Minimizes Transaction Latency
  - AHB Transfer: Word, Half Word, Byte Access
- Supports DDR2-SDRAM, Low-power DDR-SDRAM, SDR-SDRAM and Low-power SDRSDRAM
- Numerous Configurations Supported
  - 2K, 4K, 8K, 16K Row Address Memory Parts
  - SDRAM with Four Internal Banks
  - SDR-SDRAM with 16- or 32-bit Data Path
  - DDR-SDRAM with 16-bit Data Path
  - One Chip Select for SDRAM Device (256 Mbyte Address Space)
- Programming Facilities
  - Multibank Ping-pong Access (Up to 4 Banks Opened at Same Time = Reduces Average Latency of Transactions)
  - Timing Parameters Specified by Software
  - Automatic Refresh Operation, Refresh Rate is Programmable
  - Automatic Update of DS, TCR and PASR Parameters (Low-power SDRAM Devices)
- Energy-saving Capabilities

– Self-refresh, Power-down, Active Power-down and Deep Power-down Modes Supported

- SDRAM Power-up Initialization by Software
- CAS Latency of 2, 3 Supported
- Reset Function Supported (DDR2-SDRAM)
- ODT (On-die Termination) Not Supported
- Auto Precharge Command Not Used
- SDR-SDRAM with 16-bit Datapath and Eight Columns Not Supported
- DDR2-SDRAM with Eight Internal Banks Not Supported
- Clock Frequency Change in Precharge Power-down Mode Not Supported
- OCD (Off-chip Driver) Mode Not Supported

9.15 AHB DMA Controller (DMAC)

- DMAC is full featured and optimized for memory-to-memory transfers
- Acting as Two Matrix Masters
- Embeds 8 unidirectional channels with programmable priority
- Address Generation
  - Source / destination address programming
  - Address increment, decrement or no change
  - DMA chaining support for multiple non-contiguous data blocks through use of linked lists
  - Scatter support for placing fields into a system memory area from a contiguous transfer. Writing a stream of data into non-contiguous fields in system memory
  - Gather support for extracting fields from a system memory area into a contiguous transfer
  - User enabled auto-reloading of source, destination and control registers from initially programmed values at the end of a block transfer
  - Auto-loading of source, destination and control registers from system memory at end of block transfer in block chaining mode
  - Unaligned system address to data transfer width supported in hardware
  - Picture-In-Picture Mode
- Channel Buffering
  - 16-word FIFO
  - Automatic packing/unpacking of data to fit FIFO width
- Channel Control
  - Programmable multiple transaction size for each channel
  - Support for cleanly disabling a channel without data loss
  - Suspend DMA operation
  - Programmable DMA lock transfer support
- Transfer Initiation
  - Support for Software handshaking interface. Memory mapped registers can be used to control the flow of a DMA transfer in place of a hardware handshaking interface
- Interrupt

– Programmable Interrupt generation on DMA Transfer completion Block Transfer completion, Single/Multiple transaction completion or Error condition

9.16 USB Device Full Speed (UDP)

- USB V2.0 full-speed compliant, 12 MBits per second
- Embedded USB V2.0 full-speed transceiver
- Embedded 2,432-byte dual-port RAM for endpoints
- Suspend/Resume logic
- Ping-pong mode (two memory banks) for isochronous and bulk endpoints
- Six general-purpose endpoints
  - Endpoint 0 and 3: 64 bytes, no ping-pong mode
  - Endpoint 1 and 2: 64 bytes, ping-pong mode
  - Endpoint 4 and 5: 512 bytes, ping-pong mode
- Embedded pull-up on pad

9.17 USB Host Full Speed (UHP)

- Compliance with Open HCI Rev 1.0 Specification
- Compliance with USB V2.0 Full-speed and Low-speed Specification
- Supports both Low-Speed 1.5 Mbps and Full-speed 12 Mbps devices
- Root hub integrated with one downstream USB ports
- One embedded USB transceiver
- Supports power management
- Operates as a master on the Matrix

9.18 High Speed Multimedia Card Interface (HSMCI)

- 8-bit HSMCI controllers
- Compatibility with MMC Plus Specification Version 4.3
- Compatibility with MultiMedia Card Specification Version 4.1
- Compatibility with SD Memory Card Specification Version 2.0
- Compatibility with SDIO Specification Version V2.0.
- Compatibility with CE ATA

9.19 Serial Peripheral Interface (SPI)

- Two SPIs
- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash® and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors

- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

9.20 Timer Counter (TC)

- Dual three 32-bit Timer Counter Channels
- Double PWM generation
- Capture/Waveform mode
- Wide range of functions including:
  - Frequency Measurement
  - Event Counting
  - Interval Measurement
  - Pulse Generation
  - Delay Timing
  - Pulse Width Modulation
  - Up/down Capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs
  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels

9.21 Pulse Width Modulation Controller (PWM)

- 4 channels, one 32-bit counter per channel
- Common clock generator, providing Thirteen Different Clocks
  - A Modulo n counter providing eleven clocks
  - Two independent Linear Dividers working on modulo n counter outputs
- Independent channel programming
  - Independent Enable Disable Commands
  - Independent Clock Selection
  - Independent Period and Duty Cycle, with Double Buffering
  - Programmable selection of the output waveform polarity
  - Programmable center or left aligned output waveform

9.22 Two Wire Interface (TWI)

- Two TWIs
- Compatibility with standard two-wire serial memory
- One, two or three bytes for slave address
- Sequential read/write operations
- Supports either master or slave modes
- Compatible with Standard Two-wire Serial Memories
- Master, Multi-master and Slave Mode Operation
- Bit Rate: Up to 400 Kbits
- General Call Supported in Slave mode

9.23 Universal Synchronous/Asynchronous Receiver Transmitters (USART)

- Four USARTs
- Manchester Encoding/Decoding
- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - By 8 or by 16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
  - Optional Manchester Encoding
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- SPI Mode
  - Master or Slave
  - Serial Clock Programmable Phase and Polarity
  - SPI Serial Clock (SCK) Frequency up to Internal Clock Frequency MCK/4
- LIN Mode
  - Compliant with LIN 1.3 and LIN 2.0 specifications
  - Master or Slave
  - Processing of frames with up to 256 data bytes
  - Response Data length can be configurable or defined automatically by the Identifier
  - Self synchronization in Slave node configuration

  - Automatic processing and verification of the “Synch Break” and the “Synch Field”
  - The “Synch Break” is detected even if it is partially superimposed with a data byte
  - Automatic Identifier parity calculation/sending and verification
  - Parity sending and verification can be disabled
  - Automatic Checksum calculation/sending and verification
  - Checksum sending and verification can be disabled
  - Support both “Classic” and “Enhanced” checksum types
  - Full LIN error checking and reporting
  - Frame Slot Mode: the Master allocates slots to the scheduled frames automatically.
  - Generation of the Wakeup signal
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

9.24 Universal Asynchronous Receiver Transmitters (UART)

- Two UARTs
- Independent receiver and transmitter with a common programmable Baud Rate Generator
- Even, Odd, Mark or Space Parity Generation
- Parity, Framing and Overrun Error Detection
- Automatic Echo, Local Loopback and Remote Loopback Channel Modes

9.25 Analog-to-Digital Converter (ADC)

- 12-channel ADC
- 5-channel to support 4wire and 5-wire resistive Touch Screen
- 10-bit 384 Ksamples/sec. Successive Approximation Register ADC
- -3/+3 LSB Integral Non Linearity, -2/+2 LSB Differential Non Linearity
- Integrated 12-to-1 multiplexer, offering twelve independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger sources
  - Hardware or software trigger
  - External trigger pin
  - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer
  - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels
- Compare level interrupt for background signal surveillance

9.26 Serial Synchronous Controller (SSC)

- One SSC
- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I^2S, TDM Buses, Magnetic Card Reader, ...)
- Contains an independent receiver and transmitter and a common clock divider

- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

9.27 LCD Controller (LCDC)

- One AHB Master Interface
- Supports Single Scan Active TFT Display
- Supports 12-, 16-, 18- and 24-bit Output Mode through the Spatial Dithering Unit
- Asynchronous Output Mode Supported
- 1, 2, 4, 8 bits per pixel (palletized)
- 12, 16, 18, 19, 24, 25 and 32 bits per pixel (non-palletized)
- Supports One Base Layer (background)
- Little Endian Memory Organization
- Programmable Timing Engine, with Integer Clock Divider
- Programmable Polarity for Data, Line Synchro and Frame Synchro
- Display Size up to 800 x 600
- Color Lookup Table with up to 256 entries
- Programmable Negative and Positive Row Striding
- DMA User interface uses Linked List Structure and Add-to-queue Structure

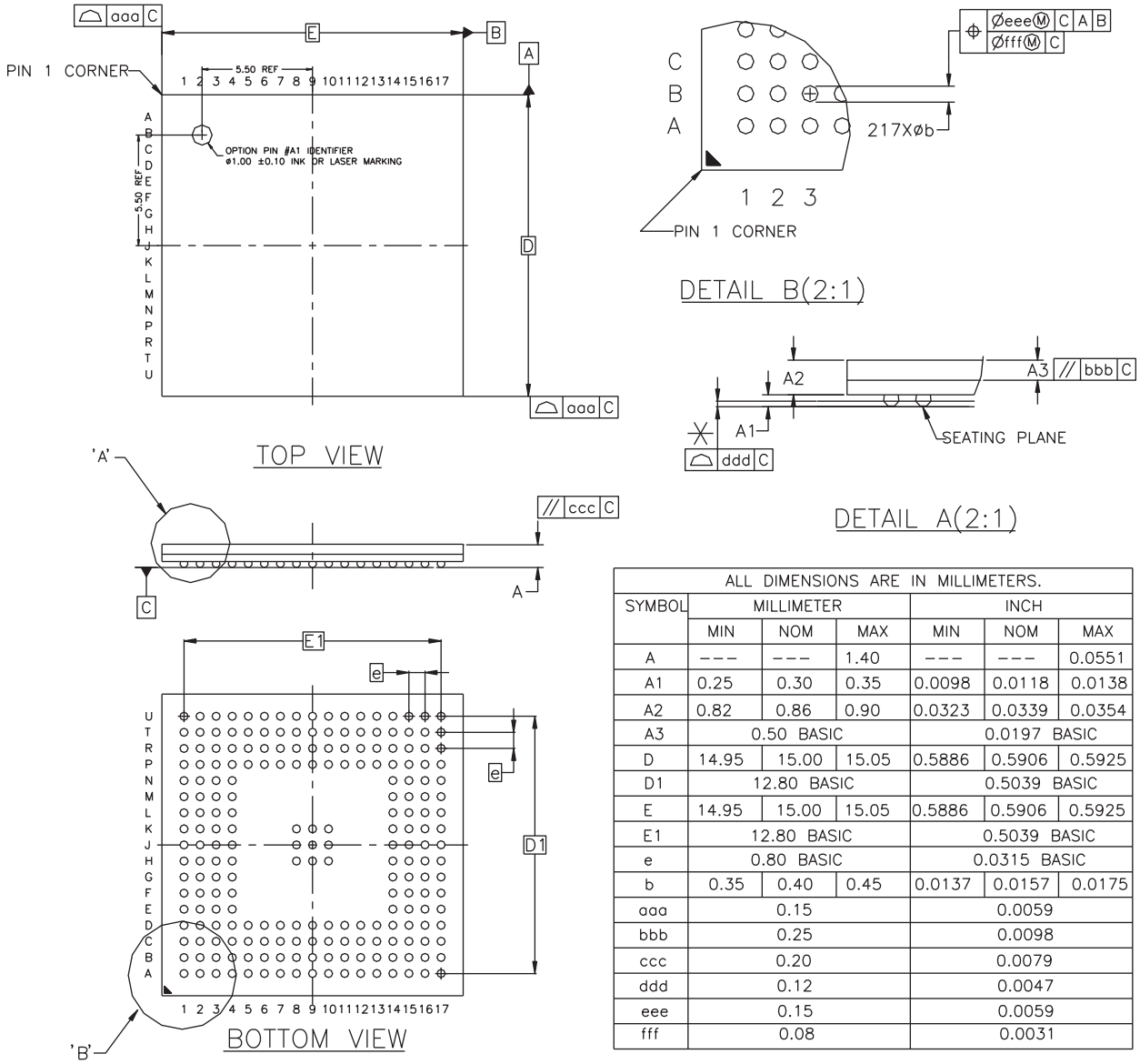
9.28 True Random Number Generator (TRNG)

- Passed NIST Special Publication 800-22 Tests Suite
- Passed Diehard Random Tests Suite
- Provides a 32-bit Random Number Every 84 Clock Cycles
- 50 Mbits/s throughput for 133 MHz Clock Frequency

10. Mechanical Characteristics

10.1 217-ball BGA Package

Figure 10-1. 217-ball BGA Package Drawing

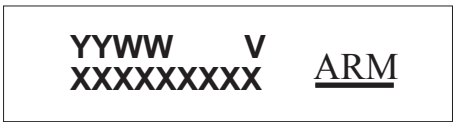


ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.0551
A1	0.25	0.30	0.35	0.0098	0.0118	0.0138
A2	0.82	0.86	0.90	0.0323	0.0339	0.0354
A3	0.50 BASIC			0.0197 BASIC		
D	14.95	15.00	15.05	0.5886	0.5906	0.5925
D1	12.80 BASIC			0.5039 BASIC		
E	14.95	15.00	15.05	0.5886	0.5906	0.5925
E1	12.80 BASIC			0.5039 BASIC		
e	0.80 BASIC			0.0315 BASIC		
b	0.35	0.40	0.45	0.0137	0.0157	0.0175
aaa	0.15			0.0059		
bbb	0.25			0.0098		
ccc	0.20			0.0079		
ddd	0.12			0.0047		
eee	0.15			0.0059		
fff	0.08			0.0031		

10.2 Marking

All devices are marked with the Atmel logo and the ordering code.

Additional marking may be in one of the following formats:



where

- “YY”: manufactory year
- “WW”: manufactory week
- “V”: revision
- “XXXXXXXXX”: lot number

11. AT91SAM9N12 Ordering Information

Table 11-1. AT91SAM9N12 Ordering Information

Ordering Code	Package	Package Type	Temperature Operating Range
AT91SAM9N12-CU	BGA217	Green	Industrial -40°C to 85°C

Revision History

In the tables that follow, the most recent version appears first. “rfo” denotes expert input during the update process.

Doc. Rev	Comments	Change Request Ref.
11096AS	First issue	

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