

High-Speed CAN Transceiver with Standby Mode CAN FD Ready

Features

- Fully ISO 11898-2, ISO 11898-5, and SAE J2284 Compliant
- CAN FD Ready
- Communication Speed up to 5 Mbps
- Low Electromagnetic Emission (EME) and High Electromagnetic Immunity (EMI)
- Differential Receiver with Wide Common-Mode Range
- ATA6560: Silent Mode (Receive Only)
- Remote Wake-Up Capability via CAN Bus
- Functional Behavior Predictable under All Supply Conditions
- Transceiver Disengages from the Bus when Not Powered Up
- RXD Recessive Clamping Detection
- High Electrostatic Discharge (ESD) Handling Capability on the Bus Pins
- Bus Pins Protected Against Transients in Automotive Environments
- Transmit Data (TXD) Dominant Time-Out Function
- Undervoltage Detection on VCC and VIO Pins
- CANH/CANL Short-Circuit and Overtemperature Protected
- Qualified According to AEC-Q100: Only ATA6560-GAQW, ATA6560-GBQW, ATA6561-GAQW, and ATA6561-GBQW
- Packages: SOIC8, VDFN8 with Wettable Flanks (Moisture Sensitivity Level 1)

Applications

Classical CAN and CAN FD networks in the following applications:

- Automotive
- Industrial
- Aerospace
- Medical
- Consumer

General Description

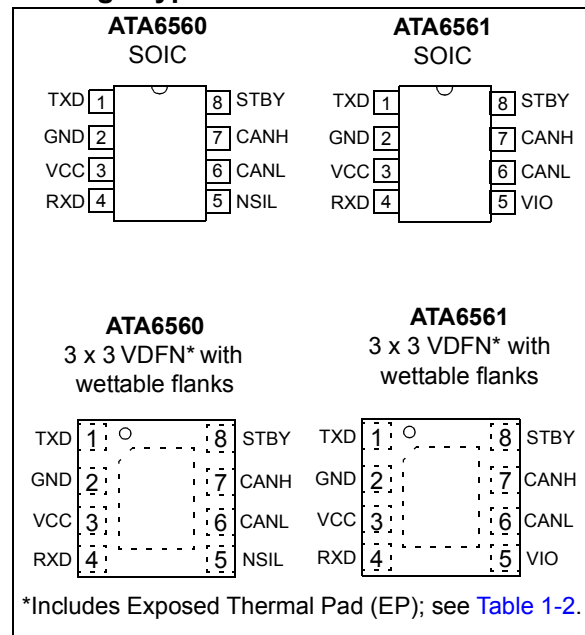
The ATA6560/1 is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed (up to 5 Mbps) CAN applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

It offers improved Electromagnetic Compatibility (EMC) and ESD performance, as well as features such as:

- Ideal passive behavior to the CAN bus when the supply voltage is off
- Direct interfacing to microcontrollers with supply voltages from 3V to 5V (ATA6561)

Three operating modes, together with the dedicated fail-safe features, make the ATA6560/1 an excellent choice for all types of high-speed CAN networks, especially in nodes requiring a Low-Power mode with wake-up capability via the CAN bus.

Package Types



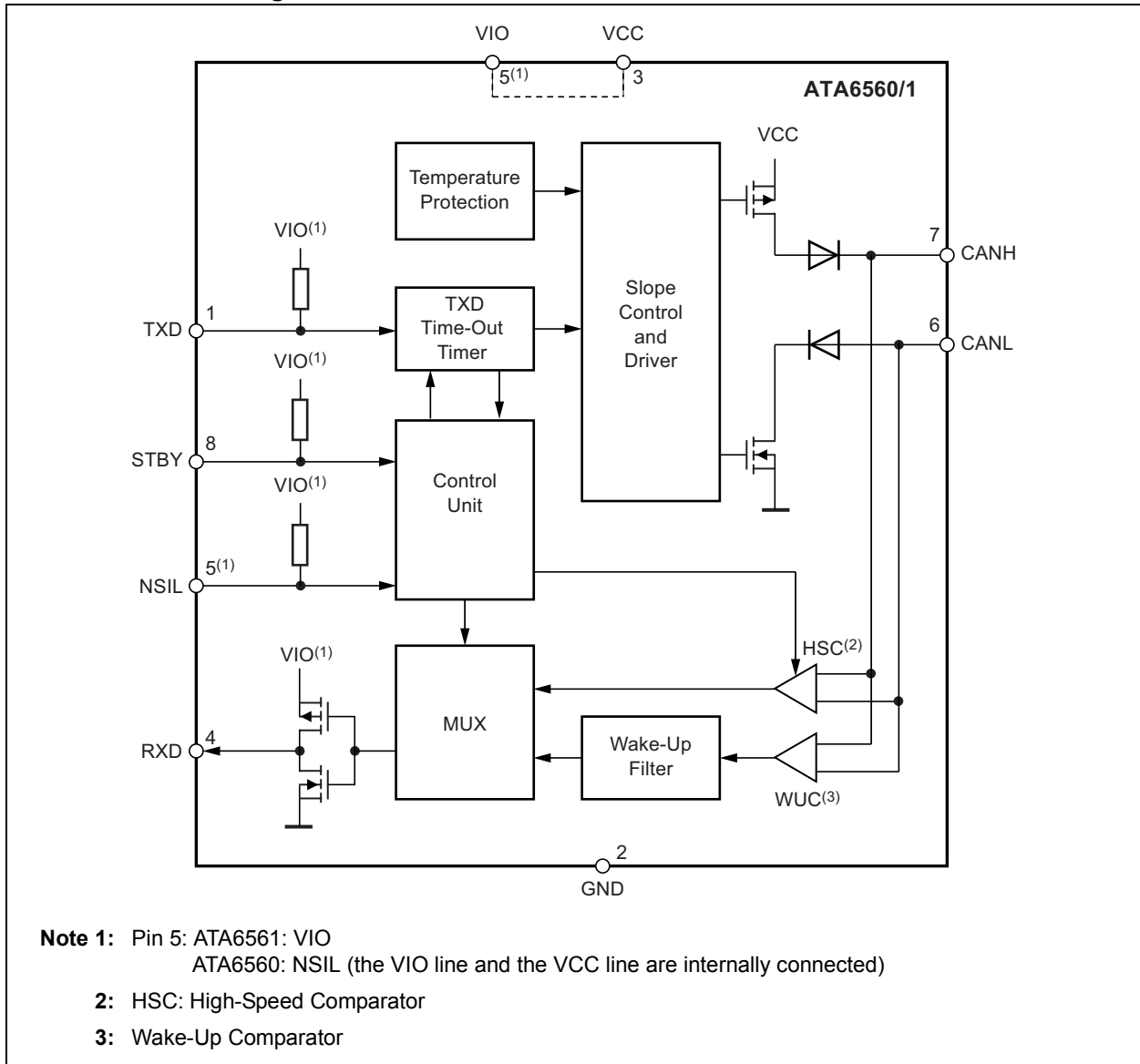
ATA6560/1

ATA6560/1 FAMILY MEMBERS

| Device | VIO Pin | NSIL Pin | VDFN8 | SOIC8 | AEC-Q100 Qualified | Description |
|----------------|---------|----------|-------|-------|--------------------|--|
| ATA6560-GAQW | | X | | X | X | Standby mode and Silent mode |
| ATA6560-GBQW | | X | X | | X | Standby mode and Silent mode |
| ATA6561-GAQW | X | | | X | X | Standby mode, VIO - pin for compatibility with 3.3V and 5V microcontroller |
| ATA6561-GBQW | X | | X | | X | Standby mode, VIO - pin for compatibility with 3.3V and 5V microcontroller |
| ATA6560-GAQW-N | | X | | X | | Standby mode and Silent mode |
| ATA6560-GBQW-N | | X | X | | | Standby mode and Silent mode |
| ATA6561-GAQW-N | X | | | X | | Standby mode, VIO - pin for compatibility with 3.3V and 5V microcontroller |
| ATA6561-GBQW-N | X | | X | | | Standby mode, VIO - pin for compatibility with 3.3V and 5V microcontroller |

Note: For ordering information, see the [Product Identification System](#) section.

Functional Block Diagram



ATA6560/1

1.0 FUNCTIONAL DESCRIPTION

The ATA6560/1 is a stand-alone, high-speed CAN transceiver, compliant with the ISO 11898-2 and ISO 11898-5 standards. It provides a very low current consumption in Standby mode and wake-up capability via the CAN bus. There are two versions available, only differing in the function of pin 5:

- ATA6560: Pin 5 is the control input for Silent mode NSIL, allowing the ATA6560 to only receive data and not send data via the bus. The output driver stage is disabled. The VIO line and the VCC line are internally connected; this sets the signal levels of the TXD, RXD, STBY, and NSIL pins to levels compatible with 5V microcontrollers.

- ATA6561: Pin 5 is the VIO pin and should be connected to the microcontroller supply voltage. This allows direct interfacing to microcontrollers with supply voltages down to 3V and adjusts the signal levels of the TXD, RXD, and STBY pins to the I/O levels of the microcontroller. The I/O ports are supplied by the VIO pin.

1.1 Operating Modes

The ATA6561 supports three operating modes: Unpowered, Standby, and Normal. The ATA6560 has an additional Silent mode. These modes can be selected via the STBY and NSIL pin. See Figure 1-1 and Table 1-1 for a description of the operating modes.

FIGURE 1-1: OPERATING MODES

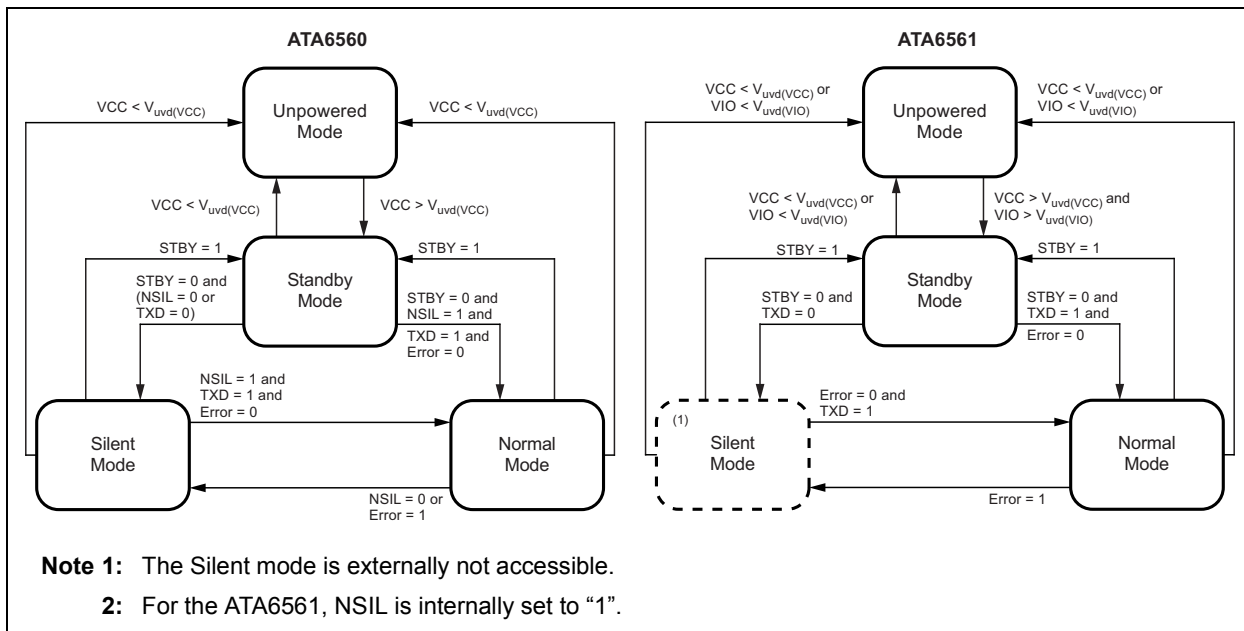


TABLE 1-1: OPERATING MODES

| Mode | Inputs | | | Outputs | |
|---------------------------|------------------|---------------------|------------------|------------|-----------------------|
| | STBY | NSIL | TXD | CAN Driver | RXD |
| Unpowered | X ⁽³⁾ | X ⁽³⁾ | X ⁽³⁾ | Recessive | Recessive |
| Standby | HIGH | X ⁽³⁾ | X ⁽³⁾ | Recessive | Active ⁽⁴⁾ |
| Silent (only for ATA6560) | LOW | LOW | X ⁽³⁾ | Recessive | Active ⁽¹⁾ |
| Normal | LOW | HIGH ⁽²⁾ | LOW | Dominant | LOW |
| | LOW | HIGH ⁽²⁾ | HIGH | Recessive | HIGH |

- Note 1:** LOW if the CAN bus is dominant, and HIGH if the CAN bus is recessive.
Note 2: Internally pulled up if not bonded out.
Note 3: Irrelevant.
Note 4: Reflects the bus only for wake-up.

1.1.1 NORMAL MODE

A low level on the STBY pin, together with a high level on pins TXD and NSIL, selects the Normal mode. In this mode, the transceiver can transmit and receive data via the CANH and CANL bus lines (see the “[Functional Block Diagram](#)”). The output driver stage is active and drives data from the TXD input to the CAN bus. The High-Speed Comparator (HSC) converts the analog data on the bus lines into digital data, which is output to pin RXD. The bus biasing is set to $V_{CC}/2$, and the undervoltage monitoring of VCC is active.

The slope of the output signals on the bus lines is controlled and optimized to ensure the lowest possible EME.

To switch the device to a normal operating mode, set the STBY pin to low and the TXD and NSIL pins (if applicable) to high (see [Table 1-1](#), [Figure 1-3](#), and [Figure 1-3](#)). Both the STBY and the NSIL pins provide a pull-up resistor to VIO, thus ensuring defined levels if the pins are open.

The device cannot enter the Normal mode as long as the TXD is at ground level. ATA6560 only switches to the Normal mode when all inputs are set accordingly.

FIGURE 1-2: SWITCHING FROM STANDBY MODE TO NORMAL MODE (NSIL = HIGH)

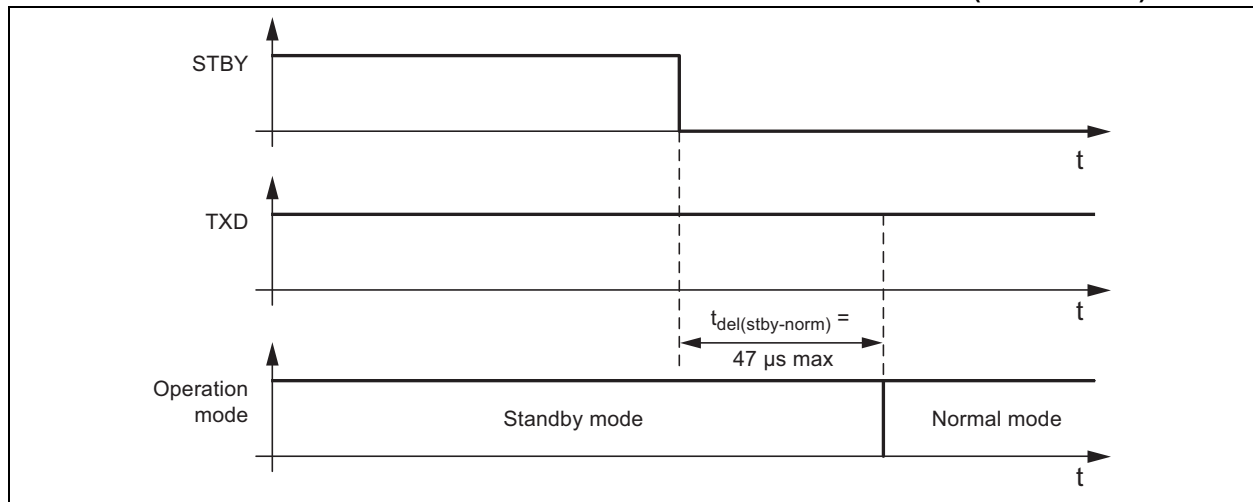
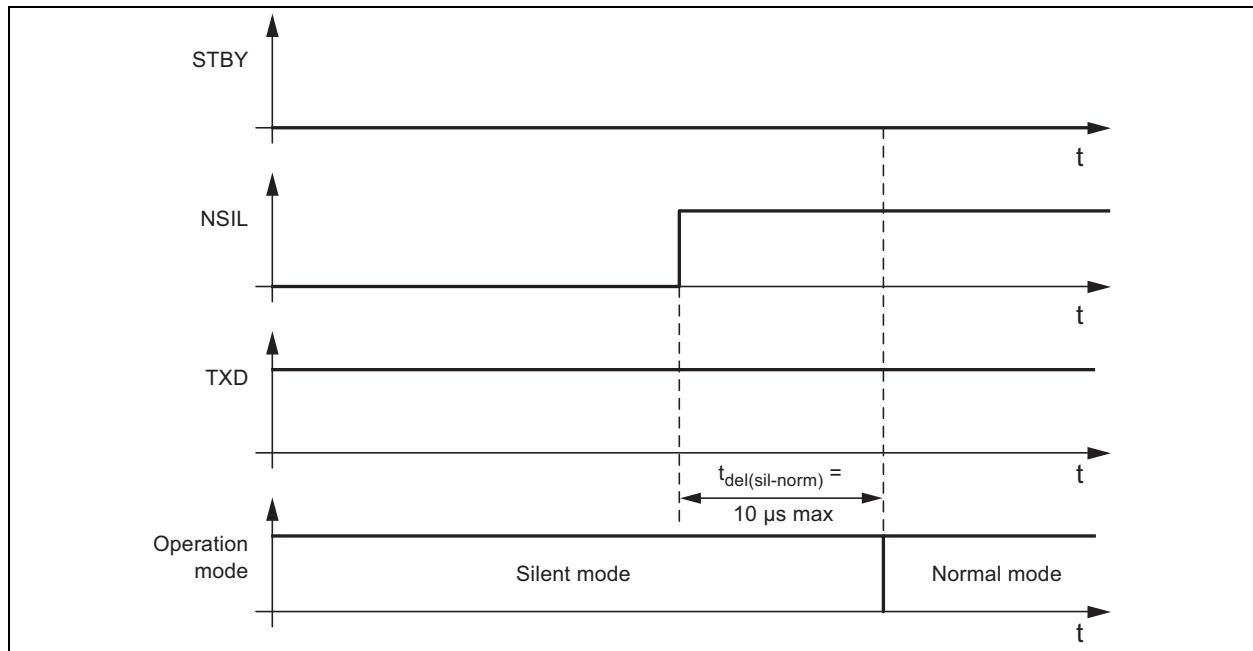


FIGURE 1-3: SWITCHING FROM SILENT MODE TO NORMAL MODE



1.1.2 SILENT MODE (ONLY FOR THE ATA6560)

A low level on the NSIL pin (available on pin 5) and on the STBY pin selects the Silent mode. This receive-only mode can be used to test the connection of the bus medium. In the Silent mode, the ATA6560 can still receive data from the bus, but the transmitter is disabled and therefore no data can be sent to the CAN bus. The bus pins are released to recessive state. All other IC functions, including the HSC, continue to operate as they do in the Normal mode. The Silent mode can be used to prevent a faulty CAN controller from disrupting all network communications.

1.1.3 STANDBY MODE

A high level on the STBY pin selects the Standby mode. In this mode, the transceiver cannot transmit or correctly receive data via the bus lines. The transmitter and the HSC are switched off to reduce current consumption, and only the low-power Wake-Up Comparator (WUC) monitors the bus lines for a valid wake-up signal. A signal change on the bus from “Recessive” to “Dominant,” followed by a dominant state longer than t_{wake} , switches the RXD pin to low to signal a wake-up request to the microcontroller.

In the Standby mode, the bus lines are biased to ground to reduce current consumption to a minimum. The WUC monitors the bus lines for a valid wake-up signal. When the RXD pin switches to low to signal a wake-up request, a transition to the Normal mode is not triggered until the microcontroller forces back the STBY pin to low. A bus dominant time-out timer prevents the device from generating a permanent wake-up request by switching the RXD pin to high.

For ATA6560 only: If the NSIL input pin is set to low in the Standby mode, the internal pull-up resistor causes an additional quiescent current from VIO to GND. Microchip recommends setting the NSIL pin to high in the Standby mode.

1.2 Fail-Safe Features

1.2.1 TXD DOMINANT TIME-OUT FUNCTION

A TXD dominant time-out timer is started when the TXD pin is set to low. If the low state on the TXD pin persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to a recessive state. This function prevents a hardware failure, software application failure, or both from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when the TXD pin is set to high ($\geq 4 \mu s$).

1.2.2 INTERNAL PULL-UP STRUCTURE AT TXD, NSIL, AND STBY INPUT PINS

The TXD, STBY, and NSIL pins have an internal pull-up to VIO. This ensures a safe, defined state in case one or all of these pins are left floating. Pull-up currents flow in these pins in all states, meaning all pins should be in a high state during the Standby mode to minimize the current consumption.

1.2.3 UNDERVOLTAGE DETECTION ON PINS VCC AND VIO

If V_{VCC} or V_{VIO} drops below its undervoltage detection level ($V_{uvd(VCC)}$ and $V_{uvd(VIO)}$, see [Section 2.0 “Electrical Characteristics”](#)), the transceiver switches off and disengages from the bus until V_{VCC} and V_{VIO} have recovered. The low-power WUC is only switched off during a VCC or VIO undervoltage. The logic state of the STBY pin is ignored until the VCC voltage or the VIO voltage has recovered.

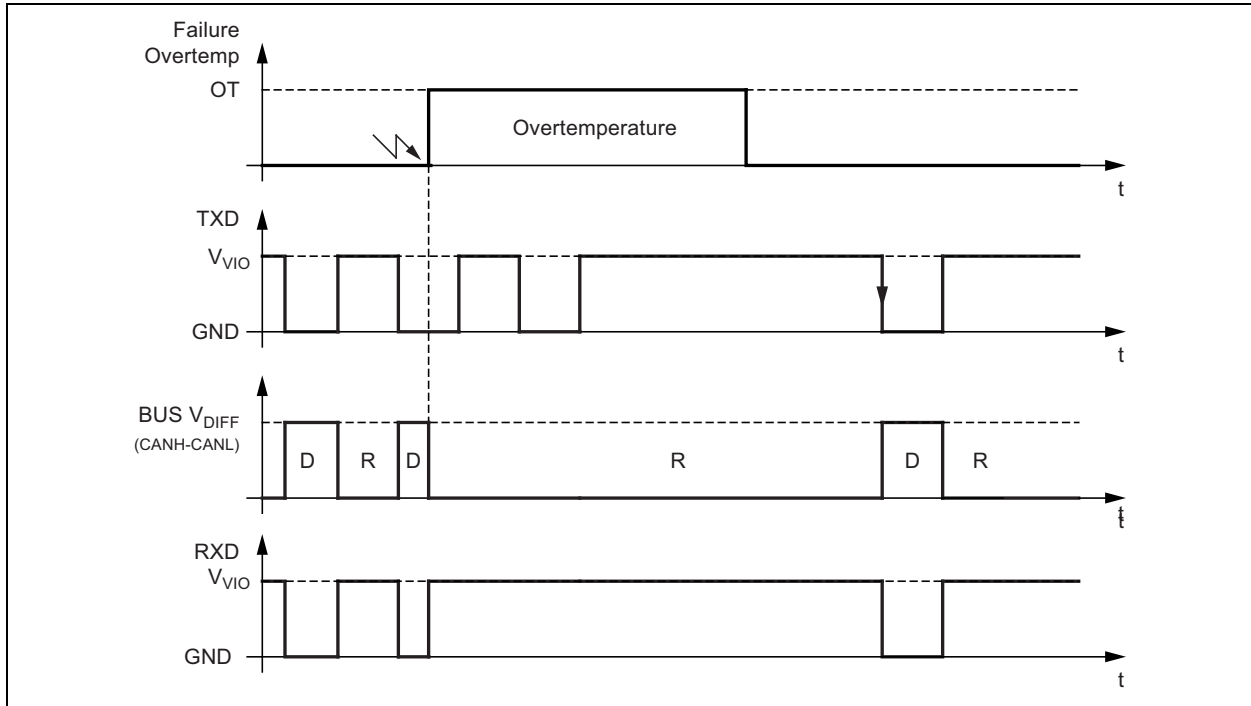
1.2.4 BUS WAKE-UP TIME-OUT FUNCTION

In the Standby mode, a bus wake-up time-out timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than t_{to_bus} , the RXD pin is switched to high. This function prevents a clamped dominant bus (due to a bus short circuit or a failure in one of the other nodes on the network) from generating a permanent wake-up request. The bus wake-up time-out timer is reset when the CAN bus changes from dominant to recessive state.

1.2.5 OVERTEMPERATURE PROTECTION

The output drivers are protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature, T_{Jsd} , the output drivers are disabled until the junction temperature drops below T_{Jsd} and pin TXD is at a high level again. The TXD condition ensures that output driver oscillations due to temperature drift are avoided.

FIGURE 1-4: RELEASE OF TRANSMISSION AFTER OVERTEMPERATURE CONDITION



1.2.6 SHORT-CIRCUIT PROTECTION OF THE BUS PINS

The CANH and CANL bus outputs are short-circuit protected, either against GND or a positive supply voltage. A current-limiting circuit protects the transceiver against damage. If the device heats up due to a continuous short on CANH or CANL, the internal overtemperature protection switches the bus transmitter off.

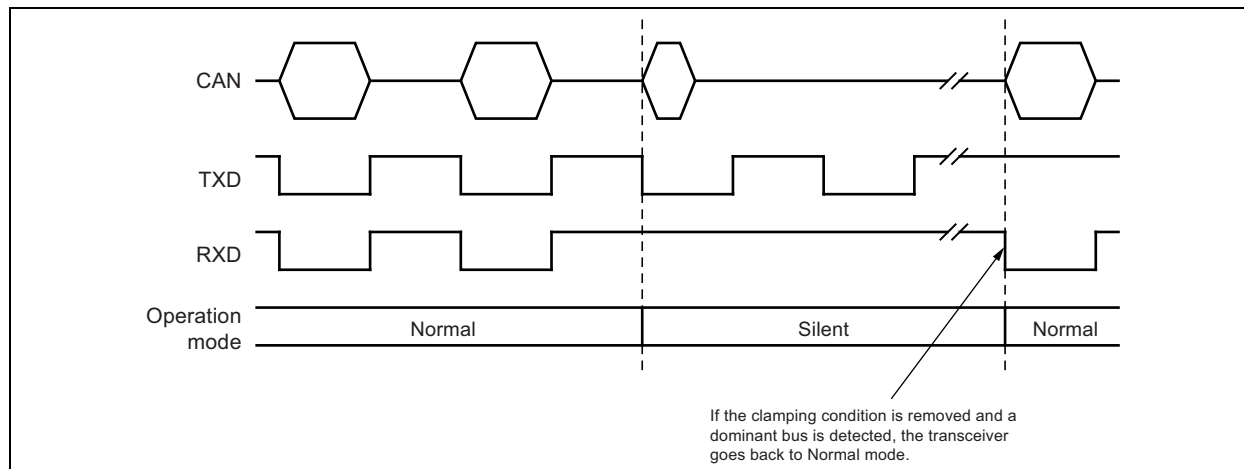
1.2.7 RXD RECESSIVE CLAMPING

This fail-safe feature prevents the controller from sending data on the bus if its RXD line is clamped to high (for example, recessive). That is, if the RXD pin cannot signal a dominant bus condition (for example, because it is shorted to VCC), the transmitter within the ATA6560/1 is disabled to avoid possible data collisions on the bus. In Normal and Silent modes (only for the ATA6560), the device permanently compares the state of the HSC to the state of the RXD pin.

If the HSC indicates a dominant bus state for more than t_{RC_det} , without the RXD pin doing the same, a recessive clamping situation is detected and the device is forced into the Silent mode. This Fail-Safe mode is released by entering either the Standby or the Unpowered mode or if the RXD pin is showing a dominant (for example, low) level again.

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FIGURE 1-5: RXD RECESSIVE CLAMPING DETECTION



1.3 Pin Description

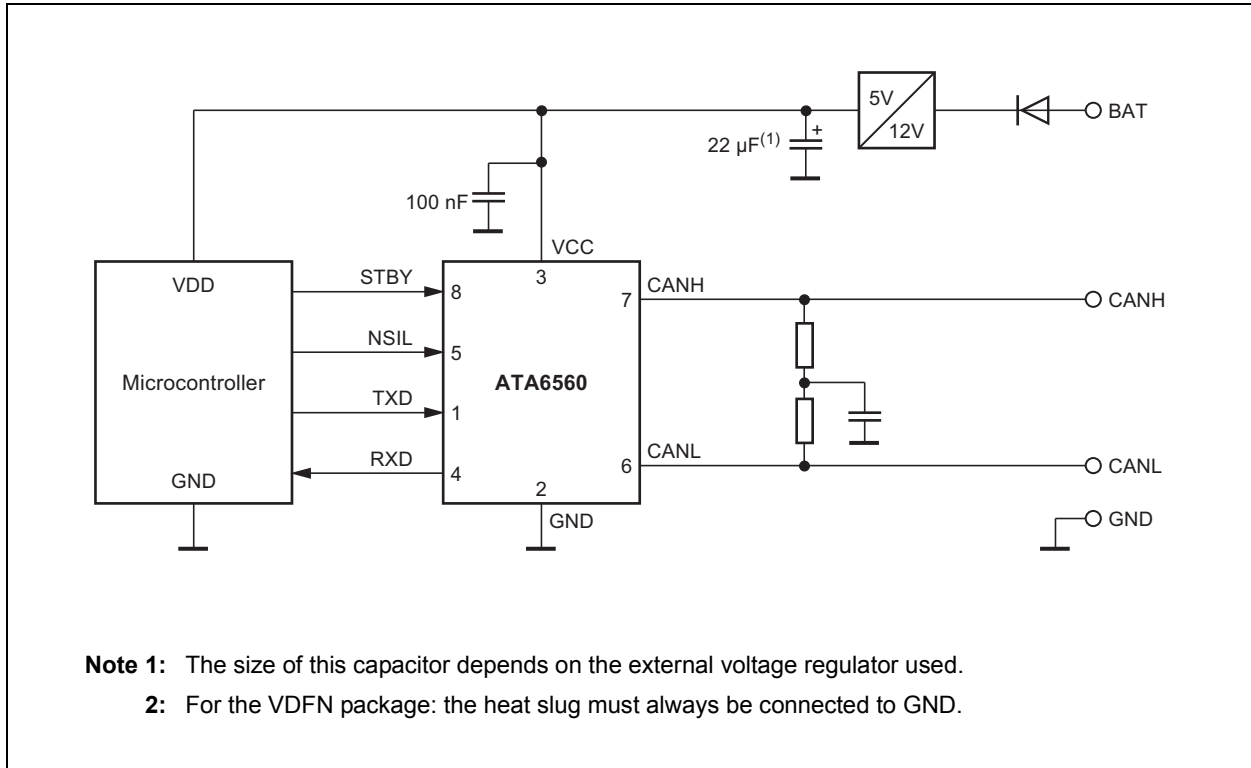
The descriptions of the pins are listed in [Table 1-2](#).

TABLE 1-2: PIN FUNCTION TABLE

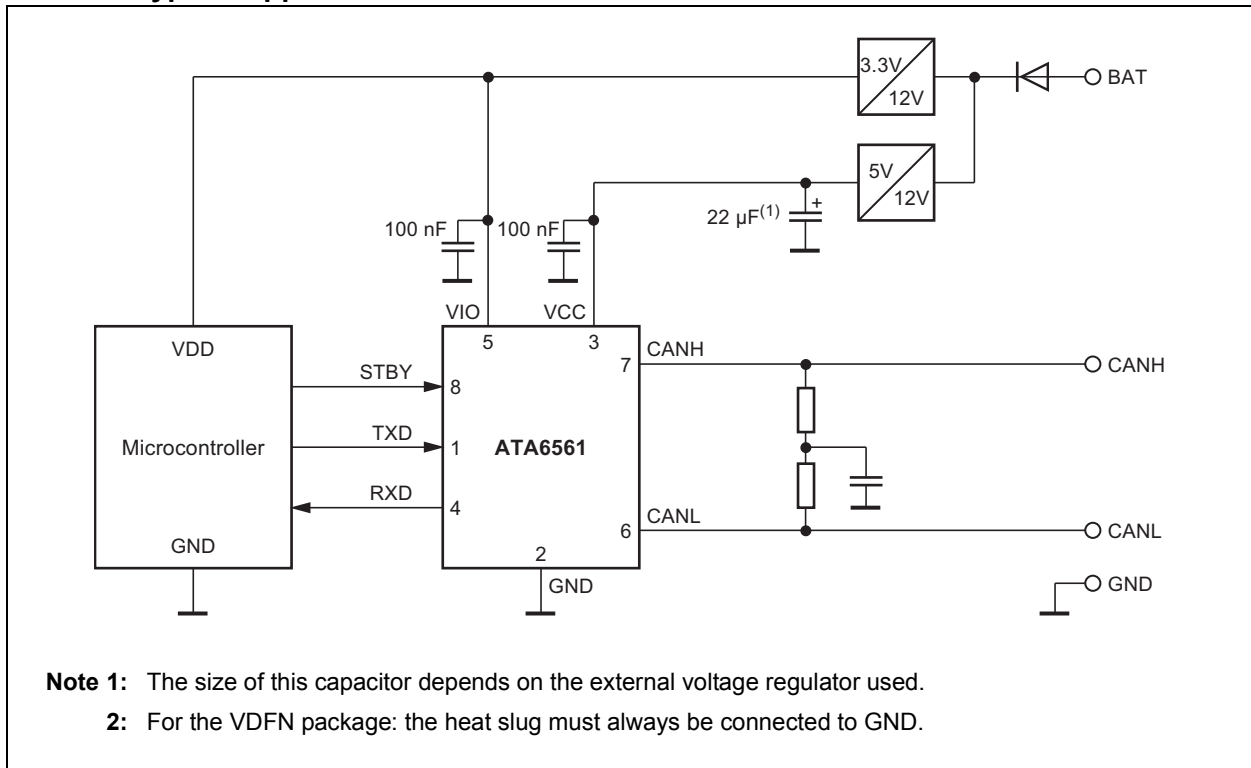
| ATA6560 | | ATA6561 | | Symbol | Description |
|---------|-------|---------|-------|--------|--|
| SOIC8 | VDFN8 | SOIC8 | VDFN8 | | |
| 1 | 1 | 1 | 1 | TXD | Transmit Data Input |
| 2 | 2 | 2 | 2 | GND | Ground Supply |
| 3 | 3 | 3 | 3 | VCC | Supply Voltage |
| 4 | 4 | 4 | 4 | RXD | Receive Data Output; reads out data from the bus lines |
| — | — | 5 | 5 | VIO | Supply Voltage for the I/O Level Adapter; the VIO and VCC lines are internally connected |
| 5 | 5 | — | — | NSIL | Silent Mode Control Input (low active) |
| 6 | 6 | 6 | 6 | CANL | Low-Level CAN Bus Line |
| 7 | 7 | 7 | 7 | CANH | High-Level CAN Bus Line |
| 8 | 8 | 8 | 8 | STBY | Standby Mode Control Input |
| — | 9 | — | 9 | EP | Exposed Thermal Pad; heat slug, internally connected to the GND pin |

1.4 Typical Application

ATA6560 Typical Application



ATA6561 Typical Application



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2.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

| | |
|---|---------------|
| DC Voltage at CANH, CANL (V_{CANH} , V_{CANL}) | -27 to +42V |
| Transient Voltage at CANH, CANL (according to ISO 7637 part 2) (V_{CANH} , V_{CANL}) | -150 to +100V |
| DC Voltage on all other pins (V_X) | -0.3 to +5.5V |
| ESD according to IBEE CAN EMC - Test specification following IEC 61000-4-2 — Pin CANH, CANL | ±8 kV |
| ESD (HBM following STM5.1 with 1.5 kΩ/100 pF) - Pins CANH, CANL to GND | ±6 kV |
| Component-Level ESD (HBM according to ANSI/ESD STM5.1, JESD22-A114, AEC-Q100 (002) | ±4 kV |
| CDM ESD STM 5.3.1 | ±750V |
| ESD Machine Model AEC-Q100-RevF(003) | ±200V |
| Virtual Junction Temperature (T_{vj}) | -40 to +150°C |
| Storage Temperature Range (T_{stg}) | -55 to +150°C |

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: $T_{vj} = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; $V_{VCC} = 4.5\text{V}$ to 5.5V ; $V_{VIO} = 2.8\text{V}$ to 5.5V ; $R_L = 60\Omega$, $C_L = 100\text{pF}$, unless otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|-----------------|------|------|------|-------|--|
| Supply, Pin VCC | | | | | | |
| Supply Voltage | V_{VCC} | 4.5 | — | 5.5 | V | |
| Supply Current in Silent Mode | I_{VCC_sil} | 1.9 | 2.5 | 3.2 | mA | Silent mode, $V_{TXD} = V_{VIO}$ |
| Supply Current in Normal Mode | I_{VCC_rec} | 2 | — | 5 | mA | Recessive, $V_{TXD} = V_{VIO}$ |
| | I_{VCC_dom} | 20 | 50 | 70 | mA | Dominant, $V_{TXD} = 0\text{V}$ |
| Supply Current in Standby Mode | I_{VCC_STBY} | — | — | 12 | μA | $V_{VCC} = V_{VIO}$, $V_{TXD} = V_{NSIL} = V_{VIO}$ |
| | I_{VCC_STBY} | — | 7 | — | μA | $T_a = +25^{\circ}\text{C}$ (Note 3) |
| Undervoltage Detection Threshold on Pin VCC | $V_{uvd(VCC)}$ | 2.75 | — | 4.5 | V | |
| I/O Level Adapter Supply, Pin VIO (only for the ATA6561) | | | | | | |
| Supply Voltage on Pin VIO | V_{VIO} | 2.8 | — | 5.5 | V | |
| Supply Current on Pin VIO | I_{IO_rec} | 10 | 80 | 250 | μA | Normal and Silent modes Recessive, $V_{TXD} = V_{VIO}$ |
| | I_{IO_rdom} | 50 | 350 | 500 | μA | Normal and Silent modes Dominant, $V_{TXD} = 0\text{V}$ |
| | I_{IO_STBY} | — | — | 1 | μA | Standby mode |
| Undervoltage Detection Threshold on Pin VIO | $V_{uvd(VIO)}$ | 1.3 | — | 2.7 | V | |

Note 1: This parameter is 100% correlation tested.

Note 2: This parameter is ensured by characterization on samples.

Note 3: This parameter is ensured by design.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: $T_{VJ} = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; $V_{VCC} = 4.5\text{V}$ to 5.5V ; $V_{VIO} = 2.8\text{V}$ to 5.5V ; $R_L = 60\Omega$, $C_L = 100\text{pF}$, unless otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|--|------------------|----------------------|----------------------|----------------------|---------------|---|
| Mode Control Input, Pin NSIL and STBY | | | | | | |
| High-Level Input Voltage | V_{IH} | $0.7 \times V_{VIO}$ | — | $V_{VIO} + 0.3$ | V | |
| Low-Level Input Voltage | V_{IL} | -0.3 | — | $0.3 \times V_{VIO}$ | V | |
| Pull-Up Resistor to VIO | R_{pu} | 75 | 125 | 175 | k Ω | $V_{STBY} = 0\text{V}$, $V_{NSIL} = 0\text{V}$ |
| High-Level Leakage Current | I_L | -2 | — | +2 | μA | $V_{STBY} = V_{VIO}$, $V_{NSIL} = V_{VIO}$ |
| CAN Transmit Data Input, Pin TXD | | | | | | |
| High-Level Input Voltage | V_{IH} | $0.7 \times V_{VIO}$ | — | $V_{VIO} + 0.3$ | V | |
| Low-Level Input Voltage | V_{IL} | -0.3 | — | $0.3 \times V_{VIO}$ | V | |
| Pull-Up Resistor to VIO | R_{TXD} | 20 | 35 | 50 | k Ω | $V_{TXD} = 0\text{V}$ |
| High-Level Leakage Current | I_{TXD} | -2 | — | +2 | μA | Normal mode, $V_{TXD} = V_{VIO}$ |
| Input Capacitance | C_{TXD} | — | 5 | 10 | pF | Note 3 |
| CAN Receive Data Output, Pin RXD | | | | | | |
| High-Level Output Current | I_{OH} | -8 | — | -1 | mA | Normal mode, $V_{RXD} = V_{VIO} - 0.4\text{V}$, $V_{VIO} = V_{VCC}$ |
| Low-Level Output Current | I_{OL} | 2 | — | 12 | mA | Normal mode, $V_{RXD} = 0.4\text{V}$, bus dominant |
| Bus Lines, Pins CANH and CANL | | | | | | |
| Dominant Output Voltage | I_{IO} | 2.75 | 3.5 | 4.5 | V | $V_{TXD} = 0\text{V}$, $t < t_{to(dom)TXD}$ pin CANH |
| | | 0.5 | 1.5 | 2.25 | V | $V_{TXD} = 0\text{V}$, $t < t_{to(dom)TXD}$ pin CANL |
| Transmitter Dominant Voltage Symmetry | $V_{dom(TX)sym}$ | $0.9 \times V_{VCC}$ | — | $1.1 \times V_{VCC}$ | V | $V_{dom(TX)sym} = V_{CANH} + V_{CANL}$ (Note 1) |
| Bus Differential Output Voltage | $V_{O(diff)bus}$ | 1.5 | — | 3 | V | $V_{TXD} = 0\text{V}$, $t < t_{to(dom)TXD}$ $R_L = 45\Omega$ to 65Ω |
| | | -50 | — | +50 | mV | $V_{VCC} = 4.75\text{V}$ to 5.25V $V_{TXD} = V_{VIO}$, receive, no load |
| Recessive Output Voltage | $V_{O(rec)}$ | 2 | $0.5 \times V_{VCC}$ | 3 | V | Normal and Silent modes, $V_{TXD} = V_{VIO}$, no load |
| | | -0.1 | — | +0.1 | V | Standby mode, $V_{TXD} = V_{VIO}$, no load |

Note 1: This parameter is 100% correlation tested.

2: This parameter is ensured by characterization on samples.

3: This parameter is ensured by design.

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: $T_{VJ} = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; $V_{VCC} = 4.5\text{V}$ to 5.5V ; $V_{VIO} = 2.8\text{V}$ to 5.5V ; $R_L = 60\Omega$, $C_L = 100\text{pF}$, unless otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---------------------|------|------|------|---------------|--|
| Differential Receiver Threshold Voltage | $V_{th(RX)dif}$ | 0.5 | 0.7 | 0.9 | V | Normal and Silent modes (HSC), $V_{cm(CAN)} = -27\text{V}$ to $+27\text{V}$ |
| | | 0.4 | 0.7 | 1 | V | Standby mode (WUC), $V_{cm(CAN)} = -27\text{V}$ to $+27\text{V}$ (Note 1) |
| Differential Receiver Hysteresis Voltage (HSC) | $V_{hys(RX)dif}$ | 50 | 120 | 200 | mV | Normal and Silent modes (HSC), $V_{cm(CAN)} = -27\text{V}$ to $+27\text{V}$ (Note 1) |
| Dominant Output Current | $I_{IO(dom)}$ | -100 | — | -35 | mA | $V_{TXD} = 0\text{V}$, $t < t_{to(dom)TXD}$, $V_{VCC} = 5\text{V}$, pin CANH, $V_{CANH} = 0\text{V}$ |
| | | 35 | — | 100 | mA | $V_{TXD} = 0\text{V}$, $t < t_{to(dom)TXD}$, $V_{VCC} = 5\text{V}$, pin CANL, $V_{CANL} = 5\text{V}/40\text{V}$ |
| Recessive Output Current | $I_{IO(rec)}$ | -5 | — | +5 | mA | Normal and Silent modes, $V_{TXD} = V_{VIO}$, no load, $V_{CANH} = V_{CANL} = -27\text{V}$ to $+32\text{V}$ |
| Leakage Current | $I_{IO(rec)}$ | -5 | 0 | +5 | μA | $V_{VCC} = V_{VIO} = 0\text{V}$, $V_{CANH} = V_{CANL} = 5\text{V}$ |
| Input Resistance | R_i | 9 | 15 | 28 | k Ω | |
| Input Resistance Deviation | ΔR_i | -1 | 0 | +1 | % | Between V_{CANH} and V_{CANL} |
| Differential Input Resistance | $R_{i(dif)}$ | 19 | 30 | 56 | k Ω | |
| | | 20 | 30 | 56 | k Ω | $T_{VJ} < +125^{\circ}\text{C}$ |
| Common-Mode Input Capacitance | $C_{i(cm)}$ | — | — | 20 | pF | Note 3 |
| Differential Input Capacitance | $C_{i(dif)}$ | — | — | 10 | pF | Note 3 |
| Transceiver Timing, Pins CANH, CANL, TXD, and RXD, see Figure 2-1 and Figure 2-2 | | | | | | |
| Delay Time from TXD to Bus Dominant | $t_{d(TXD-busdom)}$ | 40 | — | 130 | ns | Normal mode (Note 2) |
| Delay Time from TXD to Bus Recessive | $t_{d(TXD-busrec)}$ | 40 | — | 130 | ns | Normal mode (Note 2) |
| Delay Time from Bus Dominant to RXD | $t_{d(busdom-RXD)}$ | 20 | — | 100 | ns | Normal and Silent modes (Note 2) |
| Delay Time from Bus Recessive to RXD | $t_{d(busrec-RXD)}$ | 20 | — | 100 | ns | Normal and Silent modes (Note 2) |

Note 1: This parameter is 100% correlation tested.

Note 2: This parameter is ensured by characterization on samples.

Note 3: This parameter is ensured by design.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: $T_{VJ} = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; $V_{VCC} = 4.5\text{V}$ to 5.5V ; $V_{VIO} = 2.8\text{V}$ to 5.5V ; $R_L = 60\Omega$, $C_L = 100\text{ pF}$, unless otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|--|----------------------|------|------|------|---------------|--|
| Propagation Delay from TXD to RXD | $t_{PD(TXD-RXD)}$ | 40 | — | 210 | ns | Normal mode, Rising edge at pin TXD |
| | | 40 | — | 200 | ns | Normal mode, Falling edge at pin TXD |
| | $t_{PD(TXD-RXD)}$ | — | — | 300 | ns | Normal mode, Rising edge at pin TXD $R_L = 120\Omega$, $C_L = 200\text{ pF}$ (Note 3) |
| | | — | — | 300 | ns | Normal mode, Falling edge at pin TXD $R_L = 120\Omega$, $C_L = 200\text{ pF}$ (Note 3) |
| TXD Dominant Time-Out Time | $t_{to(dom)TXD}$ | 0.8 | — | 3 | ms | $V_{TXD} = 0\text{V}$, Normal mode |
| Bus Wake-Up Time-Out Time | t_{to_bus} | 0.8 | — | 3 | ms | Standby mode |
| Minimum Dominant/Recessive Bus Wake-Up Time | t_{wake} | 0.75 | 3 | 5 | μs | Standby mode |
| Delay Time for Standby Mode to Normal Mode Transition | $t_{del(stby-norm)}$ | — | — | 47 | μs | Falling edge at pin STBY NSIL = HIGH |
| Delay Time for Normal Mode to Standby Mode Transition | $t_{del(norm-stby)}$ | — | — | 5 | μs | Rising edge at pin STBY NSIL = HIGH (Note 3) |
| Delay Time for Normal Mode to Silent Mode Transition | $t_{del(norm-sil)}$ | — | — | 10 | μs | Falling edge at pin NSIL STBY = LOW (Note 3) |
| Delay Time for Silent Mode to Normal Mode Transition | $t_{del(sil-norm)}$ | — | — | 10 | μs | Rising edge at pin NSIL STBY = LOW (Note 3) |
| Delay Time for Silent Mode to Standby Mode Transition | $t_{del(sil-stby)}$ | — | — | 5 | μs | Rising edge at pin STBY NSIL = LOW (Note 3) |
| Delay Time for Standby Mode to Silent Mode Transition | $t_{del(stby-sil)}$ | — | — | 47 | μs | Rising edge at pin STBY NSIL = LOW (Note 3) |
| Debouncing Time for Recessive Clamping State Detection | t_{RC_det} | — | 90 | — | ns | $V_{(CANH-CANL)} > 900\text{ mV}$ RXD = HIGH (Note 3) |
| Transceiver Timing for higher Bit Rates, Pins CANH, CANL, TXD, and RXD, see Figure 2-1 and Figure 2-3 | | | | | | |
| Recessive Bit Time on Pin RXD | $t_{Bit(RXD)}$ | 400 | — | 550 | ns | Normal mode, $t_{Bit(TXD)} = 500\text{ ns}$ (Note 3) |
| | | 120 | — | 220 | ns | Normal mode, $t_{Bit(TXD)} = 200\text{ ns}$ |

- Note 1:** This parameter is 100% correlation tested.
Note 2: This parameter is ensured by characterization on samples.
Note 3: This parameter is ensured by design.

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TEMPERATURE SPECIFICATIONS

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|-------------|------|------|------|-------|------------|
| 8-Lead SOIC | | | | | | |
| Thermal Resistance Virtual Junction to Ambient | R_{thvJA} | — | 145 | — | K/W | |
| Thermal Shutdown of Bus Drivers | T_{Jsd} | 150 | 175 | 195 | °C | |
| 8-Lead VDFN | | | | | | |
| Thermal Resistance Virtual Junction to Heat Slug | R_{thvJC} | — | 10 | — | K/W | |
| Thermal Resistance Virtual Junction to Ambient, where Heat Slug is Soldered to PCB According to JEDEC | R_{thvJA} | — | 50 | — | K/W | |
| Thermal Shutdown of Bus Drivers | T_{Jsd} | 150 | 175 | 195 | °C | |

FIGURE 2-1: TIMING TEST CIRCUIT FOR THE ATA6560/1 CAN TRANSCEIVER

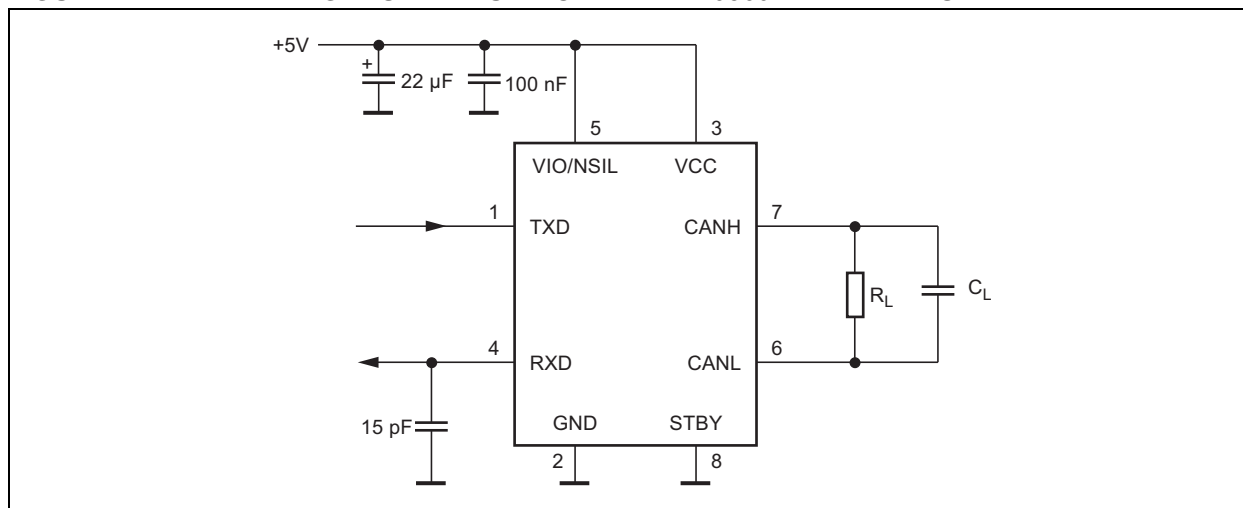


FIGURE 2-2: CAN TRANSCEIVER TIMING DIAGRAM

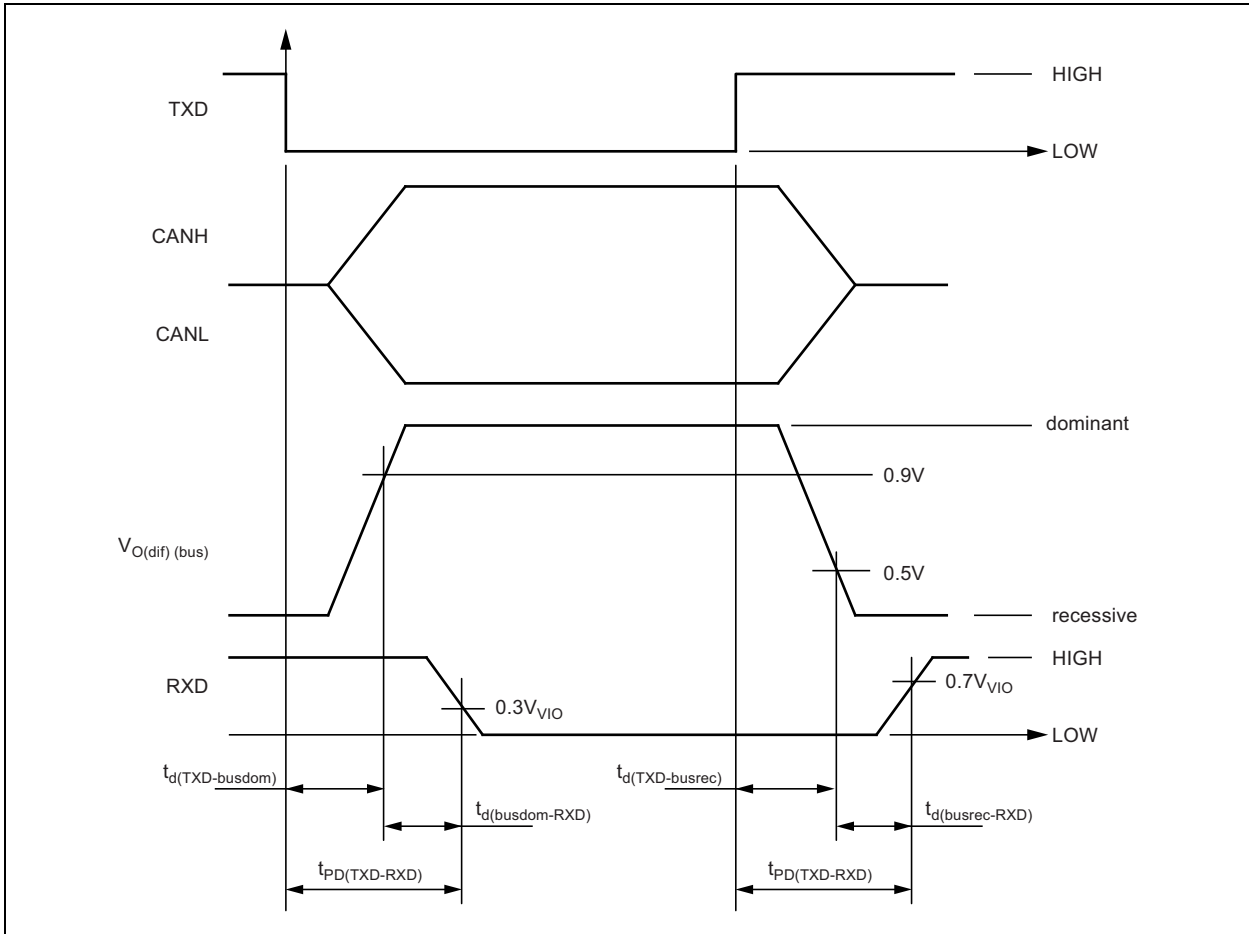
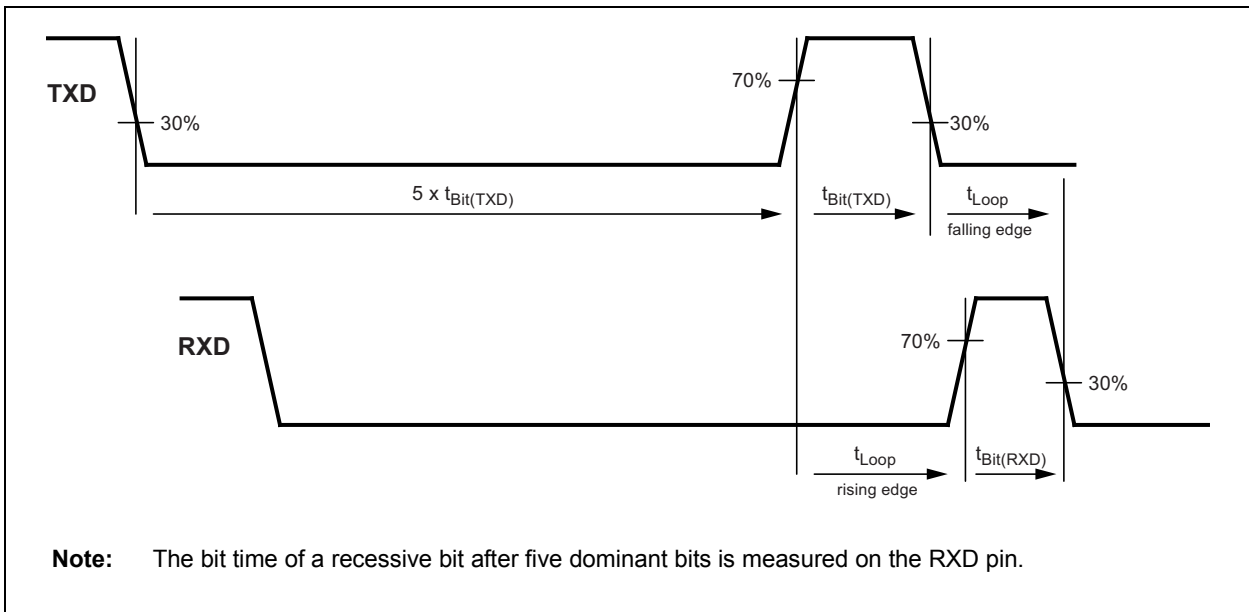


FIGURE 2-3: CAN TRANSCEIVER TIMING DIAGRAM FOR LOOP DELAY SYMMETRY

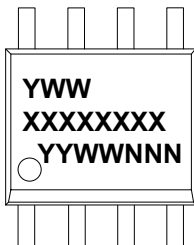


ATA6560/1

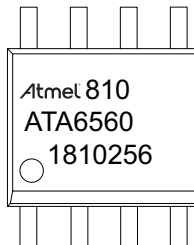
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

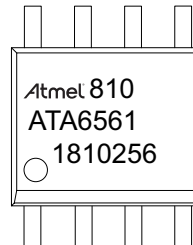
8-Lead SOIC



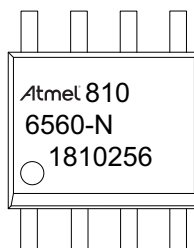
Example ATA6560



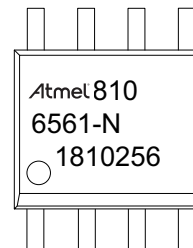
Example ATA6561



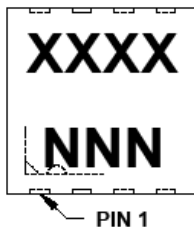
Example ATA6560
Industrial type



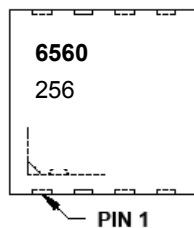
Example ATA6561
Industrial type



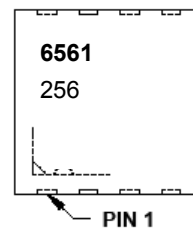
8-Lead 3 x 3 mm VDFN



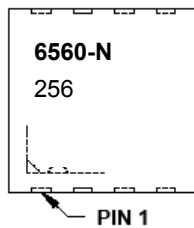
Example ATA6560



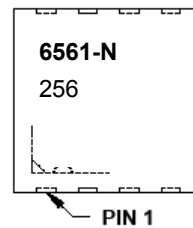
Example ATA6561



Example ATA6560
Industrial type



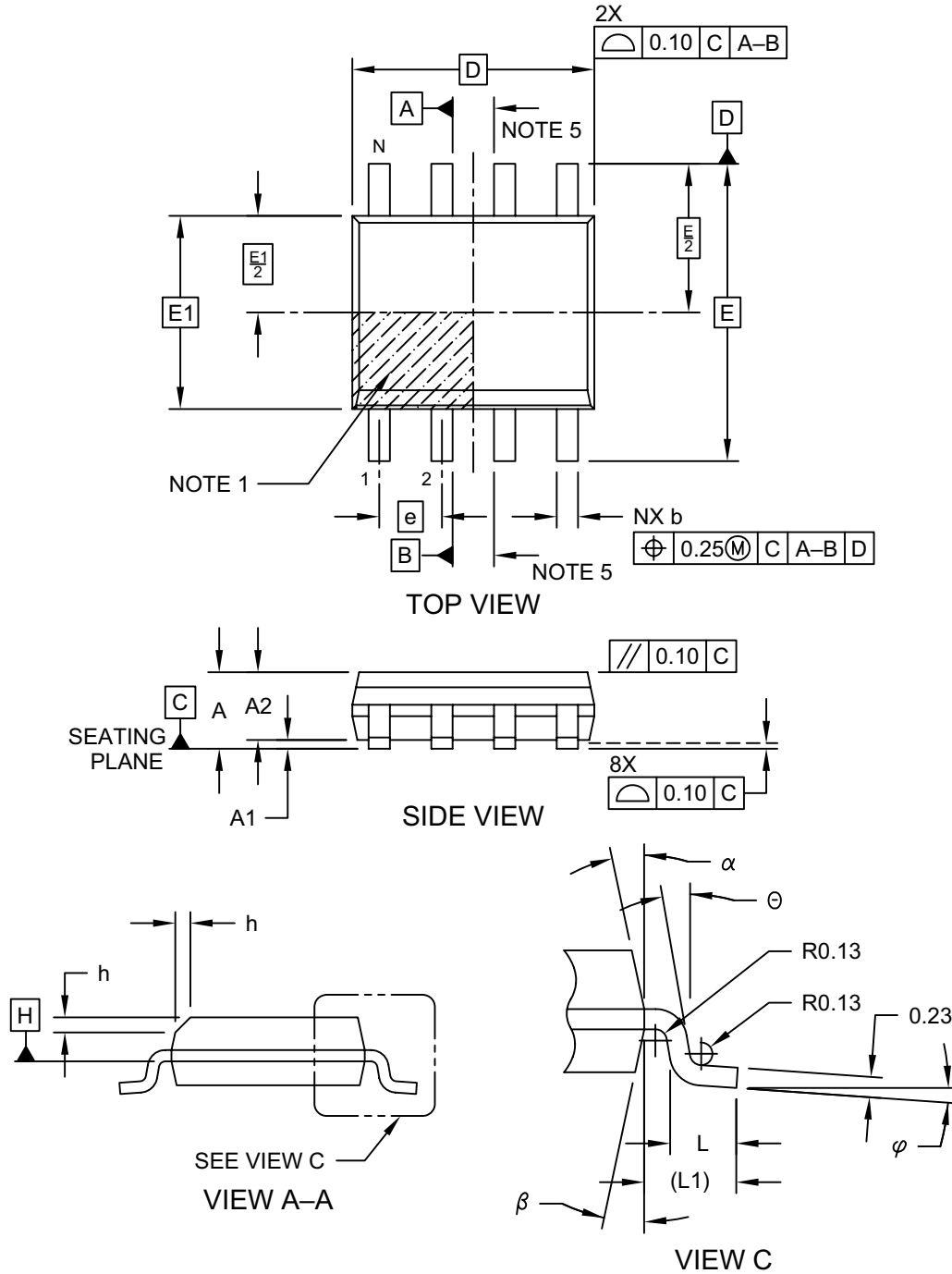
Example ATA6561
Industrial type



| | | |
|----------------|---|--|
| Legend: | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | (e3) | This package is Pb-free. The Pb-free JEDEC designator () can be found on the outer packaging for this package. (e3) |
| Note: | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. | |

8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

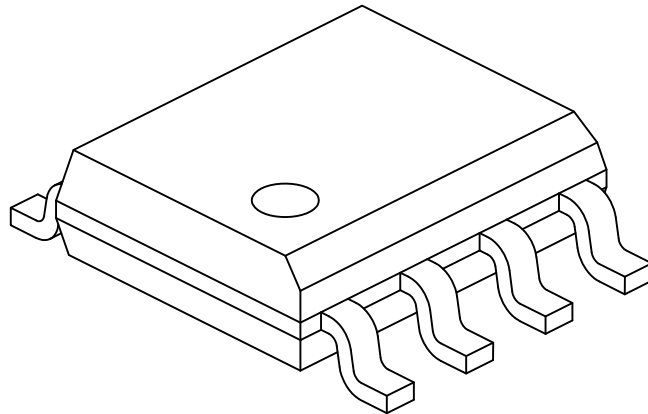


Microchip Technology Drawing No. C04-057-OA Rev E Sheet 1 of 2

ATA6560/1

8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| | | Units | MILLIMETERS | | |
|--------------------------|----|-------|-------------|-----|------|
| Dimension Limits | | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | | |
| Pitch | e | | 1.27 BSC | | |
| Overall Height | A | - | - | - | 1.75 |
| Molded Package Thickness | A2 | 1.25 | - | - | - |
| Standoff § | A1 | 0.10 | - | - | 0.25 |
| Overall Width | E | | 6.00 BSC | | |
| Molded Package Width | E1 | | 3.90 BSC | | |
| Overall Length | D | | 4.90 BSC | | |
| Chamfer (Optional) | h | 0.25 | - | - | 0.50 |
| Foot Length | L | 0.40 | - | - | 1.27 |
| Footprint | L1 | | 1.04 REF | | |
| Foot Angle | φ | 0° | - | - | 8° |
| Lead Thickness | c | 0.17 | - | - | 0.25 |
| Lead Width | b | 0.31 | - | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | - | 15° |

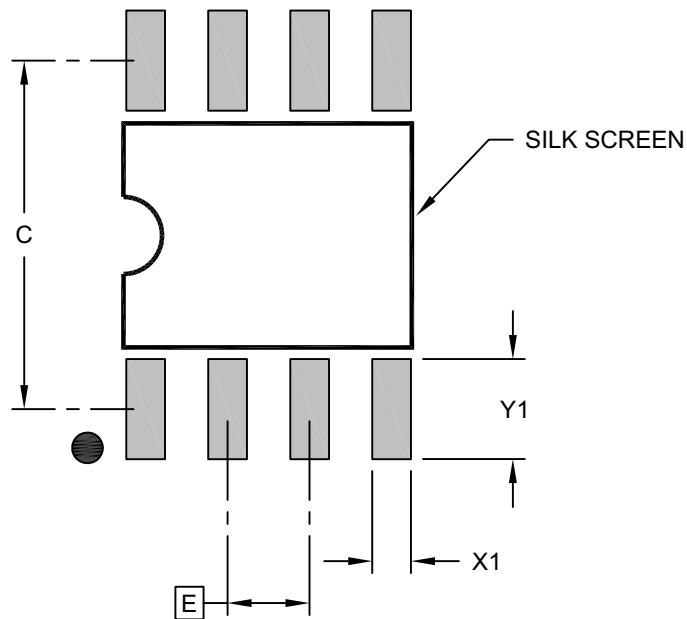
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-OA Rev E Sheet 2 of 2

8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|-------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

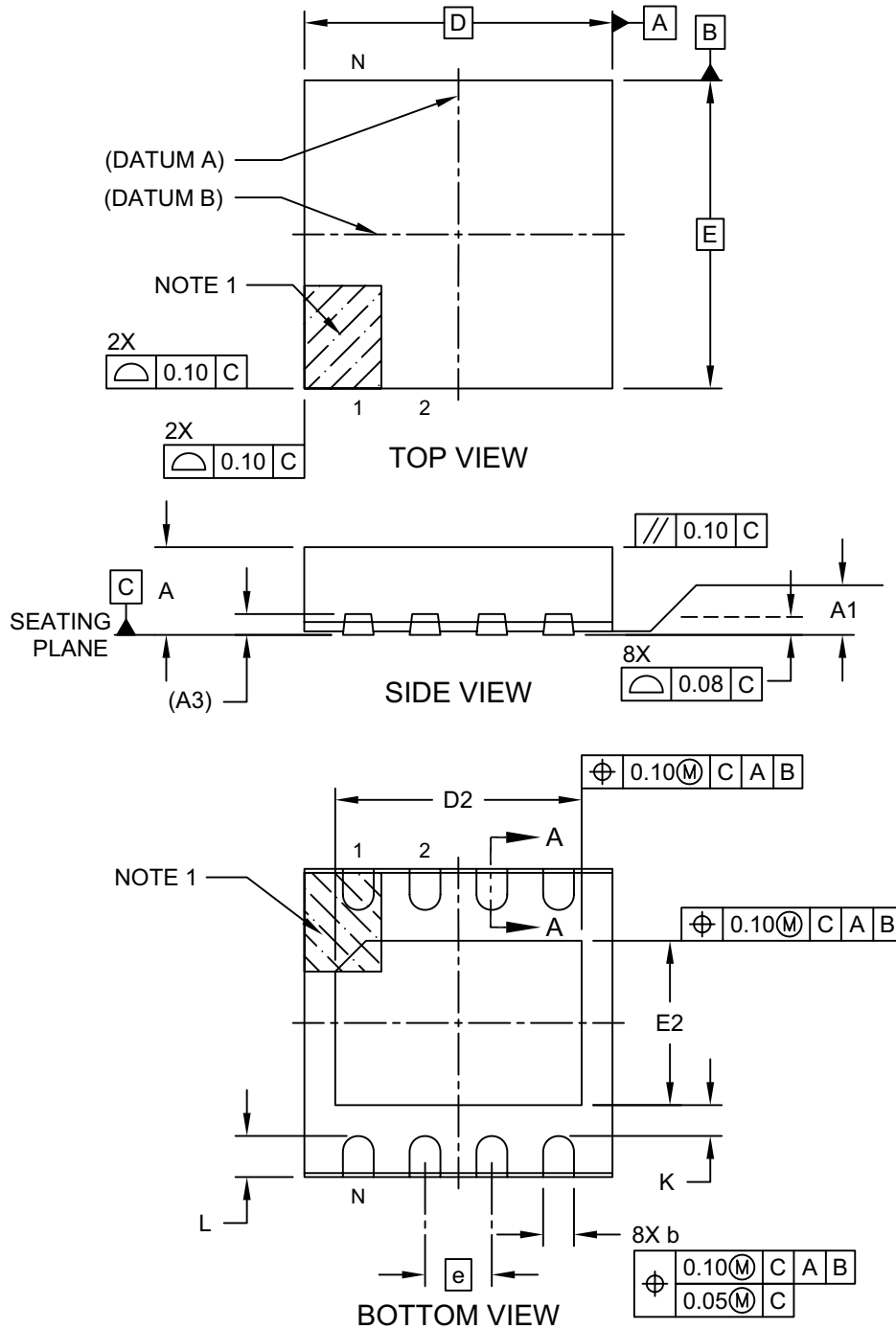
1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-OA Rev E

ATA6560/1

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy YCL

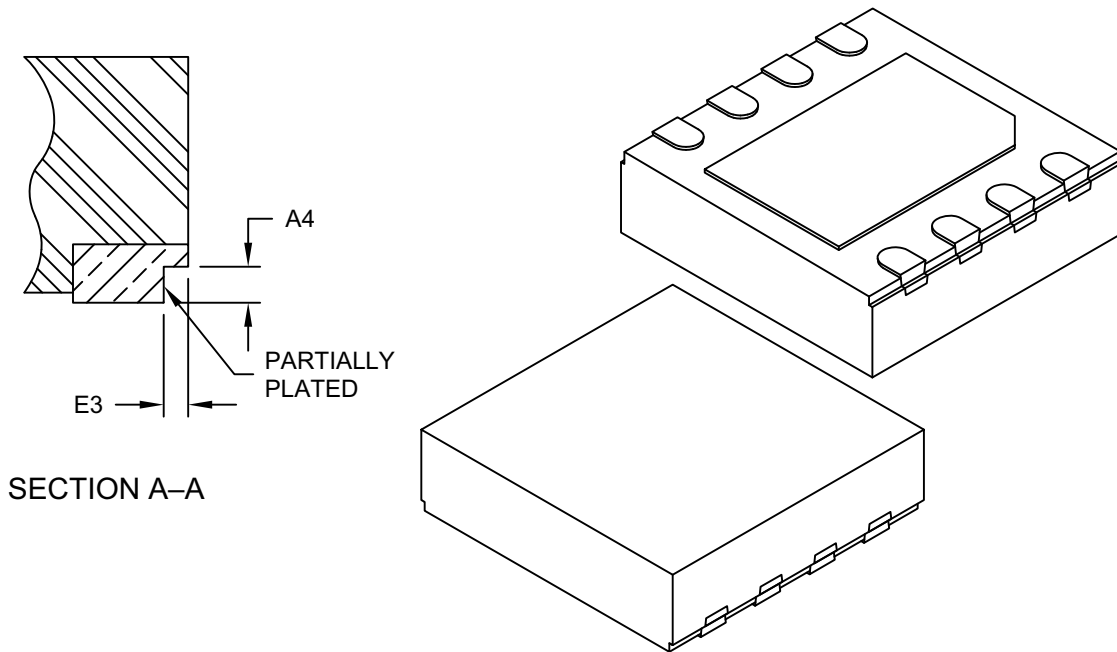
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-21358 Rev C Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy YCL

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|-------------------------------|-------|-------------|-------|-------|
| | | MIN | NOM | MAX |
| Number of Terminals | N | 8 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.035 | 0.05 |
| Terminal Thickness | A3 | 0.203 REF | | |
| Overall Length | D | 3.00 BSC | | |
| Exposed Pad Length | D2 | 2.30 | 2.40 | 2.50 |
| Overall Width | E | 3.00 BSC | | |
| Exposed Pad Width | E2 | 1.50 | 1.60 | 1.70 |
| Terminal Width | b | 0.25 | 0.30 | 0.35 |
| Terminal Length | L | 0.35 | 0.40 | 0.45 |
| Terminal-to-Exposed-Pad | K | 0.20 | - | - |
| Wettable Flank Step Cut Depth | A4 | 0.10 | - | 0.19 |
| Wettable Flank Step Cut Width | E3 | - | - | 0.085 |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

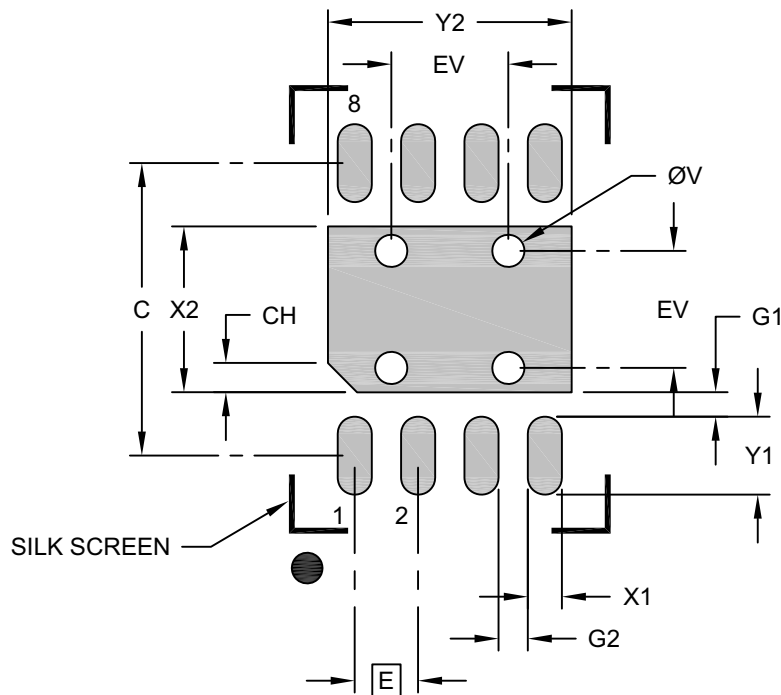
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21358 Rev C Sheet 2 of 2

ATA6560/1

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|---------------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Optional Center Pad Width | X2 | | | 1.70 |
| Optional Center Pad Length | Y2 | | | 2.50 |
| Contact Pad Spacing | C | | 3.00 | |
| Contact Pad Width (X8) | X1 | | | 0.35 |
| Contact Pad Length (X8) | Y1 | | | 0.80 |
| Contact Pad to Center Pad (X8) | G1 | 0.20 | | |
| Contact Pad to Contact Pad (X6) | G2 | 0.20 | | |
| Pin 1 Index Chamfer | CH | 0.20 | | |
| Thermal Via Diameter | V | | 0.33 | |
| Thermal Via Pitch | EV | | 1.20 | |

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23358 Rev C

APPENDIX A: REVISION HISTORY

Revision B (November 2019)

- Updated the Supply Current in Silent Mode parameter in the [Electrical Characteristics](#) table.
- Various typographical edits.

Revision A (April 2018)

- Original release of this document.
- This document replaces Atmel - 9288J-AUTO-04/15.
- Added Industrial types.
- Added table [ATA6560/1 Family Members](#).

ATA6560/1

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| PART NO. | - | XX | X ⁽¹⁾ | X | - | X |
|--|---------|----------------------|-----------------------------------|----------------|---|---|
| Device | Package | Tape and Reel Option | Package Directives Classification | Device Variant | | |
| Device: ATA6560/1: High-Speed CAN Transceiver with Standby Mode – CAN FD Ready | | | | | | |
| Package: GA = 8-Lead SOIC GB = 8-Lead VDFN | | | | | | |
| Tape and Reel Option: Q = 330 mm diameter Tape and Reel | | | | | | |
| Package Directives Classification: W = Package according to RoHS ⁽²⁾ | | | | | | |
| Device Variant N = Device Variant N (Industrial type) | | | | | | |
| Examples: | | | | | | |
| a) ATA6560-GAQW: ATA6560, 8-Lead SOIC, Qualified according to AEC-Q100, Tape and Reel, Package according to RoHS | | | | | | |
| b) ATA6560-GBQW: ATA6560, 8-Lead VDFN, Qualified according to AEC-Q100, Tape and Reel, Package according to RoHS | | | | | | |
| c) ATA6561-GAQW: ATA6561, 8-Lead SOIC, Qualified according to AEC-Q100, Tape and Reel, Package according to RoHS | | | | | | |
| d) ATA6561-GBQW: ATA6561, 8-Lead VDFN, Qualified according to AEC-Q100, Tape and Reel, Package according to RoHS | | | | | | |
| e) ATA6560-GAQW-N: ATA6560, 8-Lead SOIC, Tape and Reel, Package according to RoHS, Industrial type | | | | | | |
| f) ATA6560-GBQW-N: ATA6560, 8-Lead VDFN, Tape and Reel, Package according to RoHS, Industrial type | | | | | | |
| g) ATA6561-GAQW-N: ATA6561, 8-Lead SOIC, Tape and Reel, Package according to RoHS, Industrial type | | | | | | |
| h) ATA6561-GBQW-N: ATA6561, 8-Lead VDFN, Tape and Reel, Package according to RoHS, Industrial type | | | | | | |
| Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option. | | | | | | |
| 2: RoHS compliant; maximum concentration value of 0.09% (900 ppm) for Bromine (Br) and Chlorine (Cl) and less than 0.15% (1500 ppm) total Bromine (Br) and Chlorine (Cl) in any homogeneous material. Maximum concentration value of 0.09% (900 ppm) for Antimony (Sb) in any homogeneous material. | | | | | | |

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