

## Features

- ISO 26262 Functional Safety Ready up to ASIL B and IEC 61508 Ready up to SIL 2
- CAN FD Transceiver Fully Compliant to ISO 11898-2: 2016 and SAE J2284-1 to SAE J2284-5
  - Autonomous Bus Biasing according to ISO 11898-2: 2016
  - Standard CAN nominal bit rate up to 1 Mbit/s and CAN FD data bit rate up to 5 Mbit/s
  - TXD dominant time-out function
  - Differential Bus Receiver with Wide Common-Mode Range
  - RXD recessive clamping detection
  - The CAN transceiver disengages from the bus in overtemperature shutdown and Low-Power Supply mode
  - Bus pins short-circuit protected to GND and VCC
- LIN transceiver(s) according to ISO 17987-4 and SAE J2602-2
  - TXD dominant time-out timer
  - Bus pin short-circuit protected versus GND and battery
- 4 Mbit/s SPI Interface
- Low Electromagnetic Emission (EME) and High Electromagnetic Immunity (EMI)
- High Electrostatic Discharge (ESD) Handling Capability on the Bus Pins
- Very Low Current Consumption in Sleep and Standby Mode with Full Wake-up Capability
- Five Operating Modes:
  - Power-Off mode
  - Microcontroller Reset mode
  - Sleep mode
  - Standby mode
  - Normal mode
- Various Wake-up Sources:
  - CAN remote wake-up pattern according to ISO 11898-2:2016
  - CAN remote wake-up frame according to ISO 11898-2:2016 (selective wake up, ATA6585/6/7/8 only)
  - Local wake up via pin WAKE and WAKE2
  - 2x LIN bus remote wake up
  - Host wake up via SPI
- Wake-up Source Recognition
- Undervoltage Detection on VS, VCC and VCC\_SENSOR Pins
- CAN, LIN, VCC and VCC\_SENSOR Regulators Overtemperature Protection and Selective Overtemperature Shutdown
- Battery Supply and Bus Pins Protected Against Transients According to ISO 7637

- $V_{VS}$  Operating Voltage up to 28V,  $V_{VS}$  DC Supply Voltage up to 40V
- Watchdog with  $\mu C$  Independent Clock Source
  - Watchdog can be operated in window and Time-Out mode
  - Optional cyclic wake up in Watchdog Time-Out mode
  - Watchdog period selectable
  - Watchdog reset pulse length selectable
- Limp Home (LH) – VCC Independent High-voltage Failure Output
- 5V 150 mA Low Dropout Voltage Regulator - VCC LDO
  - $\pm 2\%$  accuracy
  - Current limitation above 160 mA
  - Max.  $R_{DSon}$  of output transistor  $5\Omega$
  - Short-circuit protected
- Second 5V/3.3V 85 mA Low Dropout Voltage Regulator ( $VCC_{\mu C}$  - ATA6582/3/7/8 only)
  - $\pm 2\%$  accuracy
  - Current limitation above 120 mA
- 5V/3.3V 30 mA Sensor Supply Voltage –  $VCC_{SENSOR}$ 
  - $\pm 2\%$  accuracy
  - Current limitation above 30 mA
  - Output voltage level configurable via SPI
  - Excellent transient response with a ceramic output load capacitor
  - Protected against short-circuits to GND and to the battery
  - High ESD robustness
- Input/Output Reset Pin (NRES) with Variable Reset Length to Support a Variety of Microcontrollers
- AEC-Q100 Qualified
- Two Ambient Temperature Grades Available:
  - ATA658x-GTQW1-VAO and ATA658x-GUQW1-VAO up to  $T_{amb} = +125\text{ }^{\circ}\text{C}$
  - ATA658x-GTQW0-VAO up to  $T_{amb} = +150\text{ }^{\circ}\text{C}$
- CAN FD Transceiver Fully Compliant to SAE J2962-2
- LIN Transceivers Fully Compliant to SAE J2962-1
- Fulfills the OEM “*Hardware Requirements for CAN Interfaces in Automotive Applications*”, Rev. 1.3
- Fulfills the OEM “*Requirements for Partial Networking*”, Rev. 2.2
- 18-Lead VDFN Package and 26-Lead VDFN Package with Wetable Flanks (Moisture Sensitivity Level 1)
- Pin and Footprint Compatibility for the Complete Family

## Description

The ATA658x device family includes 8 products:

- ATA6580/85: A CAN System Basis Chip (SBC): one CAN transceiver without or with CAN Partial Networking combined with a 5V 150 mA low drop voltage regulator and a 5V/3.3V 30 mA sensor supply
- ATA6581/86: A CAN-LIN System Basis Chip (SBC): one CAN transceiver without or with Partial Networking, one LIN transceiver, a 5V 150 mA low drop voltage regulator and a 5V/3.3V 30 mA sensor supply

- ATA6582/87: A CAN-LIN-LIN System Basis Chip (SBC): one CAN transceiver without or with Partial Networking, two LIN- transceivers, a 5V 150 mA low drop voltage regulator, a second 5V 85 mA low drop voltage regulator, a 5V/3.3V 30 mA sensor supply
- ATA6583/88: A CAN-LIN-LIN System Basis Chip (SBC): one CAN transceiver without or with Partial Networking, two LIN- transceivers, a 5V 150 mA low drop voltage regulator, a second 3.3V 85 mA low drop voltage regulator, a 5V/3.3V 30 mA sensor supply

The high speed (up to 5 Mbit/s) ISO 11898-2: 2016 compliant CAN transceiver is designed for applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller. It offers improved electromagnetic compatibility (EMC) and electrostatic discharge (ESD) performance, very low- power consumption as well as features such as:

- Ideal Passive Behavior to the CAN Bus when the Supply Voltage is Off
- Direct Interfacing to Microcontrollers with Supply Voltages 3.3V/5V
- Advanced Low-power Management with Local and Remote Wake-up Support, Always Available, even when the VCC Output is Switched Off
- Protection and Diagnostic Functions Including Bus Line Short-circuit Detection and Battery Connection Detection

The LIN transceiver is designed according to the LIN specification 2.0, 2.1, 2.2, 2.2A, ISO 17987-4 and SAE J2602-2, and is able to handle the low-speed data communication in vehicles (for example, in convenience electronics). Improved slope control at the LIN driver ensures reliable data communication up to 20 kbit/s.

All devices from this family offer low-power modes in order to minimize current consumption on applications that are permanently connected to the battery. A wake up from the low-power modes is possible via a message on the buses, or via high-voltage wake-up pins / or via SPI (only for ATA6582/3/7/8 and only when VCC\_μC is active).

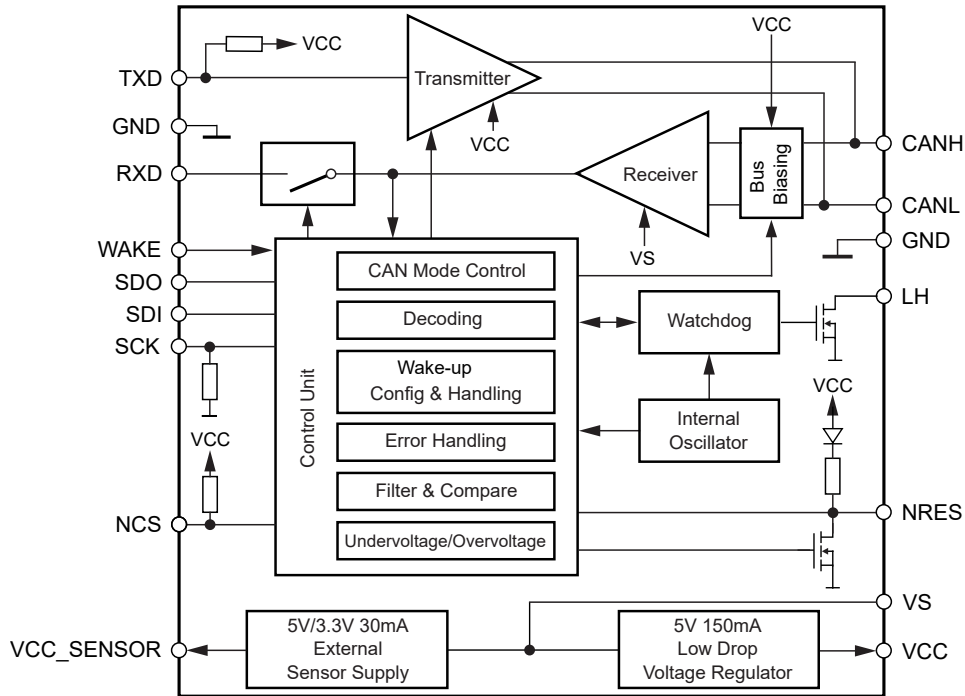
**Table 1. ATA658x Family Members**

Device	CAN PN	LIN	5V LDO	3.3V LDO	Package	Grade 0	Grade 1	Description
ATA6580-GTQW0-VAO			x		DFN18	x		CAN SBC: CAN transceiver without selective wake up, CAN FD capable, VCC=5V, VCC_SENSOR=5V/3.3V
ATA6580-GTQW1-VAO			x		DFN18		x	CAN SBC: CAN transceiver without selective wake up, CAN FD capable, VCC=5V, VCC_SENSOR=5V/3.3V
ATA6581-GTQW0-VAO		x	x		DFN18	x		CAN-LIN SBC: CAN transceiver without selective wake up, CAN FD capable, LIN transceiver, VCC=5V, VCC_SENSOR=5V/3.3V
ATA6581-GTQW1-VAO		x	x		DFN18		x	CAN-LIN SBC: CAN transceiver without selective wake up, CAN FD capable, LIN transceiver, VCC=5V, VCC_SENSOR=5V/3.3V
ATA6582-GUQW1-VAO		2x	2x		DFN26		x	CAN-LIN-LIN SBC: CAN transceiver without selective wake up, CAN FD capable, 2 LIN transceivers, VCC=5V, VCC_SENSOR=5V/3.3V, VCC_μC=5V
ATA6583-GUQW1-VAO		2x	x	x	DFN26		x	CAN-LIN-LIN SBC: CAN transceiver without selective wake up, CAN FD capable, 2 LIN transceivers, VCC=5V, VCC_SENSOR=5V/3.3V, VCC_μC=3.3V
ATA6585-GTQW0-VAO	x		x		DFN18	x		CAN SBC: CAN transceiver with selective wake up, CAN FD capable, VCC=5V, VCC_SENSOR=5V/3.3V
ATA6585-GTQW1-VAO	x		x		DFN18		x	CAN SBC: CAN transceiver with selective wake up, CAN FD capable, VCC=5V, VCC_SENSOR=5V/3.3V
ATA6586-GTQW0-VAO	x	x	x		DFN18	x		CAN-LIN SBC: LIN transceiver, CAN transceiver with selective wake up, CAN FD capable, VCC=5V, VCC_SENSOR=5V/3.3V
ATA6586-GTQW1-VAO	x	x	x		DFN18		x	CAN-LIN SBC: LIN transceiver, CAN transceiver with selective wake up, CAN FD capable, VCC=5V, VCC_SENSOR=5V/3.3V
ATA6587-GUQW1-VAO	x	2x	2x		DFN26		x	CAN-LIN-LIN SBC: CAN transceiver with selective wake up, CAN FD capable, 2 LIN transceivers, VCC=5V, VCC_SENSOR=5V/3.3V, VCC_μC=5V

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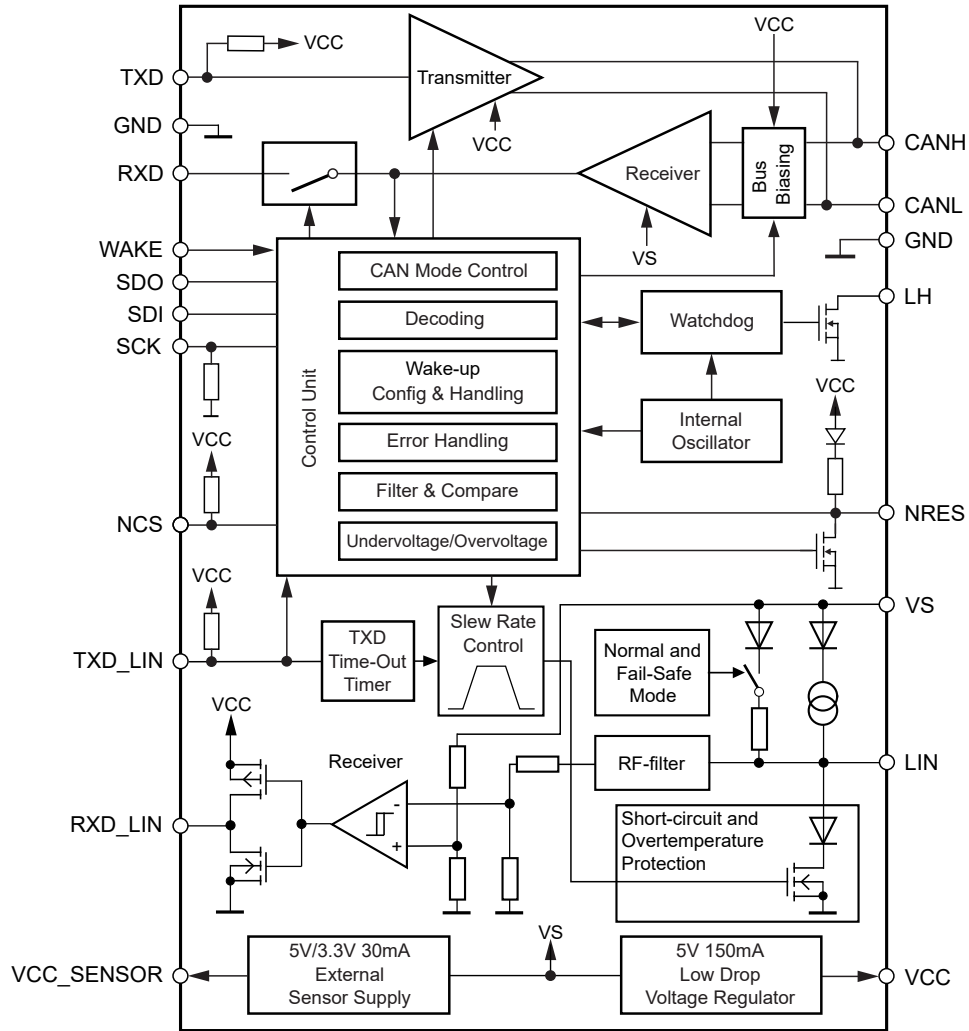
Device	CAN PN	LIN	5V LDO	3.3V LDO	Package	Grade 0	Grade 1	Description
ATA6588-GUQW1-VAO	x	2x	x	x	DFN26		x	CAN-LIN-LIN SBC: CAN transceiver with selective wake up, CAN FD capable, 2 LIN transceivers, VCC=5V, VCC_SENSOR=5V/3.3V, VCC_μC=3.3V

Figure 1. Simplified Block Diagram: CAN SBC ATA6580 and ATA6585



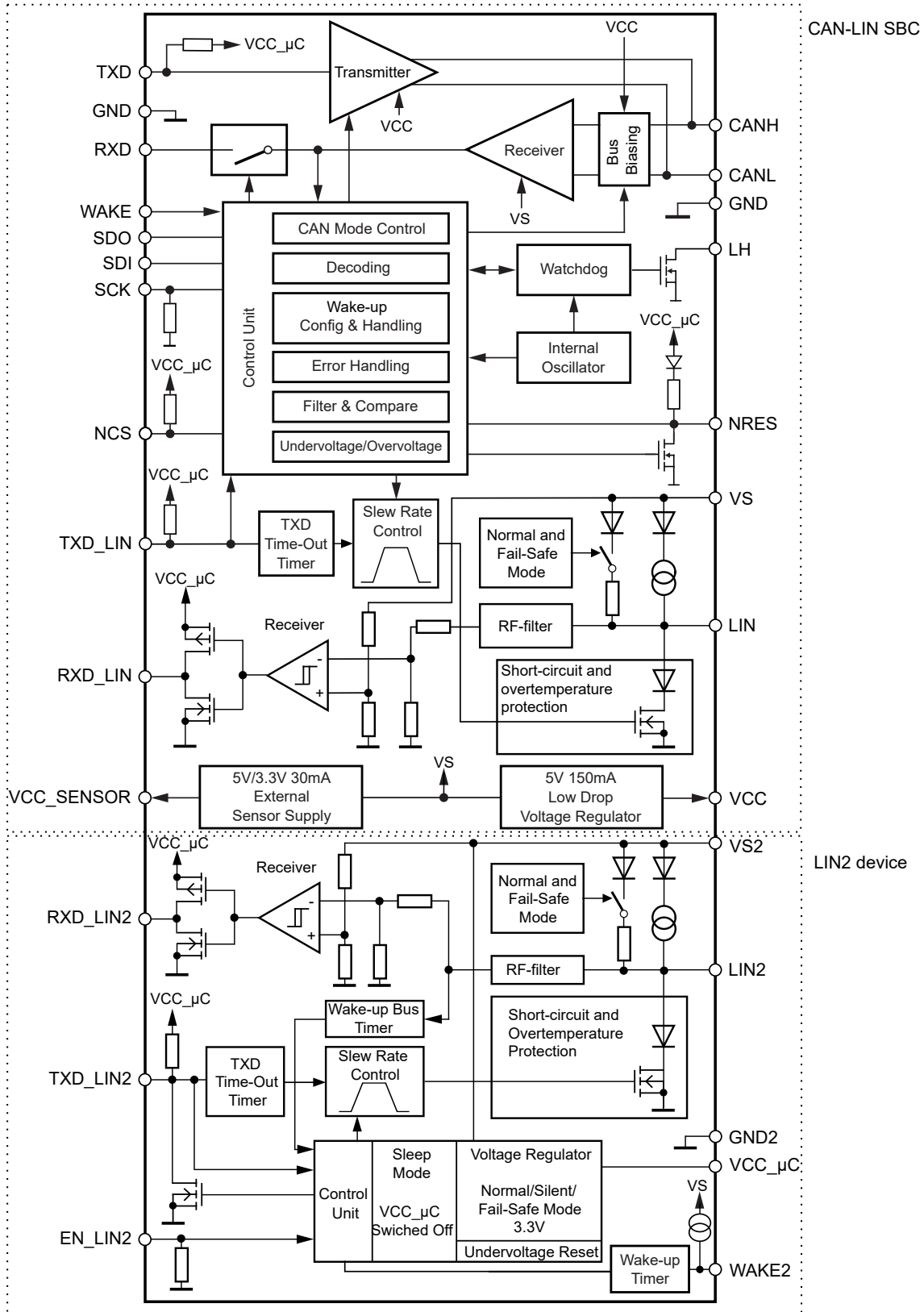
**Note:** ATA6580 is without and ATA6585 is with CAN Partial Networking functionality

Figure 2. Simplified Block Diagram: CAN-LIN SBC ATA6581 and ATA6586



**Note:** ATA6581 is without and ATA6586 is with CAN Partial Networking functionality

Figure 3. Simplified Block Diagram: CAN-LIN-LIN SBC ATA6582, ATA6583, ATA6587 and ATA6588



**Note:** ATA6582, ATA6583 is without and ATA6587, ATA6588 is with CAN Partial Networking functionality

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# 1. Pin Configuration

Figure 1-1. Pin Configuration VDFN18

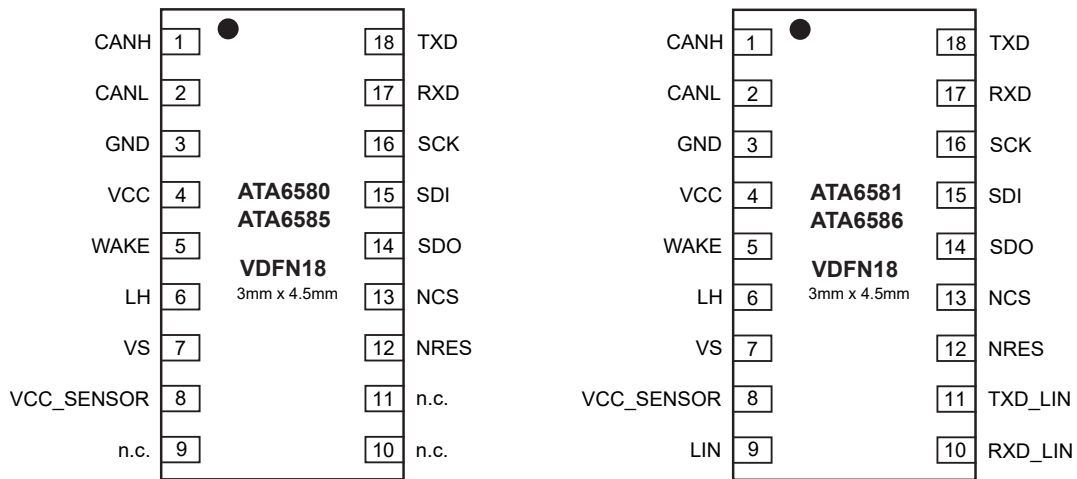


Figure 1-2. Pin Configuration VDFN26

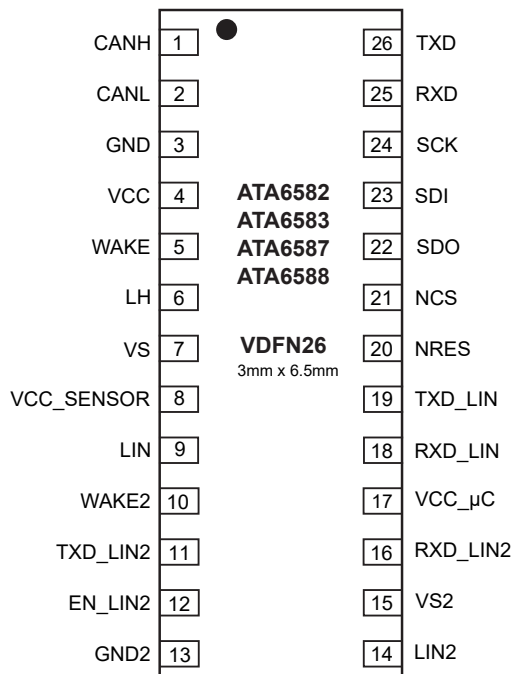


Table 1-1. Pin Description ATA6580/1/5/6

Pin	Symbol	Function
1	CANH	High-level CAN bus line (high in dominant state)
2	CANL	Low-level CAN bus line (low in dominant state)
3	GND	Ground
4	VCC	5V 150 mA output voltage
5	WAKE	High-voltage input for local wake up
6	LH	Limp Home: Failure output, open drain

.....continued

Pin	Symbol	Function
7	VS	Battery voltage supply pin
8	VCC_SENSOR	5V/3.3V 30 mA sensor supply voltage
9	n.c. / LIN	Not connected (ATA6580/5), LIN bus interface (ATA6581/6)
10	n.c. / RXD_LIN	Not connected (ATA6580/5) or receive data output from LIN transceiver (ATA6581/6)
11	n.c. / TXD_LIN	Not connected (ATA6580/5) or transmit data input from LIN transceiver (ATA6581/6)
12	NRES	Low active input/output reset pin
13	NCS	SPI chip select
14	SDO	SPI data output
15	SDI	SPI data input
16	SCK	SPI clock
17	RXD	Receive CAN data output, reads out data from the CAN-bus
18	TXD	Transmit CAN data input
Backside		Heat slug, internally connected to GND

**Table 1-2.** Pin Description ATA6582/3/7/8

Pin	Symbol	Function
1	CANH	High-level CAN bus line (high in dominant state)
2	CANL	Low-level CAN bus line (low in dominant state)
3	GND	Ground
4	VCC	5V 150 mA output voltage
5	WAKE	High-voltage input for local wake up
6	LH	Limp Home: Failure output, open drain
7	VS	Battery voltage supply pin
8	VCC_SENSOR	5V/3.3V 30 mA, sensor supply voltage
9	LIN	LIN bus interface
10	WAKE2	High-voltage input for local wake up
11	TXD_LIN2	Transmit data input from LIN2 device
12	EN_LIN2	Enable LIN2 device
13	GND2	Ground of LIN2 device
14	LIN2	LIN2 bus interface
15	VS2	Battery voltage supply pin of the LIN2 device
16	RXD_LIN2	Receive data output from LIN2 device
17	VCC_μC	5V/3.3V 85 mA supply voltage
18	RXD_LIN	Receive data output from LIN transceiver
19	TXD_LIN	Transmit data input from LIN transceiver
20	NRES	Low active input/output reset pin
21	NCS	SPI chip select
22	SDO	SPI data output
23	SDI	SPI data input
24	SCK	SPI clock
25	RXD	Receive CAN data output, reads out data from the CAN-bus
26	TXD	Transmit CAN data input
Backside		Heat slug, internally connected to GND

## 1.1 Supply Pin (VS)

The VS supply pin is the power supply pin for the ATA6580/81/85/86 device. In an application, this pin is usually connected to the battery via a serial diode for reverse battery protection. This pin sustains standard automotive conditions, such as 40V during load dump.

An undervoltage detection circuit is implemented to avoid a malfunction or false bus messages. After switching on VS, the IC starts in Standby mode and the VCC voltage regulator is switched on.

## 1.2 Supply Pin (VS2) (Only ATA6582/3/7/8)

The VS2 supply pin is the power supply pin for the LIN2 device inside the ATA6582/83/87/88, which consists of a second LIN2 transceiver and the VCC\_μC LDO. In an application, this pin usually is connected to the battery via a serial diode for reverse battery protection. This pin sustains standard automotive conditions, such as 40V during load dump.

An undervoltage detection circuit is implemented to avoid a malfunction or false bus messages. After switching on VS2, the LIN2 device starts in Fail-Safe mode and the voltage regulator (VCC\_μC) is switched on.

VS and VS2 must always be connected in order to ensure correct functionality of the device. Therefore, after switching on VS and VS2, the device starts in Standby mode. The VCC and the VCC\_μC voltage regulators are switched on.

## 1.3 Ground Pin (GND/GND2)

The IC does not affect the CAN or LIN/LIN2 bus in the event of GND disconnection.

## 1.4 Supply Output Pin (VCC)

The first 5V voltage regulator is capable of driving loads up to 150 mA, supplying the microcontroller and other ICs on the PCB. It is protected against overload by means of current limitation and overtemperature shutdown. Furthermore, the output voltage is monitored and the NRES output pin is asserted, if VCC drops below the defined threshold  $V_{VCC\_UV\_TRX\_Set}$ .

## 1.5 Supply Output Pin (VCC\_μC) (Only ATA6582/3/7/8)

The second 3.3V/5V voltage regulator is capable of driving loads up to 85 mA. It is protected against overload by means of current limitation and overtemperature shutdown. It is recommended to supply the microcontroller with the second LDO (VCC\_μC).

## 1.6 External Sensor Supply Output Pin (VCC\_SENSOR)

The VCC\_SENSOR pin is a voltage regulator output intended to supply external components, delivering up to 30 mA at 3.3/5V. The VCC\_SENSOR supply is per default switched off. The VCC\_SENSOR pin is overvoltage and undervoltage monitored if the event capture is enabled.

## 1.7 CAN Bus Pins (CANH AND CANL)

CANH is a high-side driver to VCC and CANL is a low-side driver to GND. In Normal mode and with TXD high, the CANH and CANL drivers are off, and the voltage at CANH and CANL is approximately 2.5V, provided by the internal bus biasing circuitry. This state is called recessive.

When TXD is low, CANL is pulled to GND and CANH to VCC, creating a differential voltage on the CAN bus. This is called the dominant state.

In Standby mode, the CANH and CANL drivers are off. If the device is in Unpowered mode or Sleep mode, CANH and CANL are highly resistive with extremely low leakage current to GND, making the device ideally passive.

Pins CANH and CANL have integrated ESD protection and high robustness versus external disturbance, such as EMC and electrical transients. The CANH and CANL bus outputs are short-circuit protected, both against GND or a positive supply voltage, and are also protected against overtemperature conditions.

## 1.8 Input Pin (TXD)

This is the device input pin that controls the CAN bus state. In the application, this pin is connected to the microcontroller transmit terminal. Pin TXD has an internal pull-up toward VCC or VCC\_μC to ensure a safe defined recessive driver state in case this pin is left floating.

In Normal mode, when TXD is high or floating, the CAN bus is driven to the recessive state.

TXD must be pulled to GND in order to activate the CANH and CANL drivers, and set the bus to the dominant state. A TXD dominant time-out timer is started when the TXD pin is set to low. If the low state on the TXD pin persists for longer than  $t_{to(dom)}$ , the transmitter is disabled, releasing the bus lines to the recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when the TXD pin is set to high.

The transmitter is also disabled if pin TXD is held low (e.g., by a short circuit to GND) while the device is switched into Normal mode. In this case, the bus lines are in the recessive state. The transceiver remains in this state until pin TXD goes high.

## 1.9 Output Pin (RXD)

In Normal and Silent modes, this pin reports the state of the CAN bus to the microcontroller. In the application, this pin is connected to the microcontroller receive terminal. RXD is high when the bus state is recessive. When the bus state is dominant, RXD is low.

The output is a push-pull structure. The high side is connected to VCC or VCC\_μC and the low side to GND.

In Standby mode, the RXD output is switched to VCC or VCC\_μC. When a wake-up event is detected, RXD will be driven to low.

An RXD recessive clamping function (see section 2.5.9. [RXD Recessive Clamping](#)) is implemented. This fail-safe feature prevents the controller from sending data on the CAN bus if the RXD line is clamped to high (e.g., recessive).

## 1.10 Wake Input Pin (WAKE)

This pin is a high-voltage input used for waking up the device from Sleep mode. It is usually connected to an external switch in the application to generate a local wake-up. If the WAKE pin is not needed in the application, the local wake-up should be disabled and the WAKE pin should be connected to GND to ensure optimal EMC performance.

The WAKE pin has a special design structure and is triggered by a low-to-high and/or a high-to-low transition on the WAKE pin (selectable via SPI) followed by a low level maintained for a given time period ( $> t_{local\_wu}$ ). This feature allows for maximum flexibility when designing a local wake-up circuit.

An internal filter is implemented to avoid an unwanted wake-up event due to noise. A serial resistor should be inserted in order to limit the input current mainly during transient pulses and ESD. The recommended resistor value is 3.3 kΩ. An external 10 nF capacitor is advised for better EMC and ESD performance.

## 1.11 Wake Input Pin (WAKE2) (Only ATA6582/3/7/8)

This pin is a high-voltage input used for waking up the device from Sleep mode. It is usually connected to an external switch in the application to generate a local wake up. If the WAKE2 pin is not needed in the application, the local wake up should be disabled and the WAKE2 pin should be connected to VS2 to ensure optimal EMC performance.

A pull-up current source with typically 10 μA is implemented in the WAKE2 pin. A falling edge at the WAKE2 pin followed by a low level maintained for a given time period ( $> t_{local\_wu2}$ ) results in a local wake-up request.

An internal filter is implemented to avoid an unwanted wake-up event due to noise. A serial resistor should be inserted in order to limit the input current mainly during transient pulses and ESD. The recommended resistor value is 3.3 k $\Omega$ . An external 10 nF capacitor is advised for better EMC and ESD performance.

### 1.12 SPI Serial Data In Pin (SDI)

Serial Data In input connected to an output of the microcontroller.

### 1.13 SPI Serial Data Out Pin (SDO)

Serial Data Out output connected to an input of the microcontroller; this pin is in tri-state if NCS is high.

### 1.14 SPI Clock Pin (SCK)

Serial data clock input; default level is low due to internal pull-down.

### 1.15 SPI Chip Select Pin (NCS)

Chip Select input pin: active-low. If Chip Select is not active, no data are loaded from SDI on SCK edges or provided at SDO.

### 1.16 Reset Input/Output Pin (NRES)

If the VCC voltage (ATA6580/1/5/6) or VCC\_ $\mu$ C voltage (ATA6582/3/7/8) falls below the undervoltage detection threshold  $V_{VCC\_UV\_TRX\_Set}$  (ATA6580/1/5/6) /  $V_{VCC\_UC\_UV\_TRX\_Set}$  (ATA6582/3/7/8), NRES is asserted. The NRES stays low even if  $V_{VCC} = 0V$  because NRES is internally driven from the  $V_{VS}$  voltage. If the  $V_{VS}$  voltage ramps down, NRES stays low until  $V_{VS} < 1.5V$  and then becomes highly impedant.

The implemented undervoltage delay keeps NRES low for  $t_{reset}$  after VCC reaches its nominal value.

The NRES pin is also asserted when a Watchdog Reset event is detected.

The NRES pin is also an input pin and can be asserted by the microcontroller to reset the ATA658x device.

A pull-up resistor and a diode in series is implemented.

### 1.17 Limp Home Pin (LH)

Limp Home is a high-voltage output pin for signaling unexpected system errors. The pin is driven by an open-drain NMOS switch and is activated by the following events:

1. A Watchdog Failure/Reset event
2.  $V_{VCC} < V_{VCC\_UV\_TRX\_Set}$  (ATA6580/1/5/6) &&  $RSTLVL == 1$  **OR**  $V_{VCC\_UC} < V_{VCC\_UV\_IO\_Set}$  (ATA6582/3/7/8) **OR**  $V_{VCC} < V_{VCC\_UV\_IO\_Set}$  (ATA6580/1/5/6) has been detected in Standby or Normal mode.
3.  $V_{VCC} < V_{VCC\_UV\_TRX\_Set}$  (ATA6580/1/5/6) &&  $RSTLVL == 1$  **OR**  $V_{VCC\_UC} < V_{VCC\_UV\_IO\_Set}$  (ATA6582/3/7/8) **OR**  $V_{VCC} < V_{VCC\_UV\_IO\_Set}$  (ATA6580/1/5/6) has been detected for longer than  $t_{reset}$  after entering  $\mu$ C Reset mode triggered by (e AND i in [Figure 2-1](#)).
4.  $V_{VCC} > V_{VCC\_OV\_Set}$  has been detected in  $\mu$ C Reset or Standby or Normal mode, if enabled in the LDOECR register.

LH is only cleared after the device received three consecutive valid watchdog trigger commands since LH was activated. This is independent whether the watchdog is enabled or not during a  $V_{VS}$  undervoltage.

During a  $V_{VS}$  undervoltage,  $V_{VS} < V_{VS\_PWRON}$  for the rising and  $V_{VS} < V_{VS\_PWROFF}$  for the falling  $V_{VS}$  ramp respectively, the LH output is deactivated.

### 1.18 TXD\_LIN/TXD\_LIN2

In Normal mode, the TXD\_LIN/TXD\_LIN2 pin is the microcontroller interface for controlling the state of the LIN/LIN2 output respectively. TXD\_LIN/TXD\_LIN2 must be pulled to ground in order to drive the LIN/LIN2 bus to a dominant state. If TXD\_LIN/TXD\_LIN2 is high or unconnected (internal pull-up

resistor), the LIN/LIN2 output transistor is turned off and the bus is in the recessive state. If the TXD\_LIN/TXD\_LIN2 pin stays at logic low level while switching into Normal mode, it must be pulled to high level longer than 10  $\mu$ s before the LIN/LIN2 driver can be activated. This feature prevents the bus line from accidentally being driven to dominant state after Normal mode has been activated (also in case of a short circuit at TXD\_LIN/TXD\_LIN2 to GND).

During Fail-Safe mode (LIN2 device only), the TXD\_LIN2 pin is used as an output and signals, together with the RXD\_LIN2 pin, the Fail-Safe source.

The TXD\_LIN/TXD\_LIN2 input has an internal pull-up resistor. An internal timer prevents the bus line from permanently being driven to the dominant state. If TXD\_LIN/TXD\_LIN2 is driven to low longer than  $t_{to(dom)}_{LIN}$ , the LIN/LIN2 bus driver is switched to the recessive state. Nevertheless, when switching to Sleep mode, the actual level at the TXD\_LIN/TXD\_LIN2 pin is relevant. Refer to [2.12.1. LIN2 Operating Modes](#) for more information.

To reactivate the LIN bus driver, switch TXD\_LIN/TXD\_LIN2 to high for at least  $t_{DToRel}$ .

### 1.19 RXD\_LIN/RXD\_LIN2

In Normal mode, this pin reports the state of the LIN/LIN2 bus to the microcontroller. LIN/LIN2 high (recessive state) is indicated by a high level at RXD\_LIN/RXD\_LIN2; LIN/LIN2 low (dominant state) is indicated by a low level at RXD\_LIN/RXD\_LIN2. The output is a push-pull stage switching between VCC/VCC\_μC and GND. The AC characteristics are measured with an external load capacitor of 20 pF.

If the LIN2 device is in Silent mode, the RXD\_LIN2 output switches to high.

### 1.20 LIN/LIN2

A low-side driver with internal current limitation and thermal shutdown as well as an internal pull-up resistor, according to LIN specification 2.x/ISO 17987-4, is implemented. The voltage range is from -27V to +40V. This pin exhibits no reverse current from the LIN/LIN2 bus to VS/VS2, even in the event of a GND shift or VBat disconnection. The LIN/LIN2 receiver thresholds comply with the LIN specification.

The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope-controlled.

During a short circuit at LIN/LIN2 to VBat, the output limits the output current to  $I_{BUS\_LIM}$ . If due to the power dissipation, the chip temperature exceeds  $T_{LINoff}$ , then the LIN/LIN2 output is switched off. Once the chip cools down and after a hysteresis of  $T_{hys}$ , the LIN/LIN2 output switches on again. RXD\_LIN/RXD\_LIN2 will be driven high when LIN/LIN2 is high. The VCC/VCC\_μC regulator operates independently of LIN/LIN2 overtemperature shutdown.

Despite a short circuit from LIN/LIN2 to GND, the IC can be switched into Sleep or Silent mode (LIN2 device only). If the short circuit disappears, the IC can be woken up via a remote wake up. The reverse current is < 2μA at pin LIN/LIN2 during loss of VBat. This is optimal behavior for bus systems where some LIN nodes are supplied from battery or ignition.

### 1.21 EN\_LIN2 (Only ATA6582/3/7/8)

The enable input pin controls the operating mode of the LIN2 device. If EN\_LIN2 is high, the LIN2 device is in Normal mode, with the transmission paths from TXD\_LIN2 to LIN2 and from LIN2 to RXD\_LIN2 both active. The VCC\_μC voltage regulator operates with 3.3V/5V 85mA output capability. If EN\_LIN2 is switched to low while TXD\_LIN2 is still high, the LIN2 device is forced to Silent mode and no data transmission is then possible. Refer to [2.12.1. LIN2 Operating Modes](#) for more information.

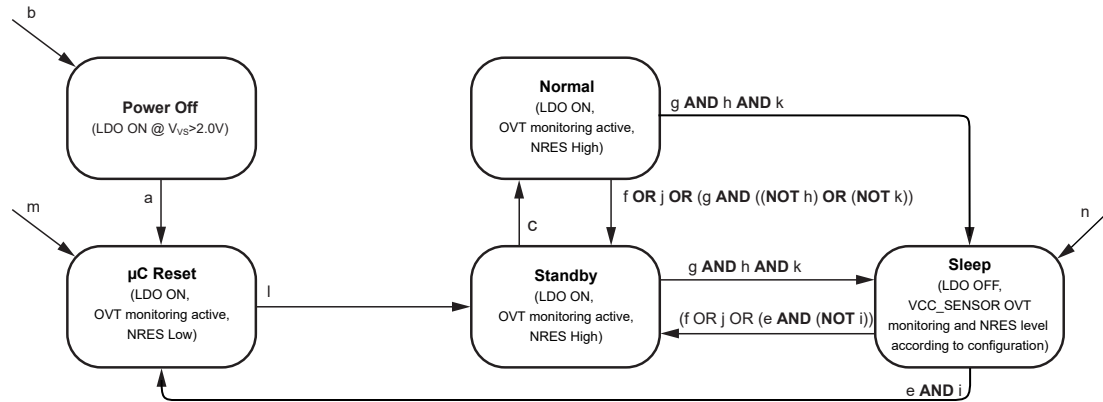
If EN\_LIN2 is switched to low while TXD\_LIN2 is low, the LIN2 device transitions to Sleep mode. No data transmission/reception is possible, and the VCC\_μC voltage regulator is switched off.

The EN\_LIN2 pin provides a pull-down resistor to force the LIN2 transceiver into Recessive mode if EN\_LIN2 is disconnected.

## 2. Functional Description

### 2.1 Device Operating Modes

Figure 2-1. Device Operating Modes State Diagram



- a:  $V_{VS} > V_{VS\_PWRON}$  (4.2V...4.55V)  
 b:  $V_{VS} < V_{VS\_PWROFF}$  (2.8V...3V)  
 c: DOPM = Normal  
 e: Wake-up event OR interrupt event  
 f: DOPM = Standby  
 g: DOPM = Sleep  
 h: No wake-up event pending  
 i: Bit RSTEN == 1  
 j: Illegal DOPM code configuration via SPI  
 k: Number of enabled wake-up source  $\geq 1$   
 l: (Reset pulse time expired AND NRES not driven low externally) AND  
 ((RSTLVL == 0 AND  $V_{VCC} > V_{VCC\_UV\_IO\_Clear}$  (ATA6580/1/5/6)) OR  
 (RSTLVL == 0 AND  $V_{VCC\_μC} > V_{VCC\_UV\_TRX\_Clear}$  (ATA6582/3/7/8)) OR  
 (RSTLVL == 1 AND  $V_{VCC} > V_{VCC\_UV\_TRX\_Clear}$  (ATA6580/1/5/6)) OR  
 (RSTLVL == 1 AND  $V_{VCC\_μC} > V_{VCC\_UV\_RST\_Clear}$  (ATA6582/7)) OR  
 (RSTLVL == don't\_care AND  $V_{VCC\_μC} > V_{VCC\_UV\_IO\_Clear}$  (ATA6583/8))  
 m: Watchdog activated AND any Reset event OR  
 ( $V_{VCC} < V_{VCC\_UV\_TRX\_Set}$  (ATA6580/1/5/6) AND RSTLVL == 1) OR  
 ( $V_{VCC\_μC} < V_{VCC\_UV\_RST\_Set}$  (ATA6582/7) AND RSTLVL == 1) OR  
 ( $V_{VCC} < V_{VCC\_UV\_IO\_Set}$  (ATA6580/1/5/6)) OR  
 ( $V_{VCC\_μC} < V_{VCC\_UV\_IO\_Set}$  (ATA6582/3/7/8)) OR  
 NRES pulled low externally  
 n: VCCOVSD == 1 &&  $V_{VCC} > V_{VCC\_OV\_Set}$  has been detected for  
 longer than  $t_{VCC\_UV\_TRX\_Clear}$  (ATA6582/3/7/8) && ATA6580/1/5/6

LH shall be activated in μC Reset mode when:

1. A watchdog failure event has been detected. (Note: watchdog timeout in Sleep mode does not activate LH even when SLPNRES == 0)
2. The device enters μC Reset mode due to VCC/VCC\_μC undervoltage event.
3. VCC/VCC\_μC undervoltage has been detected for longer than  $t_{reset}$  after entering μC Reset mode triggered by (e AND i).

SPI failure does not trigger the device mode transition. Only the SPIFS bit is set.

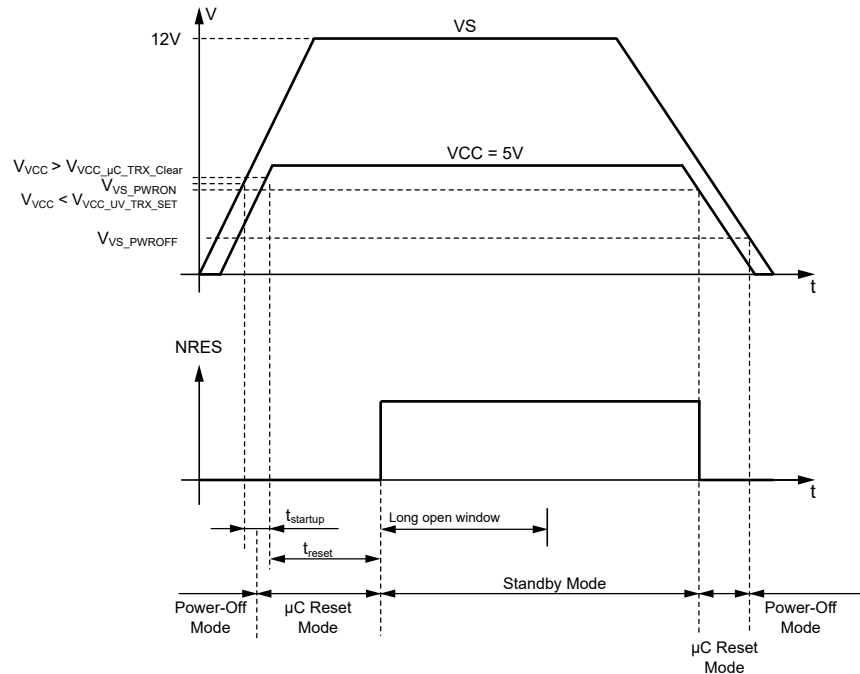
Event signalization is possible in Sleep mode.

The mode control unit in the ATA658x implements five different states, as depicted above. All of the states are briefly described in this section.

#### 2.1.1 μC Reset Mode

In the ATA6580/1/5/6, the μC Reset mode is the default mode after a Power-on-Reset. It is the reset execution state of the device. This mode ensures that the pin NRES is pulled down for a defined time to allow the microcontroller to be reset in a controlled manner.

Figure 2-2. Mode Switching during Power On Start and Power Off



In the  $\mu\text{C}$  Reset mode, the CAN and LIN transceivers and the SPI are disabled. The low dropout voltage regulator VCC and its overtemperature detection are active. Watchdog is disabled. The following events will cause the ATA6580/1/5/6 to switch to the  $\mu\text{C}$  Reset mode:

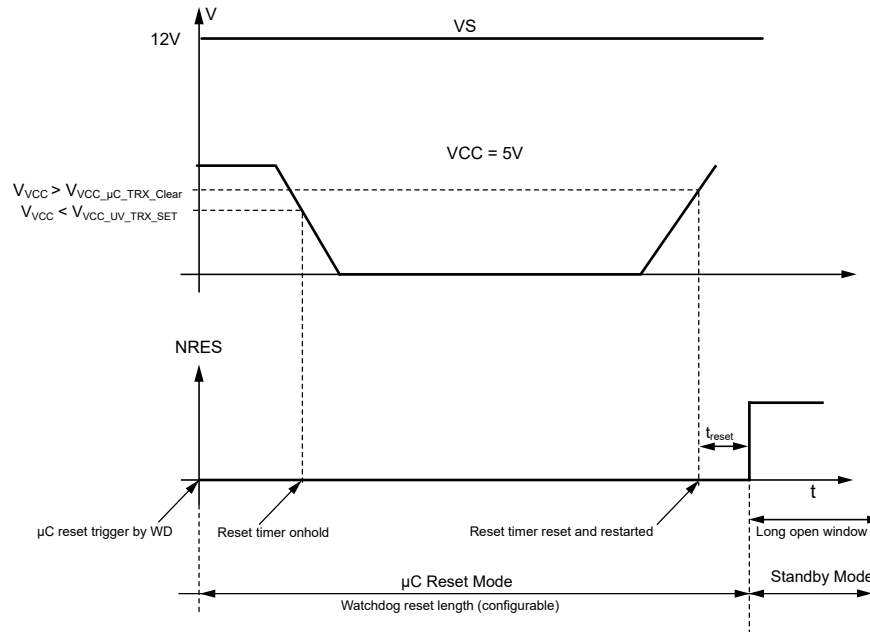
- From Sleep mode after detecting enabled wake-up event or interrupt event
- From all modes when an externally driven negative edge has been detected at NRES and low level has been kept for longer than  $t_{\text{nres\_input}}$
- Watchdog time-out
- Watchdog is triggered too early (window mode).
- An attempt is made to reconfigure the watchdog control register while the SBC is in Normal mode.
- If the bit RSTLVL in SECR register is set to 1 and  $V_{\text{VCC}} < V_{\text{VCC\_UV\_TRX\_Set}}$  has been detected. (RSTLVL is by default 1 in the ATA6580/1/2/5/6/7 and by default 0 in the ATA6583/8).
- $V_{\text{VCC}} < V_{\text{VCC\_UV\_IO\_Set}}$  has been detected (ATA6580/1/5/6) or  $V_{\text{VCC\_}\mu\text{C}} < V_{\text{VCC\_UV\_IO\_Set}}$  has been detected (ATA6582/3/7/8).

#### $\mu\text{C}$ Reset mode and VCC undervoltage events:

If the bit RSTLVL is set to '1' (default), the device will enter the  $\mu\text{C}$  Reset mode after detecting the VCC undervoltage ( $V_{\text{VCC}} < V_{\text{VCC\_UV\_TRX\_Set}}$ ). The device will stay in the  $\mu\text{C}$  Reset mode until VCC recovers ( $V_{\text{VCC}} > V_{\text{VCC\_UV\_TRX\_Clear}}$ ) and then reset and restart the reset pulse length timer. If VCC undervoltage is detected when the device has been switched into the  $\mu\text{C}$  Reset mode, the reset pulse length timer will be on hold until VCC recovers and then be reset and restarted. The ATA6580/1/5/6 device will leave the  $\mu\text{C}$  Reset mode and enter Standby mode after the  $t_{\text{reset}}$  time expires.



**Figure 2-3.** VCC undervoltage ( $V_{VCC} < V_{VCC\_UV\_TRX\_Set}$ ) in the  $\mu$ C Reset mode, RSTLVL==1

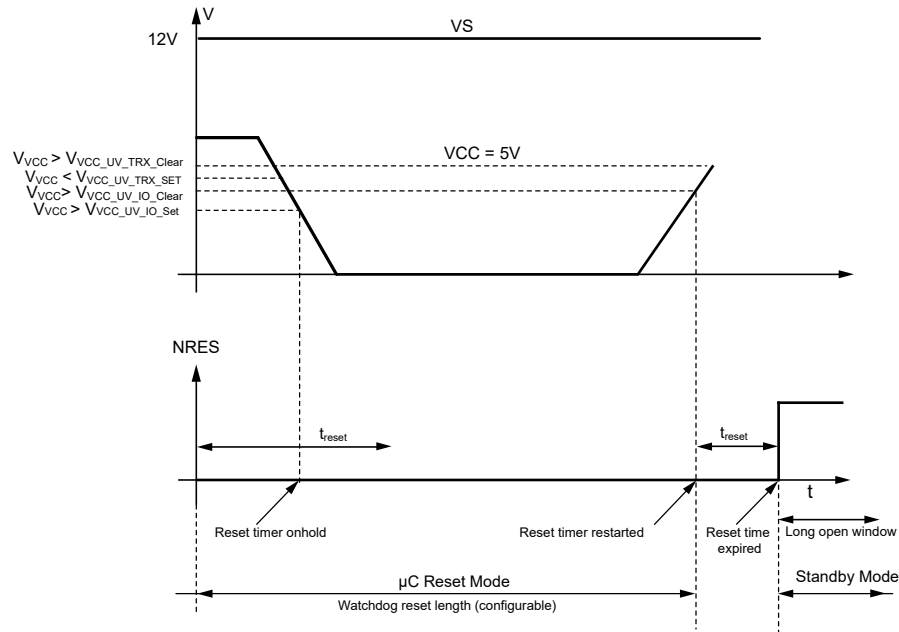


If the bit RSTLVL is not set to 1, the device will only enter  $\mu$ C Reset mode after power on start-up, or after detecting a watchdog reset event, or after detecting  $V_{VCC} < V_{VCC\_UV\_IO\_Set}$ . In this case, the device will start the reset pulse length timer after the device enters the  $\mu$ C Reset mode and  $V_{VCC} > V_{VCC\_UV\_IO\_Clear}$  has been detected. As soon as the timer expires, the device will enter Standby mode.

In the ATA6582/7, VCC\_μC will be monitored for triggering  $\mu$ C Reset. When RSTLVL is set to "1", the device will enter  $\mu$ C Reset mode after detecting  $V_{VCC\_μC} < V_{VCC\_UV\_RST\_Set}$ . The device will stay in the  $\mu$ C Reset mode until VCC\_μC recovers. When RSTLVL is set to "0", the device will enter  $\mu$ C Reset mode when the device detects  $V_{VCC\_UV} < V_{VCC\_UV\_IO\_Set}$ .

In the ATA6583/8, the RSTLVL is not used. The  $\mu$ C Reset will always be triggered when the device detects  $V_{VCC\_μC} < V_{VCC\_UV\_IO\_Set}$ .

**Figure 2-4.** Mode switching from  $\mu\text{C}$  Reset mode during VCC undervoltage ( $V_{\text{VCC}} < V_{\text{VCC\_UV\_IO\_Set}}$ ) when  $\text{RSTLVL}=0$



### 2.1.2 Power-Off Mode

The device is in Power-Off mode when the supply voltage of the device  $V_{\text{VS}}$  is lower than the defined device power-off detection voltage threshold ( $V_{\text{VS\_PWROFF}}$ ). This is the default mode when the battery is first connected. In this mode, the integrated CAN transceiver is in the CAN Off mode (see section 2.2.1. CAN Off Mode). The integrated LIN transceiver is in LIN Unpowered mode. (ATA6580/1/5/6 only) The watchdog is inactive. The pins CANH, CANL are high resistive. The device is not able to provide any functionality. As soon as  $V_{\text{VS}}$  rises above the power-on detection threshold ( $V_{\text{VS\_PWRON}}$ ), the device resets and initializes. After  $t_{\text{startup}}$ , the device transitions to Standby mode.

### 2.1.3 Standby Mode

Standby mode is the first power saving mode of the device. In Standby mode, both the integrated CAN and LIN transceiver are disabled. The primary 5V only low dropout voltage regulator is switched on. The watchdog is active by default.

In Standby mode, the device supports various remote wake-up mechanisms, like LIN bus wake up, CAN bus remote wake up via a standard wake-up pattern (WUP) or via a selective wake-up frame (WUF) and high-voltage local wake up. The CAN and LIN bus remote wake up is activated, when the register bit CWUE and LINWUE is set to '1', correspondingly (see section 2.4.5.12. TRXECR). At the same time,  $V_{\text{VS}}$  must be above the threshold  $V_{\text{VS\_UV\_TRX\_Clear}}$ . Otherwise neither LIN nor CAN bus wake up will be detected.

The CAN transceiver in the ATA6580/1/5/6 supports the automatic voltage biasing according to ISO 11898-6 in Standby mode (provided  $V_{\text{VS}} > V_{\text{VS\_UV\_TRX\_Clear}}$ ). The bus pins are biased to GND (via  $R_{\text{CAN\_H}}$ ,  $R_{\text{CAN\_L}}$ ) when the bus is inactive and at approximately 2.5V when there is a remote CAN bus wake-up request (Wake-Up Pattern, WUP, according to ISO 11898-6) detected.

If  $\text{CWUE} = \text{CPNE} = \text{PNCFOK} = '1'$ , the selective wake up via CAN bus is enabled. After a successful detection of a wake-up pattern, the bus pins are first biased to 2.5V and the device is ready for decoding further coming wake-up frames (WUF). Only after detecting a valid WUF, a wake-up event is registered and the wake-up process is finished. If the data frame is a valid WUF, the device will indicate a wake-up event. If the selective wake up is disabled and CAN remote wake up is enabled, the standard wake up via wake-up pattern (WUP) is activated. The device biases its bus pins to 2.5V after a successful detection of a wake-up pattern, registers the wake-up event and the wake-up process is finished.

The local wake up via WAKE pin is activated when the bit LWURE and/or LWUFE are/is set to '1' (see section 2.4.5.14. [WKECR](#)). In addition, the device also supports detection of several system events in Standby mode (see section 2.4.5.13. [TRXECR2](#)).

The ATA658x device provides various status registers. The internal wake-up flags LINWUS, CWUS, LWURS and LWUFS (see section 2.4.5.6. [CTRRESR](#) and section 2.4.5.7. [WKECR](#)) and system event status registers are set to '1' by the device if the corresponding event is detected. The device will not leave Standby mode after detecting a valid wake-up event. It will only set the corresponding internal status register bits. A transition to Normal mode will only happen, when the register bits DOPM are set to 0b111 via SPI.

In Standby mode, the detection of a wake-up event or an interrupt event (see section 2.4.5.13. [TRXECR2](#)) is denoted via pin RXD and RXD\_LIN, provided that the corresponding event interrupt is enabled (see section 2.4.5.10. [SECR](#) to section 2.4.5.14. [WKECR](#)). Pins RXD and RXD\_LIN are usually at the VCC or VCC\_μC level and will be forced to low if an enabled event is detected. At the same time, a set of status registers (see section 2.4.5.3. [GESR](#) to section 2.4.5.8. [BFESR](#)) is provided, which allows the microcontroller to get further detailed information about the device via SPI.

As shown in [Figure 2-2](#) the device will enter Standby mode in following cases:

1. From the μC Reset mode after reset pulse length time expired or
2. if DOPM = Sleep mode is written via SPI when there is a wake-up event pending or all wake-up sources are disabled.
3. From Normal or Sleep mode when DOPM = Standby mode is written via SPI.
4. From Sleep or Normal mode when an illegal DOPM code configuration via SPI has been detected.

The watchdog can be activated (Window or Time-Out mode) in Standby mode, and it can only be configured in Standby mode in order to avoid unwanted configuration of the watchdog.

#### 2.1.4 Sleep Mode

The Sleep mode is the most power-saving mode of the device. In this mode the primary 5V low dropout voltage regulator is switched off.

In the ATA6582/3/7/8, the CAN-LIN SBC should always be put into Sleep mode first using SPI and afterward, the LIN2 device. Otherwise, the device will end in a deadlock as the VCC\_μC would be deactivated and with it the SPI.

As in Standby mode, the device reacts to a variety of wake-up/interrupt events (see section 2.5.13. [Wake-Up and Interrupt Event Diagnostics via Pin RXD and pin RXD\\_LIN](#)). Before entering Sleep mode, the wake-up sources must be configured. The primary voltage regulator output switches on when either a LIN bus wake up (not available in the ATA6580/5), CAN bus wake-up event, a local wake up (WAKE) or an interrupt event (see section 2.5.13. [Wake-Up and Interrupt Event Diagnostics via Pin RXD and pin RXD\\_LIN](#)) is detected or a watchdog Reset (Time-Out mode is enabled) occurs and the device leaves the Sleep mode.

As shown in [Figure 2-1](#) the device enters Sleep mode in the following cases:

1. From Normal mode or Standby mode via an SPI command, if no wake-up event is pending and at least one wake-up source (see section 2.4. [Wake Up in the ATA6580/1/5/6](#)) is enabled.
2. In the ATA6580/1/5/6 from Normal, Standby or μC Reset mode when VCC overvoltage has been detected for longer than  $t_{OV\_VCC\_deb}$  and the bit VCCOVSD is set to '1'.

#### 2.1.5 Normal Mode

The ATA658x provides its full functionality in Normal mode.

Wake-up flag LINWUS (only when LIN transceiver in LIN Standby mode), CWUS and Interrupt Event Status registers will still be set to '1' by the device if the corresponding event is detected.

As shown in [Figure 2-1](#), the device will enter Normal mode from Standby mode via an SPI command.

## 2.1.6 Related Registers

### 2.1.6.1 Device Mode Control Register (address 0x01)

**Name:** DMCR  
**Offset:** 0x01  
**Reset:** 0x24  
**Property:** Read/Write

The device operating mode is selected via bits DOPM in the device mode control register. The register is accessed via SPI at address 0x01.

Bit	7	6	5	4	3	2	1	0
	Reserved[1:0]		RSTEN	VCCOVSD	SLPVCC $\mu$ C	DOPM[2:0]		
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	0	0	0	0

**Bits 7:6 – Reserved[1:0]** Reserved for future use

#### Bit 5 – RSTEN

The host shall set the RSTEN bit to '1' if it requests the device to wake-up from Sleep mode via  $\mu$ C Reset mode and shall set the RSTEN bit to '0' if it requests the device to enter Standby mode from Sleep mode when the mode transition has been triggered by wake-up events or interrupt events. The bit is only configurable in the ATA6582/3/7/8. In the ATA6580/1/5/6, the bit always has the value '1'.

#### Bit 4 – VCCOVSD

The host shall set the VCCOVSD bit to '1', if the device shall disable the VCC regulator in case a VCC overvoltage has been detected, otherwise the bit shall be set to '0'. In the ATA6580/1/5/6, the VCC regulator will be disabled by forcing the device into Sleep mode. The regulator will be enabled again when a wake-up event or interrupt event trigger a wake up of the device.

#### Bit 3 – SLPVCC $\mu$ C

Only available in the ATA6582/3/7/8. This bit configures the behavior of the device after detecting undervoltage of VCC $\mu$ C, when the device is in Sleep mode. When this bit is set, the LIN2 device must not be selected as the only wake-up source. At least one of the other wake-up sources must be selected (LWUFE=1 or LWURE=1 or CWUE=1 or CPNE=1 or LINWUE=1).

SLPVCC $\mu$ C	Device Operating Mode	VCC $\mu$ C undervoltage released
1'b0 (NRES input will be ignored in Sleep mode)	No reaction	Wake up (only if bit EXTWUE=1, otherwise no reaction)
1'b1	Enter $\mu$ C Reset mode	Leave $\mu$ C Reset mode according to the operating modes state diagram ( <a href="#">Figure 2-1</a> )

**Bits 2:0 – DOPM[2:0]** Select Device Operating Mode

DOPM[2:0]	Device Operating Mode
3'b001	Sleep mode
3'b100	Standby mode (An undefined operating mode code via SPI will trigger a transition to Standby mode.)
3'b111	Normal mode

### 2.1.6.2 Device Mode Status Register (Address 0x03)

**Name:** DMSR  
**Offset:** 0x03  
**Reset:** 0x01  
**Property:** Read-only

The register provides device operating mode transition related information.

Bit	7	6	5	4	3	2	1	0
	SMTS	OTPWS	NMTS	Reserved[3:0]				VCCS
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	1

#### Bit 7 – SMTS Sleep Mode Transition Status

The device sets the bit to '0' if the recent transition to Sleep mode was triggered by an SPI command and sets the bit to '1' if the recent transition to Sleep mode was forced by an VCC overvoltage (please refer to [2.5.6. Undervoltage and Overvoltage Detection on Pin VCC](#)).

#### Bit 6 – OTPWS Overtemperature Prewarning Status

The device sets the bit to '1' if the device temperature is higher than the overtemperature prewarning threshold and to '0' if the device temperature is below the overtemperature prewarning threshold, provided OTPWE bit (see section [2.5.10. Overtemperature Detection and Selective Overtemperature Shutdown](#)) is set to 1.

#### Bit 5 – NMTS Normal Mode Transition Status

The device sets the bit to '1' after the device has finished power-up and clears the bit when the the device switches to Normal mode.

#### Bits 4:1 – Reserved[3:0] Reserved for future use

#### Bit 0 – VCCS VCC Voltage Status

The device sets the bit to '1' if  $V_{VCC}$  is below the VCC TRX undervoltage detection threshold, otherwise to '0'. This bit is only relevant for the ATA6582/83/87/88!

## 2.2 Integrated CAN Transceiver Operating Modes

The integrated high-speed CAN transceiver in the ATA658x is designed for nominal CAN bit rates up to 1 Mbit/s and CAN Flexible Data-Rate (CAN FD) data bit rates up to 5 Mbit/s. It provides differential transmit and receive capability to a CAN protocol controller. The transceiver is ISO 11898-2, ISO 11898-5, ISO 11898-6 and ISO 11898-2:2016 compliant.

The integrated CAN transceiver supports the following operating modes: CAN Normal, CAN Silent, CAN Standby and CAN Biased Standby, CAN Off mode and CAN reduced Normal mode. The CAN transceiver operating mode depends on the device operating mode and on the setting of bits COPM in the CAN Transceiver Control register (see section [2.2.7.1. TRXCR](#)). When the device is in Normal mode, four of the operating modes can be selected via the COPM bits in the TRXCR register (see section [2.2.7.1. TRXCR](#)). The CAN Biased Standby mode is a mode which cannot be selected via COPM bits directly. Refer to section [2.2.3. CAN Biased Standby Mode](#) for the conditions for triggering a transition to the CAN Biased Standby mode. When the device is in  $\mu$ C Reset mode, Standby or Sleep mode, the transceiver is either in CAN Standby mode or in CAN Biased Standby mode.

The CAN transceiver supports automatic bus biasing according to ISO 11898-2:2016. It is active in CAN Standby mode. The bus is biased to 2.5 V if there is activity on the bus (CAN Biased Standby mode). In CAN Biased Standby mode, the CAN bias voltage is derived directly from  $V_{VS}$ . If there is no activity on the bus for  $t > t_{\text{silence}}$ , the bus is biased to GND (CAN Standby mode).

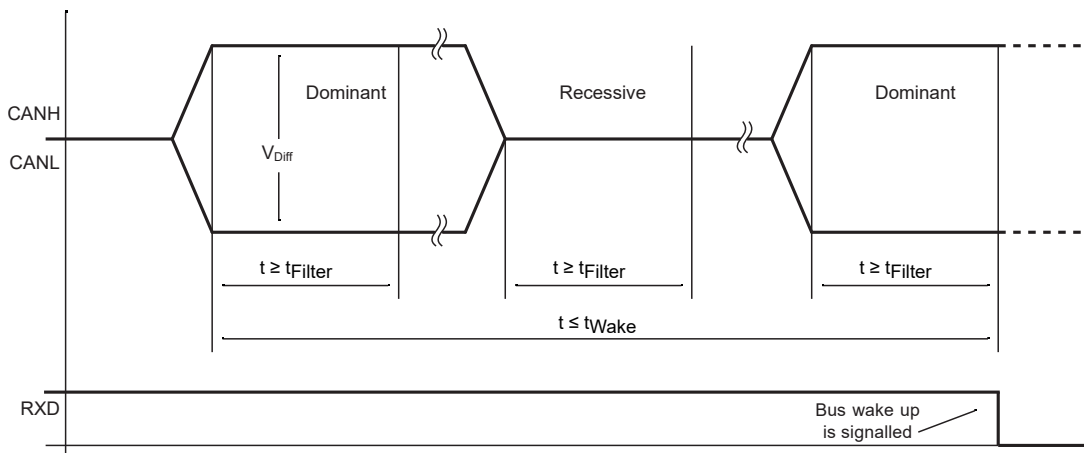


It will be switched on again and enter CAN Standby mode when  $V_{VS}$  rises above the transceiver undervoltage release threshold ( $V_{VS\_UV\_TRX\_Clear}$ ) and the device is no longer in Power Off and the temperature of the CAN transceiver drops by the hysteresis  $T < T_{VJsd\_hys}$ .

### 2.2.2 CAN Standby Mode

In CAN Standby mode, the transmitter and the receiver are switched off to reduce current consumption. If the CAN bus wake-up detection is enabled ( $CWUE = 1$ ), the wake-up comparator monitors the bus lines for a valid remote bus Wake-up Pattern (WUP). Two periods of dominant bus levels, separated by a period of recessive bus level each of at least  $t_{Filter}$ , switch the RXD pin to low to signal a wake-up request to the microcontroller. The figure below describes the process and timing of the WUP detection. In CAN Standby mode, the bus lines are biased to ground to reduce current consumption to a minimum.

**Figure 2-6.** Timing of CAN Standard Wake up via Wake-up Pattern (WUP)



As shown in [Figure 2-5](#), the CAN transceiver enters CAN Standby mode in the following cases:

1. When the device leaves Power-Off mode and the temperature of the CAN transceiver drops by the hysteresis  $T < T_{VJsd}$  and sufficient  $V_{VS}$  is applied or
2. Any of the conditions for CAN Biased Standby mode are valid for longer than  $t_{Silence}$  (see section [2.2.3. CAN Biased Standby Mode](#)).

### 2.2.3 CAN Biased Standby Mode

The CAN transceiver behavior in CAN Biased Standby mode is fundamentally the same as in the CAN Standby mode. The only difference is that in the CAN Biased Standby mode, the bus pins are biased to 2.5V. The transceiver will return to CAN Standby mode if the CAN bus is silent for longer than  $t_{Silence}$  (see section [Figure 2-8](#)).

As shown in [Figure 2-5](#), the CAN transceiver enters CAN Biased Standby mode in the following cases:

1. From CAN Silent/Normal/Reduced Normal mode, when  $t_{Silence}$  time-out is not detected and the device is in Standby ( $DOPM = 100$ ) or Sleep mode ( $DOPM = 001$ ).
2. From CAN Silent/Normal/Reduced Normal mode, when  $t_{Silence}$  time-out is not detected and the device is in Normal mode ( $DOPM = 111$ ), and the COPM is set to CAN Standby mode ( $COPM = 00$ ).
3. From CAN Standby mode when the device is in Normal mode ( $DOPM = 111$ ), COPM is set to CAN Normal mode ( $COPM = 01$ ) and  $V_{VCC} < V_{VCC\_UV\_TRX\_Set}$  has been detected.
4. From CAN Standby mode when a wake-up event is detected on the CAN bus.

## 2.2.4 CAN Silent Mode

The CAN Silent mode is a Receive-Only mode of the CAN transceiver. For instance, it can be used to test the connection of the bus medium or for the software-driven selective wake-up. In CAN Silent mode, the device can still receive data from the bus, but the transmitter is disabled, and therefore, no data can be sent to the CAN bus. The bus pins are released to the recessive state. All other IC functions continue to operate as they do in the CAN Normal mode. CAN biasing remains active. Silent mode can be used to prevent a faulty CAN controller from disrupting all network communications.

As shown in [Figure 2-5](#), the CAN transceiver enters CAN Silent mode in the following cases:

1. The device is in Normal mode (DOPM = Normal) and the CAN transceiver is in CAN Silent mode (COPM = CAN Silent).
2. The device is in Normal mode and the CAN transceiver is in CAN Normal mode, and a RXD recessive clamping failure is detected.

If the transceiver is in CAN Silent mode when VCC TRX undervoltage is detected, it will remain in CAN Silent mode before the device is switched to  $\mu$ C Reset mode. The CAN transceiver will enter and remain in CAN Silent mode when a RXD recessive clamping failure is detected, even if CAN Normal mode is selected in device Normal mode.

## 2.2.5 CAN Normal Mode

In CAN Normal mode, the integrated transceiver is able to transmit and receive data via the CANH and CANL bus lines. The output driver stage is active and drives data from the TXD input to the CAN bus. The receiver converts the analog signal on the bus lines into digital signal, which is output to pin RXD. The bus biasing is set to  $V_{VCC}/2$ .

The slope of the output signals on the bus lines is controlled and optimized in a way that ensures the lowest possible Electromagnetic Emission (EME).

As shown in [Figure 2-5](#), the CAN transceiver enters CAN Normal mode in the following cases:

1. The device is in Normal mode (DOPM = Normal) **AND** the CAN transceiver has been enabled by setting bits COPM to '01' **AND** no VCC TRX undervoltage is detected, **AND** no RXD recessive clamping is detected.
2. The transceiver is in CAN Reduced Normal mode and  $V_{VCC} > V_{VCC\_UV\_TX\_Clear}$  for  $t > t_{UV\_VCC\_TRX\_debounce}$ . Note: after  $V_{VCC}$  has recovered ( $V_{VCC} > V_{VCC\_UV\_TRX\_Clear}$ ), the CAN transceiver will enter "CAN Normal mode" but the device will transition into "Device Standby mode". The device will transition into Device Normal mode after setting DOPM=Normal.

If pin TXD is held low (e.g., by a short circuit to GND) when CAN Normal mode is selected via bits COPM, the transceiver will not enter CAN Normal mode but will switch to or remain in CAN Silent mode. It will remain in CAN Silent mode until pin TXD goes high in order to prevent a hardware and/or software application failure from driving the bus lines to an unwanted dominant state.

The application can determine whether the CAN transceiver is ready to transmit data or is disabled by reading the CAN Transmitter Status bit (TXS) in the Transceiver Status Register (see section [2.2.7.2. TRXSR](#)).

## 2.2.6 CAN Reduced Normal Mode

In CAN Reduced Normal mode, the transmitter is switched off as VCC is lower than the  $V_{VCC\_UV\_TRX\_Set}$  threshold. All other features available in CAN Normal mode are also enabled in CAN Reduced Normal mode.

As shown in [Figure 2-5](#), the CAN transceiver enters the CAN Reduced Normal mode when the transceiver is in TRX Normal mode and  $V_{VCC} < V_{VCC\_UV\_TRX\_Set}$  for  $t > t_{UV\_VCC\_debounce}$ .



## 2.2.7 Related Registers

### 2.2.7.1 CAN Transceiver Control Register (address 0x20)

**Name:** TRXCR  
**Offset:** 0x20  
**Reset:** 0x41  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved	CFDPE	PNCFOK	CPNE	Reserved[1:0]		COPM[1:0]	
Access	R	R/W	R/W	R/W	R	R	R/W	R/W
Reset	0	1	0	0	0	0	0	1

**Bit 7 - Reserved** Reserved for future use

#### Bit 6 - CFDPE

The host microcontroller should set the bit to '1' to enable the CAN FD passive feature when selective wake-up is activated, otherwise to '0'. The bit is set to 1 by default after Power-on Reset. This setting has the effect that CAN FD frames are ignored when the device is waiting for a WUP. If set to 0, the error counter will increase if FD frames with a higher databitrate are sent during that time.

#### Bit 5 - PNCFOK

The host microcontroller should set the bit to '1' after successfully configuring the partial networking registers, otherwise to '0'. In addition, the device will reset the bit to 0 automatically after any write access to the partial networking configuration related registers.

#### Bit 4 - CPNE

The host microcontroller should set the bit to '1' to enable selective wake-up and otherwise to '0'.

**Bits 3:2 - Reserved[1:0]** Reserved for future use

#### Bits 1:0 - COPM[1:0] Select CAN Transceiver Operating Mode

The TRXCR register is a control register. Therefore, the state of the transceiver will not be mirrored to this register. COPM bit only defines the targeted state of the transceiver when the device is switched to Normal mode. The finite state machine in [Figure 2-5](#) will not change the COPM bits.

COPM[2:0]	CAN Transceiver Operating Mode
2'b00	CAN Standby mode
2'b01	CAN Normal Mode
2'b11	CAN Silent mode

### 2.2.7.2 CAN Transceiver Status Register (Address 0x22)

**Name:** TRXSR  
**Offset:** 0x22  
**Reset:** 0x48  
**Property:** Read-only

Bit	7	6	5	4	3	2	1	0
	TXS	PNERRS	PNCFS	PNOSCS	CBSS	Reserved[1:0]		TXDOOTS
Access	R	R	R	R	R	R	R	R
Reset	0	1	0	0	1	0	0	0

**Bit 7 – TXS** CAN Transmitter Status

The device sets the bit to '1' if the transmitter is ready to transmit data and to '0' if CAN transmitter is disabled.

**Bit 6 – PNERRS** Partial Networking Error Detection Status

The device sets the bit to '0' if no CAN partial networking error detected (PNEFD = 0 && PNCFOK = 1 && no oscillator hardware failure detected (default)), otherwise to '1' (PNEFD = 1 || PNCFOK = 0).

**Bit 5 – PNCFS** Partial Networking Configuration Status

The device sets the bit to '0' if partial networking configuration error is detected (PNCFOK = 0), otherwise to '1'.

**Bit 4 – PNOSCS** Partial Networking Oscillator Ok

The device sets the bit to '1' if CAN partial networking oscillator is running at target frequency, otherwise to '0'.

**Bit 3 – CBSS** CAN Bus Status

The device sets the bit to '1' if CAN bus is inactive (for longer than  $t_{\text{Silence}}$ ), otherwise to '0'.

**Bits 2:1 – Reserved[1:0]** Reserved for future use

**Bit 0 – TXDOOTS** TXD Time-out Status

The device sets the bit to '1' if CAN transmitter is disabled due to a TXD dominant time-out event, to '0' if no TXD dominant time-out event was detected.

**2.2.7.3 CAN Bus Failure Indication Register (Address 0x33)**

**Name:** BFIR  
**Offset:** 0x33  
**Reset:** 0x00  
**Property:** Read-only

Bit	7	6	5	4	3	2	1	0
	Reserved[5:0]						BOUT	BSC
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

**Bits 7:2 – Reserved[5:0]** Reserved for future use

**Bit 1 – BOUT** CAN Bus Dominant Time-out Event Indicator

The BOUT bit shows the current status of the bus dominant time-out detection. If the bit reads '1', the bus is currently in dominant time-out state, otherwise the bit reads '0'.

**Bit 0 – BSC** CAN Bus Short-circuit Event Capture Indicator

The BSC bit shows the current status of the bus short-circuit event detection. If the bit reads '1', the bus is currently in short-circuit state, otherwise the bit reads '0'.

### 2.2.7.4 CAN Transceiver Event Status Register 2 (Address 0x35)

**Name:** TRXESR2  
**Offset:** 0x35  
**Reset:** 0x00  
**Property:** Read-only

Bit	7	6	5	4	3	2	1	0
	Reserved[6:0]							RXDRCS
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

**Bits 7:1 – Reserved[6:0]** Reserved for future use

**Bit 0 – RXDRCS** RXD Recessive Clamping Status

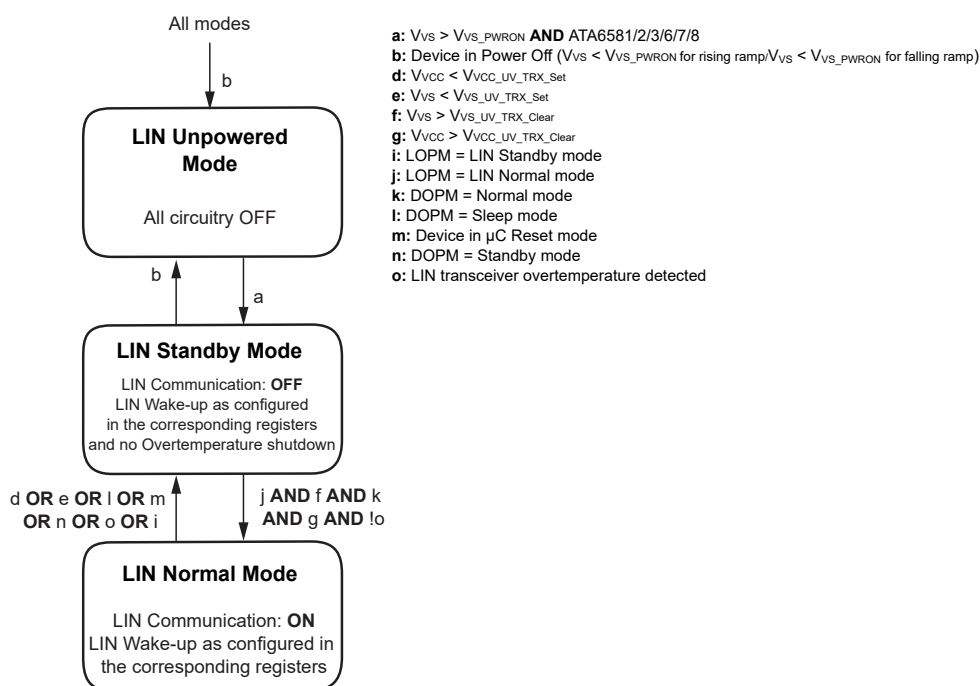
The device sets the bit to '1' if the event is enabled in the TRXECR2 register and a RXD recessive clamping event is detected. The bit is reset to '0' by the device either when the device enters Sleep, Standby or Unpowered mode or the RXD pin shows dominant again.

## 2.3 Integrated LIN Transceiver Operating Modes (not in the ATA6580/5)

The integrated LIN transceiver in the ATA658x is designed in compliance with the ISO 17987-4 and SAE J2602-2. It implements the LIN electrical physical layer. The device is designed to provide low-speed data communication in vehicles, for example, in convenience electronics. Improved slope control at the LIN bus ensures data communication up to 20Kbaud.

The integrated LIN transceiver supports the following operating modes: LIN Normal and LIN Standby. The LIN transceiver operating mode depends on the device operating mode and on the setting of bits LOPM in the LIN Mode Control register (see section 2.3.4.1. LTRXCR ). When the device is in Normal mode, the two operating modes can be selected via bits LOPM in the LIN mode control register.

**Figure 2-7. Integrated LIN Transceiver Operating Modes**



### 2.3.1 LIN Normal Mode

This is the normal transmission and receiving mode of the LIN interface. LIN bus wake up is not active in LIN Normal mode.

As shown in [Figure 2-7](#), the LIN transceiver will enter the LIN Normal mode in following case:

- From LIN Standby mode, when device operating mode is set to Normal mode **AND** no VCC TRX undervoltage is detected **AND** no VS TRX undervoltage is detected **AND** the device is switched to Normal mode **AND** no LIN transceiver overtemperature shutdown is detected **AND** LOPM is set to LIN Normal mode.

### 2.3.2 LIN Standby Mode

The LIN transceiver automatically switches to the LIN Standby mode after system power-up. In this mode, LIN communication is disabled. The internal termination resistor between the LIN pin and VS pin is disabled to minimize the current consumption in case the LIN pin is short-circuited to GND. Only a weak pull-up current (typically 10 $\mu$ A) between the LIN pin and the VS pin is present. Depending on the setting of the LINWUE bit (LIN bus wake-up event detection enable, see section [2.3.4. LIN Transceiver Related Registers](#)), the LIN bus wake up can be activated or deactivated. If the bit is set to '1', LIN bus voltage below the pre-wake detection LIN ( $V_{LINH}$ ) activates a strong pull-up current between VS and LIN to stabilize the recessive output voltage at LIN pin. At the same time, an internal LIN receiver is activated and the wake-up detection timer is started. If a valid LIN bus wake up has been detected, the register bit LINWUS will be set to '1'. The event will be signaled via the RXD and/or RXD\_LIN pin. The strong pull-up current will be switched off again when the LIN transceiver is in LIN Standby mode and the bit LINWUS is reset by the microcontroller. LIN wake up is disabled during a LIN transceiver overtemperature shutdown. As shown in [Figure 2-7](#) the LIN transceiver will enter the LIN Standby mode in the following cases:

1. From LIN Unpowered mode after device Power-on Reset.
2. From LIN Normal mode when VCC TRX undervoltage has been detected **OR** VS TRX undervoltage has been detected **OR** the device has been switched to Sleep/Standby/ $\mu$ C Reset mode **OR** LIN transceiver overtemperature shutdown has been detected **OR** if the bits LOPM in the LIN Transceiver mode control register are set to 2b01.

### 2.3.3 Behavior under Low Supply Voltage Condition

If  $V_{VS}$  is higher than the minimum VS operating threshold  $V_{VS\_PW\_RON}$ , the LIN Transceiver mode changes from LIN Unpowered mode to LIN Standby mode. As soon as  $V_{VS}$  exceeds the undervoltage threshold  $V_{VS\_UV\_TRX\_Clear}$  and  $V_{VCC} > V_{VCC\_UV\_TRX\_Clear}$ , the LIN transceiver can be activated.

If during LIN Standby mode the supply voltage on pin VS drops below the VS operating threshold  $V_{VS\_PW\_ROFF}$ , the LIN transceiver switches to LIN Unpowered mode.

If during LIN Normal mode the voltage level on the VS pin drops below the VS transceiver undervoltage detection threshold  $V_{VS\_UV\_TRX\_Set}$ , the LIN transceiver switches to LIN Standby mode. The LIN transceiver is disabled in order to avoid malfunctions and false bus messages. If the VCC voltage drops below the VCC TRX undervoltage threshold  $V_{VCC\_UV\_TRX\_Set}$ , the LIN transceiver will also switch to LIN Standby mode. LIN bus wake up is only possible when  $V_{VS}$  is higher than the VS TRX undervoltage detection level.

## 2.3.4 LIN Transceiver Related Registers

### 2.3.4.1 LIN Transceiver Control Register (address 0x21)

**Name:** LTRXCR  
**Offset:** 0x21  
**Reset:** 0x01  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved[5:0]						LOPM[1:0]	
Access	R	R	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	1

**Bits 7:2 – Reserved[5:0]** Reserved for future use

**Bits 1:0 – LOPM[1:0]** Select LIN Transceiver Operating Modes

LOPM[1:0]	LIN transceiver Operating Mode (LIN 1 transceiver in the ATA6582/3/7/8)
2'b01	LIN Standby mode
2'b10	LIN Normal mode

The LTRXCR register is a control register. Therefore, the state of the LIN transceiver will not be mirrored to this register. LOPM bit only defines the targeted state of the transceiver when the device is in Normal mode. The finite state machine in [Figure 2-7](#) will not change the LOPM bits.

### 2.3.4.2 LTRXSR – LIN Transceiver Status Register (address 0x24)

**Name:** LTRXSR  
**Offset:** 0x24  
**Reset:** 0x00  
**Property:** Read-only

Bit	7	6	5	4	3	2	1	0
	Reserved[5:0]						LTXDOUTS	LTXS
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

**Bits 7:2 – Reserved[5:0]** Reserved for future use

**Bit 1 – LTXDOUTS** TXD\_LIN Time-out Status

The device sets the bit to '1' if the LIN transmitter is disabled due to a TXD\_LIN dominant time-out event or to '0' if no TXD\_LIN dominant time-out event is detected.

**Bit 0 – LTXS** LIN Transceiver Status

The device sets the bit to '1' if the LIN transceiver is ready to transmit and receive data, otherwise to '0'.

## 2.4 Wake Up in the ATA6580/1/5/6

The ATA6580/1/5/6 can be woken up via the following wake-up sources: LIN (ATA6581/6), CAN, WAKE.

The different wake-up mechanisms are described in the following chapters.

## 2.4.1 Local Wake Up via Pin WAKE

In the ATA6580/1/5/6, the high-voltage WAKE input pin can be used to wake up the device. It is an edge-sensitive pin. The device wakes up from sleep on a low-to-high or high-to-low transition. The WAKE pin is usually connected to the ignition switch to generate a local wake up when the ignition is switched on.

A glitch suppression circuit is integrated to avoid unexpected wake up due to noise. A local wake-up request is detected only after the logic level on the WAKE pin has been stable for at least  $t_{local\_wu}$  and the new level remains stable for at least  $t_{local\_wu}$ .

Local wake up via the WAKE pin can be enabled/disabled via the register bits, LWUFE and LWURE (see section 2.4.5.14. [WKECR](#)), and the logic level at the WAKE pin can be read via the register PWKS (see section 2.4.5.2. [PWKS](#)) if  $V_{VCC}$  or  $V_{VCC\_μC}$  are within the valid range.

To reduce the battery current during Low-Power mode, the WAKE pin has internal pull-up/pull-down current sources that are activated when a stable level at the WAKE pin has been detected:

- High level on pin is followed by an internal pull-up towards VS.
- Low level is followed by an internal pull-down toward GND.

Local wake up can only be activated in Standby or Sleep mode. In Normal mode, the status of the voltage on the WAKE pin can always be read via bit PWKVS. Otherwise, PWKVS is only valid if local wake up is enabled. In applications that do not make use of the local wake-up feature, local wake up should be disabled and the WAKE pin should be connected to GND to ensure optimal EMI performance.

## 2.4.2 Remote Wake Up

### 2.4.2.1 LIN Remote Wake Up

Depending on the setting of the LINWUE bit (LIN bus wake-up event detection enable, see Section 2.3.4. [LIN Transceiver Related Registers](#)), the LIN bus wake up can be activated or deactivated. If the bit is set to '1', LIN bus voltage below the LIN driver dominant threshold activates the internal LIN receiver and starts the wake-up detection timer. A dominant bus level maintained for a certain period of time ( $> t_{bus}$ ) and the following rising edge at the LIN pin result in a remote wake-up request. If a valid LIN bus wake up has been detected, the register bit LINWUS will be set to '1'. A strong pull-up current source between VS and LIN is activated to stabilize the recessive output voltage at the LIN pin. The event will be signaled to the microcontroller via the RXD and/or RXD\_LIN pin. The strong pull-up current source will be switched off again when the LIN transceiver is in LIN Standby mode and the bit LINWUS is reset by the microcontroller.

### 2.4.2.2 Remote Wake-up Frame According to ISO 11898-2:2016

#### 2.4.2.2.1 CAN Selective Wake Up

Partial networking makes it possible for a CAN node or a CAN sub-network to be woken up individually by means of dedicated and predefined frames, the so-called Wake-up Frames (WUF). When a particular node's tasks are not required, it is put into selective Sleep mode.

The transceiver monitors the bus for dedicated CAN wake-up frames when both CAN wake up (CWUE = 1) and CAN selective wake up (CPNE = 1) are enabled, and the Partial Networking registers are configured correctly (PNCFOK = 1). An accurate oscillator and a low-power, high-speed comparator are activated to correctly detect wake-up frames.

According to ISO11898-2, a wake-up frame is a CAN frame consisting of an Identifier field (ID), a Data Length Code (DLC), a data field (optional) and a Cyclic Redundancy Check (CRC) code, including the CRC delimiter.

The wake-up CAN frame (ID and data) is fully configurable via the related registers for configuring CAN partial networking. A Standard (11-bit) or Extended (29-bit) Identifier, for the wake-up frame format, can be selected via bit IDE in the Frame Control register, CFCR (see section 2.4.4.10. [CFCR](#)).

The WUF ID is configured in the ID registers (see section 2.4.4.2. [CIDR0](#) to section 2.4.4.5. [CIDR3](#)). ID bits can be masked using the ID mask registers (see section 2.4.4.6. [CIDMR0](#) to section 2.4.4.9. [CIDMR3](#)), where a '1' means 'don't care'.

A single wake-up frame can wake up multiple groups of nodes by comparing the incoming data field with the data mask, as the data field indicates which nodes are to be woken up. Groups of nodes can be predefined and associated with bits in a data mask.

The number of data bytes expected in the data field of a CAN wake-up frame is set using the Data Length Code (bits DLC in the Frame Control register in section 2.4.4.10. [CFCR](#)). If  $DLC \neq 0000$  (one or more data bytes expected), at least one bit in the data field of the received wake-up frame must be set to '1' and at least one corresponding bit in the associated Data Mask register in the transceiver (register for data mask to be defined) must also be set to '1' for a successful wake up. Each matching pair of logic '1's indicates a group of nodes to be activated (since the data field is up to 8 bytes long, up to 64 groups of nodes can be defined).

If  $DLC = 0000$ , a node will wake up if the WUF contains a valid identifier and the received data length code is '0000', regardless of the values stored in the data mask. If  $DLC \neq 0000$  and all data mask bits are set to '0', the device cannot be woken up via the CAN bus (note that all data mask bits are '1' per default). If a WUF contains a valid ID but the DLCs (in the Frame Control register and in the WUF) do not match, the data field is ignored and no nodes will be woken up. The Data Length Code and the data field can be excluded from the evaluation of the wake-up frame. If bit  $PNDM = 0$  (see section 2.4.4.10. [CFCR](#)), only the identifier field is evaluated to determine if the frame contains a valid wake-up frame. If  $PNDM = 1$  (the default value), the data field is included as part of the wake-up filtering.

When  $PNDM = 0$ , a valid wake-up frame is detected and a wake-up event is captured (and  $CWUS$  is set to '1') when:

- The identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND
- The CRC field in the received frame (including a recessive CRC delimiter) was received without error.

When  $PNDM = 1$ , a valid wake-up frame is detected when:

- The identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND
- The frame is not a remote frame AND
- The Data Length Code in the received frame matches the configured Data Length Code (bits DLC) AND
- If the Data Length Code is greater than 0, at least one bit in the data field of the received frame is set and the corresponding bit in the associated Data Mask register is also set AND
- The CRC field in the received frame (including a recessive CRC delimiter) was received without error.

The internal error counter will be incremented when an erroneous CAN frame (e.g., a stuffing error) is received prior to the ACK field. If a CAN frame is received without any errors preceding the ACK field, the counter will be decremented. Any data received after the CRC delimiter and before the next SOF will be ignored by the partial networking module. If the counter overflows ( $FEC > ERRCNT$ , see section 2.4.4.11. [EFCR](#)), a frame detect error is captured ( $PNEFD = 1$ , see section 2.4.5.6. [CTRXESR](#)) and the device wakes up; the counter is reset to 0 when the bias is switched off.

After configuring the PN registers, the microcontroller must set the  $PNCFOK$  bit to 1. The device will clear the  $PNCFOK$  bit after a write access to any of the CAN Partial Networking Configuration registers (see section 2.4.4.1. [DRCR](#) to 2.4.4.14. [CDMR0..7](#)).

Any valid wake-up pattern (according to ISO 11898-2:2016) will trigger a wake-up event if selective wake up is disabled (CPNE = 0), or partial networking is not configured correctly (PNCFOK = 0) and the CAN transceiver is in TXD Standby mode with wake up enabled (CWUE = 1).

All wake-up patterns will be ignored, if the CAN transceiver is in CAN Normal/Silent mode or CAN wake up is disabled (CWUE = '0').

#### 2.4.2.2.2 CAN Selective Wake Up and CAN FD

CAN Flexible Data-Rate (CAN FD) is an improved CAN protocol with regard to bandwidth and payload. As specified in ISO 11898-1:2015, CAN FD is based on the CAN protocol and still uses the same arbitration method. However, after the arbitration phase, the data rate is increased and the data bits are transferred with a higher bit rate than in the arbitration phase. At the CRC delimiter, before the controllers transmit the Acknowledge bits, the bit rate is switched back to the same bit rate as used in the arbitration phase. Besides the increased bit speed, CAN FD allows data frames up to 64 bytes compared to the maximum of 8 bytes for classical CAN.

The ATA658x can be configured to recognize CAN FD frames as valid frames. When CFDPE = 1, the error counter is decremented every time the control field of a CAN FD frame is received. The device remains in Sleep mode with partial networking enabled. CAN FD frames are never recognized as valid wake-up frames, even if PNDM = 0 and the frame contains a valid ID. After receiving the control field of a CAN FD frame, the device ignores further bus signals until Idle is again detected.

When CFDPE is set to '0', CAN FD frames are interpreted as frames with errors by the partial networking module. Therefore, the error counter is incremented when a CAN FD frame is received. Bit PNEFD is set to '1' and the device wakes up if error the counter overflows.

#### 2.4.2.3 Remote Wake-up Pattern According to ISO 11898-2:2016

If the CAN transceiver is in TRX Standby mode and CAN bus wake up is enabled (CWUE = 1), but CAN selective wake up is disabled (CPNE = 0 or PNCFOK = 0), the device will monitor the bus for a standard wake-up pattern as specified in ISO 11898-2:2016.

This filtering helps avoid spurious wake-up events, which could be triggered by, for example, a dominant clamped bus or by dominant phases due to noise, spikes on the bus, transients or EMI.

The wake-up pattern consists of two dominant bus levels for a duration of at least  $t_{Filter}$ , each separated by a recessive bus level with a duration of at least  $t_{Filter}$ . Dominant or recessive bits in between the above mentioned phases that are shorter in duration than  $t_{Filter}$  are ignored.

The complete dominant-recessive-dominant pattern, as shown in [Figure 2-6](#), must be received within  $t_{Wake}$  to be recognized as a valid wake-up pattern. Otherwise, the internal wake-up logic is reset. The complete wake-up pattern will then need to be retransmitted to trigger a wake-up event.

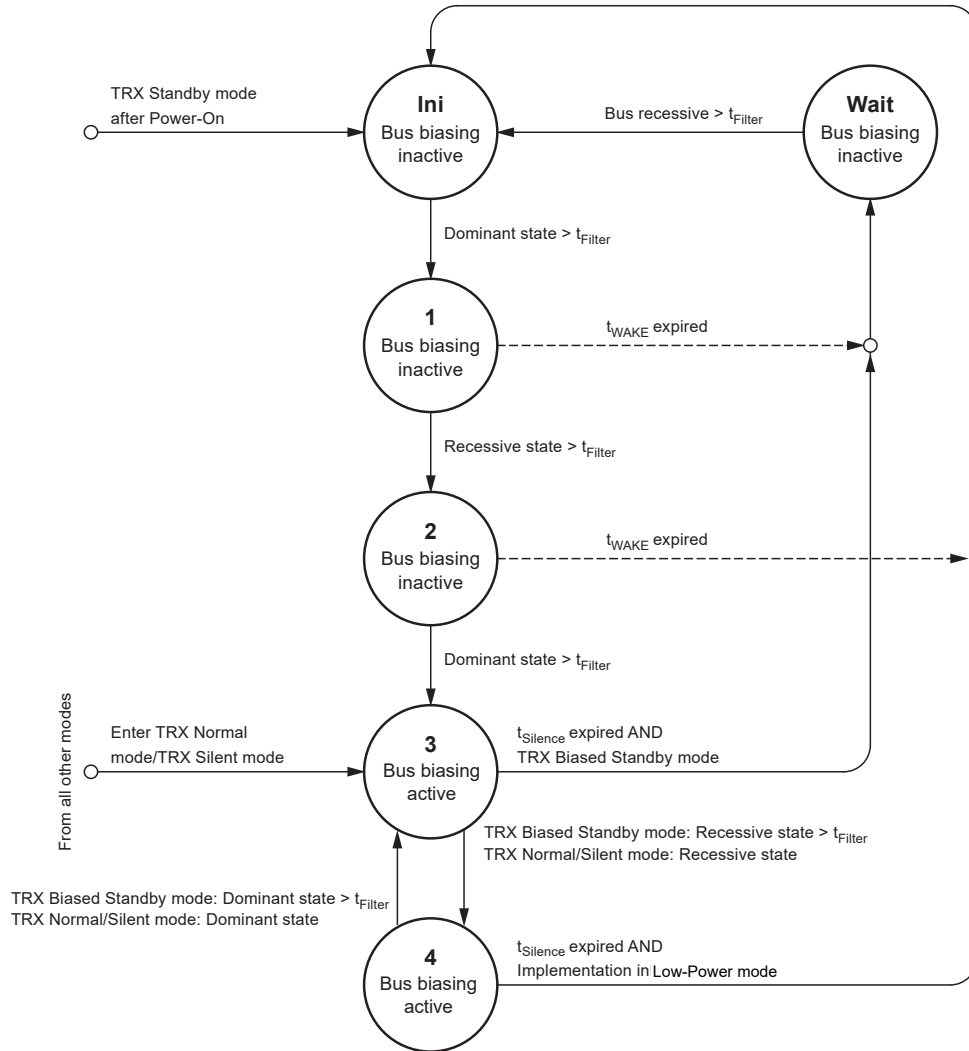
When a valid CAN WUP is detected on the bus, the wake-up bit CWUS in the Transceiver Event Status register is set (see section [2.4.5.6. CTRXESR](#)) and pin RXD is driven low.

CAN wake up via WUP can only be disabled via bit CWUE. If CWUE is set to '0', no remote wake up via the CAN bus is possible. If CWUE is set to '1' and selective wake up is disabled, the device will switch to Standby mode after detecting the Wake-up Pattern (WUP) coming from Sleep mode. If CWUE is set to '1' and the selective wake-up is enabled, the device will first switch on the bus biasing after detecting the WUP and will only switch afterward to Standby mode when it detects a valid WUF (This is described in chapter [2.4.2.2. Remote Wake-up Frame According to ISO 11898-2:2016](#)).

The figure below illustrates the control of the bus biasing and the WUP detection.



Figure 2-8. WUP Detection and Bias Control



### 2.4.3 Wake Up via SPI (ATA6582/3/7/8)

In case of an SPI command while the system is in a Low-Power mode (if VCC or VCC\_μC is active), but with enabled SPI interface, the device shall be woken up and enter the operating mode issued together with the SPI command. A SPI command failure, for instance invalid length of SPI command, write access to read-only register and etc. will also trigger an interrupt event of the device.

### 2.4.4 Related Registers for Configuring the CAN Partial Networking

#### 2.4.4.1 Data Rate Configuration Register (Address 0x26)

**Name:** DRCR  
**Offset:** 0x26  
**Reset:** 0x05  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved[4:0]					DR[2:0]		
Access	R	R	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	1	0	1

**Bits 7:3 – Reserved[4:0]** Reserved for future use

**Bits 2:0 – DR[2:0]** Select CAN Data Rate

DR[2:0]	CAN Data Rate (kbit/s)
3'b000	50
3'b001	100
3'b010	125
3'b011	250
3'b100	Reserved (intended for future use; currently selects 500kbit/s)
3'b101	500
3'b110	Reserved (intended for future use; currently selects 500kbit/s)
3'b111	1000

#### 2.4.4.2 CAN ID Register 0 (Address 0x27)

**Name:** CIDR0  
**Offset:** 0x27  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	ID0[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 7:0 – ID0[7:0]**  
ID0 bits ID07 to ID00 of the extended frame format

#### 2.4.4.3 CAN ID Register 1 (Address 0x28)

**Name:** CIDR1  
**Offset:** 0x28  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	ID1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 7:0 – ID1[7:0]**  
ID1 bits ID15 to ID08 of the extended frame format

#### 2.4.4.4 CAN ID Register 2 (Address 0x29)

**Name:** CIDR2  
**Offset:** 0x29  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	ID2[5:0]					ID2[1:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

##### Bits 7:2 – ID2[5:0]

ID2 bits ID23 to ID18 of the extended frame format; bits ID05 to ID00 of the standard frame format

##### Bits 1:0 – ID2[1:0]

ID2 bits ID17 to ID16 of the extended frame format

#### 2.4.4.5 CAN ID Register 3 (Address 0x2A)

**Name:** CIDR3  
**Offset:** 0x2A  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved[2:0]			ID3[4:0]				
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 7:5 – Reserved[2:0]** Reserved for future use

##### Bits 4:0 – ID3[4:0]

ID3 bits ID28 to ID24 of the extended frame format, bits ID10 to ID06 of the standard frame format

#### 2.4.4.6 CAN ID Mask Register 0 (Address 0x2B)

**Name:** CIDMR0  
**Offset:** 0x2B  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	IDM0[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

##### Bits 7:0 – IDM0[7:0]

IDM0 Mask bits ID07 to ID00 of the extended frame format. 1 means 'don't care'.

### 2.4.4.7 CAN ID Mask Register 1 (Address 0x2C)

**Name:** CIDMR1  
**Offset:** 0x2C  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	IDM1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

#### Bits 7:0 – IDM1[7:0]

IDM1 Mask bits ID15 to ID08 of the extended frame format. 1 means 'don't care'.

### 2.4.4.8 CAN ID Mask Register 2 (Address 0x2D)

**Name:** CIDMR2  
**Offset:** 0x2D  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	IDM2[5:0]						IDM2[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

#### Bits 7:2 – IDM2[5:0]

IDM2 Mask bits ID23 to ID18 of the extended frame format; bits ID05 to ID00 of the standard frame format.

#### Bits 1:0 – IDM2[1:0]

IDM2 Mask bits ID17 to ID16 of the extended frame format. 1 means 'don't care'.

### 2.4.4.9 CAN ID Mask Register 3 (Address 0x2E)

**Name:** CIDMR3  
**Offset:** 0x2E  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved[2:0]			IDM3[4:0]				
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 7:5 – Reserved[2:0]** Reserved for future use

#### Bits 4:0 – IDM3[4:0]

IDM2 Mask bits ID17 to ID16 of the extended frame format. 1 means 'don't care'.

### 2.4.4.10 CAN Frame Configuration Register (Address 0x2F)

**Name:** CFCR  
**Offset:** 0x2F  
**Reset:** 0x40  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	IDE	PNDM	Reserved[1:0]		DLC[3:0]			
Access	R/W	R/W	R	R	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

#### Bit 7 – IDE Identifier Format

The host microcontroller should set the bit to '1' if identifier is in extended frame format (29-bit), set to '0' if identifier is in standard frame format (11-bit).

#### Bit 6 – PNDM Partial Networking Data Mask

The host microcontroller should set the bit '1' if data length code and data field are evaluated at wake up, set to '0' if data length code and data field are 'don't care' for wake up.

#### Bits 5:4 – Reserved[1:0] Reserved for future use

#### Bits 3:0 – DLC[3:0] Data Length Configuration

Select number of data bytes expected in a CAN frame.

DLC[3:0]	Number of Data Bytes
4'b0000	0
4'b0001	1
4'b0010	2
4'b0011	3
4'b0100	4
4'b0101	5
4'b0110	6
4'b0111	7
4'b0000	8
4'b1001 to 4'b1111	Tolerated, 8 bytes expected; DM0 (data mask 0) ignored

### 2.4.4.11 Error Frame Counter Threshold Register (Address 0x3A)

**Name:** EFCR  
**Offset:** 0x3A  
**Reset:** 0x1F  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved[2:0]			EERCNT[4:0]				
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	1	1	1	1

#### Bits 7:5 – Reserved[2:0] Reserved for future use

**Bits 4:0 – EERCNT[4:0]** Set the Error Frame Counter Overflow Threshold

If the counter overflows (counter > EERCNT), a frame detect error is captured (PNEFD = 1) and the device wakes up.

**2.4.4.12 Failure Error Counter Register (Address 0x3B)**

**Name:** FECR  
**Offset:** 0x3B  
**Reset:** 0x00  
**Property:** Read-only

Bit	7	6	5	4	3	2	1	0
	Reserved[2:0]			FEC[4:0]				
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

**Bits 7:5 – Reserved[2:0]** Reserved for future use

**Bits 4:0 – FEC[4:0]**

If the device receives a CAN frame containing errors (e.g., a ‘stuffing’ error) that are received in advance of the ACK field, an internal error counter is incremented. If a CAN frame is received without any errors appearing before the ACK field, the counter is decremented. Data received after the CRC delimiter and before the next SOF is ignored by the partial networking module. If the counter overflows (FEC > EERCNT, see section FECR – Failure Error Counter Register (address 0x3B)), a frame detect error is captured (PNEFD = 1, see section TRXESR – Transceiver Event Status Register (address 0x63)) and the device wakes up; the counter is reset to zero when the bias is switched off and partial networking is re-enabled.

**2.4.4.13 Glitch Filter Threshold Register (Address 0x67)**

**Name:** GLFT  
**Offset:** 0x67  
**Reset:** 0x02  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved[4:0]				GLF[2:0]			
Access	R	R	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	1	0

**Bits 7:3 – Reserved[4:0]** Reserved for future use

**Bits 2:0 – GLF[2:0]**

Set the glitch filter threshold from 5% to 55% of the arbitration bit rate.

GLF[2:0]	#samples(≤500Kbit/s)	#samples(1Mbit/s)
3'b000	1 [<4.83%/<5.17%]	1 [<4.83%/<10.35%]
3'b001	2 [<4.83%/<7.76%]	2 [<9.66%/<15.52%]
3'b010	3 [<7.25%/<10.35%]	3 [<14.49%/<20.7%]
3'b011	4 [<9.66%/<12.94%]	4 [<19.32%/<20.87%]
3'b100	5 [<12.08%/<15.52%]	5 [<24.15%/<31.05%]
3'b101	6 [<14.49%/<18.11%]	6 [<28.99%/<36.22%]
3'b110	7 [<16.91%/<20.7%]	7 [<33.82%/<41.40%]
3'b111	24 [<57.97%/<64.69%]	13 [<62.8%/<72.45%]

## 2.4.4.14 CAN Data Mask Registers 0..7 (Address 0x68...0x6F)

**Name:** CDMR0..7  
**Offset:** 0x68...0x6F  
**Reset:** 0xFF  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	DM0...7[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

### Bits 7:0 – DM0...7[7:0] Data Mask 0...7 Configuration

**Table 2-1.** CAN Frame to Data Mask matching

Type	DLC			Type							
CAN Frame	DLC > 8	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	CRC
Data Mask	—	DLC	00	DM1	DM2	DM3	DM4	DM5	DM6	DM7	CRC
CAN Frame	DLC = 8	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	CRC
Data Mask	—	DLC	DM0	DM1	DM2	DM3	DM4	DM5	DM6	DM7	CRC
CAN Frame	DLC = 7	—	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	CRC
Data Mask	—	—	DLC	DM1	DM2	DM3	DM4	DM5	DM6	DM7	CRC
CAN Frame	DLC = 6	—	—	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	CRC
Data Mask	—	—	—	DLC	DM2	DM3	DM4	DM5	DM6	DM7	CRC
CAN Frame	DLC = 5	—	—	—	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	CRC
Data Mask	—	—	—	—	DLC	DM3	DM4	DM5	DM6	DM7	CRC
CAN Frame	DLC = 4	—	—	—	—	DLC	Byte 0	Byte 1	Byte 2	Byte 3	CRC
Data Mask	—	—	—	—	—	DLC	DM4	DM5	DM6	DM7	CRC
CAN Frame	DLC = 3	—	—	—	—	—	DLC	Byte 0	Byte 1	Byte 2	CRC
Data Mask	—	—	—	—	—	—	DLC	DM5	DM6	DM7	CRC
CAN Frame	DLC = 2	—	—	—	—	—	—	DLC	Byte 0	Byte 1	CRC
Data Mask	—	—	—	—	—	—	—	DLC	DM6	DM7	CRC
CAN Frame	DLC = 1	—	—	—	—	—	—	—	DLC	Byte 0	CRC
Data Mask	—	—	—	—	—	—	—	—	DLC	DM7	CRC

## 2.4.5 Related Registers for Configuring the CAN Partial Networking

### 2.4.5.1 Bus Failure Event Capture Enable Register (Address 0x32)

**Name:** BFECR  
**Offset:** 0x32  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved[5:0]						BOUTE	BSCE
Access	R	R	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

### Bits 7:2 – Reserved[5:0] Reserved for future use

**Bit 1 – BOUTE** Bus Dominant Time-out Event Capture Enable

The BOUTE bit must be set to '1' to enable the bus dominant time-out detection. Setting the bit to '0' disables the bus dominant time-out detection.

**Bit 0 – BSCE** Bus Short-circuit Event Capture Enable

The BSCE bit must be set to '1' to enable the bus short-circuit event detection. Setting the bit to '0' disables the bus short-circuit event detection.

**2.4.5.2 Pin WAKE Status Register (Address 0x4B)**

**Name:** PWKS  
**Offset:** 0x4B  
**Reset:** 0x00  
**Property:** Read-only

Bit	7	6	5	4	3	2	1	0
	Reserved[5:0]						PWKVS	Reserved
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

**Bits 7:2 – Reserved[5:0]** Reserved for future use

**Bit 1 – PWKVS** Pin WAKE Voltage Status

The device sets the bit to '1' if WAKE is high, to '0' if WAKE is low. PWKVS is always "0" in Power-Down mode if local wake up is disabled.

**Bit 0 – Reserved** Reserved for future use

**2.4.5.3 Global Event Status Register (Address 0x60)**

**Name:** GESR  
**Offset:** 0x60  
**Reset:** 0x01  
**Property:** Read-only

Bit	7	6	5	4	3	2	1	0
	OSCS	Reserved	BFES	LTRXES	WKES	CTRYES	LDOES	SYSES
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	1

**Bit 7 – OSCS** System Oscillator Status

The device sets the bit to '1' if a hardware failure of the system oscillator is detected and sets the bit to '0' when the system oscillator is disabled for power-saving purpose or the hardware failure disappeared after the oscillator is enabled (for instance, in device Normal mode).

**Bit 6 – Reserved** Reserved for future use

**Bit 5 – BFES** Bus Failure Event Status

The device sets the bit to '1' if there is bus failure event pending (any bit in the BFESR register is '1'). The bit reads '0' if all status bits in the BFESR register are cleared.

**Bit 4 – LTRXES** LIN Transceiver Event Status

The device sets the bit to '1' if there is a transceiver event pending (any bit in the LTRXESR register is '1'). The bit reads '0' if all status bits in the LTRXESR register are cleared.



**Bit 3 – WKES** WAKE Event Status

The device sets the bit to '1' if there is a wake-pin event pending (any bit in the WKESR register is '1'). The bit reads '0' if all status bits in the WKESR register are cleared.

**Bit 2 – CTRXES** CAN Transceiver Event Status

The device sets the bit to '1' if there is a transceiver event pending (any bit in the CTRXESR register is '1'). The bit reads '0' if all status bits in the CTRXESR register are cleared.

**Bit 1 – LDOES** Low-drop Voltage Regulators Event Status

The device sets the bit to '1' if there is a VCC or VCC sensor regulator event pending (any bit in the LDOESR register is '1').

**Bit 0 – SYSES** SYSES System Event Status

The device sets the bit to '1' if there is a system event pending (any bit in the SESR register is '1'). The bit reads '0' if all status bits in the SESR register are cleared.

**2.4.5.4 System Event Status Register (Address 0x61)**

**Name:** SESR  
**Offset:** 0x61  
**Reset:** 0x10  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	SYSE	VSUV	Reserved	PWRONS	Reserved[1:0]		SPIFS	IOUV
Access	R/W	R/W	R	R/W	R	R	R/W	R
Reset	0	0	0	1	0	0	0	0

**Bit 7 – SYSE**

Internal system error bit will be set by the device when:

1. Parity check of device trimming data registers has failed.
2. Internal voltage regulator failure has been detected.
3. Illegal internal digital state has been detected.

The bit can be reset to '0' by writing a '1' to the bit.

**Bit 6 – VSUV** VS Undervoltage Status

The device sets the bit to '1' if the event capture is enabled and the VS voltage is lower than  $V_{S\_UV\_TRX\_Set}$ . The bit can be reset to '0' by writing a '1' to the bit.

**Bit 5 – Reserved** Reserved for future use**Bit 4 – PWRONS** Power-on Status

The device sets the bit to '1' if the device has left Power-Off mode after power-on. The bit can be reset to '0' by writing a '1' to the bit.

**Bits 3:2 – Reserved[1:0]** Reserved for future use**Bit 1 – SPIFS** SPI Failure Status

The device sets the bit to '1' if the event is enabled in the SECR register and an SPI failure is detected. The bit can be reset to '0' by writing a '1' to the bit. SPIFS is also cleared when the device is forced to Sleep mode due to an undervoltage event.

### Bit 0 – IOUV IO Supply Voltage Undervoltage Event

The device sets the bit to '1' when the event capture is enabled and there is an undervoltage event detected at the IO supply ( $V_{VCC} < V_{VCC\_UV\_IO\_Set}$  in the ATA6580/1/5/6,  $V_{VCC\_μC} < V_{VCC\_UV\_IO\_Set}$  in the ATA6582/3/7/8). The bit can be reset to '0' by writing a '1' to the bit via SPI.

### 2.4.5.5 LIN Transceiver Event Status Register (Address 0x62)

**Name:** LTRXESR  
**Offset:** 0x62  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved[3:0]				LTXDOUT	OVTL	OTPWL	LINWUS
Access	R	R	R	R	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 7:4 – Reserved[3:0]** Reserved for future use

### Bit 3 – LTXDOUT LIN TXD Dominant Time-out Status

The device set the bit when an LIN TXD dominant time-out event is detected. The bit can be reset to '0' by writing a '1' to the bit.

### Bit 2 – OVTL LIN Transceiver Overtemperature Shutdown Event

The device sets the bit to '1' when the LIN transceiver temperature has exceeded the overtemperature shutdown threshold. The bit can be reset to '0' by writing a '1' to the bit.

### Bit 1 – OTPWL LIN Transceiver Overtemperature Prewarning Status

The device sets the bit to '1' if the event capture is enabled in the SECR register and the LIN transceiver temperature has exceeded the overtemperature prewarning threshold. The bit can be reset to '0' by writing a '1' to the bit.

### Bit 0 – LINWUS LIN Bus Wake-up Status

The device sets the bit to '1' if the event capture is enabled in the TRXECR register and a LIN wake-up event has been detected. The bit can be reset to '0' by writing a '1' to the bit.

### 2.4.5.6 CAN Transceiver Event Status Register (Address 0x63)

**Name:** CTRXESR  
**Offset:** 0x63  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved	PNOSCF	PNEFD	BS	OTPWC	OVTC	TRXF	CWUS
Access	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bit 7 – Reserved** Reserved for future use

### Bit 6 – PNOSCF Partial Networking Oscillator Hardware Failure

The device sets the bit to '1' if a partial networking oscillator hardware failure is detected and the event capture has been enabled (PNOSCFE= '1'). The bit can be reset to '0' by writing a '1' to the bit.

**Bit 5 – PNEFD** Partial Networking Frame Detection Status

The device sets the bit to '1' if a partial networking frame detection error is detected (error counter overflow). The bit can be reset to '0' by writing a '1' to the bit.

**Bit 4 – BS** Bus Status

The device sets the bit to '1' if the event is enabled in the TRXECR register and no activity on CAN bus is detected for  $t_{\text{silence}}$ . The bit can be reset to '0' by writing a '1' to the bit.

**Bit 3 – OTPWC** CAN Overtemperature Prewarning Status

The device sets the bit to '1' if the event capture is enabled in the SECR register and the CAN transceiver temperature has exceeded the overtemperature prewarning threshold. The bit can be reset to '0' by writing a '1' to the bit.

**Bit 2 – OVTC** CAN Transceiver Overtemperature Shutdown Event

The device sets the bit to '1' when the CAN transceiver temperature has exceeded the overtemperature shutdown threshold. The bit can be reset to '0' by writing a '1' to the bit.

**Bit 1 – TRXF** Transceiver Failure Status

The device sets the bit to '1' if the event is enabled in the TRXECR register and a CAN failure event was detected. The bit can be reset to '0' by writing a '1' to the bit. TRXF is also cleared when the device is forced to Sleep mode due to an undervoltage event. TRXF is set if:

- TXD is clamped dominant and the CAN transceiver is in CAN Normal mode.
- A VCC undervoltage is detected, the CAN transceiver is in CAN Normal or CAN Reduced Normal mode.
- A RXD recessive clamping error is detected and the CAN transceiver is in CAN Normal or CAN Reduced Normal mode or CAN Silent mode. The RXD recessive clamping error detection must additionally be enabled in the TRXECR2 register.

**Bit 0 – CWUS** CAN Wake-up Status

The device sets the bit to '1' if the event is enabled in the TRXECR register and a CAN wake-up event was detected. The bit can be reset to '0' by writing a '1' to the bit.

**2.4.5.7 WAKE Event Status Register (Address 0x64)**

**Name:** WKESR  
**Offset:** 0x64  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved[4:0]					EXTWUS	LWURS	LWUFS
Access	R	R	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 7:3 – Reserved[4:0]** Reserved for future use

**Bit 2 – EXTWUS**

Signalize a wake-up event from the LIN2 device in the ATA6582/3/7/8. The device sets the bit to '1' if the event detection is enabled and a wake-up event has been detected from the LIN2 device. The bit can be reset to '0' by writing a '1' to the bit.

**Bit 1 – LWURS** Local Wake-up Rising Edge Status

The device sets the bit to '1' if the event detection is enabled in the WKECR register and a rising edge on the WAKE pin is detected. The bit can be reset to '0' by writing a '1' to the bit. LWURS is also cleared when the device is forced to Sleep mode due to an undervoltage event.

**Bit 0 – LWUFS** Local Wake-up Falling Edge Status

The device sets the bit to '1' if the event detection is enabled in the WKECR register and a falling edge on WAKE pin is detected. The bit can be reset to '0' by writing a '1' to the bit. LWUFS is also cleared when the device is forced to Sleep mode due to an undervoltage event.

**2.4.5.8 Bus Failure Event Indication Status Register (Address 0x65)**

**Name:** BFESR  
**Offset:** 0x65  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved[5:0]						BOUTS	BSCS
Access	R	R	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 7:2 – Reserved[5:0]** Reserved for future use**Bit 1 – BOUTS** Bus Dominant Time-out Event Status Bit

The device sets the bit to '1' if a bus dominant time-out event is detected. The bit is set to '0' by writing '1' to the bit via SPI.

**Bit 0 – BSCS** Device Bus Short-Circuit Event Status Bit

The device sets the bit to '1' if a bus short-circuit event is detected. The bit is set to '0' by writing '1' to the bit via SPI.

**2.4.5.9 LDO Event Status Register (Address 0x66)**

**Name:** LDOESR  
**Offset:** 0x66  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	OVTVCC	OTPWVCC	OVVCC	UVVCC	OVTVCCSENS	OTPWVCCSE NS	OVVCCSENS	UVVCCSENS
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bit 7 – OVTVCC** VCC Regulator Overtemperature Shutdown Event

The device sets the bit to '1' when the VCC regulator temperature has exceeded the overtemperature shutdown threshold. The bit can be reset to '0' by writing a '1' to the bit.

**Bit 6 – OTPWVCC** VCC Regulator Overtemperature Prewarning Status

The device sets the bit to '1' if the event capture is enabled in the SECR register and the VCC regulator temperature has exceeded the overtemperature prewarning threshold. The bit can be reset to '0' by writing a '1' to the bit.

**Bit 5 – OVVCC** VCC Supply Voltage Overvoltage Event

The device sets the bit to '1' when the event capture is enabled and there is an overvoltage event detected at the VCC pin ( $V_{VCC} > V_{VCC\_OV\_Set}$ ). The bit can be reset to '0' by writing a '1' to the bit via SPI.

**Bit 4 – UVVCC** VCC Supply Voltage Undervoltage Event

The device sets the bit to '1' when the event capture is enabled and there is an undervoltage event detected at the VCC pin ( $V_{VCC} < V_{VCC\_UV\_TRX\_Set}$ ). The bit can be reset to '0' by writing a '1' to the bit via SPI.

**Bit 3 – OVTCCSENS** VCC Sensor Supply Overtemperature Shutdown Event

The device sets the bit to '1' when the temperature of the VCC sensor regulator has exceeded the overtemperature shutdown threshold. The bit can be reset to '0' by writing a '1' to the bit via SPI.

**Bit 2 – OTPWCCSENS** VCC Sensor Supply Overtemperature Prewarning Event

The device sets the bit to '1' when the event capture is enabled and the temperature of the VCC sensor regulator has exceeded the overtemperature prewarning threshold. The bit can be reset to '0' by writing a '1' to the bit via SPI.

**Bit 1 – OVCCSENS** Sensor Supply Voltage Overvoltage Event

The device sets the bit to '1' when the event capture is enabled and there is an overvoltage event detected at the VCC\_SENSOR pin ( $V_{VCC\_SENSOR} > V_{VCCSENS\_OV\_Set}$  for longer than  $t_{OV\_VCCSENS\_deb}$ ). The bit can be reset to '0' by writing a '1' to the bit via SPI. The VCC\_SENSOR LDO is disabled when the flag has been set and can be enabled again when the flag is reset by the microcontroller.

**Bit 0 – UVCCSENS** Sensor Supply Voltage Undervoltage Event

The device sets the bit to '1' when the event capture is enabled, and there is an undervoltage event detected at the VCC\_SENSOR pin ( $V_{VCC\_SENSOR} < V_{VCCSENS\_UV\_Set}$  for longer than  $t_{UV\_VCCSENS\_deb}$ ). The bit can be reset to '0' by writing a '1' to the bit via SPI.

**2.4.5.10 System Event Capture Enable Register (Address 0x04)**

**Name:** SECR  
**Offset:** 0x04  
**Reset:** 0x01  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved	VSUVE	Reserved[1:0]		IOUVE	OTPWE	SPIFE	RSTLVL
Access	R	R/W	R	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

**Bit 7 – Reserved** Reserved for future use

**Bit 6 – VSUVE** Enable VS TRX UV Event Capture

( $V_{VS} < V_{VS\_UV\_TRX\_Set}$ )

**Bits 5:4 – Reserved[1:0]** Reserved for future use

**Bit 3 – IOUVE** Enable IO Supply Undervoltage Event Capture

( $V_{VCC} < V_{VCC\_UV\_IO\_Set}$  in the ATA6580/1/5/6,  $V_{VCC\_μC} < V_{VCC\_UV\_IO\_Set}$  in the ATA6582/3/7/8)

**Bit 2 – OTPWE** Overtemperature Prewarning Event Capture

The OTPWE bit must be set to '1' to enable the overtemperature prewarning event capture. Setting the bit to '0' disables the overtemperature prewarning event capture.

### Bit 1 – SPIFE SPI Failure Event Capture

The SPIFE bit must be set to '1' to enable the SPI failure detection. Setting the bit to '0' disables the SPI failure detection.

### Bit 0 – RSTLVL

The bit must be set to '1' when a VCC undervoltage ( $V_{VCC} < V_{VCC\_UV\_TRX\_Set}$  in the ATA6580/1/5/6, or  $V_{VCC\_μC} < V_{VCC\_UV\_RST\_Set}$  in the ATA6582/7) shall trigger a mode switching to  $μC$  Reset mode, and to '0' when  $V_{VCC} < V_{VCC\_UV\_IO\_Set}$  in the ATA6580/1/5/6, or  $V_{VCC\_μC} < V_{VCC\_UV\_IO\_Set}$  in the ATA6582/3/7/8 shall trigger a mode switching to  $μC$  Reset mode.

## 2.4.5.11 LDO Event Capture Enable Register (Address 0x05)

**Name:** LDOECR  
**Offset:** 0x05  
**Reset:** 0x10  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved	VCCOVLHE[2:0]			VCCOVE	VCCUVE	VCCSENSOVE	VCCSENSUVE
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	0	0	0	0

**Bit 7 – Reserved** Reserved for future use

**Bits 6:4 – VCCOVLHE[2:0]** Enable VCC Overvoltage Signaling at LimpHome

VCCOVLHE	State	Description
001	Enabled (default)	A VCC overvoltage event during Standby or Normal or $μC$ Reset mode will cause the activation of the LimpHome pin
110	Disabled	A VCC overvoltage event will have no impact on the LimpHome pin
other	Enabled	Writing any other value to the bits will result in the enabled state setting

### Bit 3 – VCCOVE

Enable event capture when overvoltage is being detected at the VCC pin ( $V_{VCC} > V_{VCC\_OV\_set}$ )

### Bit 2 – VCCUVE

Enable VCC TRX undervoltage event capture ( $V_{VCC} < V_{VCC\_UV\_TRX\_Set}$ )

### Bit 1 – VCCSENSOVE

Enable overvoltage detection and event capture on the VCC\_SENSOR pin

### Bit 0 – VCCSENSUVE

Enable undervoltage event capture on the VCC\_SENSOR pin

## 2.4.5.12 Transceiver Event Capture Enable Register (Address 0x23)

**Name:** TRXECR  
**Offset:** 0x23  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved	PNOSCFE	Reserved	BSE	Reserved	LINWUE	TRXFE	CWUE
Access	R	R/W	R	R/W	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bit 7 – Reserved** Reserved for future use

**Bit 6 – PNOSCFE** Partial Networking Oscillator Hardware Failure Detection Enable

The PNOSCFE bit must be set to '1' to enable the CAN partial networking oscillator fail detection. Setting the bit to '0' disables the CAN partial networking oscillator fail detection.

**Bit 5 – Reserved** Reserved for future use

**Bit 4 – BSE** Bus Silence Detection Enable

The BSE bit must be set to '1' to enable the CAN bus silence detection. Setting the bit to '0' disables the CAN bus silence detection.

**Bit 3 – Reserved** Reserved for future use

**Bit 2 – LINWUE** LIN Transceiver Wake-up Event Capture Enable

**Bit 1 – TRXFE** Transceiver Failure Status Capture Enable

The TRXFE bit must be set to '1' to enable the CAN failure detection. Setting the bit to '0' disables the CAN failure detection.

**Bit 0 – CWUE** CAN Bus Wake-up (WUP) Detection Enable

The CWUE bit must be set to '1' to enable the CAN wake-up detection. Setting the bit to '0' disables the CAN wake-up detection.

#### 2.4.5.13 Transceiver Event Capture Enable Register 2 (Address 0x34)

**Name:** TRXECR2  
**Offset:** 0x34  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved[6:0]							RXDRCE
Access	R	R	R	R	R	R	R	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 7:1 – Reserved[6:0]** Reserved for future use

**Bit 0 – RXDRCE** RXD Recessive Clamping Capture Enable

The RXDRCE bit must be set to '1' to enable the RXD recessive clamping detection. Setting the bit to '0' disables the RXD recessive clamping detection.

#### 2.4.5.14 WAKE Event Capture Enable Register (Address 0x4C)

**Name:** WKECR  
**Offset:** 0x4C  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved[4:0]					EXTWUE	LWURE	LWUFE
Access	R	R	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 7:3 – Reserved[4:0]** Reserved for future use

#### Bit 2 – EXTWUE

Enable the event capture from the LIN2 device in the ATA6582/3/7/8

#### Bit 1 – LWURE

The bit must be set to “1” to enable the WAKE pin rising edge detection interrupt. Setting the bit to “0” disables the interrupt.

#### Bit 0 – LWUFE

The bit must be set to “1” to enable the WAKE pin falling edge detection interrupt. Setting the bit to “0” disables the interrupt.

## 2.5 Fail-Safe Features

### 2.5.1 CAN TXD Dominant Time-out Function

The CAN TXD dominant time-out timer is started when the TXD pin is set to low and the CAN transceiver is in CAN Normal mode. If the low state on the TXD pin persists for longer than  $t_{to(dom)}$ , the CAN transmitter is disabled, releasing the bus lines to the recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when the TXD pin is set to high. The TXD dominant time-out time also defines the minimum possible bit rate of 4 kbit/s.

When the TXD dominant time-out time is exceeded, a CAN failure interrupt is generated (TRXF = 1; see section 2.4.5.6. CTRXESR), if enabled (TRXFE = 1; see section 2.4.5.12. TRXECR). In addition, the status of the TXD dominant time-out can be read via the TXDOUTS bit in the Transceiver Status register (see section 2.2.7.2. TRXSR) and bit TXS is set to ‘0’. TXDOUTS is reset to ‘0’ and TXS is set to ‘1’ when the TXD pin is set to high again.

### 2.5.2 CAN TXD-to-RXD Short-Circuit Detection

When a short circuit appears between the RXD and TXD pins, the bus will be locked into a permanent dominant state due to the low-side driver of the RXD pin typically being stronger than the high-side driver of the connected microcontroller to TXD. The TXD dominant time-out timer is used to prevent this condition (refer to section 2.5.1. CAN TXD Dominant Time-out Function for the behavior in this case). The TXD dominant time-out timer is activated when the CAN transceiver is in the CAN Normal mode and the TXD pin is low.

### 2.5.3 CAN Bus Dominant Clamping Detection

A CAN bus short circuit (to VS, VCC or GND) or a failure in one of the other network nodes could result in a differential voltage on the bus high enough to represent a bus dominant state. Because a node will not start transmission if the bus is dominant, the normal bus failure detection will not detect this failure, but the bus dominant clamping detection will. The bus dominant time-out timer is activated when the transceiver is in the CAN Normal mode, the TXD pin is high and the bus is dominant. The timer for detecting the bus dominant clamping failure will be reset by any signal change at the TXD pin or on the CAN bus. When the bus dominant clamping is detected and the failure detection is enabled (BOUTE = 1; see section 2.4.5.1. BFECR), the bits, BOUT and BOUTS, are set to ‘1’ by the device and a bus failure interrupt is generated (BFES = 1; see section 2.4.5.3. GESR). The bit BOUT is reset to ‘0’ as soon as the bus state is changed to recessive again. The status of

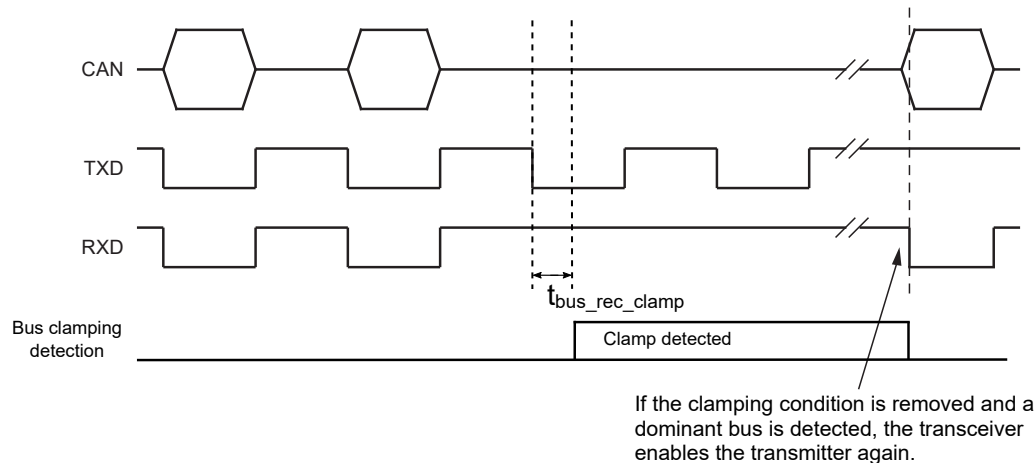


the bus dominant clamping can be read via the BOUT bit in the Bus Status register (see section 2.2.7.3. BFIR).

## 2.5.4 CAN Bus Recessive Clamping Detection

When the device detects a CAN bus recessive clamping for  $t_{\text{bus\_rec\_clamp}}$  and the failure detection is enabled (BSCE = 1; see section 2.2.7.3. BFIR), the CAN bus failure flags, BSC and BSCS, are set to '1' and a bus failure interrupt is generated (BFES = 1; see section 2.4.5.3. GESR). The status of the bus recessive clamping failure can be read via the BSC bit in the Bus Status register. The bit BSC is reset to '0' as soon as the bus state is changed to dominant again or when the CAN transceiver leaves the CAN Normal mode.

Figure 2-9. CAN bus recessive clamping detection



## 2.5.5 Internal Pull-up Structure at the TXD Input Pin

The TXD and TXD\_LIN pins have an internal pull-up structure to VCC. This ensures a safe, defined state in case the pin is left floating. The pull-up current flows into the pin in all states, therefore the pin should be in high state during CAN/LIN Standby mode to minimize the current consumption.

## 2.5.6 Undervoltage and Overvoltage Detection on Pin VCC

When an undervoltage event at the VCC pin has been detected, a status bit UWCC (see section 2.4.5.9. LDOESR) will be set if the corresponding event capture bit is set (VCCUVE = '1', see section 2.4.5.11. LDOECR). The event will be then signaled via pin RXD and/or RXD\_LIN. (Please refer to section 2.5.13. Wake-Up and Interrupt Event Diagnostics via Pin RXD and pin RXD\_LIN for details about the event signalization via the RXD and/or RXD\_LIN pins.) In addition, status bit VCCS is set to 1 (see section 2.2.7.2. TRXSR).

In the ATA658x, a CAN failure interrupt is also generated (TRXF = 1, if enabled via TRXFE = 1; see section 2.4.5.12. TRXECR) when the CAN transceiver supply voltage  $V_{\text{VCC}}$  falls below the undervoltage detection threshold ( $V_{\text{VCC\_UV\_TRX\_Set}}$ ), provided COPM = 01.

If VCCOVE is set to '1' (see section 2.4.5.11. LDOECR), the event capture for overvoltage detection is enabled for the VCC pin. In case  $V_{\text{VCC}} > V_{\text{VCC\_OV\_Set}}$  has been detected for longer than  $t_{\text{OV\_VCC\_deb}}$ , the VCC overvoltage event flag OVVCC (see section 2.4.5.9. LDOESR) will be set and the event will be signaled via the RXD and/or RXD\_LIN pin. Bit VCCOVSD (see section 2.1.6.1. DMCR) defines how the device behaves after detecting VCC overvoltage. If VCCOVSD is set to '0', the device will not react to the overvoltage besides signaling the event to the host. The host is responsible for taking care the further protection of the ECU in this case. If VCCOVSD is set to '1', the device will switch off the VCC regulator. The ATA6580/1/5/6 VCC regulator will be disabled by forcing the device into Sleep mode. The regulator will be enabled again when a wake-up event or an interrupt event triggers a wake up of the device.

The ATA6582/3/7/8 VCC regulator will be disabled without any device operating mode transition and will be again enabled when the OVVCC flag is set to '0'.

During an undervoltage or overvoltage event at VCC, the Limp Home output will be asserted.

If enabled, a CAN failure interrupt is generated ( $TRXF = 1$ ) when the CAN transceiver supply voltage,  $V_{VCC}$ , falls below the undervoltage detection threshold ( $V_{VCC\_UV\_Set}$ ), provided  $COPM = 01$ . In addition, status bit VCCS is set to '1' (see section 2.2.7.2. TRXSR).

### 2.5.7 Overvoltage Detection on Pin VCC (ATA6580/1/5/6)

When the bit VCCOVE is set to '1' (see section 2.4.5.11. LDOECR), the event capture for overvoltage detection is enabled for the VCC pin. In case  $V_{VCC} > V_{VCC\_OV\_Set}$  has been detected for longer than  $t_{OV\_VCC\_deb}$ , the VCC overvoltage event flag OVVCC (see section 2.4.5.9. LDOESR) will be set and the event will be signaled via the RXD and/or RXD\_LIN pin. Bit VCCOVSD (see section 2.1.6.1. DMCR) defines how the device behaves after detecting VCC overvoltage. If VCCOVSD is set to '0', the device will not react to the overvoltage besides signaling the event to the host. If VCCOVSD is set to '1', the device will switch off the VCC regulator. The ATA6580/1/5/6 VCC regulator will be disabled by forcing the device into Sleep mode. The regulator will be enabled again when a wake-up event or an interrupt event triggers a wake up of the device.

The ATA6582/3/7/8 VCC regulator will be disabled without any device operating mode transition and will be again enabled when the OVVCC flag is set to '0'.

If an overvoltage is detected on pin VCC for longer than the overvoltage detection debounce time,  $t_{OV\_VCC\_deb}$ , the device transitions to Sleep mode after  $t_{OV\_VCC\_deb}$  if VCCOVSD is set to '1' (see Figure 2-1). The following preventative measures are taken before the device transitions to Sleep mode to avoid deadlock and unpredictable states:

- All previously captured events (address range 0x61 to 0x66) are cleared before the device switches to Sleep mode to avoid repeated attempts to wake up while an undervoltage is present.
- Both CAN remote wake up ( $CWUE = 1$ , ATA6585/6) and local wake up via the WAKE pin ( $LWUFE = LWURE = 1$ ) are enabled to avoid that the device cannot be woken up after entering Sleep mode.
- Partial Networking is disabled ( $CPNE = 0$ , ATA6585/6) to ensure immediate wake up in response to bus traffic.
- The Partial Networking Configuration bit is cleared ( $PNCFOK = 0$ , ATA6585/6) to indicate that partial networking might not have been configured correctly when the device switched to Sleep mode.

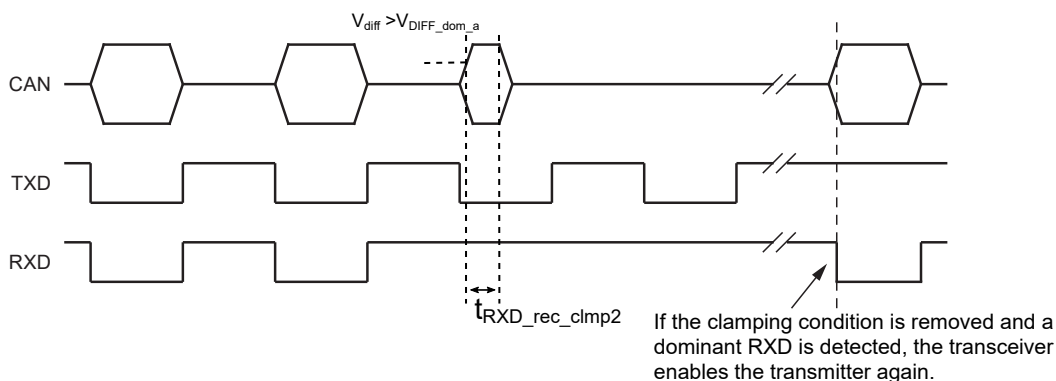
To assist in determining a diagnosis: Status bit SMTS is set to 1 when a transition to Sleep mode was caused by an overvoltage event (see section 2.1.6.1. DMCR, this bit notifies the host that the settings of the wake-up source should be reconfigured).

### 2.5.8 Short-Circuit Protection of the Bus Pins

The CANH and CANL bus outputs are short-circuit protected, either against GND or a positive supply voltage ( $V_{VS}$ ,  $V_{VCC}$ ). A current-limiting circuit protects the transceiver against damage. If the device is heating up due to a continuous short on CANH or CANL, the internal overtemperature protection switches off the bus transmitter.

### 2.5.9 RXD Recessive Clamping

This fail-safe feature prevents the controller from sending data on the CAN bus if its RXD line is clamped to high (e.g., recessive). If the RXD pin cannot signalize a dominant bus condition, e.g., because it is shorted to VCC, the transmitter is disabled to avoid possible data collisions on the bus. In CAN Normal mode and CAN Silent mode, the device permanently compares the state of the High-Speed Comparator (HSC) with the state of the RXD pin. If the HSC indicates a dominant bus state for more than  $t_{RXD\_rec\_clmp}$  without the RXD pin doing the same, a recessive clamping failure is detected.

**Figure 2-10. RXD Recessive Clamping Detection**

A CAN transceiver failure interrupt (not denoted at THE RXD pin) is generated ( $TRXF = 1$ ; see section 2.4.5.6. [CTRSES](#)), if enabled ( $TRXFE = 1$  and  $RXDRCE = 1$ ; see section 2.4.5.12. [TRXECR](#) and section 2.4.5.13. [TRXECR2](#)). In addition, the status of the RXD recessive clamping failure can be read via the  $RXDRCS$  bit in the Status register (see section 2.2.7.4. [TRXESR2](#)) and bit  $TXS$  is set to '0'. The RXD recessive clamping detection is reset by either entering Sleep, Standby or Unpowered mode, or the RXD pin shows dominant again.

### 2.5.10 Overtemperature Detection and Selective Overtemperature Shutdown

The device provides two levels of overtemperature protection and monitors the chip temperature of the LIN transceiver, CAN transceiver, VCC LDO, VCC\_SENSOR LDO and VCC\_μC.

In the case  $OTPWE$  bit is set to 1 (overtemperature prewarning monitor enable) and the temperature of one or more monitored circuit blocks rises above the overtemperature protection prewarning threshold ( $T > T_{OT\_Prew}$ ), the device will set the common status bit  $OTPWS = '1'$ . At the same time, the corresponding individual status bit will be set ( $OTPWL$  and/or  $OTPWC$  and/or  $OTPWCC$  and/or  $OTPWCCSENS$ ) and an overtemperature prewarning interrupt will be generated over RXD and/or RXD\_LIN pin. (Section section 2.5.13. [Wake-Up and Interrupt Event Diagnostics via Pin RXD and pin RXD\\_LIN](#) describes overtemperature signalization.) The bit  $OTPWS$  will be set to '0' by the device when the temperature of all monitored circuit blocks is below the overtemperature protection prewarning threshold.

When the temperature of a monitored circuit block rises above the overtemperature protection shutdown threshold ( $T_{Vsd}$ ), the overtemperature shutdown protection will be triggered for the corresponding circuit block. The integrated CAN transceiver is switched to the CAN Off mode if a CAN transceiver overtemperature shutdown has been triggered and the CAN bus pins are tri-stated. The integrated LIN transceiver is switched to the LIN Standby mode if a LIN transceiver overtemperature shutdown has been triggered. The 5V VCC LDO and/or the VCC\_SENSOR regulator are/is disabled when overtemperature shutdown has been triggered for the corresponding regulators.

At the same time, overtemperature event capture flags are set (section 2.5.13. [Wake-Up and Interrupt Event Diagnostics via Pin RXD and pin RXD\\_LIN](#)) and an interrupt will be generated over RXD and/or RXD\_LIN pin.

Further wake-up events are still detected from wake-up sources which are not disabled due to the overtemperature protection, and a pending wake-up/interrupt event will still be signaled by a low level on pin RXD and/or RXD\_LIN.

In the ATA6582/3/7/8, the LIN2 transceiver and the VCC\_μC LDO have its own temperature monitoring. The VCC\_μC LDO is protected against overload by means of current limitation and overtemperature shutdown. In case of overtemperature shutdown, the LIN2 will be also switched off. The VCC regulator works independently during LIN overtemperature shutdown.

The device provides two levels of overtemperature protection. In the case that the chip temperature rises above the Overtemperature Protection Prewarning Threshold ( $T > T_{OT\_Prew}$ ), the device will first set the status bit,  $OTPWS = 1$ . If the overtemperature prewarning event capture is enabled ( $OTPWE = 1$ ,  $COPM = '00'$  and  $DOPM = '111'$ ), an overtemperature prewarning interrupt will be generated ( $OTPW = 1$ ). If  $DOPM$  is set to  $'111'$  but  $COPM$  is not configured to  $'00'$ , and the overtemperature prewarning event capture is enabled ( $OTPWE = 1$ ), only the overtemperature prewarning flag will be set ( $OTPW = 1$ ) and no interrupt will be generated.

### 2.5.11 TXD\_LIN/TXD\_LIN2 Dominant Time-out Function

An internal timer prevents the LIN bus line from being driven permanently to the dominant state. If the low state on  $TXD\_LIN$  persists for longer than  $t_{to(dom)\_LIN}$ , the LIN transceiver will be disabled. To reactivate the LIN transceiver,  $TXD\_LIN$  has to be high for longer than  $10\ \mu s$ . The dominant time-out function on the  $TXD\_LIN2$  pin works the same way as on the  $TXD\_LIN$  pin using its own dedicated timer.

If the  $TXD\_LIN$  or  $TXD\_LIN2$  pin stays at GND level while switching into LIN Normal mode, it must be pulled to high level longer than  $10\ \mu s$  before the LIN driver can be activated. This feature prevents the bus line from being accidentally driven to the dominant state after Normal mode has been activated (also in case of a short circuit at  $TXD\_LIN$  to GND).

In the ATA6582/3/7/8, the  $TXD\_LIN2$  pin is used as an output and signals the fail-safe source when the transceiver is in the LIN Fail-Safe mode.

The  $TXD\_LIN$  Dominant Timeout function is activate in LIN Normal mode.

### 2.5.12 Loss of Power at Pin VS

In case of a power loss on the  $VS$  pin, the CAN and LIN bus and the I/O pins are tri-stated. No reverse currents will flow from the bus into the device.

### 2.5.13 Wake-Up and Interrupt Event Diagnostics via Pin RXD and pin RXD\_LIN

Wake-up and interrupt event signaling provide status information to the microcontroller. The information is stored in the Event Status registers (see section 2.4.5.4. [SESR](#) to section 2.4.5.8. [BFESR](#)) and is signaled on the  $RXD$  and  $RXD\_LIN$  pins, if enabled.

The device sets the internal wake-up flag ( $LINWUS$  (ATA6581/2/3/6/7/8 only),  $CWUS$ ,  $LWURS$  and  $LWUFS$ , see section 2.4.5.5. [LTRXESR](#), 2.4.5.6. [CTRXESR](#), if a valid wake-up event occurs. In addition  $RXD$  and/or  $RXD\_LIN$  are driven low, if  $V_{VS}$  and  $V_{VCC}$  are present.

A distinction is made between regular wake-up events and interrupt events. At least one regular wake-up source must be enabled before the device transitions to Sleep mode.

**Table 2-2.** Wake-up Events

Symbol	Event	Power On	Description
CWUS	CAN Bus Wake Up	Disabled	A CAN wake-up event was detected.
LWURS	Rising Edge on WAKE Pin	Disabled	A rising-edge wake up was detected on pin WAKE.
LWUFS	Falling Edge on WAKE Pin	Disabled	A falling-edge wake up was detected on pin WAKE.
LINWUS	LIN Bus Wake Up	Disabled	A LIN bus wake-up event was detected (ATA6581/2/3/6/7/8 only).
EXTWUS	Wake Up from the LIN2 Device	Disabled	A recover of $V_{CC\_μC}$ voltage has been detected (ATA6582/3/7/8).

**Table 2-3. Interrupt Events**

Symbol	Event	Power On	Description
PWRONS	Device Power On	Always enabled	The device has exited Power-Off mode (after battery power has been restored/connected).
OTPWL	LIN Transceiver Overtemperature Prewarning	Disabled	The LIN transceiver temperature has exceeded the overtemperature warning threshold (only in Normal mode).
OTPWC	CAN Transceiver Overtemperature Prewarning	Disabled	The CAN transceiver temperature has exceeded the overtemperature warning threshold (only in Normal mode).
OTPWVCC	VCC LDO Overtemperature Prewarning	Disabled	The 150mA VCC low dropout voltage regulator temperature has exceeded the overtemperature warning threshold (active when LDO is active).
OTPWVCCSENS	VCC Sensor LDO Overtemperature Prewarning	Disabled	The 30mA low dropout voltage regulator temperature has exceeded the overtemperature warning threshold (active when LDO is active).
OVTL	LIN Transceiver Overtemperature Shutdown	Always enabled	The LIN transceiver temperature has exceeded the overtemperature shutdown threshold (only in Normal mode).
OVTC	CAN Transceiver Overtemperature Shutdown	Always enabled	The CAN transceiver temperature has exceeded the overtemperature shutdown threshold (only in Normal mode).
OVTVCC	VCC LDO Overtemperature Shutdown	Always enabled	The 150mA VCC low dropout voltage regulator temperature has exceeded the overtemperature shutdown threshold (active when LDO is active).
OVTVCCSENS	VCC Sensor LDO Overtemperature Shutdown	Always enabled	The 30mA VCC sensor low dropout voltage regulator temperature has exceeded the overtemperature shutdown threshold (active when LDO is active).
SPIFS	SPI Failure	Disabled	SPI clock count error (only 16, 24 and 32-bit commands are valid), illegal DOPM code or attempted write access to locked register (not in Sleep mode).
PNEFD	Partial Networking Frame Detection Error	Always enabled	Partial networking frame detection error counter overflow
BS	CAN Bus Silence	Disabled	No activity on CAN bus for $t_{\text{Silence}}$
TRXF	CAN Transceiver Failure	Disabled	One of the following CAN failure events detected (not in Sleep mode): <ul style="list-style-type: none"> <li>TXD dominant time-out detected.</li> <li>CAN transceiver deactivated due to a <math>V_{\text{VCC}}</math> undervoltage event (if <math>\text{COPM} = 01</math>, <math>V_{\text{VCC}} &lt; V_{\text{VCC\_UV\_TRX\_Set}}</math>).</li> <li>RXD recessive clamping error detected (CAN Normal or CAN Reduced Normal mode or Silent mode only).</li> </ul>
BOUTS	Bus Dominant Time-out Failure	Disabled	Bus is detected as dominant for $t > t_{\text{BUS\_dom}}$ (not in Sleep mode).
BSCS	Bus Short-Circuit (Recessive Time-out) Failure	Disabled	The device detects a CAN bus recessive clamping (not in Sleep mode).
PNOSCF	Partial Networking Oscillator Hardware Failure	Disabled	The device detects the hardware failure of the partial networking oscillator.
VSUV	VS Undervoltage for Transceivers	Disabled	The device detects $V_{\text{VS}} < V_{\text{VS\_UV\_TRX\_Set}}$ .
UVCC	VCC Undervoltage for Transceivers	Disabled	The device detects $V_{\text{VCC}} < V_{\text{VCC\_UV\_TRX\_Set}}$ .
OVCC	VCC Overvoltage	Disabled	The device detects $V_{\text{VCC}} > V_{\text{VCC\_OV\_Set}}$ .
IOUV	IO Supply Undervoltage	Disabled	The device detects $V_{\text{VCC}} < V_{\text{VCC\_UV\_IO\_Set}}$ (ATA6580/1/5/6); $V_{\text{VCC\_}\mu\text{C}} < V_{\text{VCC\_UV\_IO\_Set}}$ (ATA6582/3/7/8).

.....continued

Symbol	Event	Power On	Description
UVCCSENS	VCC_SENSOR Undervoltage	Disabled	The device detects $V_{VCC\_SENSOR} < V_{VCCSENS\_UV\_Set}$ .
OVCCSENS	VCC_SENSOR Overvoltage	Disabled	The device detects $V_{VCC\_SENSOR} > V_{VCCSENS\_OV\_Set}$ .
LTXDOUT	LIN TXD Time-out Event	Disabled	LIN TXD dominant time-out detected.

PWRONS, PNEFD, all overtemperature shutdown and system events are always captured. The detection of other wake-up and interrupt events can be enabled/disabled individually using the event capture enable registers (see section 2.4.5.10. [SECR](#) to section 2.4.5.14. [WKECR](#)).

If an event occurs while the associated event capture function is enabled, the relevant event status bit is set. If the CAN and/or LIN transceiver is not active (CAN transceiver not in CAN Normal/CAN Silent mode, LIN not in LIN Normal mode), pin RXD and/or RXD\_LIN (if VCC is available) is asserted low to indicate that a wake-up or interrupt event has been detected. The detection of any enabled wake-up or interrupt event will trigger a wake up from Sleep mode. The table below describes the voltage level of the RXD and RXD\_LIN pins and which blocks are active/disabled in the different operating modes.

**Table 2-4.** Device operating mode and device functions

Block	Device Operating Mode				
	Power Off	Standby	Normal	Sleep	µC Reset
SPI	Disabled	Active	Active	Active (if VCC or VCC_µC is applied and NRES is high)	Disabled
LIN	LIN Unpowered	LIN Standby	LIN Standby/LIN Normal	LIN Standby	LIN Standby
CAN	CAN Off	CAN Standby/ CAN Biased Standby	CAN Normal/CAN Standby/CAN Biased Standby/CAN Silent (determined by bits COPM)	CAN Standby/ CAN Biased Standby	CAN Standby/ CAN Biased Standby
RXD	VCC level	VCC level/low if wake-up/interrupt event detected	CAN bit stream if COPM=01/11; otherwise same as Standby/Sleep	VCC level/low if wake-up/interrupt event detected	VCC level/low if wake-up/interrupt event pending
RXD_LIN	VCC level	VCC level/low if wake-up/interrupt event detected	VLIN bit stream if LOPM=10; otherwise same as Standby/Sleep	VCC level/low if wake-up/interrupt event pending	VCC level/low if wake-up/interrupt event pending
NRES	Low	High	High	Low	Low

The microcontroller can monitor events via the Event Status registers. An extra status register, the Event Summary Status register (see section 2.4.5.3. [GESR](#)), is provided to help speed up software polling routines. By polling the Global Event Status register, the microcontroller can quickly determine the type of event captured (system, transceiver or WAKE) and then query the relevant register, respectively.

After the event source has been identified, the status bit should be cleared (set to '0') by writing '1' to the relevant bit (writing '0' will have no effect). A number of status bits can be cleared in a single write operation by writing '1' to all relevant bits. It is strongly recommended to clear only the status bits that were set to '1' when the status registers were last read. This precaution ensures that events triggered just before the write access are not lost.

### 2.5.14 Interrupt Event/Wake-up Event Delay

Frequent interrupt or wake-up events while the CAN transceiver is in CAN Standby mode or the LIN transceiver is in LIN Standby mode, can require significant microcontroller processing time because the pin RXD/RXD\_LIN is driven low each time an interrupt/wake up is generated. Therefore, the device incorporates an interrupt/wake-up delay timer to limit the frequency of wake-up events.

When one of the event capture status bits is cleared, pin RXD/RXD\_LIN is released (high) and a timer is started. If further events occur while the timer is running, the relevant status bits are set. If one or more events are pending when the timer expires after  $t_{d\_evt\_cap}$ , pin RXD/RXD\_LIN goes low again to alert the microcontroller.

In this way, the microcontroller is interrupted once to process multiple events, rather than for each individual event. If all active event capture bits have been cleared (by the microcontroller) when the timer expires after  $t_{d\_evt\_cap}$ , pin RXD/RXD\_LIN remains high (since there are no pending events). The Event Capture registers can be read at any time.

### 2.5.15 Sleep Mode Protection

It is very important that event detection is configured correctly before the device switches to Sleep mode to ensure it will respond to a wake-up event. To avoid that the device does not wake up from Sleep mode, at least one regular wake-up event must be enabled and all event status bits must be cleared before the device transitions to Sleep mode. Otherwise, the device will transition to Standby mode in response to a Go-to-Sleep command (DOPM = Sleep).

## 2.6 Device ID

A byte is reserved at address 0x7E for a device identification code.

### 2.6.1 Device ID Register (Address 0x7E)

**Name:** DIDR  
**Offset:** 0x7E  
**Reset:** 0x8x  
**Property:** Read-only

The register provides the ID of the ATA658x.

Bit	7	6	5	4	3	2	1	0
	DID[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	1	0	0	0	x	x	x	x

#### Bits 7:0 - DID[7:0]

The device ID is 0x8x for ATA658x. x equals the product code.

## 2.7 Lock Control Register

Sections of the register address area can be write-protected to protect against unintended modifications. Note that this feature only protects locked bits from being modified via the SPI and will not prevent the device from updating status registers.

### 2.7.1 Register Write Protection Register (Address 0x0A)

**Name:** RWPR  
**Offset:** 0x0A  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved	WP6	WP5	WP4	WP3	WP2	WP1	WP0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bit 7 - Reserved** Reserved for future use

#### Bit 6 - WP6

Address area 0x67 to 0x6F – partial networking data mask registers, the host microcontroller should set the bit to '1' to enable register write protection, otherwise to '0'.

#### Bit 5 - WP5

Address area 0x50 to 0x5F – the host microcontroller should set the bit to '1' to enable register write protection, otherwise to '0'.

#### Bit 4 - WP4

Address area 0x40 to 0x4F – WAKE pin configuration, the host microcontroller should set the bit to '1' to enable register write protection, otherwise to '0'.

#### Bit 3 - WP3

Address area 0x30 to 0x3F – the host microcontroller should set the bit to '1' to enable register write protection, otherwise to '0'.

#### Bit 2 - WP2

Address area 0x20 to 0x2F – transceiver control and partial networking ID configuration, the host microcontroller should set the bit to '1' to enable register write protection, otherwise to '0'.

#### Bit 1 - WP1

Address area 0x10 to 0x1F – the host microcontroller should set the bit to '1' to enable register write protection, otherwise to '0'.

#### Bit 0 - WP0

Address area 0x06 to 0x09 – the host microcontroller should set the bit to '1' to enable register write protection, otherwise to '0'.

## 2.8 Window Watchdog

The watchdog is used to monitor the proper function of the microcontroller and to trigger a Reset if the microcontroller stops serving the watchdog due to a lock-up in the software or other malfunction. The NRES pin, which is a VCC level output pin, is pulled to low when a watchdog reset event is detected. The high-voltage open drain output pin LH (LimpHome) is asserted when a watchdog reset event is detected. The watchdog (WD) is enabled by default and starts after power-on of the device.

The watchdog supports two operating modes: Window mode (only available in device Normal mode) and Time-out mode. In Window mode, a watchdog trigger event within the closed watchdog window causes a Reset. In Time-out mode, the watchdog can be triggered any time within the trigger range by a watchdog trigger. In Time-out mode, the watchdog can also be used for cyclic wake up of the microcontroller.



Figure 2-11. Window Watchdog in Window Mode

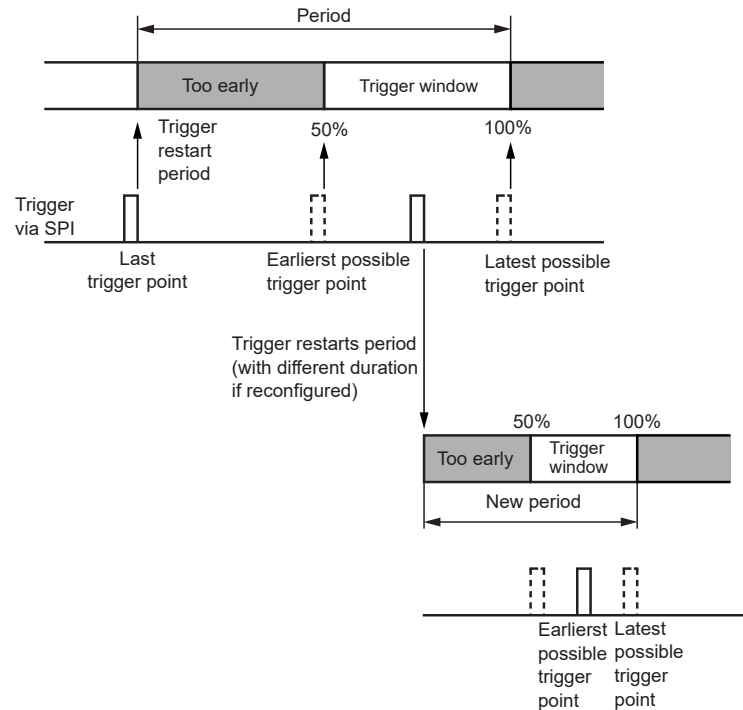
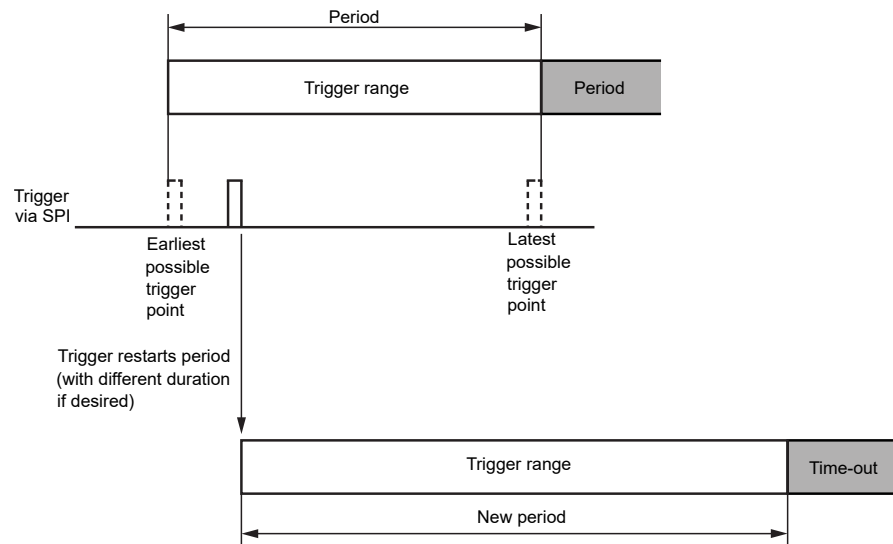


Figure 2-12. Window Watchdog in Time-out Mode



In order to avoid unwanted configuration of the watchdog, the ATA658x only allows configuration of the watchdog (write access to WDCR1 register and WDCR2) when the device is in Standby mode. If the watchdog is deactivated, the microcontroller shall configure the watchdog correctly before the watchdog is enabled ( $WDC = 010/100$ ). As soon as the watchdog is activated, the watchdog runs with the latest configuration. If the watchdog is active (default), the microcontroller is allowed to configure the watchdog any time when the device is in Standby mode. Every write access to the WDCR1 and WDCR2 registers via SPI will reset the Watchdog Timer and immediately apply

the changes. If Window mode is selected (WDC = 100), the watchdog will remain in (or switch to) Time-out mode until the device enters Normal mode (Window mode is only supported when the device is in Normal mode).

Any attempt to configure the watchdog (write access to WDCR1 register and WDCR2 register) while the device is not in Standby mode will trigger a Reset of the microcontroller, and the device will set the ILLCONF bit in the Watchdog Status register, WDSR (Illegal watchdog configuration).

**Table 2-5.** WDCR1 - Watchdog Configuration Register 1 (Address 0x36)

Bits	Symbol	Access	Value	Description
7:5	WDC	R/W		Watchdog mode control
			001	Off mode
			010	Time-out mode (default)
			100	Window mode
4:3	WDPRE	R/W		Watchdog period control (extend watchdog period by the factor defined below)
			00	Watchdog prescale factor 1 (default)
			01	Watchdog prescale factor 1.5
			10	Watchdog prescale factor 2.5
	11	Watchdog prescale factor 3.5		
2	WDSLPL	R/W		Set to '1' to let the window watchdog run in Sleep mode; otherwise, set to '0'; '0' by default.
1	WDLW	R/W		Set to '1' if a Reset to Window Watchdog Timer and a long start-up window exist after LH switch to high. Otherwise, set to '0'; '1' by default.
0				Reserved for future use.

Eight watchdog periods (8 ms to 4096 ms) are supported in the ATA658x. The watchdog period is programmable via the Watchdog Period bits (WWDP) in the Watchdog Control Register 2 (WDCR2). The selected period is valid for both Window and Time-out modes. The default watchdog period is 128 ms. A watchdog trigger event (an SPI write access to WDTRIG register with the pattern '01010101') resets the Watchdog Timer. The watchdog period and the reset pulse width can also be configured via the WRPL bits in the Watchdog Control Register 2.

To activate the watchdog when the device is in Sleep mode, the WDSLPL bit of the watchdog Control register must be set to '1'. When the device goes to Sleep mode with WDSLPL = 1, the Watchdog Timer gets reset and restarts immediately.

Figure 2-13. Watchdog in Sleep mode and Cyclic Wake-Up (RSTLVL==1)

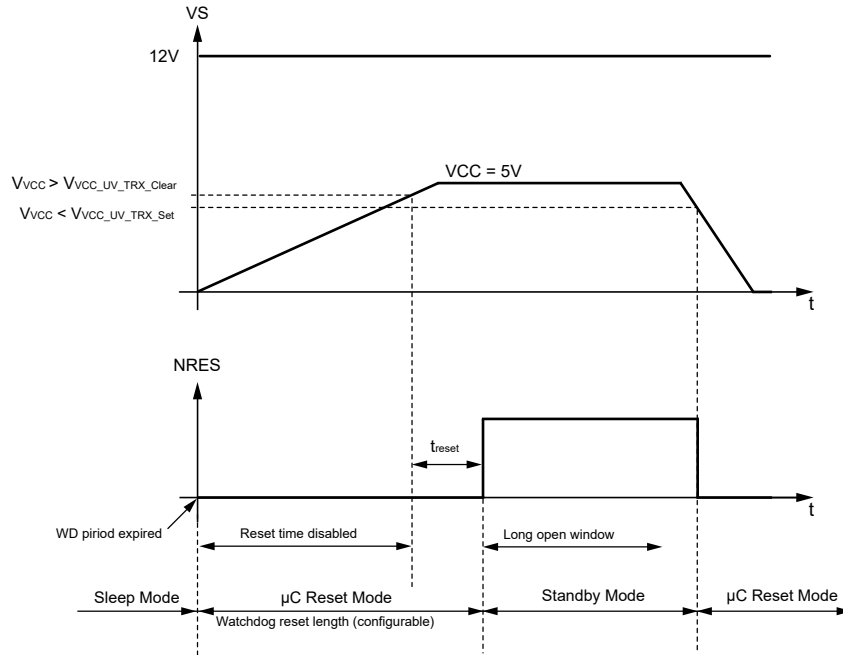
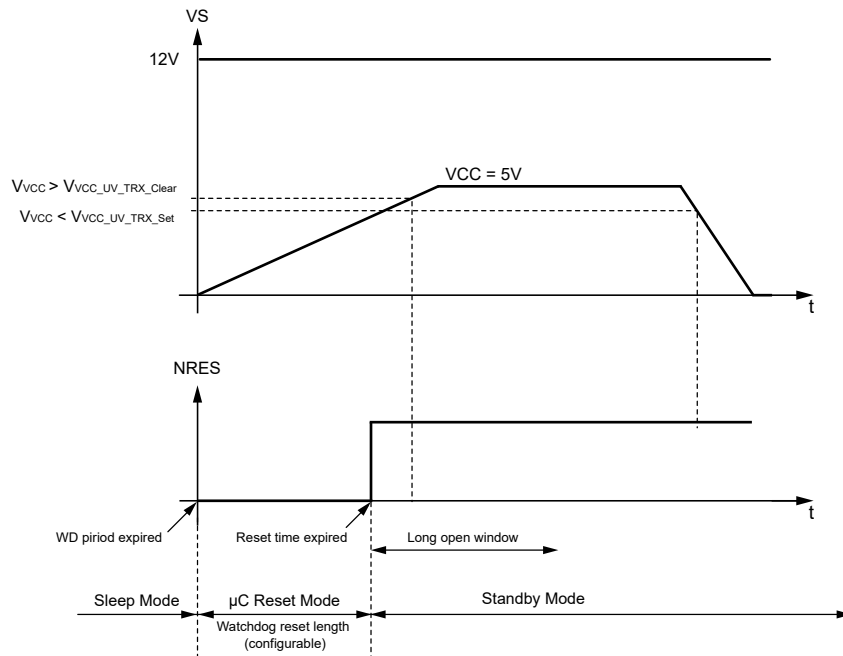


Figure 2-14. Watchdog in Sleep mode and Cyclic Wake Up (RSTLVL==0)



**Table 2-6. WDCR2 - Watchdog Control Register 2 (Address 0x37)**

Bits	Symbol	Access	Value	Description
7:4	WWDP	R/W		Window watchdog period configuration (ms, prescale factor = 1, ±10%)
			1000	8
			0001	16
			0010	32
			1011	64
			0100	128 (default)
			1101	256
			1110	1024
			0111	4096
0:3	WRPL	R/W		Window Watchdog Reset pulse length (ms)
			1000	1 to 1.5
			0001	3.6 to 5 (default)
			0010	10 to 12.5
			1011	20 to 25
			0100	40 to 50
			1101	60 to 75
			1110	100 to 125
0111	150 to 190			

The watchdog is an important safety mechanism, that must be configured correctly. Two mechanisms are provided to prevent watchdog parameters from being changed by mistake:

- All configuration bitfields in the registers WDC, WWDP and WRPL have a hamming distance of at least two for valid states.
- Reconfiguration protection: Only configurable in Standby mode.

Having a hamming distance of at least two for all valid states for the control bitfields, WDC, WWDP and WRPL, ensures that a single bit error cannot cause the watchdog to be configured incorrectly (at least two bits must be flipped to reconfigure WDC, WWDP or WRPL). If an attempt is made to write an invalid code to the WDCR1 register or WDCR2 register, the SPI write to the WDCRx register is ignored and the CACC bit in the Watchdog Status register is set.

**After the device transitions from  $\mu$ C Reset mode to Standby mode, the microcontroller should trigger the watchdog prior to writing to a watchdog configuration register!**

**Table 2-7. WDSR - Watchdog Status Register (Address 0x38)**

Bits	Symbol	Access	Description
			Watchdog Status register
7	OFF	R	Window watchdog is off.
6	CACC	R/W	Corrupted write access to the Window Watchdog Configuration registers
5	ILLCONF	R/W	An attempt is made to reconfigure the Watchdog Control register while the device is not in Standby mode.
4	TRIGS	R	The device sets the bit to '1' if window watchdog is in the first half of window and sets the bit to '0' if window watchdog is in second half of window. If the watchdog is not in Window mode, the bit will always be set to '0'.
3	OF	R/W	Watchdog overflow (Time-out mode or Window mode in Standby or Normal mode)
2	OFSLP	R/W	Watchdog overflow in Sleep mode (Time-out mode)

.....continued			
Bits	Symbol	Access	Description
1	ETRIG	R/W	Watchdog triggered too early (Window mode)
0	-	R	

Writing '1' to the corresponding bit of the Watchdog Status register will reset the bit.

A microcontroller Reset is triggered immediately in response to an illegal watchdog configuration (configuration of the watchdog in Normal or Sleep mode), an incorrect watchdog trigger event in Window mode (watchdog overflow or triggered too early) or when the watchdog overflows in Time-out mode. If a Reset is triggered by the window watchdog, the Window Watchdog Reset Event register will be set. The device will enter the  $\mu$ C Reset mode and enter Standby mode after the Reset is finished.

If there is a corrupted write access to the Window Watchdog Configuration registers and/or an illegal configuration of the Watchdog Control register when the watchdog is in Off mode, the corresponding status register bit will be set. If the register bits are not reset to zero before enabling the window watchdog, a Reset will be triggered to the microcontroller immediately after enabling the window watchdog.

### 2.8.1 Watchdog Trigger Register (Address 0x39)

**Name:** WDTRIG  
**Offset:** 0x39  
**Reset:** 0x00  
**Property:** Write-only

Bit	7	6	5	4	3	2	1	0
	WDTRIG[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

#### Bits 7:0 - WDTRIG[7:0]

A watchdog trigger event (an SPI write access to WDTRIG register with the pattern 01010101) resets the Watchdog Timer.

### 2.8.2 Watchdog Behavior in Window Mode

The watchdog runs continuously in Window mode. The watchdog will be in Window mode if WDC = 100 and the device enters Normal mode. In Window mode, the watchdog can only be triggered during the second half of the watchdog period. If the watchdog overflows or is triggered in the first half of the watchdog period (defined by WWDP in WDCR2 in Table 2-6), the device enters  $\mu$ C Reset mode (NRES and LH pin asserted for a defined length). The reset source (either 'watchdog triggered too early' or 'watchdog overflow') is captured in the watchdog status bits in the Watchdog Status register (WDSR). If the watchdog is triggered in the second half of the watchdog period, the Watchdog Timer is restarted.

### 2.8.3 Watchdog Behavior in Time-out Mode

The watchdog runs continuously in Time-out mode. The watchdog will be in Time-out mode if WDC = 010. In Time-out mode, the Watchdog Timer can be reset at any time by a watchdog trigger. If the watchdog overflows, a watchdog failure event is captured in the Watchdog Status register (WDSR). In Time-out mode, the watchdog can be used as a cyclic wake-up source for the microcontroller when the ATA658x is in Sleep mode. When the device is in Sleep mode with Watchdog Time-out mode selected, a wake-up event is generated after the nominal Watchdog Period (WWDP). The device switches to  $\mu$ C Reset mode.

## 2.8.4 Watchdog Behavior During Power On and After $\mu$ C Reset

For a safe start-up after  $\mu$ C Reset, it is recommended to send a SPI command that triggers the watchdog and then a second SPI command that configures it. After power-on, the device enters first  $\mu$ C Reset mode and then Standby mode. As soon as the device enters Standby mode, the watchdog starts a long open window  $t_{LW}$ . Within this long open window, the watchdog must be triggered by the microcontroller. Otherwise, the watchdog will trigger a Reset of the microcontroller via the NRES pin. After the first trigger within the long open window, the WD starts its normal operating modes.

The watchdog cannot be disabled and configured in the following cases:

1. After power-on of the device and before it receives the first trigger in Long Open Window mode.
2. In all other cases when the device moves from  $\mu$ C Reset mode to Standby mode and before the watchdog receives the first trigger (in case the watchdog is enabled).

If the WDLW bit from the Watchdog Control register is set to 1 (default value), the Watchdog Timer will always be reset when it starts the long open window. Otherwise, the WD will continue its normal operation.

## 2.8.5 Watchdog During VCC Undervoltage and Overtemperature

In the ATA6580/1/5/6, the watchdog is stopped and reset if the device detects a  $V_{VCC} < V_{VCC\_UV\_TRX\_Set}$  event, when RSTLVL is set to '1'. The device will enter  $\mu$ C Reset mode and stay in  $\mu$ C Reset mode until VCC recovers. When RSTLVL is set to '0', the device will enter  $\mu$ C Reset mode when the device detects  $V_{VCC} < V_{VCC\_UV\_IO\_Set}$  and the watchdog is stopped and reset. After VCC recovers, the NRES pin will be pulled to Low for the reset pulse length time and afterward, the device enters Standby mode. If Long Open Window mode is enabled, the watchdog will start the long open window after the device enters Standby mode.

In the ATA6582/7, VCC\_ $\mu$ C will be monitored for triggering a  $\mu$ C Reset. The watchdog is stopped and reset if the device detects  $V_{VCC\_μC} < V_{VCC\_UV\_RST\_Set}$ , when RSTLVL is set to '1'. The device will enter  $\mu$ C Reset mode and stay in  $\mu$ C Reset mode until VCC recovers. When RSTLVL is set to '0', the device will enter  $\mu$ C Reset mode when the device detects  $V_{VCC\_μC} < V_{VCC\_UV\_IO\_Set}$  and the watchdog is stopped and reset.

In the ATA6583/8, the RSTLVL is not used. The  $\mu$ C Reset will always be triggered when the device detects  $V_{VCC\_μC} < V_{VCC\_UV\_IO\_Set}$ .

Figure 2-15. Watchdog during VCC undervoltage  $V_{VCC} < V_{VCC\_UV\_TRX\_Set}$  (RSTLVL==1)

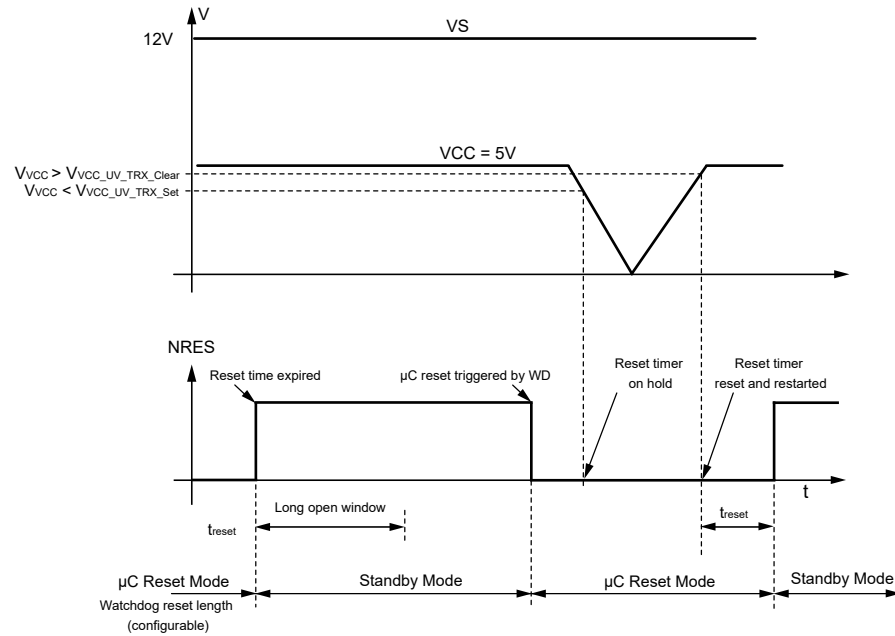
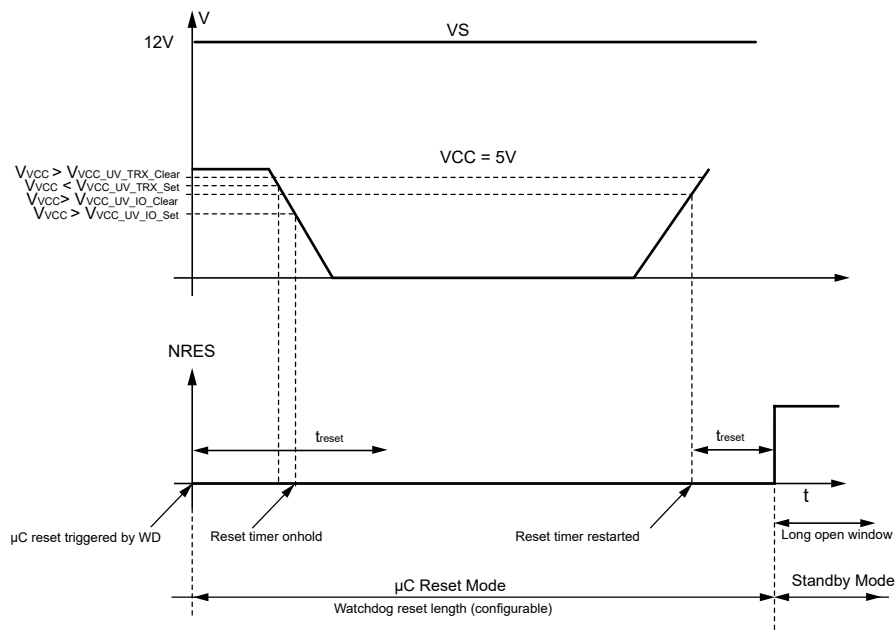


Figure 2-16. Watchdog during VCC undervoltage  $V_{VCC} < V_{VCC\_UV\_IO\_Set}$  (RSTLVL==0)



## 2.9 General Purpose Memory (GPMn)

The device allocates 4 bytes of RAM as general purpose registers for storing user information. The general purpose registers can be accessed via the SPI at addresses 0x06 to 0x09.

### 2.9.1 General purpose memory 0 (Address 0x06)

**Name:** GPM0  
**Offset:** 0x06  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	GPM0[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 7:0 – GPM0[7:0]** General Purpose Memory Bits

### 2.9.2 General purpose memory 1 (Address 0x07)

**Name:** GPM1  
**Offset:** 0x07  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	GPM1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 7:0 – GPM1[7:0]** General Purpose Memory Bits

### 2.9.3 General purpose memory 2 (Address 0x08)

**Name:** GPM2  
**Offset:** 0x08  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	GPM2[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 7:0 – GPM2[7:0]** General Purpose Memory Bits

### 2.9.4 General purpose memory 3 (Address 0x09)

**Name:** GPM3  
**Offset:** 0x09  
**Reset:** 0x00  
**Property:** Read/Write

Bit	7	6	5	4	3	2	1	0
	GPM3[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 7:0 – GPM3[7:0]** General Purpose Memory Bits



## 2.10 VCC LDO

The VCC pin has a nominal voltage output level of 5V.

The voltage regulator requires an external capacitor for compensation and for filtering disturbances from the microcontroller. It is recommended to use a MLC capacitor with a capacitance of 1.87 $\mu$ F (minimum, tolerance included) in parallel to a 100nF ceramic capacitor. The values of these capacitors depend on the application. During a short circuit at VCC, the output limits the output current to  $I_{VCClim}$ . In the ATA6580/1/5/6, if the LDO temperature exceeds the threshold  $T_{Vj\text{sd}}$ , the VCC output will be switched off. Then, the chip cools down, and after the LDO temperature drops by  $T_{Vj\text{sd\_hys}}$ , the regulator will be switched on again. In the ATA6582/3/7/8, the VCC regulator behaves exactly the same as in the ATA6580/1/5/6.

When the ATA658x is soldered onto the PCB, it is mandatory to connect the heat slug with a wide GND plate on the printed board to get a good heat sink. The main power dissipation of the IC is created from the VCC output current  $I_{VCC}$  and the VCC\_μC output current  $I_{VCC\_μC}$  (ATA6582/3/7/8), which is needed for the application.

$V_{VCC}$  supply voltage remains active until  $V_{VS}$  falls below approximately 2V.

The internal CAN transceiver consumes 50 mA (typ) while driving a dominant bus state, leaving 100 mA available for the external load on pin VCC. The average current consumption of the CAN transceiver is lower ( $\approx$  25 mA), depending on the application, leaving more current available for the load.

## 2.11 External sensor supply

The VCC\_SENSOR pin is intended to supply power to external components, delivering up to 30mA at 3.3/5V. The REGEN bits in the VCC\_SENSOR control register REGCR are used to configure in which modes VCC\_SENSOR is enabled. The default value of the REGCR register at power-on is 2'b00, i.e. the VCC\_SENSOR supply is switched off. The VCC\_SENSOR pin is overvoltage and undervoltage monitored if event capture is enabled.

**Table 2-8.** REGCR - VCC\_SENSOR Configuration Register (Address 0x25)

Bits	Symbol	Access	Value	Description
7:2	Reserved	R		
1:0	REGEN	R/W		VCC_SENSOR configuration
			00	VCC_SENSOR off in all modes
			01	VCC_SENSOR on in Normal mode
			10	VCC_SENSOR on in Normal, Standby and μC Reset mode
			11	VCC_SENSOR on in Normal, Standby, Sleep and μC Reset mode

The output voltage level at the VCC\_SENSOR pin is selected via the LDOCR register (LDO configuration register).

**Table 2-9.** LDOCR - VCC\_SENSOR Output Configuration Register (Address 0x02)

Bits	Symbol	Access	Value	Description
7:3	Reserved	R		
2:0	VCCSENSOUT	R/W		VCC_SENSOR output voltage level configuration bits
			010	VCC_SENSOR 3.3V output voltage level
			101	VCC_SENSOR 5V output voltage level

VCC\_SENSOR pin has a default output voltage level of 3.3V. The configuration register is only write accessible in device Standby mode. Any incorrect configuration or a configuration attempt while not in Standby mode will reset the REGCR and LDOCR registers and set the output level to 3.3V.

## 2.12 LIN2 Device (ATA6582/3/7/8 only)

The ATA6582/3/7/8 is a dual die CAN-LIN-LIN SBC, which contains the die of the ATA6586 and the die of the ATA663232/55. The ATA6582/3/7/8 devices provide one CAN transceiver (with or without partial networking), two LIN transceivers, one 5V / 150mA low dropout voltage regulator (VCC), one 5V/3.3V / 85mA low dropout voltage regulator (VCC\_μC) and one 5V/3.3V / 30mA low dropout voltage regulator for supplying external loads (VCC\_Sensor).

The two dies work as a single system and communicate with each other to ensure that a wake-up/interrupt event wakes up both dies without requiring any external components, like a microcontroller.

### 2.12.1 LIN2 Operating Modes

Figure 2-17. LIN2 Operating Modes

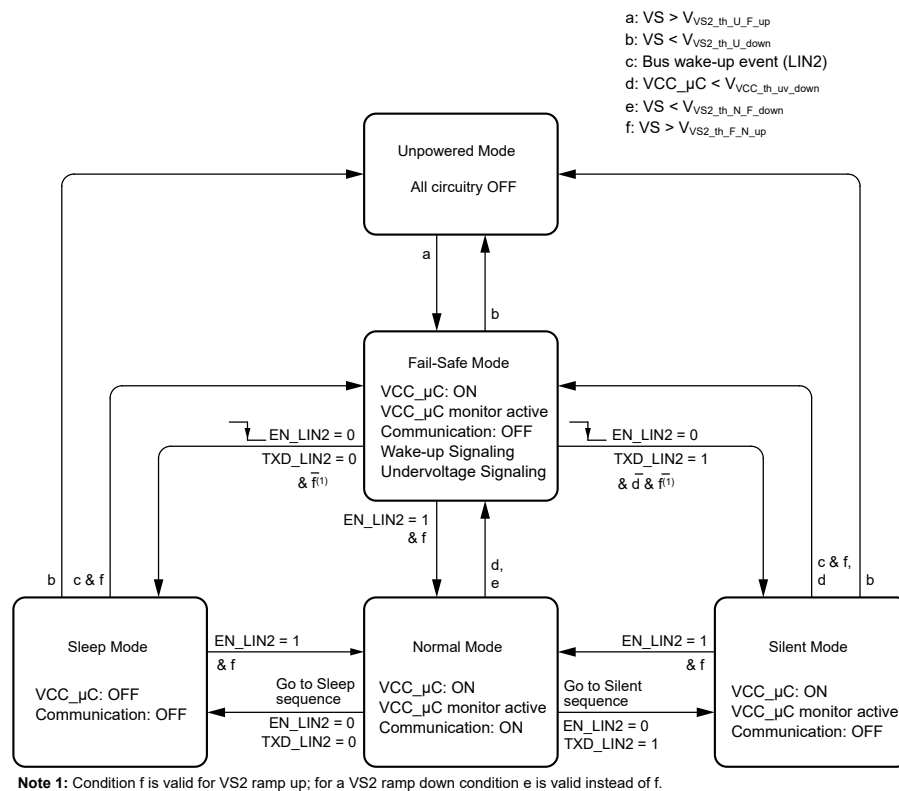


Table 2-10. LIN2 Operating Modes

Operating Mode	Transceiver	$V_{VCC\_μC}$	LIN2	TXD_LIN2	RXD_LIN2
LIN2 Fail-Safe	OFF	3.3V/5V	Recessive	Signaling Fail-Safe sources (see Table <a href="#">Signaling in Fail-Safe mode</a> )	
LIN2 Normal	ON	3.3V/5V	TXD_LIN2-dependent	Follows data transmission	
LIN2 Silent	OFF	3.3V/5V	Recessive	High	High
LIN2 Sleep/Unpowered	OFF	0V	Recessive	Low	Low

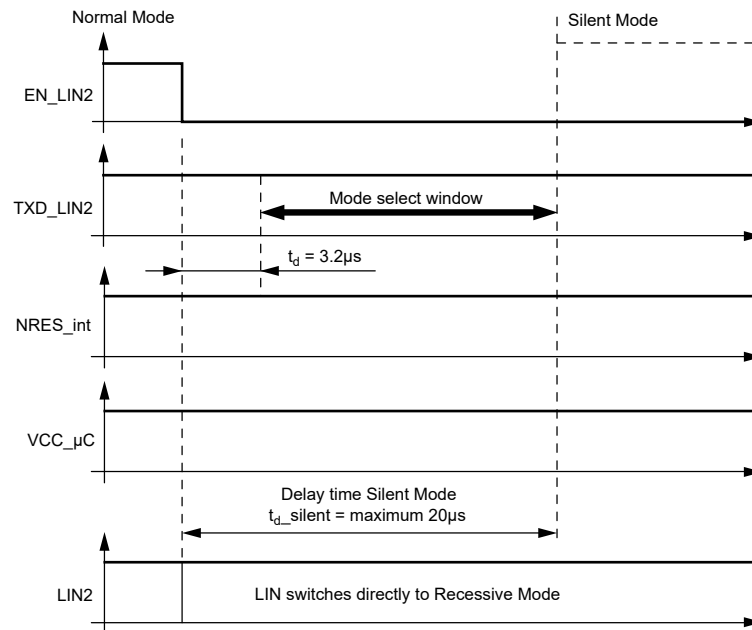
#### 2.12.1.1 LIN2 Normal Mode

This is the normal transmitting and receiving mode of the LIN2 interface. The VCC\_μC voltage regulator operates at 3.3V/5V output voltage, with a maximum tolerance of  $\pm 2\%$  and a maximum output current of 85mA. If a VCC\_μC undervoltage condition occurs, the internal reset NRES\_int signal switches to low and the LIN2 device changes its state to Fail-Safe mode.

### 2.12.1.2 LIN2 Silent Mode

A falling edge at EN\_LIN2 while TXD\_LIN2 is high switches the LIN2 device into LIN2 Silent mode. The TXD\_LIN2 signal has to be logic high during the mode select window. The transmission and reception are disabled in LIN2 Silent mode. The VCC\_μC voltage regulator is active.

**Figure 2-18.** Switching to LIN2 Silent Mode



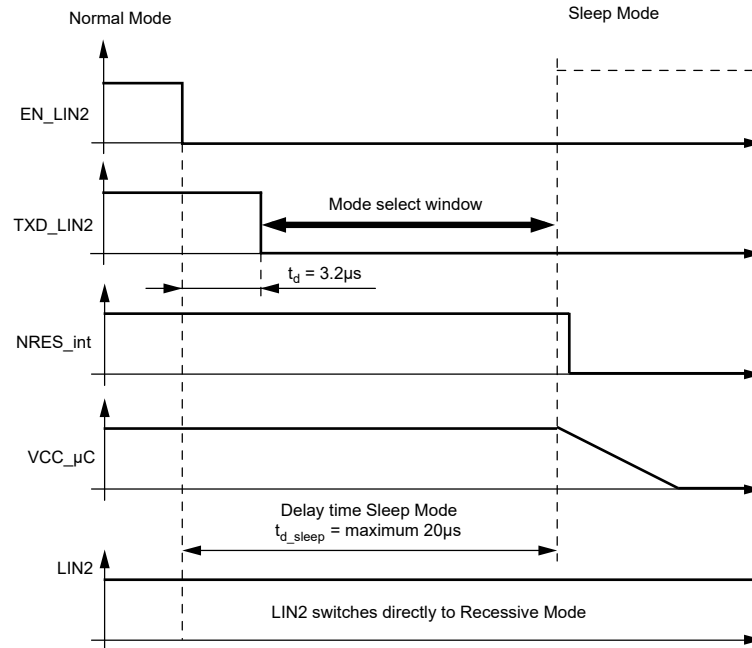
In LIN2 Silent mode, the internal termination resistor between the LIN2 pin and VS2 pin is disabled to minimize the current consumption in case the LIN2 pin is short-circuited to GND. Only a weak pull-up current (typically 10  $\mu\text{A}$ ) between the LIN2 pin and VS2 pin is present. LIN2 Silent mode can be activated independently from the current level on pin LIN2.

If an undervoltage condition occurs, NRES\_int switches to low and the LIN2 device changes its state to LIN2 Fail-Safe mode.

### 2.12.1.3 LIN2 Sleep Mode

A falling edge at EN\_LIN2 while TXD\_LIN2 is low switches the LIN2 device into Sleep mode. The TXD\_LIN2 signal has to be logic low during the mode select window (see the following figure).

**Figure 2-19. Switching to LIN2 Sleep Mode**



In order to avoid any influence to the LIN2 pin when switching into Sleep mode, it is possible to switch the EN\_LIN2 up to 3.2  $\mu\text{s}$  earlier to low than the TXD\_LIN2. It is recommended to switch TXD\_LIN2 and EN\_LIN2 at the same time.

In the ATA6582/3/7/8, the CAN-LIN SBC must always be put into Sleep mode first and then the LIN2 device. Otherwise the VCC\_μC would be deactivated and with it the SPI without the possibility to reconfigure the device.

In Sleep mode, communication is disabled. The VCC\_μC regulator is switched off; NRES\_int and RXD\_LIN2 are low. The internal termination resistor between the LIN2 pin and VS2 pin is disabled to minimize the current consumption in case the LIN2 pin is shorted to GND. Only a weak pull-up current (typically 10  $\mu\text{A}$ ) between the LIN2 pin and the VS2 pin is present. The Sleep mode can be activated independently of the current level on the LIN2 pin. Voltage below the LIN2 pre-wake detection,  $V_{\text{LIN2L}}$ , at the LIN2 pin activates the internal LIN2 receiver and starts the wake-up detection timer.

If the TXD pin is short-circuited to GND, it is possible to switch to LIN2 Sleep mode using EN\_LIN2 after  $t > t_{\text{to(dom)}\_LIN2}$ .

#### 2.12.1.4 LIN2 Fail-Safe Mode

The LIN2 device automatically switches to LIN2 Fail-Safe mode at system power-up. The VCC\_μC voltage regulator is switched on. The internal NRES\_int signal remains low for  $t_{\text{res}} = 4 \text{ ms}$ . LIN2 communication is switched off. The LIN2 device stays in this mode until EN\_LIN2 is switched to high, which causes a transition to LIN2 Normal mode. A low at the internal NRES\_int signal switches the LIN2 device into LIN2 Fail-Safe mode directly. During LIN2 Fail-Safe mode, the TXD\_LIN2 pin is an output, and together with the RXD\_LIN2 output pin, signals the LIN2 Fail-Safe source.

If the LIN2 device enters LIN2 Fail-Safe mode coming from the LIN2 Normal mode (EN\_LIN2 = 1) due to an VS2 undervoltage condition ( $V_{\text{VS2}} < V_{\text{VS2\_th\_N\_F\_down}}$ ), it is possible to switch into LIN2 Sleep or LIN2 Silent mode by a falling edge at the EN\_LIN2 input pin, which further reduces the current consumption.

A wake-up event from either LIN2 Silent or LIN2 Sleep mode is signaled to the microcontroller using the RXD\_LIN2 pin and the TXD\_LIN2 pin. A VS2 undervoltage condition is also signaled at these two pins. The encoding is shown in the table below.

A wake-up event switches the LIN2 device to LIN2 Fail-Safe mode.

**Table 2-11.** Signaling in LIN2 Fail-Safe Mode

LIN2 Fail-Safe Sources/Signals	TXD_LIN2	RXD_LIN2
LIN bus wake up (LIN2 pin)	Low	Low
Local wake up (WAKE2 pin)	Low	High
VS2 undervoltage detection ( $V_{VS2} < 3.9V$ )	High	Low

### 2.12.2 Local wake up in the ATA6582/3/7/8

ATA6582/3/7/8 supports local wake up from both WAKE and WAKE2 pins. Local wake up via the WAKE pin in the ATA6582/3/7/8 behaves exactly the same as the WAKE pin in the ATA6580/1/5/6 (see section 2.4.1. [Local Wake Up via Pin WAKE](#)).

A falling edge at the WAKE2 pin followed by a low level maintained for a minimum time period of  $t_{local\_wu2}$  results in a local wake-up request. The LIN2 device switches to LIN2 Fail-Safe mode. The internal LIN termination resistor is switched on. The local wake-up request is indicated by a low level at the TXD\_LIN2 pin to generate an interrupt to the microcontroller. When the WAKE2 pin is low, it is possible to switch the LIN2 device to LIN2 Silent mode or LIN2 Sleep mode via the EN\_LIN2 pin. In this case, the WAKE2 pin must be switched to high  $> 10\mu s$  before the negative edge at WAKE2 starts a new local wake-up request.

**Figure 2-20.** Local Wake up via WAKE2 pin from LIN2 Sleep Mode

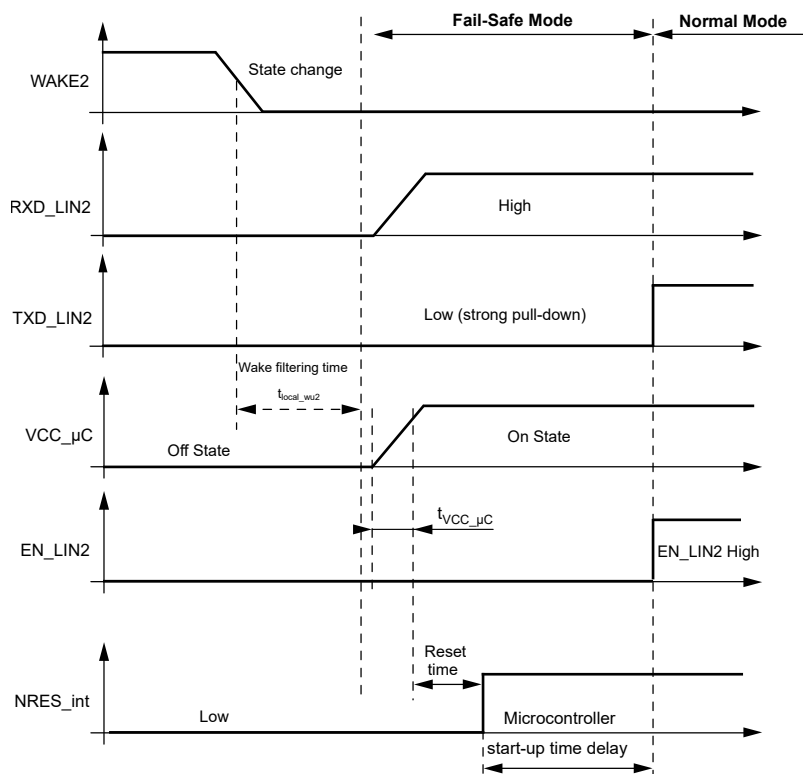
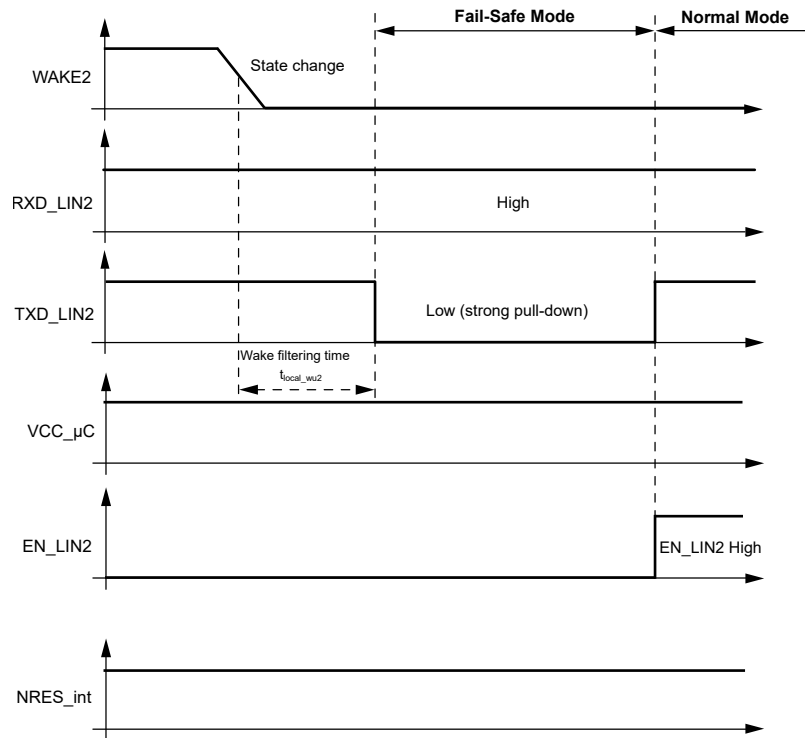


Figure 2-21. Local Wake up via WAKE2 pin from LIN2 Silent Mode

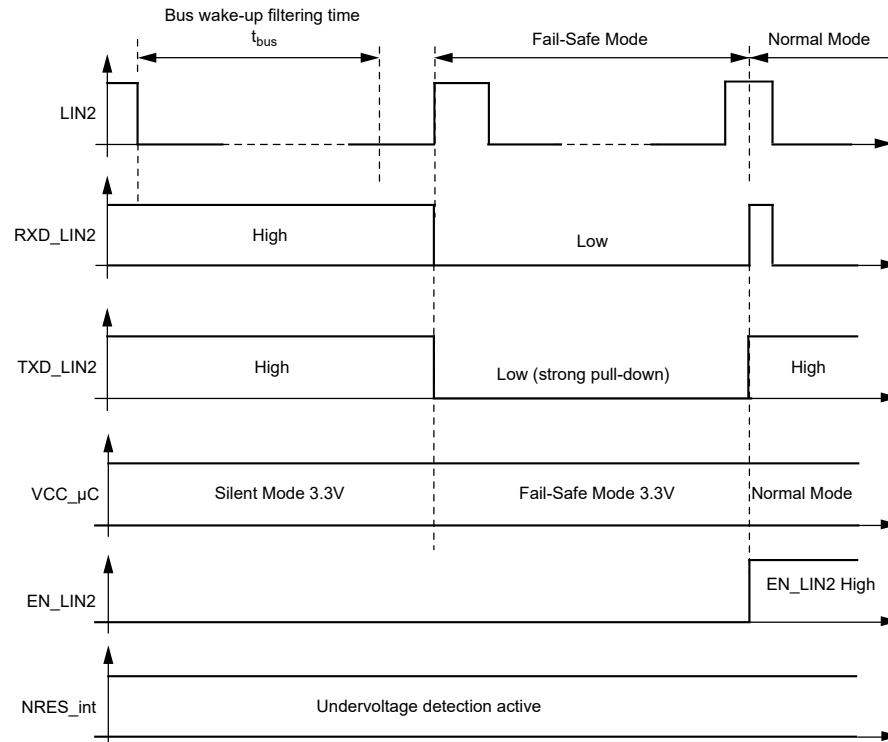


### 2.12.3 LIN bus wake up via LIN2 pin in the ATA6582/3/7/8

#### 2.12.3.1 LIN2 Remote Wake up from LIN Silent Mode (ATA6582/3/7/8)

A remote wake up from LIN2 Silent mode is only possible if TXD\_LIN2 is high. A voltage less than the LIN2 pre-wake detection  $V_{LIN2L}$  at the LIN2 pin activates the internal LIN2 receiver and starts the wake-up detection timer. A falling edge at the LIN2 pin followed by a dominant bus level maintained for a minimum period of time ( $> t_{bus}$ ) and the following rising edge at pin LIN2 result in a remote wake-up request. The LIN2 device switches from LIN2 Silent mode to LIN2 Fail-Safe mode, the VCC\_μC voltage regulator remains activated and the internal LIN2 responder termination resistor is switched on. The remote wake-up request is indicated by a low level at the RXD\_LIN2 pin and TXD\_LIN2 pin (strong pull-down at TXD\_LIN2). If pin EN\_LIN2 is high, the device transitions directly to LIN2 Normal mode.

Figure 2-22. LIN2 Wake up from Silent Mode

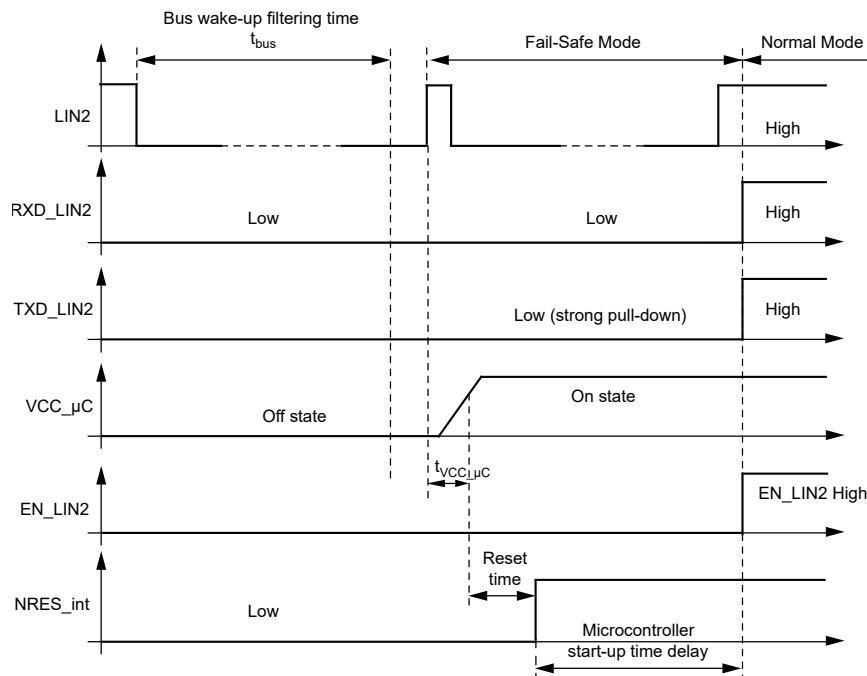


### 2.12.3.2 LIN2 Remote Wake up from LIN2 Sleep Mode (ATA6582/3/7/8)

A falling edge at the LIN2 pin, followed by a dominant bus level maintained for a minimum period of time ( $t_{bus}$ ) and a rising edge at the LIN2 pin, results in a remote wake-up request, causing the LIN2 device to switch from LIN2 Sleep mode to LIN2 Fail-Safe mode. The VCC\_μC regulator is activated, and the internal LIN2 termination resistor is switched on. The remote wake-up request is indicated by a low level at RXD\_LIN2 and TXD\_LIN2 (strong pull-down at TXD\_LIN2).

EN\_LIN2 high can be used to switch directly from LIN2 Sleep/LIN2 Silent mode to LIN2 Normal mode. If EN\_LIN2 is still high after V<sub>VCC\_μC</sub> ramp-ups and after the undervoltage reset time, the LIN2 transceiver switches to LIN2 Normal mode.

Figure 2-23. LIN2 Wake up from Sleep Mode



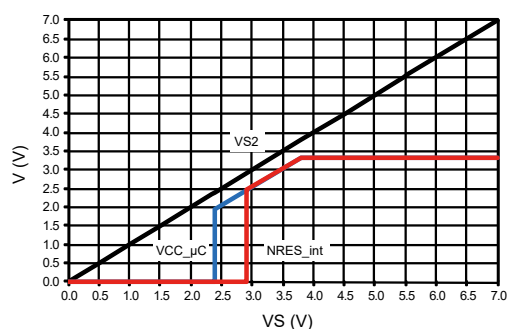
### 2.12.3.3 Behavior of the LIN2 Device under Low Supply Voltage Condition

After the battery voltage has been connected to the application circuit, the voltage at the VS2 pin increases according to the bypass capacitor used in the application. If  $V_{VS2}$  is higher than the minimum VS2 operating threshold  $V_{VS2\_th\_U\_F\_up}$ , the LIN2 device changes from Unpowered mode to LIN2 Fail-Safe mode. As soon as  $V_{VS2}$  exceeds the undervoltage threshold  $V_{VS2\_th\_F\_N\_up}$ , the LIN2 transceiver can be activated.

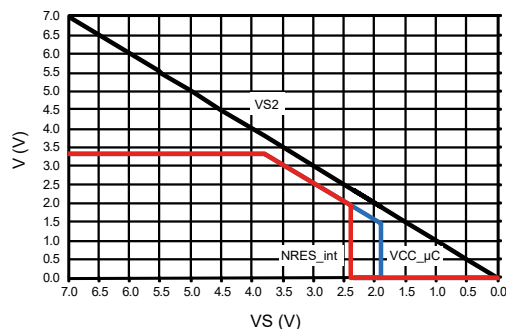
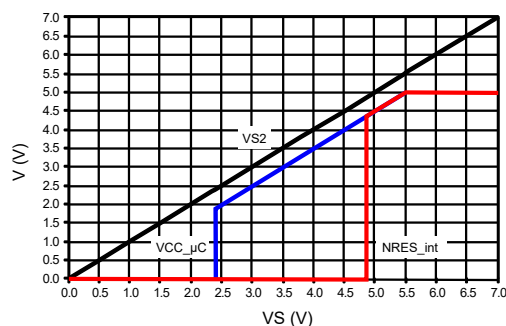
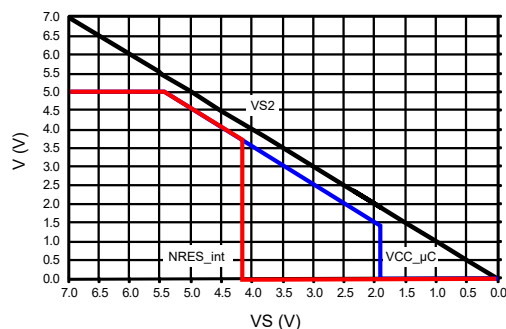
The VCC\_μC output voltage reaches its nominal value after  $t_{VCC\_μC}$ . This time depends on the externally applied VCC\_μC capacitor and the load. The internal reset NRES\_int signal is low for the reset time delay  $t_{reset}$ . No mode change is possible during  $t_{reset}$ .

The behavior of VCC\_μC, the internal reset NRES\_int and VS2 is shown in the following diagrams (ramp-up and ramp-down):

Figure 2-24. VCC\_μC and the internal NRES\_int signal versus VS2 (Ramp-up) for 3.3V





**Figure 2-25.** VCC<sub>μC</sub> and the internal NRES\_int signal versus VS2 (Ramp-Down) for 3.3V**Figure 2-26.** VCC<sub>μC</sub> and the internal NRES\_int signal versus VS2 (Ramp-up) for 5V**Figure 2-27.** VCC<sub>μC</sub> and the internal NRES\_int signal versus VS2 (Ramp-Down) for 5V

Note that the graphs above are only valid if the VS2 ramp-up and ramp-down times are much slower than the VCC<sub>μC</sub> ramp-up time,  $t_{VCC_{\mu C}}$ , and the NRES\_int delay time,  $t_{reset}$ .

If during Sleep mode, the voltage level of  $V_{VS2}$  drops below the undervoltage detection threshold,  $V_{VS2\_th\_N\_F\_down}$  (typ. 4.3V), the operating mode is not changed and no wake up is possible. If the supply voltage on pin VS2 drops below the VS2 operating threshold,  $V_{VS2\_th\_U\_down}$  (typ. 2.05V), the LIN2 device switches to LIN2 Unpowered mode.

If during LIN2 Silent mode, the  $V_{VCC_{\mu C}}$  voltage drops below the VCC<sub>μC</sub> undervoltage threshold,  $V_{VCC_{\mu C\_th\_uv\_down}}$ , the LIN2 device switches into LIN2 Fail-Safe mode. If the supply voltage on pin VS2 drops below the VS2 operating threshold,  $V_{VS\_th\_U\_down}$  (typ. 2.05V), the LIN2 device switches to LIN2 Unpowered mode.

If during LIN2 Normal mode, the voltage level on the VS2 pin drops below the VS2 undervoltage detection threshold,  $V_{VS2\_th\_N\_F\_down}$  (typ. 4.3V), the LIN2 device switches to LIN2 Fail-Safe mode. In Fail-Safe mode, the LIN2 transceiver is disabled to avoid malfunction or corrupted bus messages. The VCC<sub>μC</sub> voltage regulator remains active.

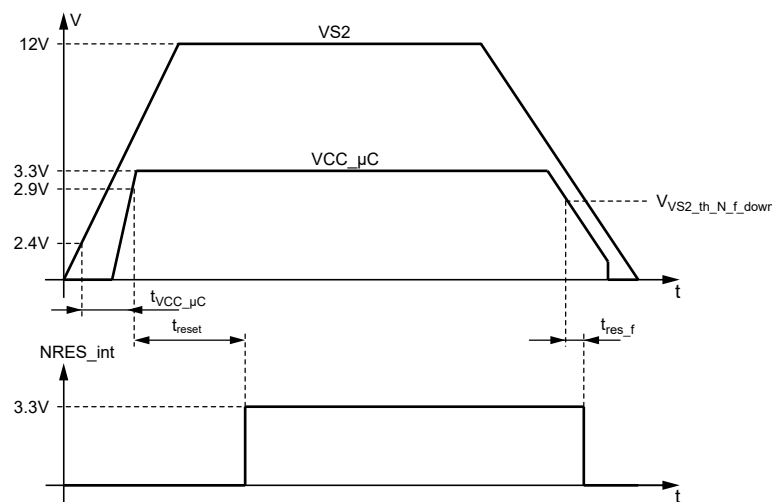
**For  $V_{VCC\_μC}=3.3V$ :** In a VS2 undervoltage situation, it is possible to switch the device into LIN2 Sleep mode or LIN2 Silent mode by a falling edge at the EN\_LIN2 input. Switching into these two current-saving modes is always possible, allowing current consumption to be reduced even further. When the VCC\_μC voltage drops below the VCC\_μC undervoltage threshold,  $V_{VCC\_μC\_th\_uv\_down}$  (typ. 2.6V), the LIN2 device switches into LIN2 Fail-Safe mode.

**For  $V_{VCC\_μC}=5V$ :** A VS2 undervoltage situation causes a VCC\_μC undervoltage, the LIN2 device transitions to LIN2 Fail-Safe mode and can be switched into LIN2 Sleep mode only.

**Note:** It is possible that a  $V_{VS}/V_{VS2}$  undervoltage, while the device is in Sleep mode, causes a partial wake up of the device of which it can not recover with the usual wake-up sources. If an undervoltage condition is possible during Sleep mode, the user must connect EN\_LIN2 and VCC with an external circuitry as shown in the typical application diagram to prevent that state.

#### 2.12.4 3.3V/5V VCC\_μC Low Drop Voltage Regulator (ATA6582/3/7/8 only)

Figure 2-28. 3.3V/5V VCC\_μC Low Drop Voltage Regulator: Supply Voltage Ramp-up and Ramp-Down



The VCC\_μC voltage regulator requires an external capacitor for compensation and to filter the disturbances from the microcontroller. It is recommended to use an MLC capacitor with a minimum capacitance of 1.8 μF, in parallel to a 100 nF ceramic capacitor. The values of these capacitors are dependent on the application.

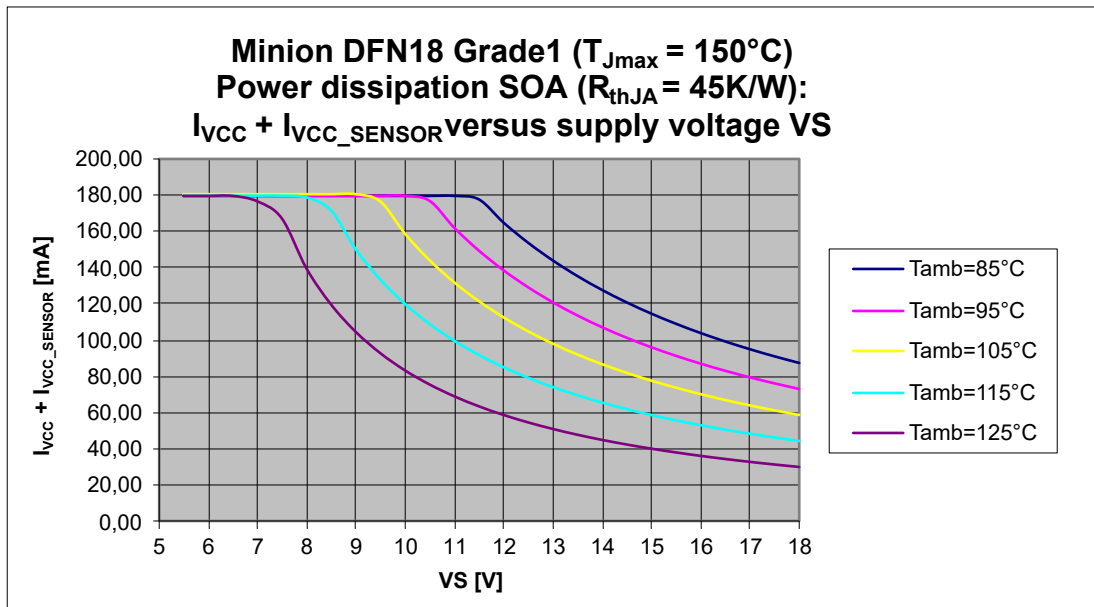
During a short circuit at VCC\_μC in the ATA6582/7/8, the output limits the output current to  $I_{VCC\_μC\_lim}$ . In case of an undervoltage, NRES\_int switches to low. If the die temperature exceeds  $T_{VCC\_μC\_off}$ , the VCC\_μC output switches off. The device cools down, and after a hysteresis of  $T_{hys}$ , switches the output on again.

When the ATA658x is soldered onto the PCB, it is mandatory to connect the heat slug with a wide GND plate on the printed board to get a good heat sink.

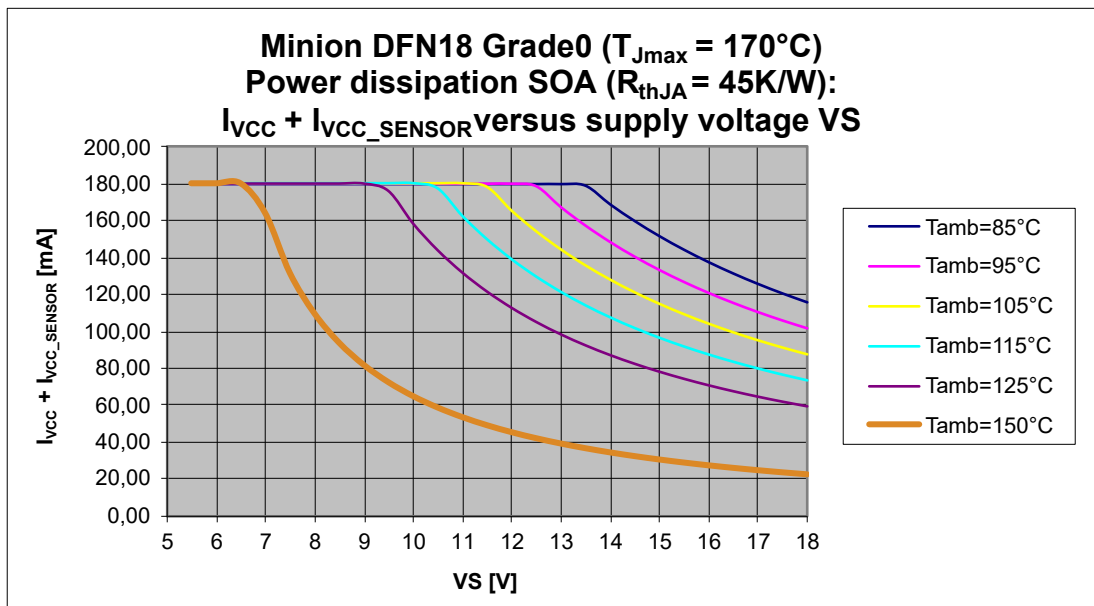
### 2.13 Power Dissipation and Safe Operating Area

When the ATA658x is being soldered onto the PCB, it is mandatory to connect the heat slug with a wide GND plate on the printed board to get a good heat sink. The power dissipation of the IC is mainly determined by the VCC, VCC\_μC and VCC\_Sensor output currents  $I_{VCC}$ ,  $I_{VCC\_μC}$  and  $I_{VCC\_SENSOR}$ , which are consumed by the application. The following figures show Power Dissipation and Safe Operating Area of the ATA658x as a function of the Regulator Output Currents versus Supply Voltage.

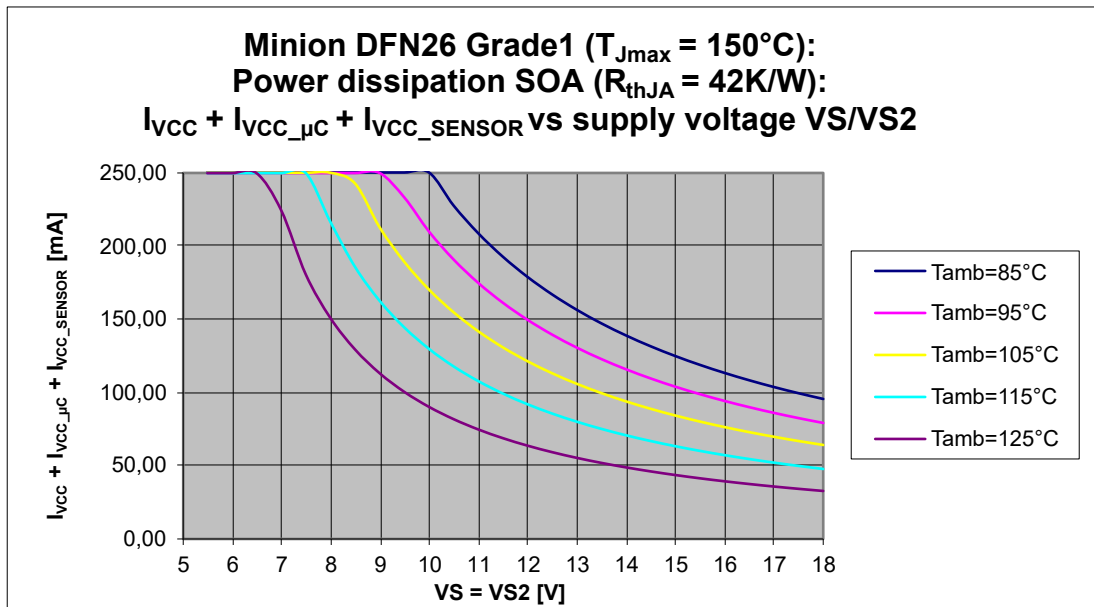
**Figure 2-29.** Power Dissipation and Safe Operating Area (18-pin package; Grade1): Regulator Output Currents  $I_{VCC} + I_{VCC\_SENSOR}$  versus Supply Voltage VS at different Ambient Temperatures ( $R_{thJA} = 45K/W$  assumed)



**Figure 2-30.** Power Dissipation and Safe Operating Area (18-pin package; Grade0): Regulator Output Currents  $I_{VCC} + I_{VCC\_SENSOR}$  versus Supply Voltage VS at different Ambient Temperatures ( $R_{thJA} = 45K/W$  assumed)



**Figure 2-31.** Power Dissipation and Safe Operating Area (26-pin package; Grade1): Regulator Output Currents  $I_{VCC} + I_{VCC\_MIC} + I_{VCC\_SENSOR}$  versus Supply Voltage  $V_S$  at different Ambient Temperatures ( $R_{thJA} = 42K/W$  assumed)



The internal CAN transceiver consumes 50 mA (typ) while driving a dominant bus state, leaving 100 mA available for the external load on pin VCC. The average typical current consumption of the CAN transceiver is lower (< 25 mA), depending on the application, leaving more current available for the load.

## 2.14 Serial Peripheral Interface (SPI)

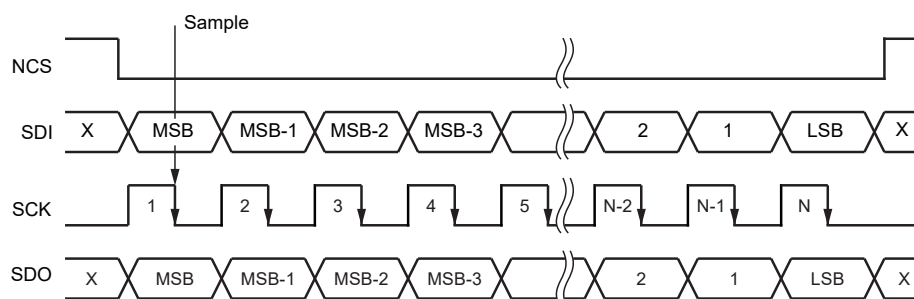
### 2.14.1 General

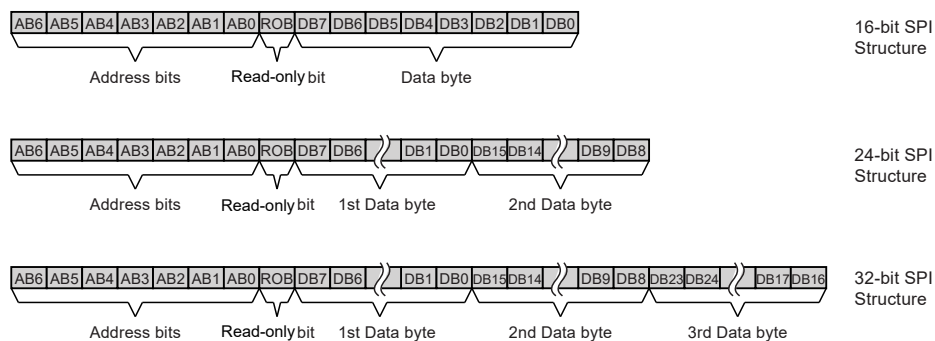
The SPI is used to communicate with a microcontroller. The ATA658x is configured and operated using SPI transfers.

The SPI allows full-duplex data transfer. Status information is returned when new control data are shifted in. The interface also offers read-only access, allowing registers to be read back without changing the register content.

Bits are sampled at the falling edge of the clock and data are shifted in/out on the rising edge, as illustrated in the figure below.

**Figure 2-32.** SPI Timing Protocol



**Figure 2-33. SPI Data Structure for Write Operation**

The SPI data is stored in dedicated 8-bit registers and each register is assigned a unique 7-bit address. 16 bits must be transmitted to the device for a single register write operation. The first byte contains the 7-bit address, along with a 'read-only' bit (the LSB). The read-only bit must be '0' to indicate a write operation. If this bit is '1', a read operation is performed and any data after this bit are ignored. The second byte contains the data to be written to the register. The contents of the addressed register(s) are shifted out via pin SDO, while a read or write operation is performed. For faster programming, 24 and 32-bit read and write operations are also supported. In this case, the register address is automatically incremented: once for a 24-bit operation and twice for a 32-bit operation.

The first byte on the SDO line is always 0x00, regardless of whether a read or write command is performed.

Attempting to write to non-existing registers is not prohibited; if the available address space is exceeded during a write operation, the data outside the valid address range are ignored (without generating an SPI failure event).

The number of the transmitted SPI bits is always monitored during SPI transfers and if the number of bits does not equal 16, 24 or 32, the SPI transfer is aborted. An SPI failure event is captured (SPIF = 1) if the SPI failure detection is enabled (SPIFE = 1) and the following SPI failure is detected:

1. SPI clock count error (only 16, 24 and 32-bit commands are valid), both read and write operations.
2. Illegal DOPM code.
3. Attempted write access to locked register.

If more than 32 bits are clocked in on pin SDI during a read operation, the data stream on SDO is looped back on SDO from bit 33 onwards.

## 2.15 Register Summary

The ATA658x contains 128 registers with addresses from 0x00 to 0x7F. An overview of the register mapping is provided in the table below. Undocumented registers and bits are reserved for future use. Reserved bits should be written to 0 unless otherwise stated.

Addr.	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
<b>Device control registers</b>										
0x01	DMCR	-	-	RSTEN	VCCOVSD	SLPVCC <sub>μ</sub> C	DOPM[2:0]			
0x02	LDOCR	-	-	-	-	-	VCCSENSOUT[2:0]			
0x03	DMSR	SMTS	OTPWS	NMTS	-	-	-	-	VCCS	
0x04	SECR	-	VSUVE	-	-	IOUVE	OTPWE	SPIFE	RSTLVL	
0x05	LDOECR	-	VCCOVLHE[2:0]			VCCOVE	VCCUVE	VCCSENSOVE	VCCSENSUVE	
0x06	GPM0						GPM0[7:0]			
0x07	GPM1						GPM1[7:0]			
0x08	GPM2						GPM2[7:0]			
0x09	GPM3						GPM3[7:0]			
0x0A	RWPR	-	WP6	WP5	WP4	WP3	WP2	WP1	WP0	
<b>TRX control registers</b>										
0x20	TRXCR	-	CFDPE	PNCFOK	CPNE	-	-	COPM[1:0]		
0x21	LTRXCR	-	-	-	-	-	-	LOPM[1:0]		
0x22	TRXSR	TXS	PNERRS	PNCFS	PNOSCS	CBSS	-	-	TXDOUTS	
0x23	TRXECR	-	PNOSCFE	-	BSE	-	LINWUE	TRXFE	CWUE	
0x24	LTRXSR	-	-	-	-	-	-	LTXDOUTS	LTXS	
0x25	REGCR	-	-	-	-	-	-	REGEN[1:0]		
0x26	DRCR	-	-	-	-	DR[3:0]				
0x27	CIDR0						ID0[7:0]			
0x28	CIDR1						ID1[7:0]			
0x29	CIDR2						ID2[7:0]			
0x2A	CIDR3	-	-	-	-	ID3[4:0]				
0x2B	CIDMR0						IDM0[7:0]			
0x2C	CIDMR1						IDM1[7:0]			
0x2D	CIDMR2						IDM2[7:0]			
0x2E	CIDMR3	-	-	-	-	IDM3[4:0]				
0x2F	CFCR	IDE	PNDM	-	-	DLC[3:0]				
0x32	BFECR	-	-	-	-	-	-	BOUTE	BSCE	
0x33	BFIR	-	-	-	-	-	-	BOUT	BSC	
0x34	TRXECR2	-	-	-	-	-	-	-	RXDRCE	
0x35	TRXESR2	-	-	-	-	-	-	-	RXDRCS	
0x36	WDCR1	WDC[2:0]			WDPRE[1:0]		WDSLP	WDLW	-	
0x37	WDCR2	WWDP[3:0]				WRPL[3:0]				
0x38	WDSR	OFF	CACC	ILLCONF	TRIGS	OF	OFSLP	ETRIG	-	
0x39	WDTRIG	WDTRIG[7:0]								
0x3A	EFCR	-	-	-	ERRCNT[4:0]					
0x3B	FECD	-	-	-	FEC[4:0]					
0x67	GLFT	-	-	-	-	-	GLF[2:0]			
0x68	CDMR0						DM0[7:0]			
0x69	CDMR1						DM1[7:0]			
0x6A	CDMR2						DM2[7:0]			

.....continued									
Addr.	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x6B	CDMR3					DM3[7:0]			
0x6C	CDMR4					DM4[7:0]			
0x6D	CDMR5					DM5[7:0]			
0x6E	CDMR6					DM6[7:0]			
0x6F	CDMR7					DM7[7:0]			
<b>WAKE control and status registers</b>									
0x4B	PWKS	-	-	-	-	-	-	PWKVS	-
0x4C	WKECR	-	-	-	-	-	EXTWUE	LWURE	LWUFE
<b>Event status registers</b>									
0x60	GESR	OSCS	-	BFES	LTRXES	WKES	CTRXES	LDOES	SYSES
0x61	SESR	SYSE	VSUV	-	PWRONS	-	-	SPIFS	IOUV
0x62	LTRXESR	-	-	-	-	LTXDOUT	OVTL	OTPWL	LINWUS
0x63	CTRXESR	-	PNOSCF	PNEFD	BS	OTPWC	OVTC	TRXF	CWUS
0x64	WKESR	-	-	-	-	-	EXTWUS	LWURS	LWUFS
0x65	BFESR	-	-	-	-	-	-	BOUFS	BSCS
0x66	LDOESR	OVTVCC	OTPWVCC	OVVCC	UVVCC	OVTVCCSENS	OTPWVCCSENS	OVVCCSENS	UVVCCSENS
<b>Device ID register</b>									
0x7E	DIDR					DIDR[7:0]			

### 3. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions, beyond those indicated in the Electrical Characteristics of this data sheet, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
DC Voltage on Pin VS, VS2	$V_{VS}, V_{VS2}$	-0.3	+40	V
DC Voltage on Pin LH, VCC_SENSOR, WAKE2	$V_{LH}, V_{VCC\_SENSOR}, V_{WAKE2}$	-0.3	+40	V
DC Voltage on WAKE	$V_{WAKE}$	-1.2	+40	V
CANH, CANL, WAKE, VCC_SENSOR, LIN, WAKE2, LIN2 Transient Voltage according to ISO 7637 Part 3	-	-150	+100	V
DC Voltage @ CANH, CANL	$V_{CANH}, V_{CANL}$	-27	+42	V
Maximum Differential Bus Voltage	$V_{Diff}$	-40	+40	V
LIN, LIN2 - DC voltage - Pulse time < 500ms	$V_{LIN}, V_{LIN2}$	-27	+40 +43.5	V
DC Voltage on Pins TXD, RXD, SDO, SDI, NCS, SCK, VCC, NRES, RXD, TXD_LIN, RXD_LIN, TXD_LIN2, RXD_LIN2, VCC_μC, EN_LIN2	$V_x$	-0.3	+5.5	V
ESD according to IBEE CAN EMC test specification following IEC 62228, IEC 61000-4-2: (330 Ω/150pF) - Pin CANH, CANL, VS, VCC_SENSOR, WAKE, VS2, WAKE2 to GND	-	±8	-	kV
ESD following IEC 61000-4-2: (330 Ω/150pF) - Pin LIN, LIN2	-	±6	-	kV
HBM JESD22-A114/AEC-Q100-002 - Pin LIN/LIN2, CANH, CANL to GND	-	±6	-	kV
HBM JESD22-A114/AEC-Q100-002 - All pins	-	±4	-	kV
Charged Device Model ESD AEC-Q100-011	-	±750	-	V
Machine Model ESD AEC-Q100-003	-	±100	-	V
Storage Temperature	$T_{stg}$	-55	+150	°C
Virtual Junction Temperature	$T_{vj}$	-40	+175	°C



## 4. Thermal Characteristics

**Table 4-1.** Thermal Characteristics 18-Lead VDFN

Parameters	Symbol	Min.	Typ.	Max.	Unit
<b>Thermal Package Resistance</b>					
Thermal Resistance Virtual Junction to Case	$R_{thvjC}$	—	8	—	K/W
Thermal Resistance Virtual Junction to Ambient, Where device is Soldered to PCB According to JEDEC	$R_{thvjA}$	—	45	—	K/W
<b>Thermal Shutdown of the Bus Drivers Output and voltage regulators (VCC, VCC_SENSOR, LIN, CANH, CANL)</b>					
ATA658x-GTQW1 (Grade 1)	$T_{vjSD}$	150	—	175	°C
ATA658x-GTQW0 (Grade 0)	$T_{vjSD}$	170	—	195	°C
Thermal shutdown hysteresis	$T_{vjSD\_hys}$	—	15	—	°C

**Table 4-2.** Thermal Characteristics 26-Lead VDFN

Parameters	Symbol	Min.	Typ.	Max.	Unit
<b>Thermal Package Resistance</b>					
Thermal Resistance Virtual Junction to Case	$R_{thvjC}$	—	8	—	K/W
Thermal Resistance Virtual Junction to Ambient, Where device is Soldered to PCB According to JEDEC	$R_{thvjA}$	—	42	—	K/W
<b>Thermal Shutdown of the Bus Drivers Output and voltage regulators (VCC, VCC_SENSOR, VCC_μC, LIN, LIN2, CANH, CANL)</b>					
ATA658x-GUQW1 (Grade 1)	$T_{vjSD}$	150	—	175	°C
Thermal shutdown hysteresis	$T_{vjSD\_hys}$	—	15	—	°C

## 5. Electrical Characteristics

All parameters valid for  $3V \leq V_{VSx} \leq 28V$ ,  $4.5V \leq V_{VCC} \leq 5.5V$ , all voltages are defined with respect to ground,  $R_{(CANH-CANL)} = 60\Omega$ , Grade 1:  $T_{amb} = -40^{\circ}C$  to  $+125^{\circ}C$  and Grade 0:  $T_{amb} = -40^{\circ}C$  to  $+150^{\circ}C$ ,  $T_{vj} \leq +170^{\circ}C$ , typical values are given at  $V_{VS} = 13V$ ,  $T_{amb} = +25^{\circ}C$ , unless otherwise noted.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
<b>VS, VS2</b>									
0.10	Supply Voltage Threshold for Power-On Detection	$V_{VS}$ rising	VS	$V_{VS\_PWRON}$	4.1	-	4.55	V	A
0.20	Supply Voltage Threshold for Power-Off Detection	$V_{VS}$ falling	VS	$V_{VS\_PWROFF}$	2.8	-	3.1	V	A
0.30	Supply Voltage Threshold for CAN/LIN TRX Undervoltage Detection Release	$V_{VS}$ rising	VS	$V_{VS\_UV\_TRX\_Clear}$	4.5	-	5	V	A
0.40	Supply Voltage Threshold for CAN/LIN TRX Undervoltage Detection Set	$V_{VS}$ falling	VS	$V_{VS\_UV\_TRX\_Set}$	4.1	-	4.55	V	A
0.50	VS Supply Current	<b>ATA6580/1/5/6:</b> $V_{VS} = 7V$ to $18V$ ; DOPM = Sleep; CWUE = 1; CAN Standby mode; no SPI communication; LINWUE=0 and LIN Standby mode in the ATA6581/6; watchdog inactive; VCC_SENSOR disabled	VS	$I_{VS\_SLP\_L}$	-	-	30	$\mu A$	A
0.51	VS Supply Current	<b>ATA6581/6:</b> $V_{VS} = 7V$ to $18V$ ; DOPM = Sleep; CWUE = 1; CAN Standby mode; LINWUE=1; LIN Standby mode; $V_{LIN} > V_{VS} - 0.5V$ ; watchdog active; VCC_SENSOR disabled	VS	$I_{VS\_SLP\_1}$	-	-	50	$\mu A$	A
0.52	VS Supply Current	<b>ATA6580/5:</b> $V_{VS} = 7V$ to $18V$ ; DOPM = Sleep; CWUE = 1; CAN Standby mode; watchdog active; VCC_SENSOR disabled	VS	$I_{VS\_SLP\_2}$	-	-	45	$\mu A$	A
0.53	VS, VS2 Supply Current	<b>ATA6582/3/7/8:</b> $V_{VS}, V_{VS2} = 7V$ to $18V$ ; DOPM = Sleep; CWUE=1; CAN Standby mode; LINWUE=0; LIN Standby mode; watchdog inactive; no SPI communication; $V_{LIN} > V_{VS} - 0.5V$ ; LIN2 device in Sleep mode; $V_{LIN2} > V_{VS2} - 0.5V$ ; VCC_SENSOR disabled	VS & VS2	$I_{VS\_SLP\_L\_SIP}$	-	-	48	$\mu A$	A
0.54	VS, VS2 Supply Current	<b>ATA6582/3/7/8:</b> $V_{VS}, V_{VS2} = 7V$ to $18V$ ; DOPM = Sleep; CWUE=1; CAN Standby mode; LINWUE=1; LIN Standby mode; watchdog active; SPI communication for watchdog trigger; $V_{VCC\_uC}=0V$ ; $V_{LIN} > V_{VS} - 0.5V$ ; LIN2 device in Sleep mode; $V_{LIN2} > V_{VS2} - 0.5V$ ; VCC_SENSOR disabled	VS & VS2	$I_{VS\_SLP\_H\_SIP}$	-	-	68	$\mu A$	A

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
0.55	VS Supply Current	<b>ATA6581/6:</b> $V_{VS} = 7V$ to 18V; DOPM = Standby; CWUE=1; CAN Standby mode; LIN standby; LINWUE=1; watchdog active; $V_{LIN} > V_{VS} - 0.5V$ ; SPI communication for watchdog trigger; VCC_SENSOR disabled	VS	$I_{VS\_STB\_1}$	-	-	80	$\mu A$	A
0.56	VS Supply Current	<b>ATA6580/5:</b> $V_{VS} = 7V$ to 18V; DOPM = Standby; CWUE=1; CAN Standby mode; watchdog active; SPI communication for watchdog trigger; VCC_SENSOR disabled	VS	$I_{VS\_STB\_2}$	-	-	75	$\mu A$	A
0.57	VS, VS2 Supply Current	<b>ATA6582/3/7/8:</b> $V_{VS}, V_{VS2} = 7V$ to 18V; DOPM = Standby; CWUE=1; CAN Standby mode; LINWUE=1; LIN Standby mode; LIN2 device in Silent mode; $V_{LIN} > V_{VS} - 0.5V$ ; $V_{LIN2} > V_{VS2} - 0.5V$ ; watchdog active; SPI communication for watchdog trigger; VCC_SENSOR disabled	VS & VS2	$I_{VS\_STB\_SIP}$	-	-	144	$\mu A$	A
0.58	VS Supply Current	<b>ATA6585/6:</b> $V_{VS} = 7V$ to 18V; DOPM = Sleep; CWUE=1; CAN Biased Standby mode; in the ATA6586 LINWUE=0; LIN Standby mode; watchdog inactive; CPNE=1; PNCFOK=1; CAN bus active; VCC_SENSOR disabled	VS	$I_{VS\_PN\_ACT\_SLP}$	-	-	500	$\mu A$	A
0.59	VS Supply Current	<b>ATA6585/6:</b> $V_{VS} = 7V$ to 18V; DOPM = Standby; CWUE=1; CAN Biased Standby mode; in the ATA6586 LINWUE=0; LIN Standby mode; watchdog inactive; CPNE=1; PNCFOK=1; CAN bus active; VCC_SENSOR disabled	VS	$I_{VS\_PN\_ACT\_STB}$	-	-	550	$\mu A$	A
0.60	VS Supply Current	<b>ATA6580/1/5/6:</b> $V_{VS} = 7V$ to 18V; DOPM = Normal; CWUE=1; CAN Normal mode; TXD=High; in the ATA6586 Partial Networking inactive; in the ATA6581/6 LINWUE=0; LIN Standby mode; TXD_LIN=High; VCC_SENSOR disabled	VS	$I_{VS\_NORM\_CAN\_REC}$	-	-	5	mA	A
0.61	VS Supply Current	<b>ATA6580/1/5/6:</b> $V_{VS} = 7V$ to 18V; DOPM = Normal; CWUE=1; CAN Normal mode; TXD=Low; in the ATA6586 Partial Networking inactive; in the ATA6581/6 LINWUE=0; LIN Standby mode; TXD_LIN=High; VCC_SENSOR disabled	VS	$I_{VS\_NORM\_CAN\_DOM}$	25	55	75	mA	A
0.612	VS Supply CAN Dominant Short Current	$V_{TXD} = 0V$ , short between CANH and CANL	VS	$I_{CAN\_short}$	-	-	80	mA	B

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
0.62	VS Supply Current	ATA6581/6: $V_{VS} = 7V$ to $18V$ ; DOPM = Normal; CWUE=1; CAN Standby mode; TXD=High; in the ATA6586 Partial Networking inactive; LIN Normal mode; TXD_LIN=Low; LINWUE=0; VCC_SENSOR disabled	VS	$I_{VS\_NORM\_LIN\_REC}$	-	300	400	$\mu A$	A
0.63	VS Supply Current	ATA6581/6: $V_{VS} = 7V$ to $18V$ ; DOPM = Normal; CWUE=1; CAN Standby mode; TXD=High; in the ATA6586 Partial Networking inactive; LIN Normal mode; TXD_LIN=High; LINWUE=0; VCC_SENSOR disabled	VS	$I_{VS\_NORM\_LIN\_DOM}$	-	800	1400	$\mu A$	A
<b>VCC</b>									
1.10	Output Voltage	$V_{VS} > 5.8V$ $I_{VCC} = 0$ to $-150mA$	VCC	$V_{VCCnom}$	4.9	-	5.1	V	A
1.101	Load Step Response	$V_{VS} > 5.8V$ $C_{VCC} = 2.2\mu F$ (MLC capacitor) $I_{VCC} = 0$ to $-150mA$ $I_{VCC} = -150$ to $0mA$	VCC	$V_{VCC\_LoadStep}$	-2	-	+2	%	C
1.20	Output voltage at low VS	$4V < V_{VS} < 5.75V$ ( $I_{VCC} = 0$ to $-150mA$ )	VCC	$V_{VCClow}$	$V_{VS} - V_{Dx}$	-	5.1	V	A
1.30	Regulator Drop Voltage	$V_{VS} > 4V$ , $I_{VCC} = -20mA$	VCC	$V_{D1}$	-	-	100	mV	A
1.31		$V_{VS} > 4V$ , $I_{VCC} = -50mA$	VCC	$V_{D2}$	-	-	250	mV	A
1.32		$V_{VS} > 4V$ , $I_{VCC} = -150mA$	VCC	$V_{D3}$	-	-	750	mV	A
1.33		$2V < V_{VS} < 3V$ , $I_{VCC} = -2mA$	VCC	$V_{D4}$	-	-	100	mV	A
1.34		$2V < V_{VS} < 3V$ , $I_{VCC} = -200\mu A$	VCC	$V_{D5}$	-	-	10	mV	A
1.40	Line regulation maximum	$5.75V < V_{VS} < 28V$ $I_{VCC} = 20mA$	VCC	$V_{VCCline}$	-	-	0.2	%	A
1.50	Load regulation maximum	$V_{VS} = 12V$ $-5mA > I_{VCC} > -150mA$	VCC	$V_{VCCload}$	-	-	0.7	%	C
1.51	Load regulation maximum	$V_{VS} = 12V$ $-5mA > I_{VCC} > -150mA$ $T=125^{\circ}C$	VCC	$V_{VCCload}$	-	-	0.6	%	C
1.60	Output current limitation	$V_{VS} = 5.75V$	VCC	$I_{VCClim}$	-360	-230	-160	mA	A
1.70	Load capacitance	MLC capacitor	VCC	$C_{load}$	1.87	2.2	-	$\mu F$	D
1.80	Ramp-up time	$V_{VS} > 5.75V$ , after enable VCC regulator to $V_{VCC}$ reach $V_{VCC} = 4.3V$ , $C_{VCC} = 2.2\mu F$ , $R_{load} = 1k\Omega$ at VCC	VCC	$t_{VCC\_startup}$	-	-	0.5	ms	B
1.90	VCC TRX undervoltage set threshold	$V_{VCC}$ falling	VCC	$V_{VCC\_UV\_TRX\_Set}$	4.5	-	4.7	V	A
1.100	VCC TRX undervoltage clear threshold	$V_{VCC}$ rising	VCC	$V_{VCC\_UV\_TRX\_Clear}$	4.6	-	4.8	V	A
1.110	VCC TRX undervoltage hysteresis	-	VCC	-	0.08	0.1	0.12	V	C

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.120	VCC IO undervoltage Set	V <sub>VCC</sub> falling (ATA6580/1/5/6) V <sub>VCC_μC</sub> falling (ATA6582/3/7/8)	VCC/ VCC_μC	V <sub>VCC_UV_IO_Set</sub>	2.4	-	2.7	V	A
1.130	VCC IO undervoltage Clear	V <sub>VCC</sub> rising (ATA6580/1/5/6) V <sub>VCC_μC</sub> rising (ATA6582/3/7/8)	VCC/ VCC_μC	V <sub>VCC_UV_IO_Clear</sub>	2.5	-	2.8	V	A
1.140	VCC IO undervoltage hysteresis	-	VCC/ VCC_μC	-	0.08	0.1	0.12	V	C
1.150	VCC_μC reset undervoltage set threshold	V <sub>VCC_μC</sub> falling (ATA6582/7)	VCC_μC	V <sub>VCC_μC_UV_RST_Set</sub>	4.5	-	4.7	V	A
1.160	VCC_μC reset undervoltage clear threshold	V <sub>VCC_μC</sub> rising (ATA6582/7)	VCC_μC	V <sub>VCC_μC_UV_RST_Clear</sub>	4.6	-	4.8	V	A
1.170	VCC_μC reset undervoltage hysteresis	(ATA6582/7)	VCC_μC	-	0.08	0.1	0.12	V	C
1.180	VCC overvoltage set detection threshold	V <sub>VCC</sub> rising	VCC	V <sub>VCC_OV_Set</sub>	5.25	-	5.5	V	A
1.190	VCC overvoltage clear detection threshold	V <sub>VCC</sub> falling	VCC	V <sub>VCC_OV_Clear</sub>	5.20	-	5.45	V	A
1.200	VCC overvoltage hysteresis	VCC_UV_RST_hys	VCC	-	0.03	0.05	0.07	V	C
<b>VCC_SENSOR</b>									
2.10	Output voltage	I <sub>VCC_SENSOR</sub> = -30 mA to 0 mA, V <sub>VS</sub> ≥ 6.5V (5V configuration)	VCC_SE NSOR	V <sub>VCC_SENSOR</sub>	4.9	5	5.1	V	A
2.11		I <sub>VCC_SENSOR</sub> = -30 mA to 0 mA, V <sub>VS</sub> ≥ 4.8V (3.3V configuration)	VCC_SE NSOR	V <sub>VCC_SENSOR</sub>	3.234	3.3	3.366	V	A
2.20	Regulator drop voltage	4V < V <sub>VS</sub> < 6.5V (5V config.) 4V < V <sub>VS</sub> < 4.8V (3.3V config.) I <sub>load</sub> = 30mA	VCC_SE NSOR	V <sub>D</sub>	-	-	1.5	V	A
2.21	Regulator drop voltage	3V < V <sub>VS</sub> < 4V (5V config.) 3 < V <sub>VS</sub> < 4V (3.3V config.) I <sub>load</sub> = 30mA	VCC_SE NSOR	V <sub>D</sub>	-	-	1.5	V	C
2.30	Undervoltage detection voltage set	5V configuration	VCC_SE NSOR	V <sub>VCC_SENSOR_UV_Set</sub>	4.5	-	4.7	V	A
2.40	Undervoltage detection voltage clear	5V configuration	VCC_SE NSOR	V <sub>VCC_SENSOR_UV_Clear</sub>	4.6	-	4.8	V	A
2.50	VCC_SENSOR undervoltage/ overvoltage detection hysteresis	5V/3.3V configuration	VCC_SE NSOR	V <sub>VCC_SENSOR_UV_HYS</sub>	0.08	0.1	0.12	V	C
2.60	Short-circuit output current limitation	5V/3.3V configuration	VCC_SE NSOR	I <sub>VCC_SENSOR_Lim</sub>	-120	-75	-30	mA	A
2.70	Overvoltage detection threshold	5V configuration	VCC_SE NSOR	I <sub>VCCSENS_OV_Set</sub>	6.5	-	7	V	A
2.80	Undervoltage detection voltage set	3.3V configuration	VCC_SE NSOR	V <sub>VCCSENS_UV_Set_33</sub>	2.7	-	2.8	V	A
2.90	Undervoltage detection voltage clear	3.3V configuration	VCC_SE NSOR	V <sub>VCCSENS_UV_Clear_33</sub>	2.8	-	2.9	V	A
2.100	Overvoltage detection threshold	3.3V configuration	VCC_SE NSOR	V <sub>VCCSENS_OV_33_Set</sub>	4.3	-	4.6	V	A
2.110	Line regulation maximum	6.5 V < V <sub>VS</sub> < 28V, for 5V config. 4.8 V < V <sub>VS</sub> < 28V, for 3.3V config. I <sub>VCC</sub> = 30mA	VCC_SE NSOR	V <sub>VCC_SENSOR_line</sub>	-	-	0.2	%	A

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
2.120	Load regulation maximum	$V_{VS} = 12V$ $-1mA < I_{VCC} < -30mA$	VCC_SE NSOR	$V_{VCC\_SENSOR\_load}$	-	-	0.5	%	C
2.170	Load capacitance	MLC capacitor	VCC_SE NSOR	$C_{VCC\_SENSOR}$	1.87	2.2	-	$\mu F$	D
2.180	Ramp-up time	$V_{VS} > 6.5V$ , from enable regulator to $V_{VCC\_SENSOR}$ reach 90% of $V_{VCCSENS\_UV\_Clear\_5V}$ or $V_{VCCSENS\_UV\_Clear\_33}$ (3.3V), $C_{VCC\_SENSOR}=2.2\mu F$ , $R_{load}=1k\Omega$ at VCC_SENSOR	VCC_SE NSOR	$t_{VCC\_SENSOR\_startup}$	-	-	0.5	ms	B
<b>SDI, SCK, NCS, TXD, TXD_LIN, RXD</b>									
3.10	High-Level Input Voltage	-	SDI, SCK, NCS, TXD, TXD_LIN	$V_{SDI\_H}, V_{SCK\_H}, V_{NCS\_H},$ $V_{TXD\_H}, V_{TXD\_LIN\_H}$	$0.7 \times$ $V_{VCC}/$ $V_{VCC\_uC}$	-	$V_{VCC}/$ $V_{VCC\_uC}$ $+ 0.3$	V	A
3.20	Low-Level Input Voltage	-	SDI, SCK, NCS, TXD, TXD_LIN	$V_{SDI\_H}, V_{SCK\_H}, V_{NCS\_H},$ $V_{TXD\_H}, V_{TXD\_LIN\_H}$	-0.3	-	$V_{VCC}/$ $V_{VCC\_uC}$ $\times 0.3$	V	A
3.30	Input Current	-	SDI	$I_{I\_SDI}$	-5	-	+5	$\mu A$	A
3.40	Pull-Up Resistance on Pin NCS, TXD, TXD_LIN	-	NCS	$R_{PU\_NCS}$	40	60	80	$k\Omega$	A
3.50	Pull-Down Resistance on Pin SCK	-	SCK	$R_{PD\_SCK}$	40	60	80	$k\Omega$	A
<b>SDO, RXD, RXD_LIN</b>									
4.10	High-Level Output Voltage	$I = -4 mA$	SDO, RXD, RXD_LIN	$V_{SDO\_H}, V_{RXD\_H}$	$V_{VCC}/$ $V_{VCC\_uC}$ $- 0.4$	-	$V_{VCC}/$ $V_{VCC\_uC}$	V	A
4.20	Low-Level Output Voltage	$I = 4 mA$	SDO, RXD, RXD_LIN	$V_{SDO\_L}, V_{RXD\_L}$	-	-	0.4	V	A
4.40	OFF State Leakage Current	-	SDO	$I_{leak\_SDO}$	-5	-	+5	$\mu A$	A
<b>WAKE</b>									
6.10	High-Level Input Current	$V_{WAKE} = 4.2V, V_{VS} \geq 5.2V$	WAKE	$I_{WAKE\_H}$	-10	-5	-1	$\mu A$	A
6.20	Low-Level Input Current	$V_{WAKE} = 2.3V$	WAKE	$I_{WAKE\_L}$	1	5	10	$\mu A$	A
6.30	WAKE Threshold Voltage	WAKE rising, $V_{VS} \geq 4.2V$	WAKE	$V_{WAKE\_TH\_R}$	2.8	-	4.1	V	A
6.31		WAKE falling, $V_{VS} \geq 4.2V$	WAKE	$V_{WAKE\_TH\_F}$	2.4	-	3.75	V	A
6.40	Input Hysteresis Voltage	-	WAKE	$V_{WAKE\_hys}$	0.2	-	0.6	V	C
<b>WAKE2</b>									
6.50	WAKE2 Threshold Voltage	WAKE2 rising, $V_{VS} \geq 4.2V$	WAKE2	$V_{WAKE2\_TH\_R}$	2.8	-	4.1	V	A
6.51		WAKE2 falling, $V_{VS} \geq 4.2V$ Initializes a wake-up signal	WAKE2	$V_{WAKE2\_TH\_F}$	2.4	-	3.75	V	A
6.60	Input Hysteresis Voltage	-	WAKE2	$V_{WAKE2\_hys}$	0.2	-	0.6	V	C
6.70	High-Level Leakage Current	$V_{VS} = 28V, V_{WAKE2} = 28V$	WAKE2	$I_{WAKE2}$	-	900	-	nA	C
6.80	WAKE2 pull-up	$V_{VS} < 28V, V_{WAKE2} = 0V$	WAKE2	$I_{WAKE2\_pu}$	-30	-10	-	$\mu A$	A
<b>LH open drain output pin</b>									
7.10	Output drain-to-source on resistance	$V_{VS} \geq 4.2V, T_j = 170^\circ C, I_{LH} = 4mA$	LH	$R_{DSon,HS}$	-	-	50	$\Omega$	A
7.20	Leakage current	$V_{LH} < 40V$	LH	$I_{leak,LH}$	-	-	2	$\mu A$	A
<b>NRES open drain output/input pin</b>									

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.10	Low-Level Output Voltage	$I_{NRES} = 2 \text{ mA}$	NRES	$V_{NRESL}$	-	0.2	0.4	V	A
8.20	Undervoltage reset time	$C_{NRES} = 20\text{pF}$	NRES	$t_{reset}$	According to the setting in the register WDCR2			ms	B
8.30	Pull-up resistance in series with a diode	-	NRES	$R_{Pu}$	6.5	10	13.5	k $\Omega$	A
8.40	High-level input voltage	-	NRES	$V_{NRES\_H}$	$0.7 \times V_{VCC}$	-	-	V	A
8.50	Low-level input voltage	-	NRES	$V_{NRES\_L}$	-	-	$0.3 \times V_{VCC}$	V	A
8.60	Debounce time for reset detection	-	NRES	$t_{nres\_input}$	60	-	80	$\mu\text{s}$	B
<b>CANH, CANL (see Figure 6-4 for the definition of <math>R_L</math> and the test circuit)</b>									
9.10	Single-Ended Dominant Output Voltage	$R_L = 50\Omega$ to $65\Omega$	CANH	$V_{CANH}$	2.75	3.5	4.5	V	A
9.11			CANL	$V_{CANL}$	0.5	1.5	2.25	V	A
9.20	Transmitter Dominant Voltage Symmetry	$V_{dom(TX)sym} = V_{VCC} - (V_{CANH} + V_{CANL})$	-	$V_{dom(TX)sym}$	-400	-	+400	mV	D
9.30	Transmitter Voltage Symmetry	$V_{Sym} = (V_{CANH} + V_{CANL}) / V_{VCC}$ , $R_L = 60\Omega / \text{tol.} < 1\%$ , $C_{split} = 4.7 \text{ nF}$ $f_{TXD} = 1 \text{ MHz}$ , input impedance of oscilloscope: $\leq 20\text{pF} / \geq 1 \text{ M}\Omega$	-	$V_{Sym}$	0.9	1.0	1.1	-	C
9.40	Bus Differential Output Voltage	CAN Normal mode, $V_{TXD} = 0\text{V}$ , $t < t_{to(dom)} R_L = 50\Omega$ to $65\Omega$ , $V_{VCC} = 4.7\text{V}$ to $5.5\text{V}$	-	$V_{Diff}$	1.5	-	3	V	B
9.41		CAN Normal mode, $V_{TXD} = 0\text{V}$ , $t < t_{to(dom)} R_L = 45\Omega$ to $70\Omega$ , $V_{VCC} = 4.7\text{V}$ to $5.5\text{V}$	-	$V_{Diff}$	1.4	-	3.2	V	B
9.42		CAN Normal mode, $V_{TXD} = 0\text{V}$ , $t < t_{to(dom)} R_L = 224 \text{ } 0\Omega$ $V_{VCC} = 4.7\text{V}$ to $5.5\text{V}$	-	$V_{Diff}$	1.5	-	5	V	B
9.50	Recessive Output Voltage	Single-ended output voltage on CANH/CANL, CAN Normal mode, $V_{VCC} > 4.3\text{V}$ , $V_{TXD} = V_{VCC}$ , no load	CANH, CANL	$V_{CANH}, V_{CANL}$	2	$0.5 \times V_{VCC}$	3	V	A
9.51		Single-ended output voltage on CANH/CANL, CAN Standby mode, $V_{TXD} = V_{VCC}$ , no load	CANH, CANL	$V_{CANH}, V_{CANL}$	-0.1	-	+0.1	V	A
9.52		Single-ended output voltage on CANH/CANL, CAN Biased Standby/CAN Silent mode, $V_{TXD} = V_{VCC}$ , no load	CANH, CANL	$V_{CANH}, V_{CANL}$	2	2.5	3	V	A
9.53		Differential output voltage (bus biasing active), no load	-	$V_{Diff}$	-50	-	+50	mV	A
9.54		Differential output voltage (bus biasing inactive), no load	-	$V_{Diff}$	-50	-	+50	mV	A
9.60	Differential Receiver Threshold Voltage	CAN Normal/CAN Silent modes, $V_{CANL} = V_{CANH} = -12\text{V}$ to $+12\text{V}$	-	$V_{Diff\_rx\_th}$	0.5	0.7	0.9	V	A
9.61		CAN Standby mode, $V_{CANL} = V_{CANH} = -12\text{V}$ to $+12\text{V}$	-	$V_{Diff\_rx\_th}$	0.4	0.7	1.15	V	A
9.70	Differential Receiver Hysteresis Voltage	CAN Normal/CAN Silent mode, $V_{CANL} = V_{CANH} = -12\text{V}$ to $+12\text{V}$	-	$V_{Hys\_rx}$	50	120	200	mV	C

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9.80	Leakage Current	$V_{VS} = V_{VCC} =$ connected to GND with 47 k $\Omega$ $V_{CANH} = V_{CANL} = 5V$	CANH, CANL	$I_{leak\_in}(ICAN\_H, ICAN\_L)$	-5	-	+5	$\mu A$	D
9.81		$V_{VS} = V_{VCC} = 0V$ $V_{CANH} = V_{CANL} = 5V$	-	$I_{leak\_in}(ICAN\_H, ICAN\_L)$	-5	-	+5	$\mu A$	A
9.90	Maximum Driver Output Current	CAN Normal mode; CAN dominant, $V_{TXD} = 0$ , $t < t_{to(dom)}$ , $V_{VCC} = 5V$ , $V_{CANH} = -5V$	CANH	$I_{CANH\_max}$	-75	-	-33	mA	A
9.91		CAN Normal mode, CAN dominant; $V_{TXD} = 0$ , $t < t_{to(dom)}$ , $V_{VCC} = 5V$ , $V_{CANL} = +18V$	CANL	$I_{CANL\_max}$	33	-	75	mA	A
9.92		CAN Normal mode, CAN dominant; $V_{TXD} = 0$ , $t < t_{to(dom)}$ , $V_{VCC} = 5V$ , $V_{CANL} = +27V$	CANL	$I_{CANL\_max}$	33	-	75	mA	D
9.100	CAN dominant current	$V_{TXD}=0V$	CANH, CANL	$I_{CAN\_dom}$	-	-	80	mA	A
9.120	Single-Ended Input Resistance	$-2V \leq V_{CANH} \leq 7V$ $-2V \leq V_{CANL} \leq 7V$	CANH, CANL	$R_{CANH}, R_{CANL}$	9	15	28	k $\Omega$	D
9.131	Matching of Internal Resistance between CANH and CANL	$V_{CANH}, V_{CANL}: 5V$ $mR = 2 \times (R_{CANH} - R_{CANL}) / (R_{CANH} + R_{CANL})$	-	mR	-0.01	-	+0.01	-	A
		$-2V \leq V_{CANH} \leq 7V$ $-2V \leq V_{CANL} \leq 7V$ $mR = 2 \times (R_{CANH} - R_{CANL}) / (R_{CANH} + R_{CANL})$	-	mR	-0.01	-	+0.01	-	D
9.140	Differential Internal Resistance	$V_{CANH} = V_{CANL} = 5V$	-	$R_{Diff}$	18	30	56	k $\Omega$	A
		$-2V \leq V_{CANH} \leq 7V$ $-2V \leq V_{CANL} \leq 7V$	-	$R_{Diff}$	18	30	56	k $\Omega$	D
9.150	Common-Mode Input Capacitance	$f = 500$ kHz, CANH and CANL referred to GND	-	$C_{i(cm)}$	-	-	20	pF	D
9.160	Differential Input Capacitance	$f = 500$ kHz, between CANH and CANL	-	$C_{Diff}$	-	-	10	pF	D
9.170	Differential Bus Voltage Range for Recessive State Detection	Bus biasing active	-	$V_{Diff\_rec\_a}$	-3.0	-	+0.5	V	D
		Bus biasing inactive	-	$V_{Diff\_rec\_i}$	-3.0	-	+0.4	V	D
9.180	Differential Bus Voltage Range for Dominant State Detection	Bus biasing active	-	$V_{DIFF\_dom\_a}$	0.9	-	8.0	V	D
		Bus biasing inactive	-	$V_{DIFF\_dom\_i}$	1.15	-	8.0	V	D
<b>LIN bus driver: bus load conditions: <math>5V &lt; V_S &lt; 18V</math>; Load 1 (Small): 1nF, 1k<math>\Omega</math>; Load 2 (Large): 10nF, 500<math>\Omega</math>; CRXD = 20pF, Load 3 (Medium): 6.8nF, 660<math>\Omega</math> characterized on samples 11.280 to 11.290 specifies the timing parameters for proper operation at 20kb/s and 11.300 and 11.310 at 10.4kb/s</b>									
10.10	Driver recessive output voltage	Load1/Load2	LIN	$V_{BUSrec}$	$0.9 \times V_{VS}$	-	$V_{VS}$	V	A



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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10.20	Driver-dominant voltage	$V_{VS} = 7V$ $R_{load} = 500\Omega$	LIN	$V_{LoSUP}$	-	-	1.2	V	A
10.21		$V_{VS} = 18V$ $R_{load} = 500\Omega$	LIN	$V_{HiSUP}$	-	-	2	V	A
10.22		$V_{VS} = 7V$ $R_{load} = 1000\Omega$	LIN	$V_{LoSUP\_1k}$	0.6	-	-	V	A
10.23		$V_{VS} = 18V$ $R_{load} = 1000\Omega$	LIN	$V_{HiSUP\_1k}$	0.8	-	-	V	A
10.30	Pull-up resistor to VS	With a series diode to VS	LIN	$R_{LIN}$	20	30	47	k $\Omega$	A
10.40	Voltage drop at the serial diodes	In pull-up path with $R_{LIN}$ $I_{SerDiode} = 10mA$	LIN	$V_{SerDiode}$	0.4	-	1.0	V	D
10.50	LIN current limitation $V_{LIN} = V_{VS\_max}$	In pull-up path with $R_{LIN}$ $I_{SerDiode} = 10mA$	LIN	$I_{BUS\_LIM}$	40	120	200	mA	A
10.60	Input leakage current at the receiver including pull-up resistor as specified	Input leakage current $V_{LIN} = 0V$	LIN	$I_{BUS\_PAS\_dom}$	-1	-0.35	-	mA	A
10.70	Leakage current LIN recessive	Driver off $8V < V_{VS} < 18V$ $8V < V_{LIN} < 18V$	LIN	$I_{BUS\_PAS\_rec}$	-	-	20	$\mu A$	A
10.80	Leakage current when control unit disconnected from ground. Loss of local ground must not affect communication in the residual network.	$GND_{Device} = V_{VS} = 12V$ $0V < V_{LIN} < 18V$	LIN	$I_{BUS\_NO\_gnd}$	-10	+0.5	+10	$\mu A$	A
10.90	Leakage current at disconnected battery. Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.	VS connected to ground GND $0V < V_{LIN} < 18V$	LIN	$I_{BUS\_NO\_bat}$	-	0.1	2	$\mu A$	A
10.100	Capacitance on the LIN pin to GND	-	LIN	$C_{LIN}$	-	-	20	pF	D
10.110	Center of receiver threshold	$V_{BUS\_CNT} = (V_{th\_dom} + V_{th\_rec})/2$	LIN	$V_{BUS\_CNT}$	$0.475 \times V_{VS}$	$0.5 \times V_{VS}$	$0.525 \times V_{VS}$	V	A
10.120	Receiver dominant state	-	LIN	$V_{BUSdom}$	-27	-	$0.4 \times V_{VS}$	V	A
10.130	Receiver recessive state	-	LIN	$V_{BUSrec}$	$0.6 \times V_{VS}$	-	40	V	A
10.140	Receiver input hysteresis	$V_{hys} = V_{th\_rec} - V_{th\_dom}$	LIN	$V_{BUShys}$	$0.028 \times V_{VS}$	$0.1 \times V_{VS}$	$0.175 \times V_{VS}$	V	A
10.150	Pre-wake detection LIN High-level input voltage	-	LIN	$V_{LINH}$	$V_{VS} - 2$	-	$V_{VS} + 0.3$	V	A
10.160	Pre-wake detection LIN Low-level input voltage	Activates the LIN receiver	LIN	$V_{LINL}$	- 27	-	$V_{VS} - 3.4$	V	A
<b>Timing, Pins CANH, CANL, LIN, LH, TXD, TXD_LIN, RXD and RXD_LIN. Refer to to the figures at the end of the chapter and Figure 6-4 for the definition of the timing parameters and the test circuit.</b>									
11.10	Delay Time from TXD to Bus Dominant	$R_L = 60\Omega$ , $C_2 = 100$ pF (R and C tolerance $\leq \pm 1\%$ )	CANH, CANL, TXD	$t_{TXDBUS\_dom}$	-	65	-	ns	C
11.20	Delay Time from TXD to Bus Recessive	$R_L = 60\Omega$ , $C_2 = 100$ pF (R and C tolerance $\leq \pm 1\%$ )	CANH, CANL, TXD	$t_{TXDBUS\_rec}$	-	90	-	ns	C
11.30	Delay Time from Bus Bominant to RXD	$R_L = 60\Omega$ , $C_2 = 100$ pF (R and C tolerance $\leq \pm 1\%$ )	CANH, CANL, RXD	$t_{BUSRXD\_dom}$	-	60	-	ns	C

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
11.40	Delay Time from Bus Recessive to RXD	$R_L = 60\Omega$ , $C_2 = 100\text{ pF}$ (R and C tolerance $\leq \pm 1\%$ )	CANH, CANL, RXD	$t_{BUSRXD\_rec}$	-	65	-	ns	C
11.50	Propagation Delay from TXD to RXD (the input signal on TXD shall have rise and fall times (10%/90%) of less than 10 ns.) (Time span from signal edge on TXD input to next signal edge with the same polarity on RXD output, the maximum delay of both signal edges is to be considered.)	$R_L = 60\Omega$ , $C_2 = 100\text{ pF}$ , $C_{RXD} = 15\text{ pF}$ (R and C tolerance $\leq \pm 1\%$ )	TXD, RXD	$t_{Loop}$	40	-	190	ns	A
11.51		$R_L = 150\Omega$ , $C_2 = 100\text{ pF}$ , $C_{RXD} = 15\text{ pF}$ , $f_{TXD} = 250\text{ kHz}$ (R and C tolerance $\leq \pm 1\%$ )	TXD, RXD	$t_{Loop}$	-	-	300	ns	C
11.60	Received Recessive Bit Time on Pin RXD	$t_{B\_TXD} = 500\text{ ns}$ , $R_L = 60\Omega$ , $C_2 = 100\text{ pF}$ , $C_{RXD} = 15\text{ pF}$	RXD	$t_{Bit(RXD)}$	400	-	550	ns	C
11.61		$t_{B\_TXD} = 200\text{ ns}$ , $R_L = 60\Omega$ , $C_2 = 100\text{ pF}$ , $C_{RXD} = 15\text{ pF}$	RXD	$t_{Bit(RXD)}$	120	-	220	ns	A
11.70	Receiver Timing Symmetry	$\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}t_{B\_TXD} = 500\text{ ns}$ (Refer to the 11.100 for $t_{Bit(Bus)}$ )	-	$\Delta t_{Rec}$	-65	-	+40	ns	C
11.71		$\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}t_{B\_TXD} = 200\text{ ns}$ (Refer to the 11.110 for $t_{Bit(Bus)}$ )	-	$\Delta t_{Rec}$	-45	-	+15	ns	A
11.80	TXD Dominant Time-out Time	$V_{TXD} = 0V$ , Normal mode	TXD	$t_{to(dom)}$	2.7	-	3.3	ms	B
11.90	Bus Dominant Time-out Time	$V_{CANH-CANL} > 0.9\text{ V}$	-	$t_{BUS\_dom}$	2.7	-	3.3	ms	B
11.100	Transmitted Recessive Bit Width on the Bus	$t_{B\_TXD} = 500\text{ ns}$ $R_L = 60\Omega$ , $C_2 = 100\text{ pF}$ , $C_{RXD} = 15\text{ pF}$	-	$t_{Bit(Bus)}$	435	-	530	ns	C
11.110		$t_{B\_TXD} = 200\text{ ns}$ $R_L = 60\Omega$ , $C_2 = 100\text{ pF}$ , $C_{RXD} = 15\text{ pF}$	-	$t_{Bit(Bus)}$	155	-	210	ns	A
11.120	CAN Activity Filter Time for Standard Remote Wake-up Pattern (WUP)	First pulse (after first recessive) and second pulse for wake-up on pins CANH and CANL, CAN TRX Standby	CANH, CANL	$t_{Filter}$	0.5	-	1.8	$\mu\text{s}$	A
11.130	Delay time from bus active to bias on	$R_L = 60\Omega$ ; $C_1 = 4.7\text{ nF}$ ; $C_2 = 0\text{ pF}$ (not present), $C_{RXD} = 0\text{ pF}$ (not present)	CANH, CANL	$t_{Bias}$	-	-	200	$\mu\text{s}$	C
11.140	Time-out Time for Bus Inactivity	Bus recessive time measurement started in all CAN modes; $R_L = 120\Omega$	CANH, CANL	$t_{Silence}$	0.95	-	1.17	s	B
11.150	CAN Start-up Time	When switching to CAN TRX Normal mode	CANH, CANL	$t_{TRX\_startup}$	-	-	220	$\mu\text{s}$	A
11.160	Event Capture Delay Time	CAN Standby mode	RXD	$t_{d\_evt\_cap}$	0.9	-	1.1	ms	B
11.170	Undervoltage detection filter time	-	VCC	$t_{UV\_VCC\_TRX\_debounce}$ , $t_{UV2Filter}$	6	-	54	$\mu\text{s}$	A
11.180	Debouncing time for detecting VCC interface undervoltage	-	VCC	$t_{UV\_VCC\_IO\_debounce}$	6	-	54	$\mu\text{s}$	A
11.181	Debouncing time for detecting VCC undervoltage	-	VCC	$t_{UV\_VCC\_debounce}$	6	-	54	$\mu\text{s}$	A
11.190	Start-up Time after Power On	From $V_{VS}$ rises above the power-on detection threshold $V_{VS\_PWRON}$ until pin $V_{VCC} > V_{VCC\_UV\_TRX\_Clear}$	VS	$t_{startup}$	-	-	1	ms	A

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
11.200	Standard Remote Wake-up Time-out Time	Between first and second dominant pulses, CAN Standby mode	-	tWake	900	-	1200	μs	B
11.210	Debouncing Time for Recessive Clamping State Detection	V(CANH-CANL) > 900 mV, RXD = high	RXD	tRXD_rec_clmp	60	90	175	ns	D
11.211	Reaction Time For RXD Recessive clamping detection to disable transmit	-	RXD/ CANH, CANL	tRXD_rec_clmp2	-	-	8	μs	D
11.220	Local Wake-up Time	-	WAKE	tlocal_wu	5	-	50	μs	A
11.221	Local Wake-up Time Wake2	-	WAKE2	tlocal_wu2	-	-	300	μs	D
11.230	Transmitter Resume Time	From TXD goes high to TX operates after TXD dominant timeout event detected	-	tTX_resume_TXDOUT	6	-	-	μs	D
11.240	Bus Recessive Clamping Detection Time	Bus recessive clamping detection time after TXD goes low	-	tbus_rec_clamp	1	-	-	μs	D
11.250	Debouncing time for detecting VCC_SENSOR undervoltage	-	VCC_SE NSOR	tUV_VCCSENS_deb	6	-	54	μs	A
11.260	Dominant time for wake up	V <sub>LIN</sub> = 0V	LIN	t <sub>bus</sub>	50	100	150	μs	A
11.270	TXD_LIN dominant time-out time	V <sub>TXD</sub> = 0V	TXD_LIN	t <sub>to(dom)_LIN</sub>	20	40	60	ms	A
11.280	Duty cycle 1	TH <sub>Rec(max)</sub> = 0.744×V <sub>VS</sub> TH <sub>Dom(max)</sub> = 0.581×V <sub>VS</sub> V <sub>VS</sub> = 7.0V to 18V t <sub>Bit</sub> = 50μs D1 = t <sub>bus_rec(min)</sub> /(2×t <sub>Bit</sub> )	LIN	D1	0.396	-	-	-	A
11.290	Duty cycle 2	TH <sub>Rec(min)</sub> = 0.422×V <sub>VS</sub> TH <sub>Dom(min)</sub> = 0.284×V <sub>VS</sub> V <sub>VS</sub> = 7.6V to 18V t <sub>Bit</sub> = 50μs D2 = t <sub>bus_rec(max)</sub> /(2×t <sub>Bit</sub> )	LIN	D2	-	-	0.581	-	A
11.300	Duty cycle 3	TH <sub>Rec(max)</sub> = 0.778×V <sub>VS</sub> TH <sub>Dom(max)</sub> = 0.616×V <sub>VS</sub> V <sub>VS</sub> = 7.0V to 18V t <sub>Bit</sub> = 96μs D1 = t <sub>bus_rec(min)</sub> /(2×t <sub>Bit</sub> )	LIN	D3	0.417	-	-	-	A
11.310	Duty cycle 4	TH <sub>Rec(min)</sub> = 0.389×V <sub>VS</sub> TH <sub>Dom(min)</sub> = 0.251×V <sub>VS</sub> V <sub>VS</sub> = 7.6V to 18V t <sub>Bit</sub> = 96μs D1 = t <sub>bus_rec(max)</sub> /(2×t <sub>Bit</sub> )	LIN	D4	-	-	0.590	-	A
11.330	TXD release time after dominant time-out detection	-	TXD_LIN	t <sub>DTOrel</sub>	10	-	20	μs	B
11.340	Propagation delay of receiver	Receiver Electrical AC Parameters of the LIN Physical Layer LIN Receiver, RXD Load Conditions: C <sub>RXD</sub> = 20pF, V <sub>VS</sub> = 7.0V to 18V, t <sub>rx_pd</sub> = max(trx_pdr, trx_pdf)	RXD_LIN	t <sub>rx_pd</sub>	-	-	6	μs	A

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
11.350	Symmetry of receiver propagation delay rising edge minus falling edge	Receiver Electrical AC Parameters of the LIN Physical Layer LIN Receiver, RXD Load Conditions: $C_{RXD} = 20\text{pF}$ , $V_{VS} = 7.0\text{V to } 18\text{V}$ , $t_{rx\_pd} = \max(t_{rx\_pdr}, t_{rx\_pdf})$ , $V_S = 7.0\text{V to } 18\text{V}$ $t_{rx\_sym} = t_{rx\_pdr} - t_{rx\_pdf}$	RXD_LIN	$t_{rx\_sym}$	-2	-	+2	$\mu\text{s}$	A
11.360	Watchdog long open window	-	-	$t_{LW}$	560	-	700	ms	B
11.370	Debouncing time for detecting VCC_SENSOR overvoltage	-	VCC_SE NSOR	$t_{OV\_VCCSENS\_deb}$	6	-	54	$\mu\text{s}$	A
11.380	Debouncing time for detecting VCC overvoltage	-	VCC	$t_{OV\_VCC\_deb}$	6	-	54	$\mu\text{s}$	A
<b>SPI Timing</b>									
12.10	Clock Cycle Time	Normal/Standby/Sleep mode	SPI	$t_{clk}$	250	-	-	ns	D
12.20	SPI Enable Lead Time	Normal/Standby/Sleep mode	SPI	$t_{EN\_Lead}$	50	-	-	ns	D
12.30	SPI Enable Lag Time	Normal/Standby/Sleep mode	SPI	$t_{EN\_Lag}$	50	-	-	ns	D
12.40	Clock High Time	Normal/Standby/Sleep mode	SPI	$t_{Clk\_H}$	125	-	-	ns	D
12.50	Clock Low Time	Normal/Standby/Sleep mode	SPI	$t_{Clk\_L}$	125	-	-	ns	D
12.60	Data Input Setup Time	Normal/Standby/Sleep mode	SPI	$t_{Setup}$	50	-	-	ns	D
12.70	Data Input Hold Time	Normal/Standby/Sleep mode	SPI	$t_{Hold}$	50	-	-	ns	D
12.80	Data Output Valid Time	Normal/Standby/Sleep mode	SPI	$t_{Dout\_v}$	-	-	65	ns	D
12.90	Chip Select Pulse Width High	Normal/Standby/Sleep mode, pin SDO, $C_L = 20\text{ pF}$	SPI	$t_{NCS\_pw}$	250	-	-	ns	D
<b>Overtemperature Prewarning</b>									
13.10	Overtemperature Protection Prewarning Threshold (Grade 1)	-	-	$T_{OT\_Prew\_1}$	120	-	145	$^{\circ}\text{C}$	B
13.20	Overtemperature Protection Prewarning Threshold (Grade 0)	-	-	$T_{OT\_Prew\_0}$	140	-	165	$^{\circ}\text{C}$	B
13.30	Overtemperature Protection Prewarning Hysteresis	-	-	$T_{OT\_hys}$	-	15	-	$^{\circ}\text{C}$	C
<b>VS2</b>									
1.7	VS2 undervoltage threshold (switching from normal to Fail-Safe mode)	Decreasing supply voltage	VS2	$V_{VS2\_th\_N\_F\_down}$	3.9	4.3	4.7	V	A
		Increasing supply voltage	VS2	$V_{VS2\_th\_F\_N\_up}$	4.1	4.6	4.9	V	A
1.8	VS2 undervoltage hysteresis	-	VS2	$V_{VS2\_hys\_F\_N}$	0.1	0.25	0.4	V	A
1.9	VS2 operating threshold (switching to Unpowered mode)	Switch to Unpowered mode	VS2	$V_{VS2\_th\_U\_down}$	1.9	2.05	2.3	V	A
		Switch from Unpowered to Fail-Safe mode	VS2	$V_{VS2\_th\_U\_up}$	2.0	2.25	2.5	V	A
1.10	VS2 undervoltage hysteresis	-	VS2	$V_{VS2\_hys\_U}$	0.1	0.2	0.3	V	A
<b>RXD_LIN2</b>									
2.1	Low-level output sink capability	Normal mode, $V_{LIN2} = 0\text{V}$ , $I_{RXD\_LIN2} = 2\text{mA}$	RXD_LIN2	$V_{RXD\_LIN2\_L}$	-	0.2	0.4	V	A
2.1	High-level output source capability	Normal mode, $V_{LIN2} = V_{VS2}$ , $I_{RXD\_LIN2} = 2\text{mA}$	RXD_LIN2	$V_{RXD\_LIN2\_H}$	$V_{VCC\_}\mu\text{C}-0.4$	$V_{VCC\_}\mu\text{C}-0.2$	-	V	A
<b>TXD_LIN2</b>									
3.1	Low-level voltage input	-	TXD_LIN2	$V_{TXD\_LIN2\_L}$	-0.3	-	+0.8	V	A
3.2	High-level voltage input	-	TXD_LIN2	$V_{TXD\_LIN2\_H}$	2	-	$V_{VCC\_}\mu\text{C}+0.3$	V	A

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3.3	Pull-up resistor	$V_{TXD\_LIN2} = 0V$	TXD_LIN2	RTXD_LIN2	40	70	100	k $\Omega$	A
3.4	High-level leakage current	$V_{TXD\_LIN2} = V_{VCC\_μC}$	TXD_LIN2	ITXD_LIN2	-3	-	+3	$\mu A$	A
3.7	Low-level output sink current at LIN2 wake-up request	Fail-Safe Mode $V_{LIN2} = V_{VS2}$ $V_{TXD\_LIN2} = 0.4V$	TXD_LIN2	ITXD_LIN2	2	2.5	8	mA	A
<b>EN_LIN2</b>									
4.1	Low-level voltage input	-	EN_LIN2	$V_{EN\_LIN2\_L}$	-0.3	-	+0.8	V	A
4.2	High-level voltage input	-	EN_LIN2	$V_{EN\_LIN2\_H}$	2	-		V	A
4.3	Pull-down resistor	$V_{EN\_LIN2} = V_{VCC\_μC}$	EN_LIN2	$R_{EN\_LIN2}$	50	125	200	k $\Omega$	A
4.4	Low-level input current	$V_{EN\_LIN2} = 0V$	EN_LIN2	$I_{EN\_LIN2}$	-3	-	+3	$\mu A$	A
<b>Internal Reset NRES_int LIN2</b>									
5.1	Low-level voltage input	$V_{VS\_LIN2} = 5.5V$	-	$t_{reset\_int\_LIN2}$	2	4	6	ms	B
5.2	Reset debounce time for falling edge	$V_{VS\_LIN2} = 5.5V$	-	$t_{res\_f}$	0.5	-	10	$\mu s$	D
<b>VCC_μC (3.3V)</b>									
8.1	Output Voltage	$4V < V_{VS2} < 18V$ (0 mA to 50 mA)	VCC_μC	$V_{VCC\_μC\_Vnor}$	3.234	-	3.366	V	A
		$4.5V < V_{VS2} < 18V$ (0 mA to 85 mA)	VCC_μC	$V_{VCC\_μC\_Vnor}$	3.234	-	3.366	V	B
8.2	Output Voltage $V_{VCC\_μC}$ at Low $V_{VS2}$	$3V < V_{VS2} < 4V$	VCC_μC	$V_{VCC\_μC\_low}$	$V_{VS2} - V_D$	-	3.366	V	A
8.3	Regulator DropVoltage	$V_{VS2} > 3V$ , $I_{VCC\_μC} = -15$ mA	VCC_μC	$V_{D1}$	-	100	150	mV	A
8.4	Regulator DropVoltage	$V_{VS2} > 3V$ , $I_{VCC\_μC} = -50$ mA	VCC_μC	$V_{D2}$	-	300	500	mV	A
8.5	Line Regulation Maximum	$4V < V_{VS2} < 18V$	VCC_μC	$V_{VCC\_μC\_line}$	-	-	0.2	%	A
8.6	Load Regulation Maximum	$5mA < I_{VCC\_μC} < 50mA$	VCC_μC	$V_{VCC\_μC\_load}$	-	-	0.5	%	A
8.7	Output CurrentLimitation	$V_{VS2} > 4V$	VCC_μC	$I_{VCC\_μC\_lim}$	-	-180	-120	mA	A
8.8	Load Capacitance	MLC capacitor	VCC_μC	$C_{load}$	3.5	4.7	-	$\mu F$	D
8.9	VCC_μC Undervoltage Threshold (NRES_int low)	Referred to VCC_μC $V_{VS2} > 4V$	VCC_μC	$V_{VCC\_μC\_th\_uv\_down}$	2.2	2.5	2.8	V	A
	VCC_μC Undervoltage Threshold (NRES_int high)	Referred to VCC_μC $V_{VS2} > 4V$	VCC_μC	$V_{VCC\_μC\_th\_uv\_up}$	2.4	2.6	2.9	V	A
8.10	Hysteresis of VCC_μC Undervoltage Threshold	$V_{VS2} > 4V$	VCC_μC	$V_{VCC\_μC\_hys\_uv}$	100	200	300	mV	A
8.11	Ramp-Up Time $V_{VS2} > 4V$ to $V_{VCC\_μC} = 2.8V$	$C_{VCC\_μC} > 3.5$ $\mu F$ $I_{load} = -5$ mA at VCC_μC	VCC_μC	$t_{VCC\_μC}$	-	1	1.5	ms	A
<b>VCC_μC (5.0V)</b>									
9.1	Output Voltage	$5.5V < V_{VS2} < 18V$ (0 mA to 50 mA)	VCC_μC	$V_{VCC\_μC\_Vnor}$	4.9	-	5.1	V	A
		$6V < V_{VS2} < 18V$ (0 mA to 85 mA)	VCC_μC	$V_{VCC\_μC\_Vnor}$	4.9	-	5.1	V	B
9.2	Output Voltage $V_{VCC\_μC}$ at Low $V_{VS2}$	$4V < V_{VS2} < 5.5V$	VCC_μC	$V_{VCC\_μC\_low}$	$V_{VS2} - V_D$	-	5.1	V	A
9.3	Regulator DropVoltage	$V_{VS2} > 4V$ , $I_{VCC\_μC} = -20$ mA	VCC_μC	$V_{D1}$	-	100	200	mV	A
9.4	Regulator DropVoltage	$V_{VS2} > 4V$ , $I_{VCC\_μC} = -50$ mA	VCC_μC	$V_{D2}$	-	300	500	mV	A
9.5	Regulator DropVoltage	$V_{VS2} > 3.3V$ , $I_{VCC\_μC} = -15$ mA	VCC_μC	$V_{D3}$	-	-	150	mV	A
9.6	Line Regulation Maximum	$5.5V < V_{VS2} < 18V$	VCC_μC	$V_{VCC\_μC\_line}$	-	-	0.2	%	A

.....continued

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9.7	Load Regulation Maximum	5mA < I <sub>VCC_μC</sub> < 50mA	VCC_μC	VCC_μC <sub>load</sub>	-	-	0.5	%	A
9.8	Output Current Limitation	V <sub>Vs2</sub> > 5.5V	VCC_μC	I <sub>VCC_μC_lim</sub>	-	-180	-120	mA	A
9.9	Load Capacitance	MLC capacitor	VCC_μC	C <sub>load</sub>	3.5	4.7	-	μF	D
9.10	VCC_μC Undervoltage Threshold (NRES_int low)	Referred to VCC_μC V <sub>Vs2</sub> > 5.5V	VCC_μC	V <sub>VCC_μC_th_uv_down</sub>	4.2	4.4	4.6	V	A
	VCC_μC Undervoltage Threshold (NRES_int high)	Referred to VCC_μC V <sub>Vs2</sub> > 5.5V	VCC_μC	V <sub>VCC_μC_th_uv_up</sub>	4.3	4.6	4.8	V	A
9.11	Hysteresis of VCC_μC Undervoltage Threshold	Referred to VCC_μC V <sub>Vs2</sub> > 5.5V	VCC_μC	V <sub>VCC_μC_hys_uv</sub>	100	200	300	mV	A
9.12	Ramp-Up Time V <sub>Vs2</sub> > 5.5V to V <sub>VCC_μC</sub> = 4.3V	C <sub>VCC_μC</sub> = 4.7 μF I <sub>load</sub> = -5 mA at VCC_μC	VCC_μC	t <sub>VCC_μC</sub>	-	1	1.5	ms	A
<b>LIN2 Bus Driver: Bus Load Conditions: Load 1 (small): 1 nF, 1 kΩ; Load 2 (large): 10 nF, 500Ω; C<sub>RXD_LIN2</sub> = 20 pF, Load 3 (medium): 6.8 nF, 660Ω characterized on samples 12.7 and 12.8 specifies the timing parameters for proper operation at 20 kb/s and 12.9 and 12.10 at 10.4 kb/s</b>									
10.1	Driver Recessive Output Voltage	Load1 / Load2	-	V <sub>BUSrec</sub>	0.9 * V <sub>Vs2</sub>	-	V <sub>Vs2</sub>	V	A
10.2	Driver Dominant Voltage	V <sub>Vs2</sub> = 7V, R <sub>load</sub> = 500Ω	-	V <sub>LoSUP</sub>	-	-	1.2	V	A
10.3	Driver Dominant Voltage	V <sub>Vs2</sub> = 18V, R <sub>load</sub> = 500Ω	-	V <sub>HiSUP</sub>	-	-	2	V	A
10.4	Driver Dominant Voltage	V <sub>Vs2</sub> = 7V, R <sub>load</sub> = 1000Ω	-	V <sub>LoSUP_1k</sub>	0.6	-	-	V	A
10.5	Driver Dominant Voltage	V <sub>Vs2</sub> = 18V, R <sub>load</sub> = 1000Ω	-	V <sub>HiSUP_1k</sub>	0.8	-	-	V	A
10.6	Pull-Up Resistor to V <sub>Vs2</sub>	The serial diode is mandatory.	-	R <sub>LIN2</sub>	20	30	47	kΩ	A
10.7	Voltage Drop at the Serial Diodes	In pull-up path with R <sub>LIN2</sub> I <sub>SerDiode</sub> = 10 mA	-	V <sub>SerDiode</sub>	0.4	-	1.0	V	D
10.8	LIN2 Current Limitation V <sub>BUS</sub> = V <sub>Bat_max</sub>	-	-	I <sub>BUS_LIM</sub>	40	120	200	mA	A
10.9	Input Leakage Current at the Receiver Including Pull-Up Resistor as Specified	Input leakage current driver off V <sub>BUS</sub> = 0V V <sub>Bat</sub> = 12V	-	I <sub>BUS_PAS_dom</sub>	-1	-0.35	-	mA	A
10.10	Leakage Current LIN2 Recessive	Driver off 8V < V <sub>Bat</sub> < 18V 8V < V <sub>BUS</sub> < 18V V <sub>BUS</sub> >= V <sub>Bat</sub>	-	I <sub>BUS_PAS_rec</sub>	-	10	20	μA	A
10.11	Leakage Current when Control Unit Disconnected from Ground. Loss of local ground must not affect communication in the residual network.	GND <sub>Device</sub> = V <sub>Vs2</sub> V <sub>Bat</sub> = 12V 0V < V <sub>BUS</sub> < 18V	-	I <sub>BUS_NO_gnd</sub>	-10	+0.5	+10	μA	A
10.12	Leakage Current at Disconnected Battery. Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.	V <sub>Bat</sub> disconnected V <sub>SUP_Device</sub> = GND 0V < V <sub>BUS</sub> < 18V	-	I <sub>BUS_NO_bat</sub>	-	0.1	2	μA	A
10.13	Capacitance on pin LIN2 to GND	-	-	C <sub>LIN2</sub>	-	-	20	pF	D
<b>LIN2 Bus Receiver</b>									
11.1	Center of Receiver Threshold	V <sub>BUS_CNT</sub> = (V <sub>th_dom</sub> + V <sub>th_rec</sub> )/2	-	V <sub>BUS_CNT</sub>	0.475 * V <sub>Vs2</sub>	0.5 * V <sub>Vs2</sub>	0.525 * V <sub>Vs2</sub>	V	A
11.2	Receiver Dominant State	V <sub>EN_LIN2</sub> = 5V/3.3V	-	V <sub>BUSdom</sub>	-27	-	0.4 * V <sub>Vs2</sub>	V	A
11.3	Receiver Recessive State	V <sub>EN_LIN2</sub> = 5V/3.3V	-	V <sub>BUSrec</sub>	0.6 * V <sub>Vs2</sub>	-	40	V	A

.....continued									
No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
11.4	Receiver Input Hysteresis	$V_{hys} = V_{th\_rec} - V_{th\_dom}$	-	$V_{BUShys}$	0.028 * $V_{VS2}$	0.1* $V_{VS2}$	0.175 * $V_{VS2}$	V	A
11.5	Pre-Wake Detection LIN2 High-Level Input Voltage	-	-	$V_{LIN2H}$	$V_{VS2} - 2$	-	$V_{VS2} + 0.3$	V	A
11.6	Pre-Wake Detection LIN2 Low-Level Input Voltage	Activates the LIN receiver	-	$V_{LIN2L}$	-27	-	$V_{VS2} - 3.3$	V	A
<b>Internal Timers LIN2 device</b>									
12.1	Dominant Time for Wake-Up via LIN2 Bus	$V_{LIN2} = 0V$	-	$t_{bus}$	50	100	150	$\mu s$	A
12.2	Time Delay for Mode Change from Fail-Safe into Normal Mode via EN_LIN2 Pin	$V_{EN\_LIN2} = 5V/3.3V$	-	$t_{norm}$	5	15	20	$\mu s$	A
12.3	Time Delay for Mode Change from Normal Mode to Sleep Mode via EN_LIN2 Pin	$V_{EN\_LIN2} = 0V$	-	$t_{d\_sleep}$	5	15	20	$\mu s$	A
12.4	Time Delay between EN_LIN2 and TXD_LIN2 for mode Change from Normal Mode to Sleep Mode	$V_{EN\_LIN2} = 0V$	-	$t_d$	-	-	3.2	$\mu s$	D
12.5	TXD Dominant Time-Out Time	$V_{TXD\_LIN2} = 0V$	-	$t_{to(dom)\_LIN2}$	20	40	60	ms	A
12.6	Time Delay for Mode Change from Silent Mode into Normal Mode via EN_LIN2 Pin	$V_{EN\_LIN2} = 5V/3.3V$	-	$t_{s\_n}$	5	15	40	$\mu s$	A
12.7	Duty Cycle 1	$TH_{Rec(max)} = 0.744 \times V_{VS}$ $TH_{Dom(max)} = 0.581 \times V_{VS}$ $V_{VS} = 7.0V$ to 18V $t_{Bit} = 50\mu s$ $D1 = t_{bus\_rec(min)}/(2 \times t_{Bit})$	LIN2	D1	0.396	-	-	-	A
12.8	Duty Cycle 2	$TH_{Rec(min)} = 0.422 \times V_{VS}$ $TH_{Dom(min)} = 0.284 \times V_{VS}$ $V_{VS} = 7.6V$ to 18V $t_{Bit} = 50\mu s$ $D2 = t_{bus\_rec(max)}/(2 \times t_{Bit})$	LIN2	D2	-	-	0.581	-	A
12.9	Duty Cycle 3	$TH_{Rec(max)} = 0.778 \times V_{VS}$ $TH_{Dom(max)} = 0.616 \times V_{VS}$ $V_{VS} = 7.0V$ to 18V $t_{Bit} = 96\mu s$ $D1 = t_{bus\_rec(min)}/(2 \times t_{Bit})$	LIN2	D3	0.417	-	-	-	A
12.10	Duty Cycle 4	$TH_{Rec(min)} = 0.389 \times V_{VS}$ $TH_{Dom(min)} = 0.251 \times V_{VS}$ $V_{VS} = 7.6V$ to 18V $t_{Bit} = 96\mu s$ $D1 = t_{bus\_rec(max)}/(2 \times t_{Bit})$	LIN2	D4	-	-	0.590	-	A
12.11	Slope Time Falling and Rising Edge at LIN2	$V_{VS2} = 7.0V$ to 18V	-	$V_{LIN2L}$	3.5	-	22.5	$\mu s$	A
<b>LIN2 device Receiver Electrical AC Parameters of the LIN2 Physical Layer LIN2 Receiver, RXD Load Conditions: <math>C_{RXD\_LIN2} = 20</math> pF</b>									
13.1	Propagation Delay of Receiver	$V_{VS2} = 7.0V$ to 18V $t_{rx\_pd} = \max(t_{rx\_pdr}, t_{rx\_pdf})$	-	$t_{rx\_pd}$	-	-	6	$\mu s$	A
13.2	Symmetry of Receiver Propagation Delay Rising Edge Minus Falling Edge	$V_{VS2} = 7.0V$ to 18V $t_{rx\_sym} = t_{rx\_pdr} - t_{rx\_pdf}$	-	$t_{rx\_sym}$	-2	-	+2	$\mu s$	A

.....continued

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
<b>Notes:</b>									
	• A = 100% tested								
	• B = 100% correlation tested								
	• C = Characterized on samples								
	• D = Design parameter								

Figure 5-1. CAN Transceiver Timing Diagram 1

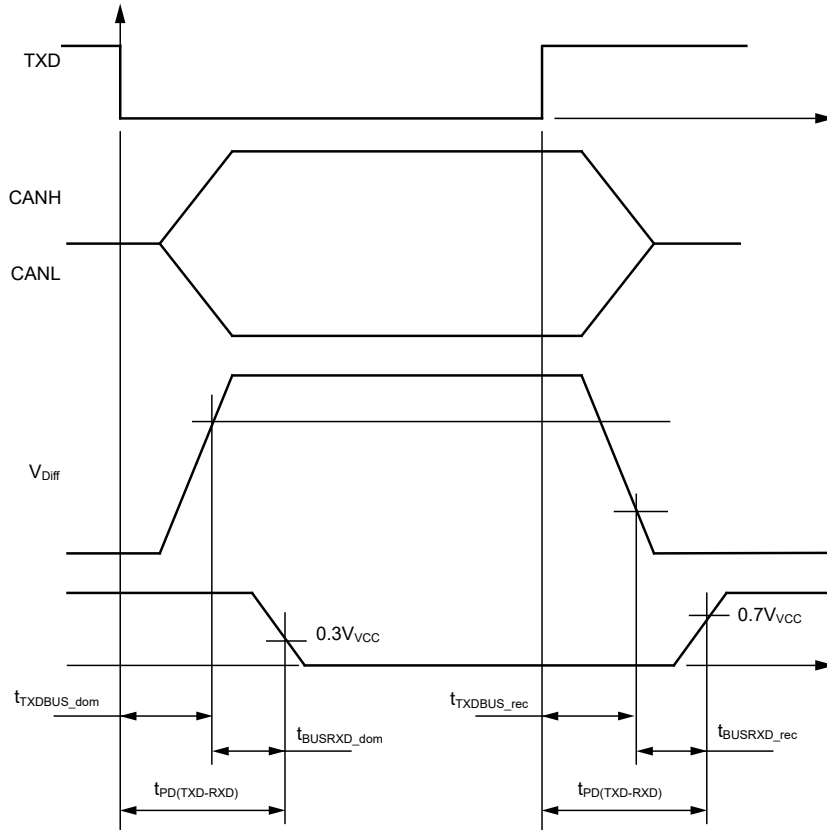
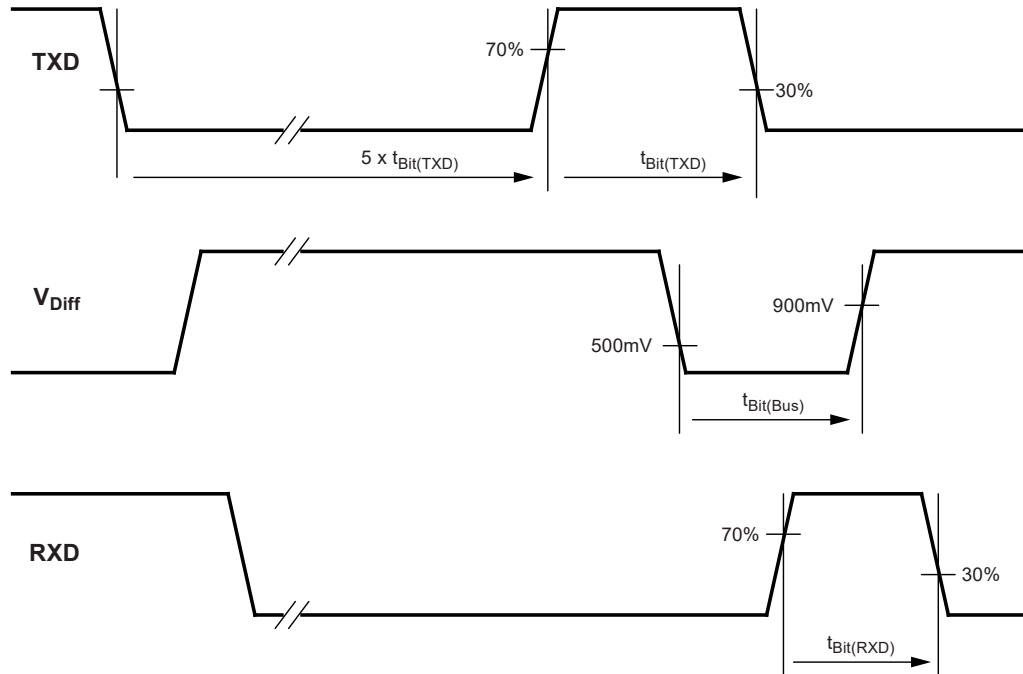




Figure 5-2. CAN Transceiver Timing Diagram 2



## 6. Application Circuits

Figure 6-1. Typical Application Circuit ATA6580 and ATA6585

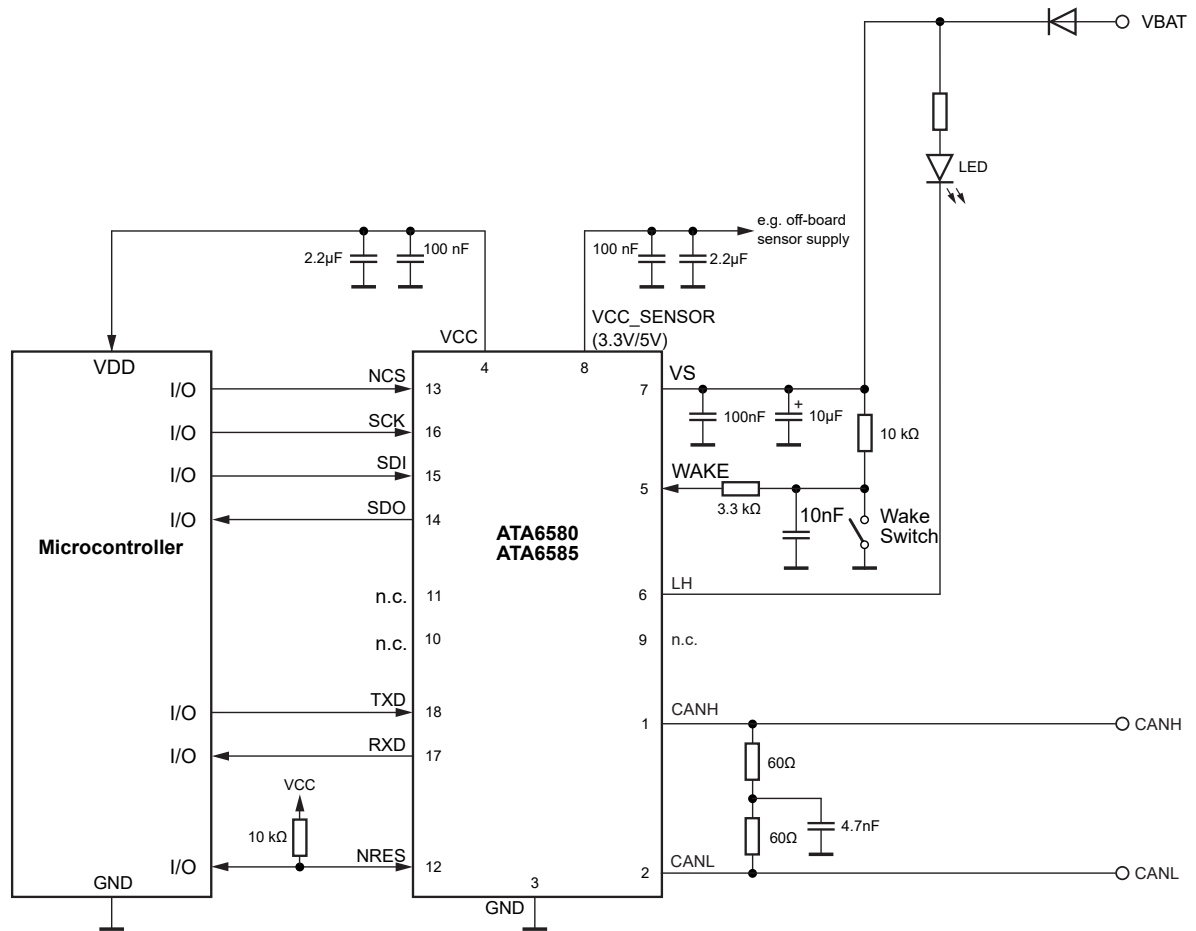


Figure 6-2. Typical Application Circuit ATA6581 and ATA6586

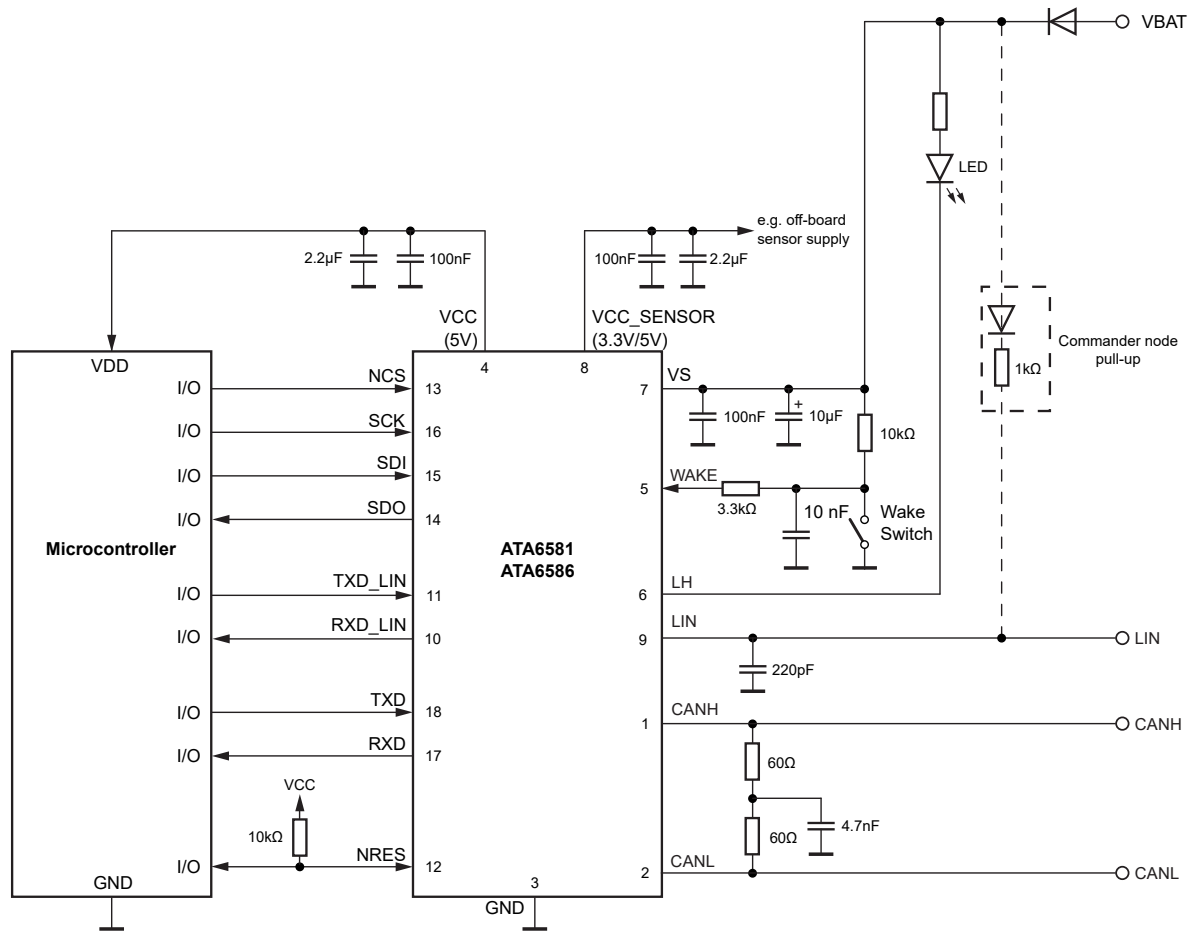


Figure 6-3. Typical Application Circuit ATA6582, ATA6583, ATA6587 and ATA6588

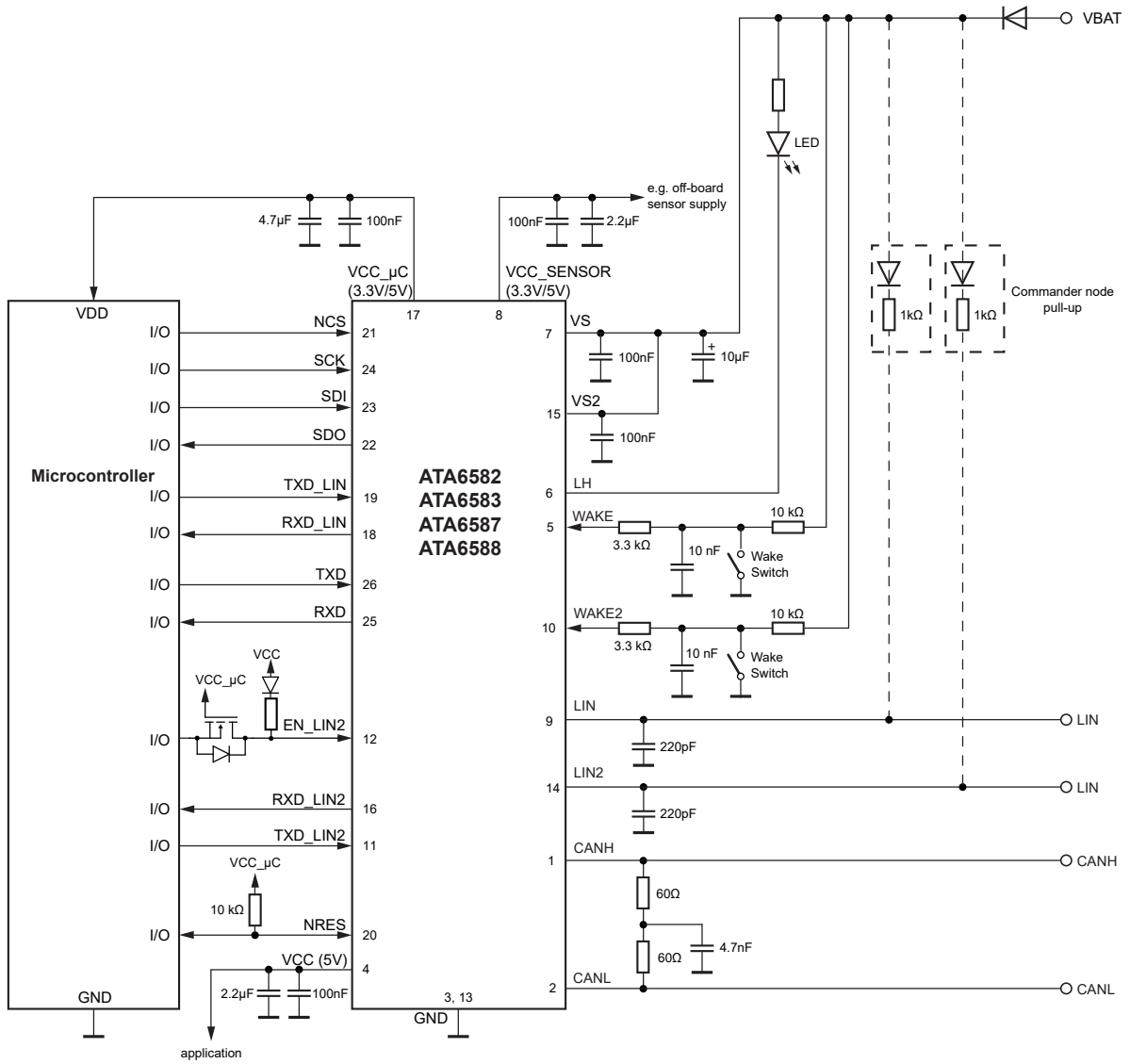
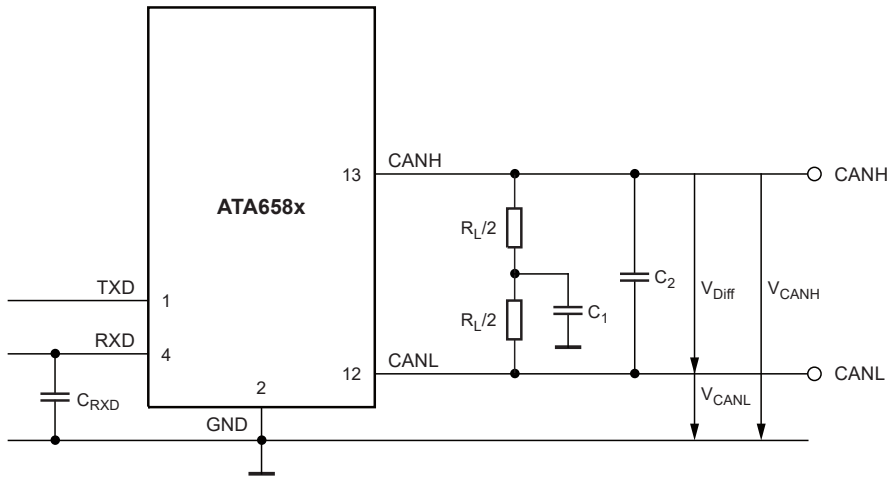


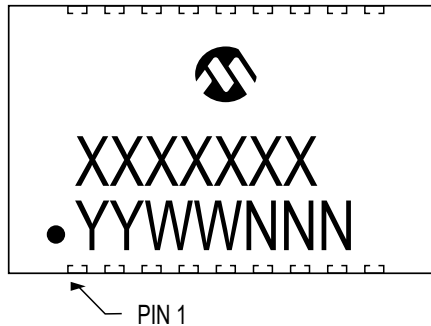
Figure 6-4. ATA658x Test Circuit



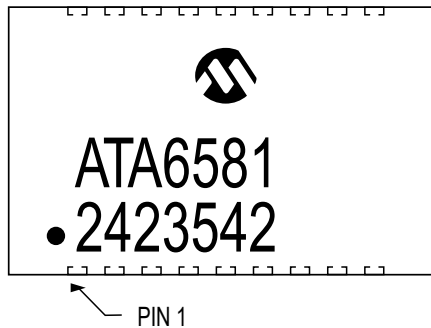
## 7. Package Information

### Package Marking Information

18-Lead 4.5x3mm VDFN

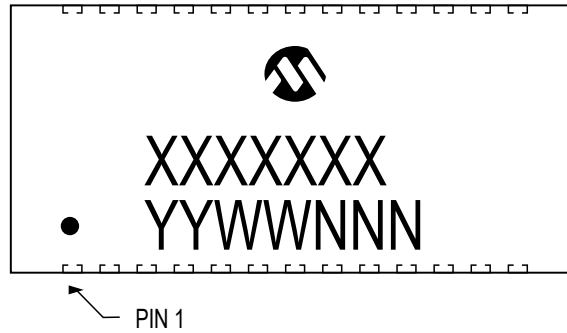


Example

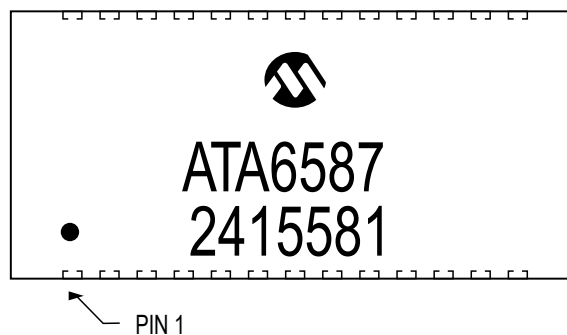


Legend:	XX...X	Customer specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last two digits of calendar year)
	WW	Week code (week of January 1st is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the other packaging for this package.
<p>Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.</p>		

26-Lead 6.5x3mm VDFN



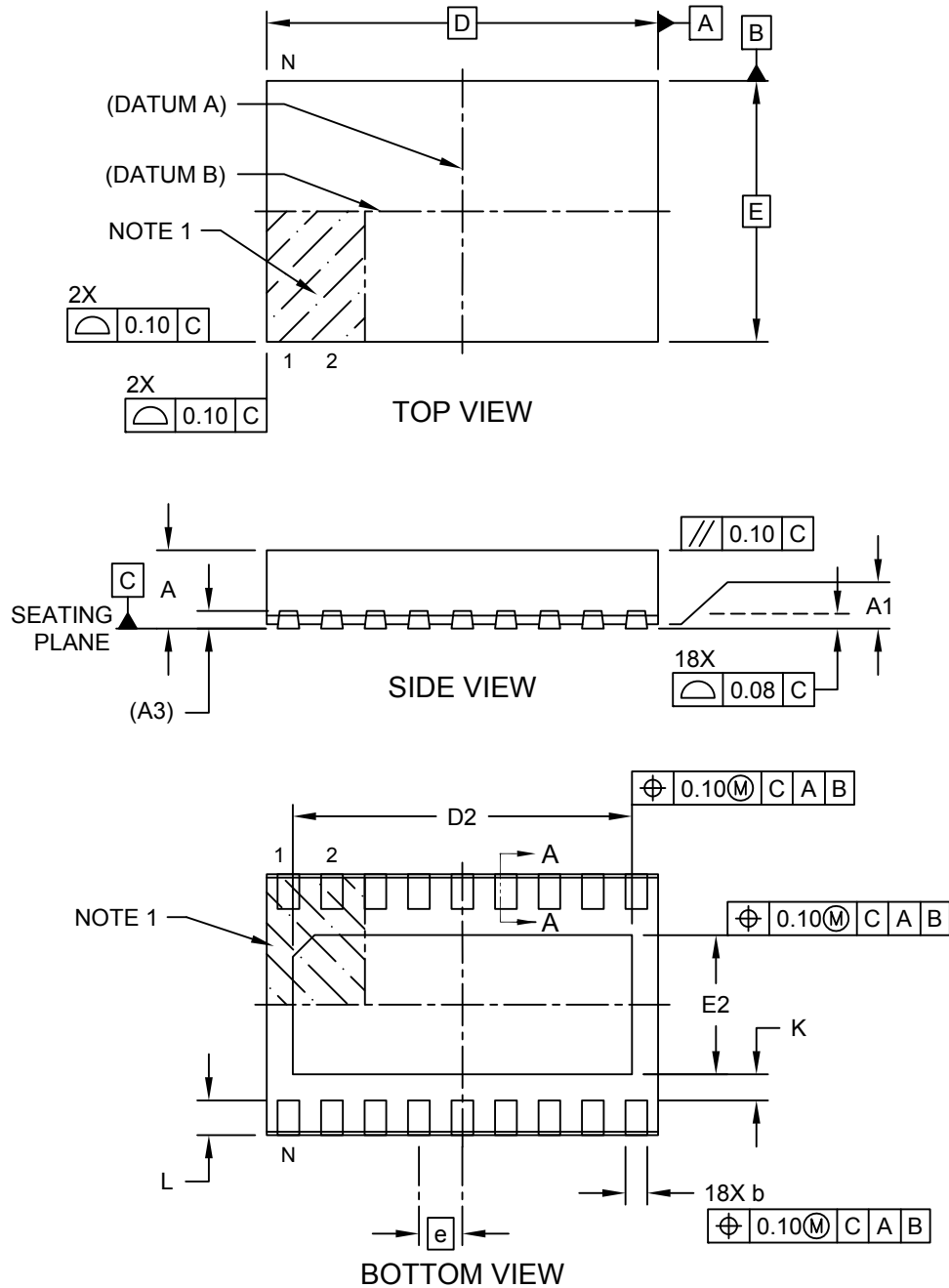
Example



Legend:	XX...X	Customer specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last two digits of calendar year)
	WW	Week code (week of January 1st is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the other packaging for this package.
<p>Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.</p>		

**18-Lead Very Thin Dual Flatpack No-Lead Package (QQB) 4.5x3 mm Body (VDFN)  
With Stepped Wettable Flanks**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

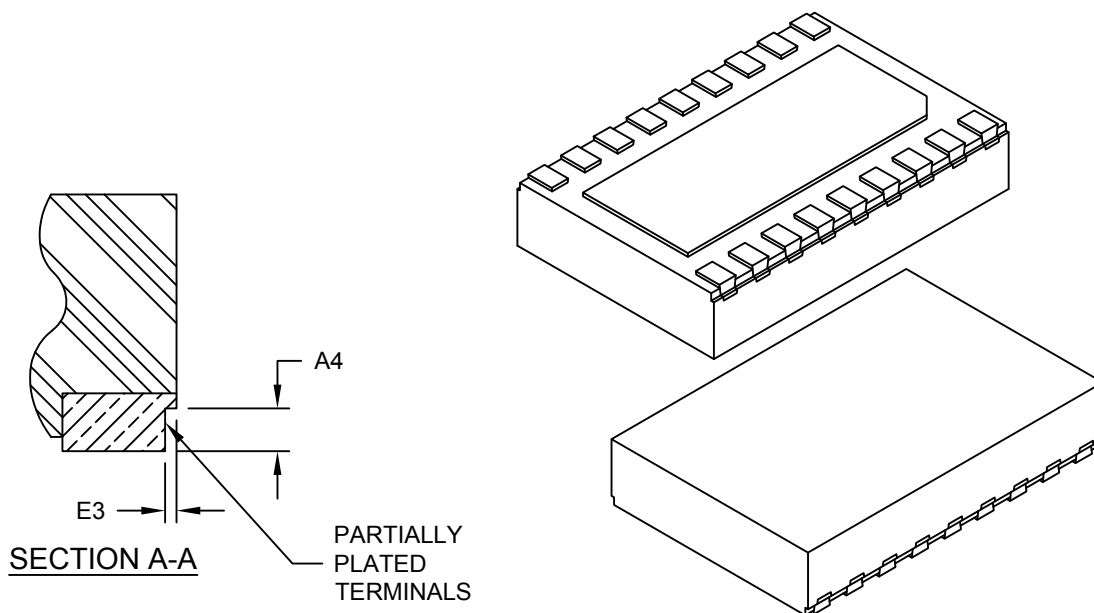


Microchip Technology Drawing C04-21458 Rev. B Sheet 1 of 2



## 18-Lead Very Thin Dual Flatpack No-Lead Package (QQB) 4.5x3 mm Body (VDFN) With Stepped Wettable Flanks

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	18		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.03	0.05
Terminal Thickness	A3	0.203 REF		
Overall Length	D	4.50 BSC		
Exposed Pad Length	D2	3.80	3.90	4.00
Overall Width	E	3.00 BSC		
Exposed Pad Width	E2	1.50	1.60	1.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step	A4	0.10	-	0.19
Wettable Flank Step	E3	-	-	0.085

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M

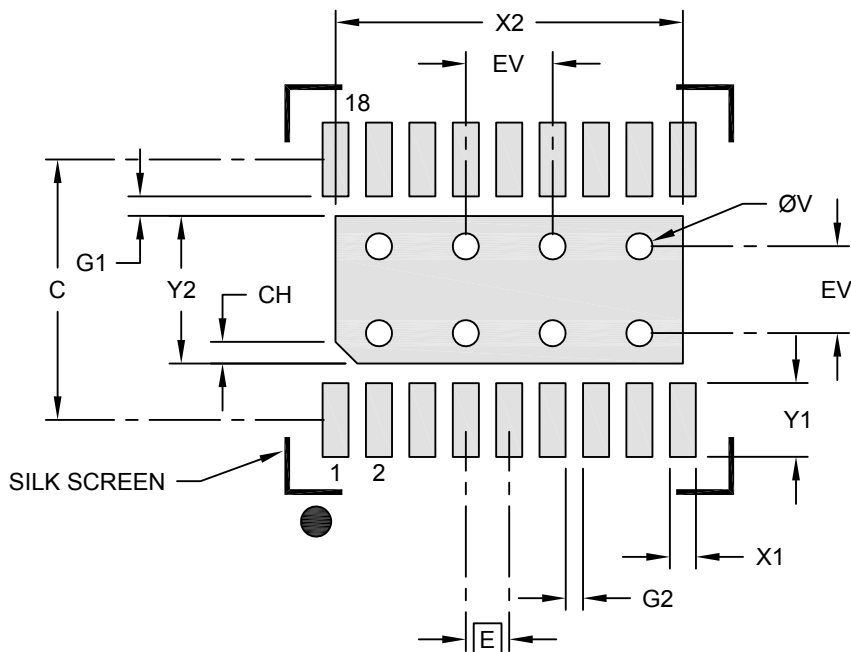
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21458 Rev. B Sheet 2 of 2

### 18-Lead Very Thin Dual Flatpack No-Lead Package (QQB) 4.5x3 mm Body (VDFN) With Stepped Wettable Flanks

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



#### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			4.00
Optional Center Pad Length	Y2			1.70
Contact Pad Spacing	C		3.00	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.85
Pin 1 Index Chamfer	CH		0.25	
Contact Pad to Center Pad (X18)	G1	0.20		
Contact Pad to Contact Pad (X16)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

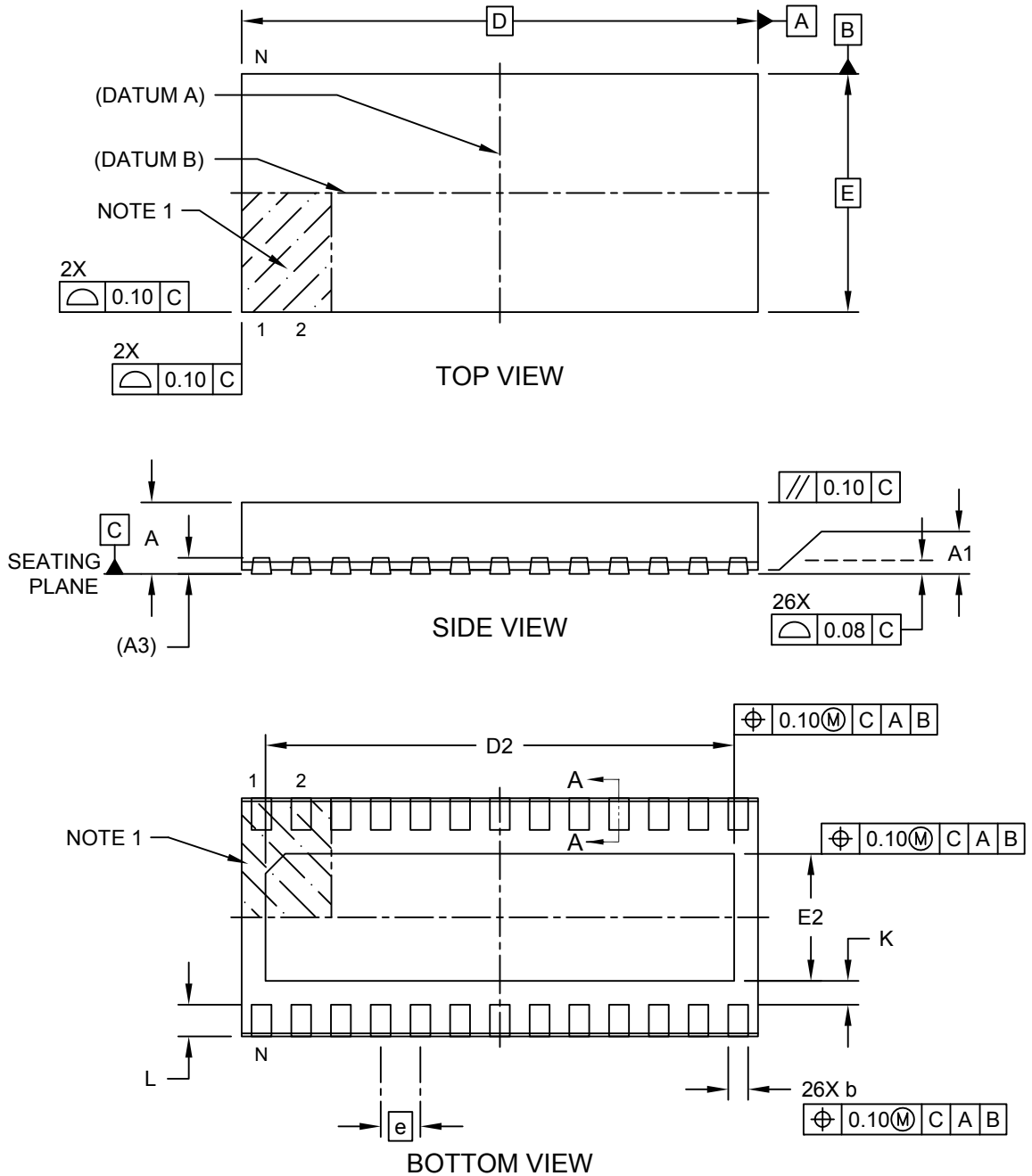
**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23458 Rev. B

## 26-Lead Very Thin Dual Flatpack No-Lead Package (QRB) 6.5x3 mm Body (VDFN) With Stepped Wettable Flanks

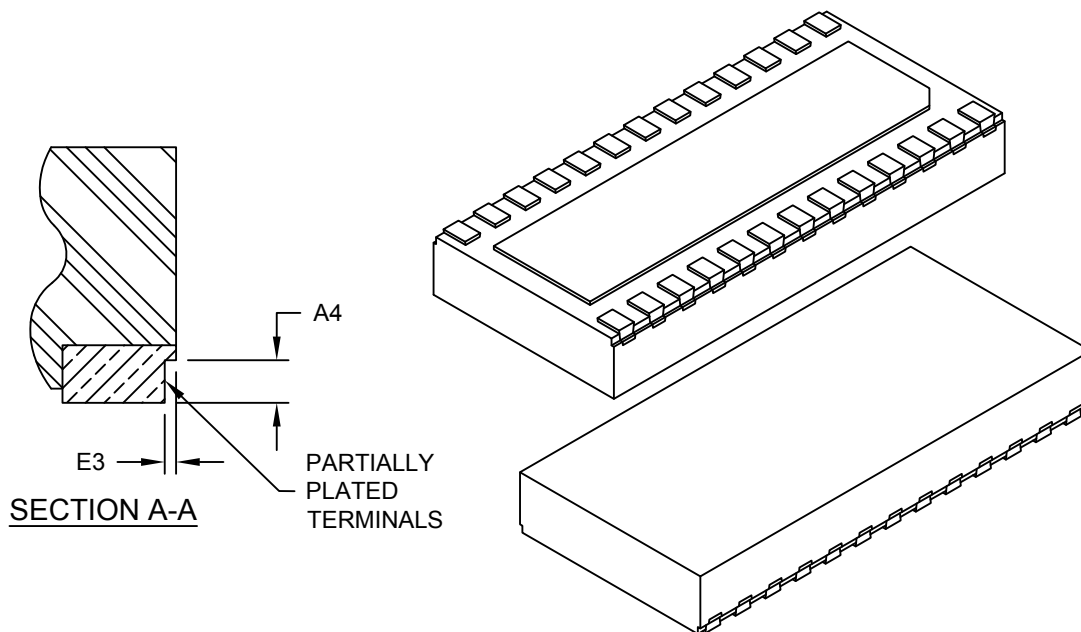
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-21459 Rev. B Sheet 1 of 2

## 26-Lead Very Thin Dual Flatpack No-Lead Package (QRB) 6.5x3 mm Body (VDFN) With Stepped Wettable Flanks

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	26		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.03	0.05
Terminal Thickness	A3	0.203 REF		
Overall Length	D	6.50 BSC		
Exposed Pad Length	D2	5.80	5.90	6.00
Overall Width	E	3.00 BSC		
Exposed Pad Width	E2	1.50	1.60	1.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step	A4	0.10	-	0.19
Wettable Flank Step	E3	-	-	0.085

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M

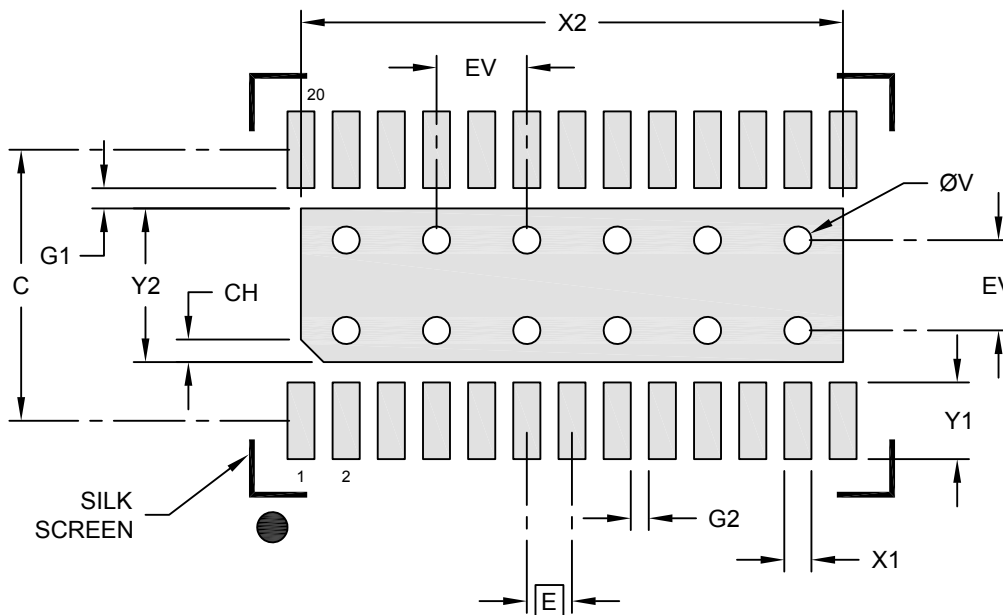
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21459 Rev. B Sheet 2 of 2

## 26-Lead Very Thin Dual Flatpack No-Lead Package (QRB) 6.5x3 mm Body (VDFN) With Stepped Wettable Flanks

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			6.00
Optional Center Pad Length	Y2			1.70
Contact Pad Spacing	C	3.00		
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.85
Pin 1 Index Chamfer	CH	0.25		
Contact Pad to Center Pad (X26)	G1	0.20		
Contact Pad to Contact Pad (X24)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

**Notes:**

- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23459 Rev. B

## 8. Revision History

### Revision B (March 2024)

- Corrected package size in Chapter [1. Pin Configuration](#).
- Corrected part number in Chapter [4. Thermal Characteristics](#).
- Added clarification about the first byte of SPI transfers in Chapter [2.14.1. General](#).
- Editorial Changes

### Revision A (February 2024)

Original release of this document.

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- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
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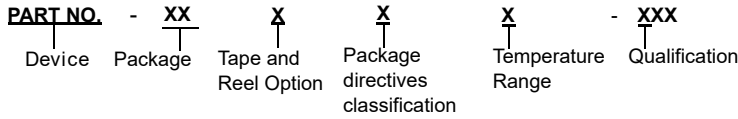
- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: [www.microchip.com/support](http://www.microchip.com/support)

## Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Device:	ATA658x	
Package:	GT	VDFN18
	GU	VDFN26
Tape and Reel option:	Q	330 mm diameter Tape and Reel <sup>(1)</sup>
Package directives classification:	W	Package according to RoHS <sup>(3)</sup>
Temperature range:	0	Temperature Grade 0 (-40°C to +150°C)
	1	Temperature Grade 1 (-40°C to +125°C)
Qualification	VAO	Standard Automotive Part

### Examples:

- ATA6580-GTQW0-VAO: CAN transceiver without selective wake-up, CAN FD capable, VCC=5V, VCC\_SENSOR=5V/3.3V, Grade0
- ATA6580-GTQW1-VAO: CAN transceiver without selective wake-up, CAN FD capable, VCC=5V, VCC\_SENSOR=5V/3.3V, Grade1
- ATA6581-GTQW0-VAO: LIN transceiver, CAN transceiver without selective wake-up, CAN FD capable, VCC=5V, VCC\_SENSOR=5V/3.3V, Grade0
- ATA6581-GTQW1-VAO: LIN transceiver, CAN transceiver without selective wake-up, CAN FD capable, VCC=5V, VCC\_SENSOR=5V/3.3V, Grade1
- ATA6582-GUQW1-VAO: CAN transceiver without selective wake-up, CAN FD capable, 2 LIN transceivers, VCC=5V, VCC\_SENSOR=5V/3.3V, VCC\_μC=5V, Grade1
- ATA6583-GUQW1-VAO: CAN transceiver without selective wake-up, CAN FD capable, 2 LIN transceivers, VCC=5V, VCC\_SENSOR=5V/3.3V, VCC\_μC=3.3V, Grade1
- ATA6585-GTQW0-VAO: CAN transceiver with selective wake-up, CAN FD capable, VCC=5V, VCC\_SENSOR=5V/3.3V, Grade0
- ATA6585-GTQW1-VAO: CAN transceiver with selective wake-up, CAN FD capable, VCC=5V, VCC\_SENSOR=5V/3.3V, Grade1
- ATA6586-GTQW0-VAO: LIN transceiver, CAN transceiver with selective wake-up, CAN FD capable, VCC=5V, VCC\_SENSOR=5V/3.3V, Grade0
- ATA6586-GTQW1-VAO: LIN transceiver, CAN transceiver with selective wake-up, CAN FD capable, VCC=5V, VCC\_SENSOR=5V/3.3V, Grade1
- ATA6587-GUQW1-VAO: CAN transceiver with selective wakeup, CAN FD capable, 2 LIN transceivers, VCC=5V, VCC\_SENSOR=5V/3.3V, VCC\_μC=5V, Grade1
- ATA6588-GUQW1-VAO: CAN transceiver with selective wakeup, CAN FD capable, 2 LIN transceivers, VCC=5V, VCC\_SENSOR=5V/3.3V, VCC\_μC=3.3V, Grade1



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