APPLICATION NOTE

ATA6620, ATA6620N, ATA6623, ATA6623C, ATA6625, ATA6625C Development Board

ATA6620/23/25

Introduction

The development board for the Atmel® ATA6620/23/25 (ATA6620-EK, ATA6623-EK, ATA6625-EK) is designed to give designers a quick start with these ICs and for the prototyping and testing of new LIN designs.

The Atmel ATA6620 and the Atmel ATA6625 are fully integrated LIN transceivers including a low-drop voltage regulator providing 5V/85mA. The only difference between the two parts is the improved EMC behavior of the Atmel ATA6625. The Atmel ATA6623 is pin and function compatible with the Atmel ATA6620/25, but on the Atmel ATA6623 the voltage at the regulator's output is 3.3V instead of 5V. The combination of LIN transceiver and voltage regulator makes it possible to develop simple, powerful, and cheap slave nodes in LIN bus systems.

The ICs are designed to handle the low-speed data communication in vehicles, for example in convenience electronics. Improved slope control at the LIN-driver ensures secure data communication up to 20Kbaud.

Besides normal mode there are two other modes, sleep mode and silent mode, which give the designer the opportunity to create modules which meet the different requirements of the application with respect to low current consumption.

This document has been developed to give the user a quick start using the development board for the Atmel ATA6620/23/25. For more detailed information about the devices themselves, refer to the corresponding datasheets.

Figure 1. Atmel ATA6620/23/25 Development Board

Development Board Features

The development board for the Atmel® ATA6620/23/25 supports the following features:

- All components necessary for all three circuits are mounted
- All pins are easily accessible
- Can be used for master or slave operation
- One board for three devices

Quick Start

The development board for the Atmel ATA6620/23/25 is shipped with all necessary components to start the development of a LIN slave node immediately.

Connecting an external 12V DC power supply with the terminals VBAT and GND puts the Atmel ATA6620/23/25 in pre-normal mode, where a 5V (3.3V) DC voltage provided by the internal voltage regulator can be measured between VCC and GND. In addition, the following voltages can be measured at the pins RXD and LIN:

Table 1. Quick Start

	ATA6620	ATA6623	ATA6625			
	VCC	VCC	VCC	RXD	LIN	Transceiver
Pre-normal mode	5V	3.3V	5V	High	Recessive	Off
Normal mode	5V	3.3V	5V	High	Recessive	On

Note that the communication is still inactive during pre-normal mode.

In order to communicate via the LIN bus interface you have to switch to normal mode by applying the VCC voltage (5V or 3.3V, as appropriate) at pin EN.

1. Hardware Description

In the following chapters only the normal operating conditions will be described. For specific information concerning one of the mentioned features, refer to the corresponding datasheet.

1.1 Power Supply (VBAT and GND)

In order to get the development board running, an external 5.7V to 18V DC power supply is required between the terminals VBAT and GND. The input circuit is protected against inverse polarity by the protection diode D1, so that there is a difference of approximately 0.7V between the VBAT and VS levels.

1.2 Voltage Regulator (VCC)

The internal 5V (3.3V, as appropriate) low-drop voltage regulator is capable of driving loads with up to 85mA. This makes it possible to supply a microcontroller, sensors and/or other ICs. The voltage regulator is protected against overloads by means of current limitation and overtemperature shut-down. In addition, the output voltage is monitored and will cause a reset signal at pin NRES if it drops below the under-voltage threshold.

1.3 LIN Interface (LIN, TXD and RXD)

1.3.1 Bus Pin (LIN)

A low-side driver with internal current limitation and thermal shutdown and an internal pull-up resistor in compliance with the LIN specification 2.0 is implemented. LIN receiver thresholds are compatible with the LIN protocol specification.

At the LIN pin there is a 220-pF capacitor to ground on the board. There is the possibility of additionally mounting the two extra components diode D2 (LL4148) in series with resistor R1 (1kΩ) on the board at their designated placeholders, necessary when using the development board for a LIN master application.

1.3.2 Input Pin (TXD)

This pin is the microcontroller interface to control the state of the LIN output. TXD must be pulled to ground in order to have the LIN bus low. If TXD is high, the LIN output transistor is turned off and the bus is in the recessive state, pulled up by the internal resistor. If TXD is low, the LIN output transistor is turned on and the bus is in the dominant state. An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD is forced to low longer than t_{DOM} > 20ms, the LIN bus driver is switched to the recessive state.

1.3.3 Output Pin (RXD)

This pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is reported by a high level at RXD, LIN low (dominant state) is reported by a low level at RXD. The output has an internal pull-up structure with typ. 5kΩ resistance to VCC and is short circuit protected.

1.4 Undervoltage Reset Output (NRES)

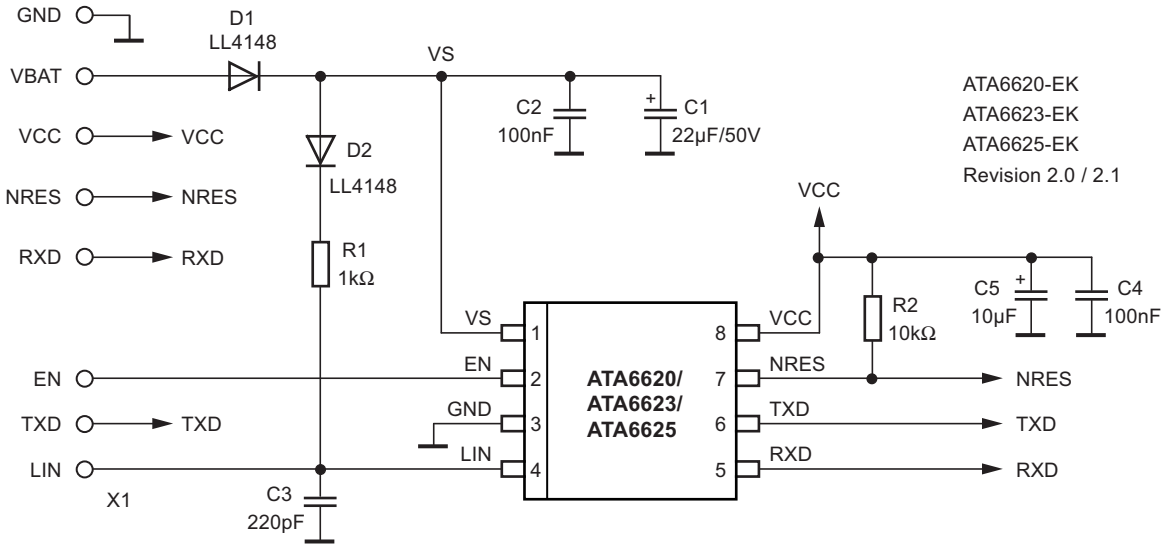
In the Atmel® ATA6620, the Reset output is a push-pull stage supplied by the VCC voltage. If the VCC voltage falls below the undervoltage threshold, NRES switches to LOW after a debounce time of approximately 2µs. The implemented undervoltage delay keeps NRES at a low level for approximately 10ms after VCC reaches its nominal value.

In the Atmel ATA6623 and Atmel ATA6625, the Reset output is an open-drain output implemented using a single MOS transistor which is switched on in the case of a VCC undervoltage. In order to pull up the output of the Atmel ATA6623/25, an external resistor connected to VCC is necessary. Space for this resistor (R2) is available on the development board.

If a reset occurs (NRES is low), the circuit switches to pre-normal mode.

2. Schematic and Layout of the Development Board for the Atmel ATA6620/23/25

Figure 2-1. Schematic of the Development Board for the Atmel ATA6620/23/25



Notes: 1. D2 and R1 are only necessary for a master node.
2. R2 is only needed for Atmel ATA6623 and Atmel ATA6625.

Figure 2-2. Board Component Placement; Top Side, Top View

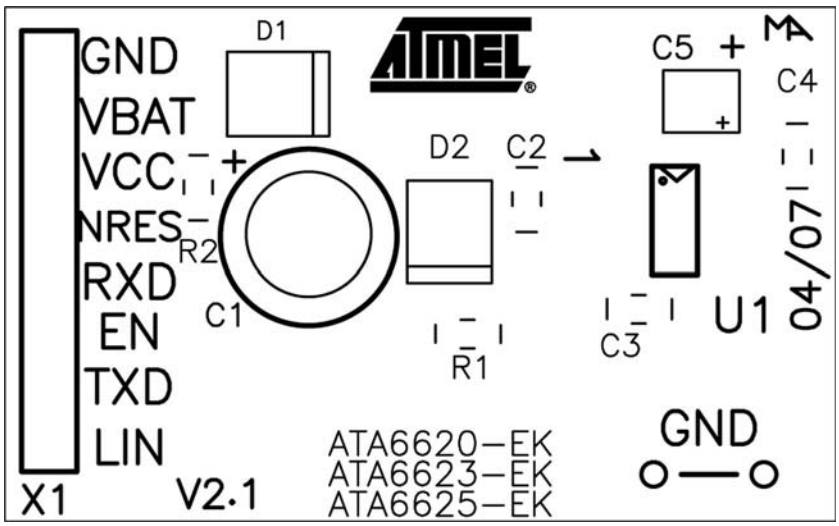


Figure 2-3. Atmel ATA6620/23/25 Development Board; Top Side, Top View

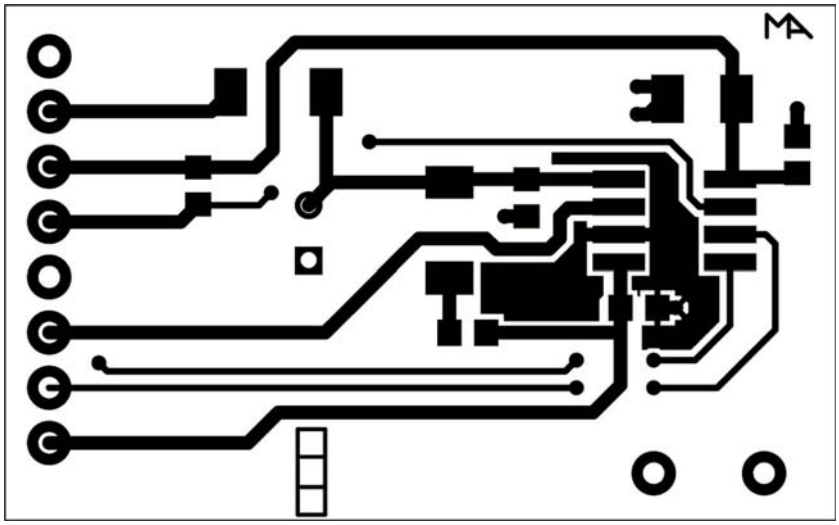
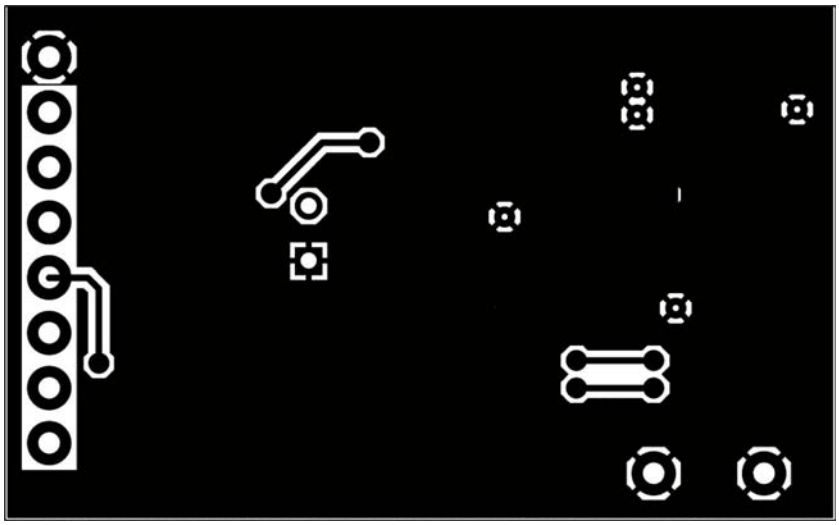


Figure 2-4. Atmel ATA6620/23/25 Development Board; Bottom Side, Top View (as if PCB Were Transparent)



3. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4969C-AUTO-07/15	• Put document in the latest template

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