

## Features

- Transparent RF receiver ICs for 315MHz (Atmel® ATA8201) and 433.92MHz (Atmel ATA8202) with high receiving sensitivity
- Fully integrated PLL with low phase noise VCO, PLL, and loop filter
- High FSK/ASK sensitivity:
  - -105dBm (Atmel ATA8201, FSK, 9.6Kbits/s, Manchester, BER  $10^{-3}$ )
  - -114dBm (Atmel ATA8201, ASK, 2.4Kbits/s, Manchester, BER  $10^{-3}$ )
  - -104dBm (Atmel ATA8202, FSK, 9.6Kbits/s, Manchester, BER  $10^{-3}$ )
  - -113dBm (Atmel ATA8202, ASK, 2.4Kbits/s, Manchester, BER  $10^{-3}$ )
- Supply current: 6.5mA in Active Mode (3V, 25°C, ASK Mode)
- Data rate: 1Kbit/s to 10Kbits/s Manchester ASK, 1Kbit/s to 20Kbits/s Manchester FSK with four programmable bit rate ranges
- Switching between modulation types ASK/FSK and different data rates possible in  $\leq 1$ ms typically, without hardware modification on board to allow different modulation schemes
- Low standby current: 50 $\mu$ A at 3V, 25°C
- ASK/FSK receiver uses a low-IF architecture with high selectivity, blocking, and low intermodulation (typical 3-dB blocking 68.0dBC at  $\pm 3$ MHz/74.0dBC at  $\pm 20.0$ MHz, system I1dBCP = -31dBm/system IIP3 = -24dBm)
- Telegram pause up to 52ms supported in ASK Mode
- Wide bandwidth AGC to handle large out-of-band blockers above the system I1dBCP
- 440-kHz IF frequency with 30-dB image rejection and 420-kHz IF bandwidth to support PLL transmitters with standard crystals or SAW-based transmitters
- RSSI (received signal strength indicator) with output signal dynamic range of 65dB
- Low in-band sensitivity change of typically  $\pm 2.0$ dB within  $\pm 160$ -kHz center frequency change in the complete temperature and supply voltage range
- Sophisticated threshold control and quasi-peak detector circuit in the data slicer
- Fast and stable XTO start-up circuit ( $> -1.4$  k $\Omega$  worst-case start impedance)
- Clock generation for microcontroller
- ESD protection at all pins ( $\pm 4$ kV HBM,  $\pm 200$ V MM,  $\pm 500$ V FCDM)

- Dual supply voltage range: 2.7V to 3.3V or 4.5V to 5.5V
- Temperature range: –40°C to +85°C
- Small 5mm × 5mm QFN24 package

## Applications

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- Industrial/aftermarket keyless entry and tire pressure monitoring systems
- Alarm, telemetering and energy metering systems
- Remote control systems for consumer and industrial markets
- Access control systems
- Home automation
- Home entertainment
- Toys

## Benefits

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- Supports header and blanking periods of protocols common in RKE and TPM systems (up to 52ms in ASK Mode)
- All RF relevant functions are integrated. The single-ended RF input is suited for easy adaptation to  $\lambda / 4$  or printed-loop antennas
- Allows a low-cost application with only 8 passive components
- Optimal bandwidth maximizes sensitivity while maintaining SAW transmitter compatibility
- Clock output provides an external microcontroller crystal-precision time reference
- Well suited for use with Atmel® PLL transmitter ATA8401/ATA8402/ATA8403/ATA8404/ATA8405

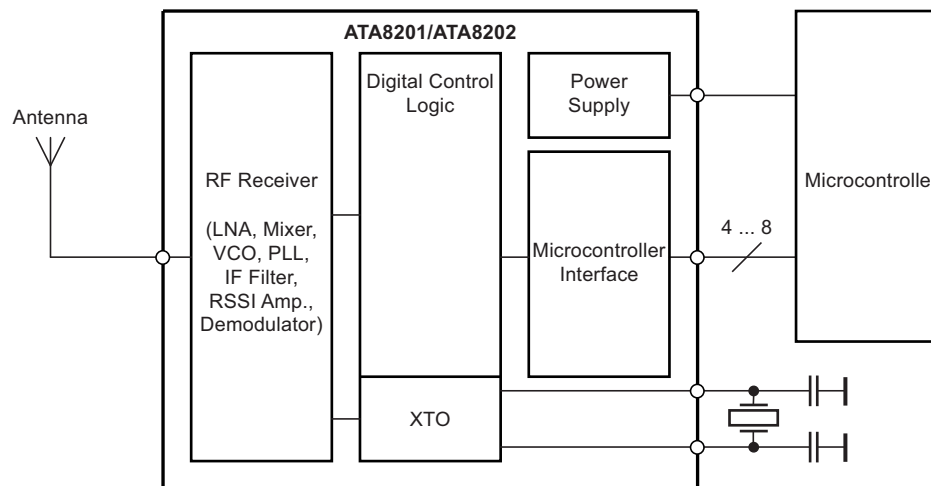
## 1. General Description

The Atmel® ATA8201/ATA8202 is a UHF ASK/FSK transparent receiver IC with low power consumption supplied in a small QFN24 package (body 5mm × 5mm, pitch 0.65mm). Atmel ATA8202 is used in the 433MHz to 435MHz band of operation, and Atmel ATA8201 in 313MHz to 317MHz.

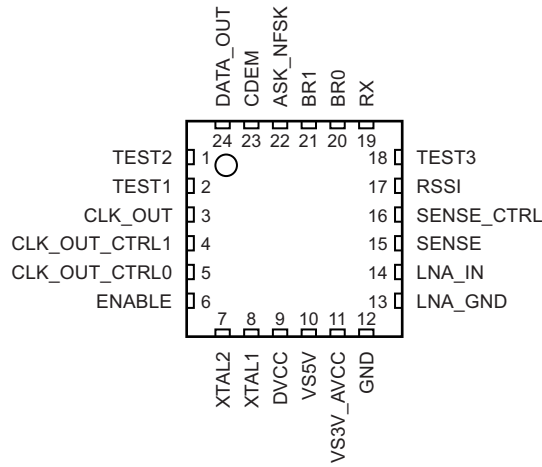
For improved image rejection and selectivity, the IF frequency is fixed to 440kHz. The IF block uses an 8th-order band pass yielding a receive bandwidth of 420kHz. This enables the use of the receiver in both SAW- and PLL-based transmitter systems utilizing various types of data-bit encoding such as pulse width modulation, Manchester modulation, variable pulse modulation, pulse position modulation, and NRZ. Prevailing encryption protocols such as Keeloq® are easily supported due to the receiver's ability to hold the current data slicer threshold for up to 52ms when incoming RF telegrams contain a blanking interval. This feature eliminates erroneous noise from appearing on the demodulated data output pin, and simplifies software decoding algorithms. The decoding of the data stream must be carried out by a connected microcontroller device. Because of the highly integrated design, the only required RF components are for the purpose of receiver antenna matching.

Atmel ATA8201 and Atmel ATA8202 support Manchester bit rates of 1Kbit/s to 10Kbits/s in ASK and 1Kbit/s to 20Kbits/s in FSK mode. The four discrete bit rate passbands are selectable and cover 1.0Kbit/s to 2.5Kbits/s, 2.0Kbits/s to 5.0Kbits/s, 4.0Kbits/s to 10.0Kbits/s, and 8.0Kbits/s to 10.0Kbits/s or 20.0Kbits/s (for ASK or FSK, respectively). The receiver contains an RSSI output to provide an indication of received signal strength and a SENSE input to allow the customer to select a threshold below which the DATA signal is gated off. ASK/FSK and bit rate ranges are selected by the connected microcontroller device via pins ASK\_NFSK, BR0, and BR1.

**Figure 1-1. System Block Diagram**



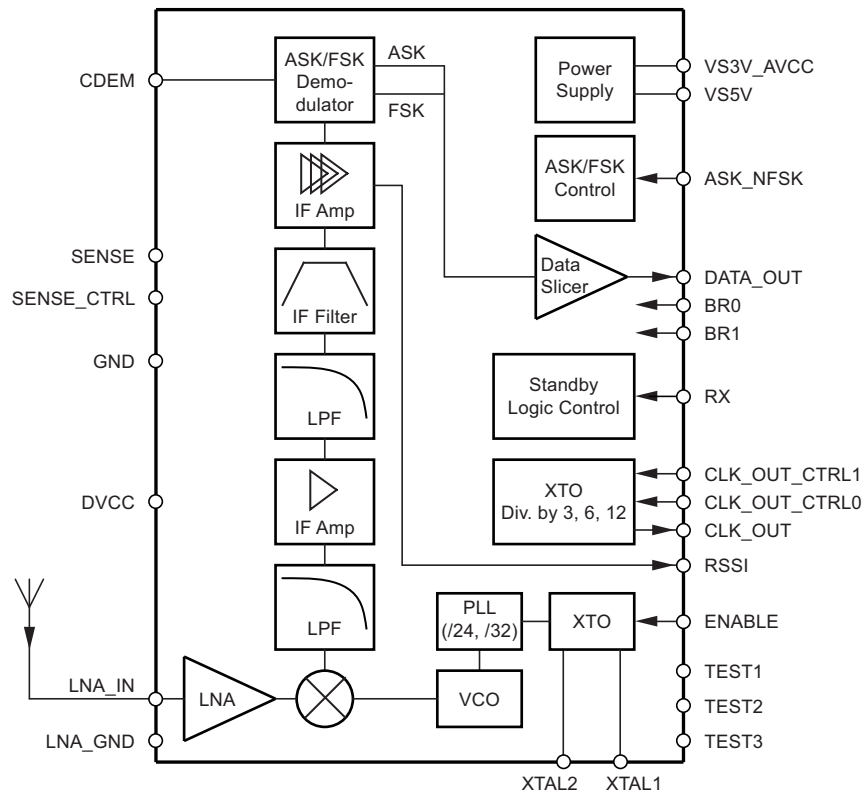
**Figure 1-2. Pinning QFN24**



**Table 1-1. Pin Description**

Pin	Symbol	Function
1	TEST2	Test pin, during operation at GND
2	TEST1	Test pin, during operation at GND
3	CLK_OUT	Output to clock a connected microcontroller
4	CLK_OUT_CTRL1	Input to control CLK_OUT (MSB)
5	CLK_OUT_CTRL0	Input to control CLK_OUT (LSB)
6	ENABLE	Input to enable the XTO
7	XTAL2	Reference crystal
8	XTAL1	Reference crystal
9	DVCC	Digital voltage supply blocking
10	VS5V	Power supply input for voltage range 4.5V to 5.5V
11	VS3V_AVCC	Power supply input for voltage range 2.7V to 3.3V
12	GND	Ground
13	LNA_GND	RF ground
14	LNA_IN	RF input
15	SENSE	Sensitivity control resistor
16	SENSE_CTRL	Sensitivity selection Low: Normal sensitivity, High: Reduced sensitivity
17	RSSI	Output of the RSSI amplifier
18	TEST3	Test pin, during operation at GND
19	RX	Input to activate the receiver
20	BR0	Bit rate selection, LSB
21	BR1	Bit rate selection, MSB
22	ASK_NFSK	FSK/ASK selection Low: FSK, High: ASK
23	CDEM	Capacitor to adjust the lower cut-off frequency data filter
24	DATA_OUT	Data output
	GND	Ground/backplane (exposed die pad)

Figure 1-3. Block Diagram



## 2. RF Receiver

As seen in [Figure 1-3 on page 5](#), the RF receiver consists of a low-noise amplifier (LNA), a local oscillator, and the signal processing part with mixer, IF filter, IF amplifier with analog RSSI, FSK/ASK demodulator, data filter, and data slicer.

In receive mode, the LNA pre-amplifies the received signal which is converted down to a 440-kHz intermediate frequency (IF), then filtered and amplified before it is fed into an FSK/ASK demodulator, data filter, and data slicer. The received signal strength indicator (RSSI) signal is available at the pin RSSI.

### 2.1 Low-IF Receiver

The receive path consists of a fully integrated low-IF receiver. It fulfills the sensitivity, blocking, selectivity, supply voltage, and supply current specification needed to design, e.g., an industrial/ aftermarket integrated receiver for RKE and TPM systems. A benefit of the integrated receive filter is that no external components needed.

At 315MHz, the Atmel® ATA8201 receiver (433.92MHz for the Atmel ATA8202 receiver) has a typical system noise figure of 6.0dB (7.0dB), a system I1dBCP of -31dBm (-30dBm), and a system IIP3 of -24dBm (-23dBm). The signal path is linear for out-of-band disturbers up to the I1dBCP and hence there is no AGC or switching of the LNA needed, and a better blocking performance is achieved. This receiver uses an IF (intermediate frequency) of 440kHz, the typical image rejection is 30dB and the typical 3-dB IF filter bandwidth is 420kHz ( $f_{IF} = 440\text{kHz} \pm 210\text{kHz}$ ,  $f_{lo\_IF} = 230\text{kHz}$  and  $f_{hi\_IF} = 650\text{kHz}$ ). The demodulator needs a signal-to-noise ratio of 8.5dB for 10Kbits/s Manchester with  $\pm 38\text{kHz}$  frequency deviation in FSK mode, thus, the resulting sensitivity at 315MHz (433.92MHz) is typically -105dBm (-104dBm).

Due to the low phase noise and spurs of the synthesizer together with the 8th-order integrated IF filter, the receiver has a better selectivity and blocking performance than more complex double superhet receivers, without using external components and without numerous spurious receiving frequencies.

A low-IF architecture is also less sensitive to second-order intermodulation (IIP2) than direct conversion receivers where every pulse or amplitude modulated signal (especially the signals from TDMA systems like GSM) demodulates to the receiving signal band at second-order non-linearities.

### 2.2 Input Matching at LNA\_IN

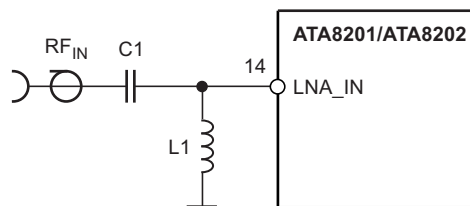
The measured input impedances as well as the values of a parallel equivalent circuit of these impedances can be seen in [Table 2-1](#). The highest sensitivity is achieved with power matching of these impedances to the source impedance.

**Table 2-1. Measured Input Impedances of the LNA\_IN Pin**

$f_{RF}$ [MHz]	$Z_{in}(RF\_IN)$ [ $\Omega$ ]	$R_{in\_p}/C_{in\_p}$ [pF]
315	(72.4 - j298)	1300 $\Omega$ //1.60
433.92	(55 - j216) $\Omega$	900 $\Omega$ //1.60

The matching of the LNA input to 50 $\Omega$  is done using the circuit shown in [Figure 2-1](#) and the values of the matching elements given in [Table 2-2](#). The reflection coefficients were always  $\leq -10\text{dB}$ . Note that value changes of C1 and L1 may be necessary to compensate individual board layout parasitics. The measured typical FSK and ASK Manchester-code sensitivities with a bit error rate (BER) of  $10^{-3}$  are shown in [Table 2-3](#) and [Table 2-4 on page 7](#). These measurements were done with wire-wound inductors having quality factors reported in [Table 2-2](#), resulting in estimated matching losses of 0.8dB at 315MHz and 433.92MHz. These losses can be estimated when calculating the parallel equivalent resistance of the inductor with  $R_{loss} = 2 \times \pi \times f \times L \times Q_L$  and the matching loss with  $10 \log(1 + R_{in\_p} / R_{loss})$ .

**Figure 2-1. Input Matching to 50 $\Omega$**



**Table 2-2. Input Matching to 50Ω**

$f_{RF}$ [MHz]	$C_1$ [pF]	$L_1$ [nH]	$Q_{L1}$
315	2.2	68	20
433.92	2.2	36	15

**Table 2-3. Measured Typical Sensitivity FSK, ±38 kHz, Manchester, BER = 10<sup>-3</sup>**

RF Frequency	BR_Range_0 1.0Kbit/s	BR_Range_0 2.5Kbits/s	BR_Range_1 5Kbits/s	BR_Range_2 10Kbits/s	BR_Range_3 10Kbits/s	BR_Range_3 20Kbits/s
315MHz	-108dBm	-108dBm	-107dBm	-105dBm	-104dBm	-104dBm
433.92MHz	-107dBm	-107dBm	-106dBm	-104dBm	-103dBm	-103dBm

**Table 2-4. Measured Typical Sensitivity 100% ASK, Manchester, BER = 10<sup>-3</sup>**

RF Frequency	BR_Range_0 1.0Kbit/s	BR_Range_0 2.5Kbits/s	BR_Range_1 5Kbits/s	BR_Range_2 10Kbits/s	BR_Range_3 10Kbits/s
315MHz	-114dBm	-114dBm	-113dBm	-111dBm	-109dBm
433.92MHz	-113dBm	-113dBm	-112dBm	-110dBm	-108dBm

Conditions for the sensitivity measurement:

The given sensitivity values are valid for Manchester-modulated signals. For the sensitivity measurement the distance from edge to edge must be evaluated. As can be seen in [Figure 6-1 on page 21](#), in a Manchester-modulated data stream, the time segments  $T_{EE}$  and  $2 \times T_{EE}$  occur.

To reach the specified sensitivity for the evaluation of  $T_{EE}$  and  $2 \times T_{EE}$  in the data stream, the following limits should be used ( $T_{EE}$  min,  $T_{EE}$  max,  $2 \times T_{EE}$  min,  $2 \times T_{EE}$  max).

**Table 2-5. Limits for Sensitivity Measurements**

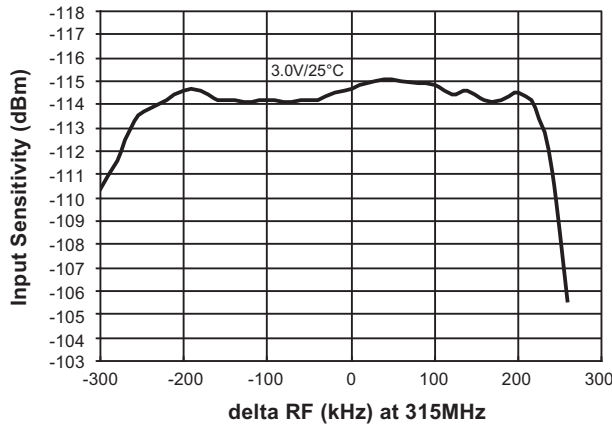
Bit Rate	$T_{EE}$ Min	$T_{EE}$ Typ	$T_{EE}$ Max	$2 \times T_{EE}$ Min	$2 \times T_{EE}$ Typ	$2 \times T_{EE}$ Max
1.0Kbit/s	260μs	500μs	790μs	800μs	1000μs	1340μs
2.4Kbits/s	110μs	208μs	310μs	320μs	416μs	525μs
5.0Kbits/s	55μs	100μs	155μs	160μs	200μs	260μs
9.6Kbits/s	27μs	52μs	78μs	81μs	104μs	131μs

## 2.3 Sensitivity Versus Supply Voltage, Temperature and Frequency Offset

To calculate the behavior of a transmission system, it is important to know the reduction of the sensitivity due to several influences. The most important are frequency offset due to crystal oscillator (XTO) and crystal frequency (XTAL) errors, temperature and supply voltage dependency of the noise figure, and IF-filter bandwidth of the receiver. Figure 2-2 and Figure 2-3 on page 8 show the typical sensitivity at 315MHz, ASK, 2.4Kbits/s and 9.6Kbits/s, Manchester, Figure 2-4 and Figure 2-5 on page 9 show a typical sensitivity at 315MHz, FSK, 2.4Kbits/s and 9.6Kbits/s,  $\pm 38\text{kHz}$ , Manchester versus the frequency offset between transmitter and receiver at  $T_{\text{amb}} = +25^\circ\text{C}$  and supply voltage  $V_S = V_{S3V\_AVCC} = V_{S5V} = 3.0\text{V}$ .

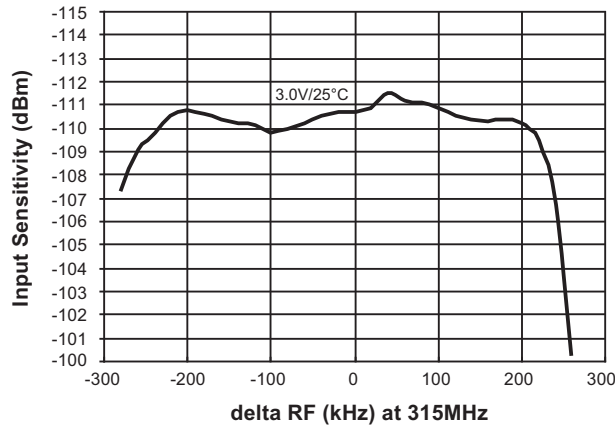
**Figure 2-2. Measured Sensitivity (315MHz, ASK, 2.4Kbits/s, Manchester) Versus Frequency Offset**

Input Sensitivity (dBm) at BER < 1e-3, ATA8201, ASK, 2.4Kbits/s (Manchester),  
BR = 0



**Figure 2-3. Measured Sensitivity (315MHz, ASK, 9.6Kbits/s, Manchester) Versus Frequency Offset**

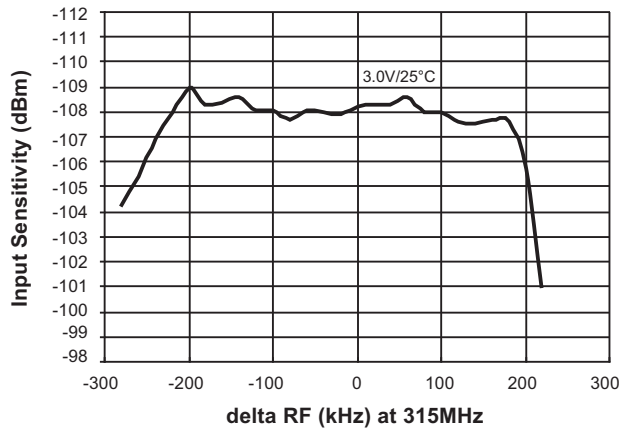
Input Sensitivity (dBm) at BER < 1e-3, ATA8201, ASK, 9.6Kbits/s (Manchester),  
BR = 2





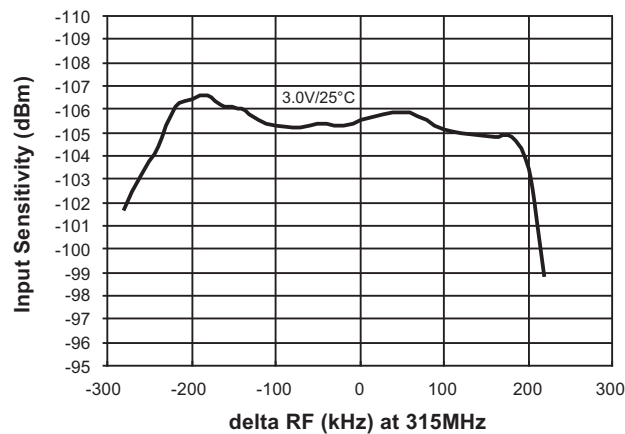
**Figure 2-4. Measured Sensitivity (315MHz, FSK, 2.4Kbits/s, ±38kHz, Manchester) Versus Frequency Offset**

Input Sensitivity (dBm) at BER < 1e-3, ATA8201, FSK, 2.4Kbits/s (Manchester),  
BR = 0



**Figure 2-5. Measured Sensitivity (315MHz, FSK, 9.6Kbits/s, ±38kHz, Manchester) Versus Frequency Offset**

Input Sensitivity (dBm) at BER < 1e-3, ATA8201, FSK, 9.64Kbits/s (Manchester),  
BR = 2



As can be seen in [Figure 2-5 on page 9](#), the supply voltage has almost no influence. The temperature has an influence of about  $\pm 1.0$ dB, and a frequency offset of  $\pm 160$ kHz also influences by about  $\pm 1$ dB. All these influences, combined with the sensitivity of a typical IC ( $-105$ dB), are then within a range of  $-103.0$ dBm and  $-107.0$ dBm over temperature, supply voltage, and frequency offset. The integrated IF filter has an additional production tolerance of  $\pm 10$ kHz, hence, a frequency offset between the receiver and the transmitter of  $\pm 160$ kHz can be accepted for XTAL and XTO tolerances.

Note: For the demodulator used in the Atmel® ATA8201/ATA8202, the tolerable frequency offset does not change with the data frequency. Hence, the value of  $\pm 160$ kHz is valid for 1Kbit/s to 10Kbits/s.

This small sensitivity change over supply voltage, frequency offset, and temperature is very unusual in such a receiver. It is achieved by an internal, very fast, and automatic frequency correction in the FSK demodulator after the IF filter, which leads to a higher system margin. This frequency correction tracks the input frequency very quickly. If, however, the input frequency makes a larger step (for example, if the system changes between different communication partners), the receiver has to be restarted. This can be done by switching back to Standby mode and then again to Active mode (pin RX 1  $\rightarrow$  0  $\rightarrow$  1) or by generating a positive pulse on pin ASK\_NFSK (0  $\rightarrow$  1  $\rightarrow$  0).

## 2.4 RX Supply Current Versus Temperature and Supply Voltage

Table 2-7 shows the typical supply current of the receiver in Active mode versus supply voltage and temperature with  $V_S = VS3V\_AVCC = VS5V$ .

**Table 2-6. Measured Current in Active Mode ASK**

$V_S = VS3V\_AVCC = VS5V$	3.0V
$T_{amb} = 25^\circ\text{C}$	6.5mA

**Table 2-7. Measured Current in Active Mode FSK**

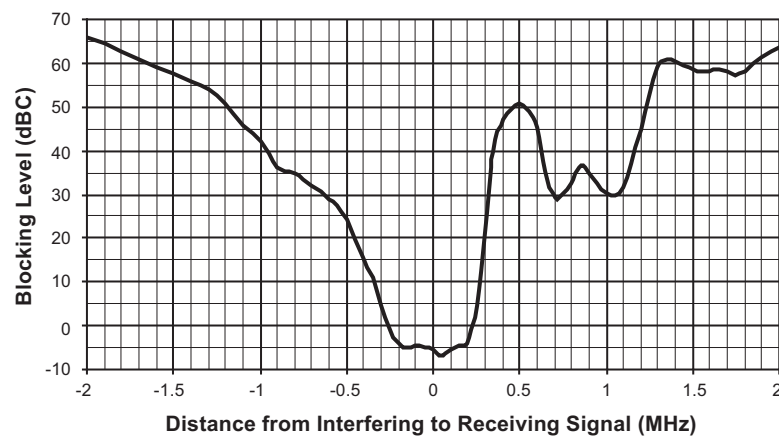
$V_S = VS3V\_AVCC = VS5V$	3.0V
$T_{amb} = 25^\circ\text{C}$	6.7mA

## 2.5 Blocking, Selectivity

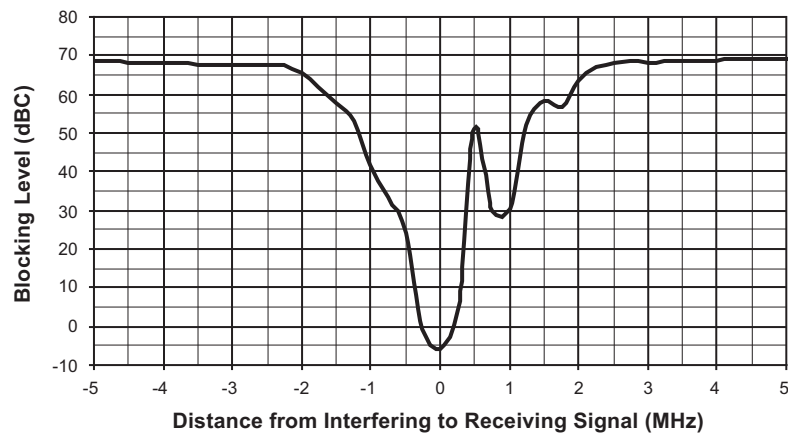
As can be seen in Figure 2-6 on page 10, and Figure 2-7 and Figure 2-8 on page 11, the receiver can receive signals 3dB higher than the sensitivity level in the presence of large blockers of  $-34.5\text{dBm}$  or  $-28\text{dBm}$  with small frequency offsets of  $\pm 3\text{MHz}$  or  $\pm 20\text{MHz}$ .

Figure 2-6, and Figure 2-7 on page 11 show the narrow-band blocking, and Figure 2-8 on page 11 shows the wide-band blocking characteristic. The measurements were done with a useful signal of 315MHz, FSK, 10Kbits/s,  $\pm 38\text{kHz}$ , Manchester, BR\_Range2 with a level of  $-105\text{dBm} + 3\text{dB} = -102\text{dBm}$ , which is 3dB above the sensitivity level. The figures show how much larger than  $-102\text{dBm}$  a continuous wave signal can be, until the BER is higher than  $10^{-3}$ . The measurements were done at the  $50\Omega$  input shown in Figure 2-1 on page 6. At 3 MHz, for example, the blocker can be 67.5dBC higher than  $-102\text{dBm}$ , or  $-102\text{dBm} + 67.5\text{dBC} = -34.5\text{dBm}$ .

**Figure 2-6. Close-in 3-dB Blocking Characteristic and Image Response at 315MHz**



**Figure 2-7. Narrow-band 3-dB Blocking Characteristic at 315MHz**



**Figure 2-8. Wide-band 3-dB Blocking Characteristic at 315MHz**

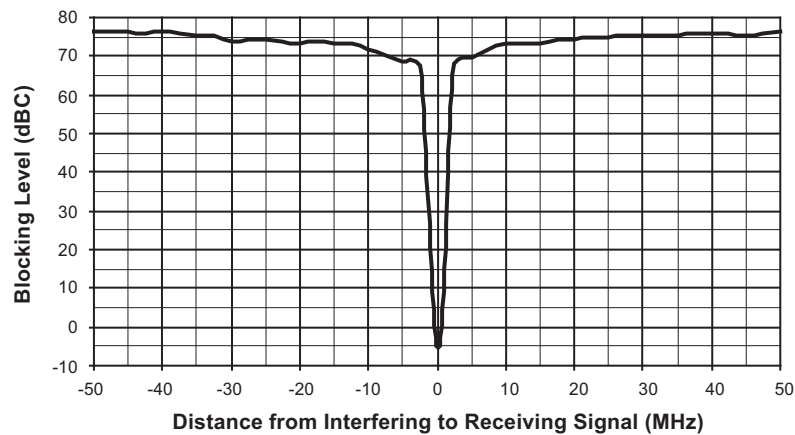


Table 2-8 shows the blocking performance measured relative to  $-102\text{dBm}$  for some frequencies. Note that sometimes the blocking is measured relative to the sensitivity level  $104\text{dBm}$  (denoted dBS), instead of the carrier  $-102\text{dBm}$  (denoted dBC).

**Table 2-8. Blocking 3dB Above Sensitivity Level With BER <  $10^{-3}$**

Frequency Offset	Blocking Level	Blocking
+1.5MHz	$-44.5\text{dBm}$	57.5dBC, 60.5dBS
-1.5MHz	$-44.5\text{dBm}$	57.5dBC, 60.5dBS
+2MHz	$-39.0\text{dBm}$	63dBC, 66dBS
-2MHz	$-36.0\text{dBm}$	66dBC, 69dBS
+3MHz	$-34.5\text{dBm}$	67.5dBC, 70.5dBS
-3MHz	$-34.5\text{dBm}$	67.5dBC, 70.5dBS
+20MHz	$-28.0\text{dBm}$	74dBC, 77dBS
-20MHz	$-28.0\text{dBm}$	74dBC, 77dBS

The Atmel® ATA8201/ATA8202 can also receive FSK and ASK modulated signals if they are much higher than the  $11\text{dBCP}$ . It can typically receive useful signals at  $-10\text{dBm}$ . This is often referred to as the nonlinear dynamic range (that is, the maximum to minimum receiving signal), and is  $95\text{dB}$  for  $10\text{Kbits/s}$  Manchester (FSK). This value is useful if the transmitter and receiver are very close to each other.

## 2.6 In-band Disturbers, Data Filter, Quasi-peak Detector, Data Slicer

If a disturbing signal falls into the received band, or if a blocker is not a continuous wave, the performance of a receiver strongly depends on the circuits after the IF filter. Hence, the demodulator, data filter, and data slicer are important.

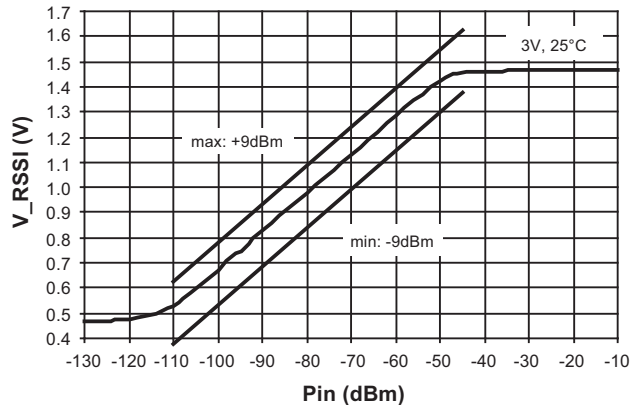
The data filter of the Atmel® ATA8201/ATA8202 functions also as a quasi-peak detector. This results in a good suppression of above mentioned disturbers and exhibits a good carrier-to-noise performance. The required useful-signal-to-disturbing-signal ratio, at a BER of  $10^{-3}$ , is less than 14dB in ASK mode and less than 3dB (BR\_Range\_0 to BR\_Range\_2) and 6dB (BR\_Range\_3) in FSK mode. Due to the many different possible waveforms, these numbers are measured for the signal, as well as for disturbers, with peak amplitude values. Note that these values are worst-case values and are valid for any type of modulation and modulating frequency of the disturbing signal, as well as for the receiving signal. For many combinations, lower carrier-to-disturbing-signal ratios are needed.

## 2.7 RSSI Output

The output voltage of the pin RSSI is an analog voltage, proportional to the input power level. Using the RSSI output signal, the signal strength of different transmitters can be distinguished. The usable dynamic range of the RSSI amplifier is 65dB, the input power range  $P(RF_{IN})$  is

-110dBm to -45dBm, and the gain is 15mV/dB. Figure 2-9 shows the RSSI characteristic of a typical device at 315MHz with  $VS3V\_AVCC = VS5V = 3V$  and  $T_{amb} = 25^{\circ}C$  with a matched input as shown in Table 2-2 and Figure 2-1 on page 6. At 433.92MHz, 1 dB more signal level is needed for the same RSSI results.

Figure 2-9. Typical RSSI Characteristic at 315MHz Versus Temperature and Supply Voltage



As can be seen in Figure 2-9 on page 12, for single devices there is a variance over temperature and supply voltage range of  $\pm 3$ dB. The total variance over production, temperature, and supply voltage range is  $\pm 9$ dB.

## 2.8 Frequency Synthesizer

The LO generates the carrier frequency for the mixer via a PLL synthesizer. The XTO (crystal oscillator) generates the reference frequency  $f_{XTO}$ . The VCO (voltage-controlled oscillator) generates the drive voltage frequency  $f_{LO}$  for the mixer.  $f_{LO}$  is divided by the factor 24 (Atmel ATA8201) or 32 (Atmel ATA8202). The divided frequency is compared to  $f_{XTO}$  by the phase frequency detector. The current output of the phase frequency detector is connected to the fully integrated loop filter, and thereby generates the control voltage for the VCO. By means of that configuration, the VCO is controlled in a way, such that  $f_{LO} / 24$  ( $f_{LO} / 32$ ) is equal to  $f_{XTO}$ . If  $f_{LO}$  is determined,  $f_{XTO}$  can be calculated using the following formula:  $f_{XTO} = f_{LO} / 24$  ( $f_{XTO} = f_{LO} / 32$ ). The synthesizer has a phase noise of  $-130$ dBc/Hz at 3MHz and spurs of  $-75$ dBc.

Care must be taken with the harmonics of the CLK output signal, as well as with the harmonics produced by a microprocessor clocked using the signal, as these harmonics can disturb the reception of signals.

### 3. XTO

The XTO is an amplitude-regulated Pierce oscillator type with external load capacitances ( $2 \times 16\text{pF}$ ). Due to additional internal and board parasitics ( $C_p$ ) of approximately  $2\text{pF}$  on each side, the load capacitance amounts to  $2 \times 18\text{pF}$  ( $9\text{pF}$  total).

The XTO oscillation frequency  $f_{\text{XTO}}$  is the reference frequency for the integer-N synthesizer. When designing the system in terms of receiving and transmitting frequency offset, the accuracy of the crystal and XTO have to be considered.

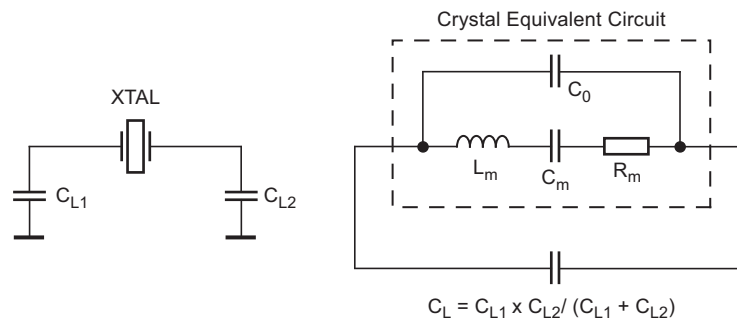
The XTO's additional pulling (including the  $R_m$  tolerance) is only  $\pm 5\text{ppm}$ . The XTAL versus temperature, aging, and tolerances is then the main source of frequency error in the local oscillator.

The XTO frequency depends on XTAL properties and the load capacitances  $C_{L1,2}$  at pin XTAL1 and XTAL2. The pulling ( $p$ ) of  $f_{\text{XTO}}$  from the nominal  $f_{\text{XTAL}}$  is calculated using the following formula:

$$p = \frac{C_m}{2} \times \frac{C_{LN} - C_L}{(C_0 + C_{LN}) \times (C_0 + C_L)} \times 10^{-6} \text{ ppm}$$

$C_m$ , the crystal's motional capacitance;  $C_0$ , the shunt capacitance; and  $C_{LN}$ , the nominal load capacitance of the XTAL, are found in the datasheet.  $C_L$  is the total actual load capacitance of the crystal in the circuit, and consists of  $C_{L1}$  and  $C_{L2}$  connected in series.

**Figure 3-1. Crystal Equivalent Circuit**



With  $C_m \leq 10\text{fF}$ ,  $C_0 \geq 1.0\text{pF}$ ,  $C_{LN} = 9\text{pF}$  and  $C_{L1,2} = 16\text{pF} \pm 1\%$ , the pulling amounts to  $P \leq \pm 1\text{ppm}$ .

The  $C_0$  of the XTAL has to be lower than  $C_{L\text{min}} / 2 = 7.9\text{pF}$  for a Pierce oscillator type in order to not enter the steep region of pulling versus load capacitance where there is risk of an unstable oscillation.

To ensure proper start-up behavior, the small signal gain and the negative resistance provided by this XTO at start is very large. For example, oscillation starts up even in the worst case with a crystal series resistance of  $1.5\text{k}\Omega$  at  $C_0 \leq 2.2\text{pF}$  with this XTO. The negative resistance is approximately given by

$$\text{Re}\{Z_{\text{xtocore}}\} = \text{Re}\left\{ \frac{Z_1 \times Z_3 + Z_2 \times Z_3 + Z_1 \times Z_3 \times gm}{Z_1 + Z_2 + Z_3 + Z_1 \times Z_2 \times gm} \right\}$$

with  $Z_1$  and  $Z_2$  as complex impedances at pins XTAL1 and XTAL2, hence

$$Z_1 = -j / (2 \times p \times f_{\text{XTO}} \times C_{L1}) + 5\Omega \text{ and } Z_2 = -j / (2 \times p \times f_{\text{XTO}} \times C_{L2}) + 5\Omega.$$

$Z_3$  consists of crystal  $C_0$  in parallel with an internal  $110\text{-k}\Omega$  resistor, hence

$Z_3 = -j / (2 \times p \times f_{\text{XTO}} \times C_0) / 110 \text{ k}\Omega$ ,  $gm$  is the internal transconductance between XTAL1 and XTAL2, with typically  $20\text{mS}$  at  $25^\circ\text{C}$ .

With  $f_{\text{XTO}} = 13.5\text{MHz}$ ,  $gm = 20\text{mS}$ ,  $C_L = 9\text{pF}$ , and  $C_0 = 2.2\text{pF}$ , this results in a negative resistance of about  $2\text{k}\Omega$ . The worst case for technology, supply voltage, and temperature variations is then always higher than  $1.4\text{k}\Omega$  for  $C_0 \leq 2.2\text{pF}$ .

Due to the large gain at start, the XTO is able to meet a very low start-up time. The oscillation start-up time can be estimated with the time constant  $\tau$ .

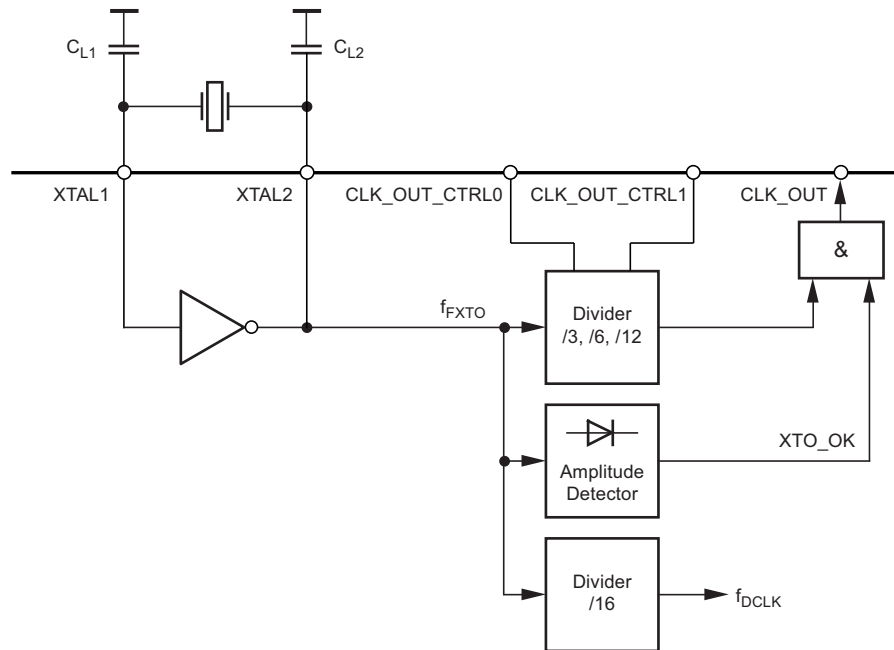
$$\tau = \frac{2}{4 \times \pi^2 \times f_{\text{XTAL}}^2 \times C_m \times (\text{Re}(Z_{\text{xtocore}}) + R_m)}$$

After  $10\tau$  to  $20\tau$ , an amplitude detector detects the oscillation amplitude and sets XTO\_OK to High if the amplitude is large enough; this activates the CLK\_OUT output if it is enabled via the pins CLK\_OUT\_CTRL0 and CLK\_OUT\_CTRL1. Note that the necessary conditions of the DVCC voltage also have to be fulfilled.

It is recommended to use a crystal with  $C_m = 3.0\text{fF}$  to  $10\text{fF}$ ,  $C_{LN} = 9\text{pF}$ ,  $R_m < 120\Omega$  and  $C_0 = 1.0\text{pF}$  to  $2.2\text{pF}$ .

Lower values of  $C_m$  can be used, slightly increasing the start-up time. Lower values of  $C_0$  or higher values of  $C_m$  (up to  $15\text{fF}$ ) can also be used, with only little influence on pulling.

**Figure 3-2. XTO Block Diagram**



The relationship between  $f_{XTO}$  and the  $f_{RF}$  is shown in [Table 3-1](#).

**Table 3-1. Calculation of  $f_{RF}$**

Frequency [MHz]	$f_{XTO}$ [MHz]	$f_{RF}$
433.92 (Atmel ATA8202)	13.57375	$f_{XTO} \times 32 - 440\text{kHz}$
315.0 (Atmel ATA8201)	13.1433	$f_{XTO} \times 24 - 440\text{kHz}$

Attention must be paid to the harmonics of the CLK\_OUT output signal  $f_{CLK\_OUT}$  as well as to the harmonics produced by a microprocessor clocked with it, since these harmonics can disturb the reception of signals if they get to the RF input. If the CLK\_OUT signal is used, it must be carefully laid out on the application PCB. The supply voltage of the microcontroller must also be carefully blocked.

### 3.1 Pin CLK\_OUT

Pin CLK\_OUT is an output to clock a connected microcontroller. The clock is available in Standby and Active modes. The frequency  $f_{\text{CLK\_OUT}}$  can be adjusted via the pins CLK\_OUT\_CTRL0 and CLK\_OUT\_CTRL1, and is calculated as follows:

**Table 3-2. Setting of  $f_{\text{CLK\_OUT}}$**

CLK_OUT_CTRL1	CLK_OUT_CTRL0	Function
0	0	Clock on pin CLK_OUT is switched off (Low level on pin CLK_OUT)
0	1	$f_{\text{CLK\_OUT}} = f_{\text{XTO}} / 3$
1	0	$f_{\text{CLK\_OUT}} = f_{\text{XTO}} / 6$
1	1	$f_{\text{CLK\_OUT}} = f_{\text{XTO}} / 12$

The signal at CLK\_OUT output has a nominal 50% duty cycle. To save current, it is recommended that CLK\_OUT be switched off during Standby mode.

### 3.2 Basic Clock Cycle of the Digital Circuitry

The complete timing of the digital circuitry is derived from one clock. As seen in [Figure 3-2 on page 14](#), this clock cycle,  $T_{\text{DCLK}}$ , is derived from the crystal oscillator (XTO) in combination with a divider.

$$f_{\text{DCLK}} = \frac{f_{\text{XTO}}}{16}$$

$T_{\text{DCLK}}$  controls the following application relevant parameters:

- Debouncing of the data signal stream
- Start-up time of the RX signal path

The start-up time and the debounce characteristic depend on the selected bit rate range (BR\_Range) which is defined by pins BR0 and BR1. The clock cycle  $T_{\text{XDCLK}}$  is defined by the following formulas for further reference:

BR\_Range  $\Rightarrow$

BR_Range 0:	$T_{\text{XDCLK}} = 8 \times T_{\text{DCLK}}$
BR_Range 1:	$T_{\text{XDCLK}} = 4 \times T_{\text{DCLK}}$
BR_Range 2:	$T_{\text{XDCLK}} = 2 \times T_{\text{DCLK}}$
BR_Range 3:	$T_{\text{XDCLK}} = 1 \times T_{\text{DCLK}}$

## 4. Sensitivity Reduction

The output voltage of the RSSI amplifier is internally compared to a threshold voltage  $V_{Th\_red}$ .  $V_{Th\_red}$  is determined by the value of the external resistor  $R_{Sense}$ .  $R_{Sense}$  is connected between the pins SENSE and VS3V\_AVCC (see [Figure 10-1 on page 25](#)). The output of the comparator is fed into the digital control logic. By this means, it is possible to operate the receiver at a lower sensitivity.

If the level on input pin SENSE\_CTRL is low, the receiver operates at full sensitivity.

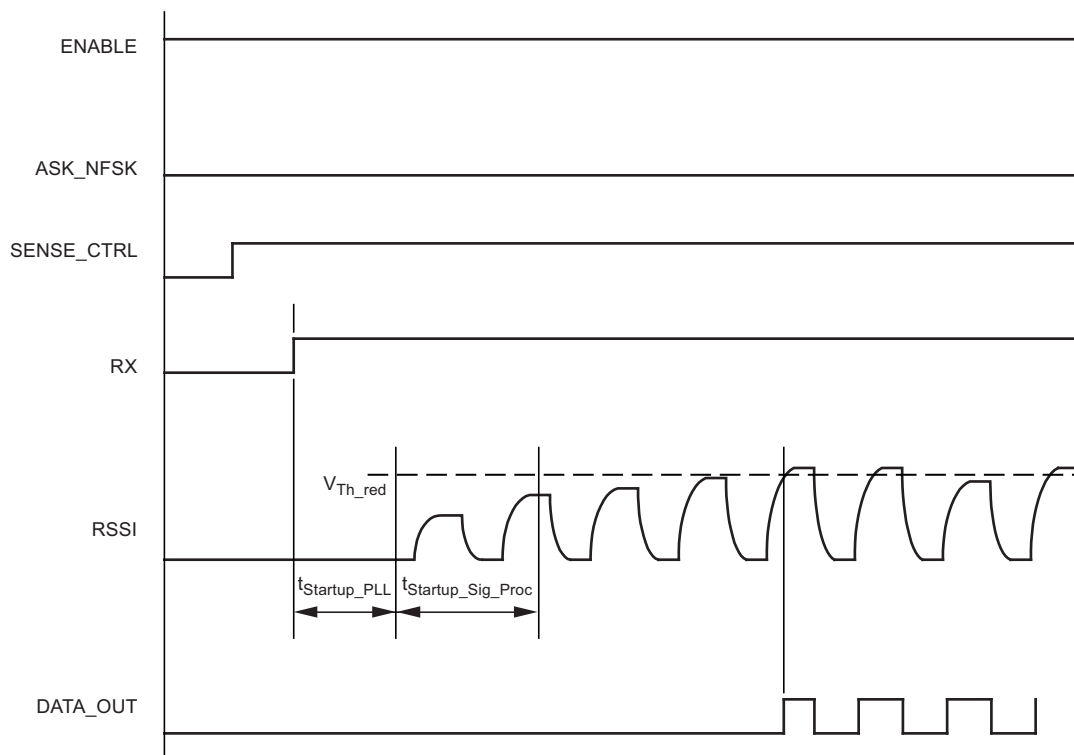
If the level on input pin SENSE\_CTRL is high, the receiver operates at a lower sensitivity. The reduced sensitivity is defined by the value of  $R_{Sense}$ , the maximum sensitivity by the signal-to-noise ratio of the LNA input. The reduced sensitivity depends on the signal strength at the output of the RSSI amplifier.

Since different RF input networks may exhibit slightly different values for the LNA gain, the sensitivity values given in the electrical characteristics refer to a specific input matching. This matching is illustrated in [Figure 2-1 on page 6](#) and exhibits the best possible sensitivity.

If the sensitivity reduction feature is not used, pin SENSE can be left open, pin SENSE\_CTRL must be set to GND.

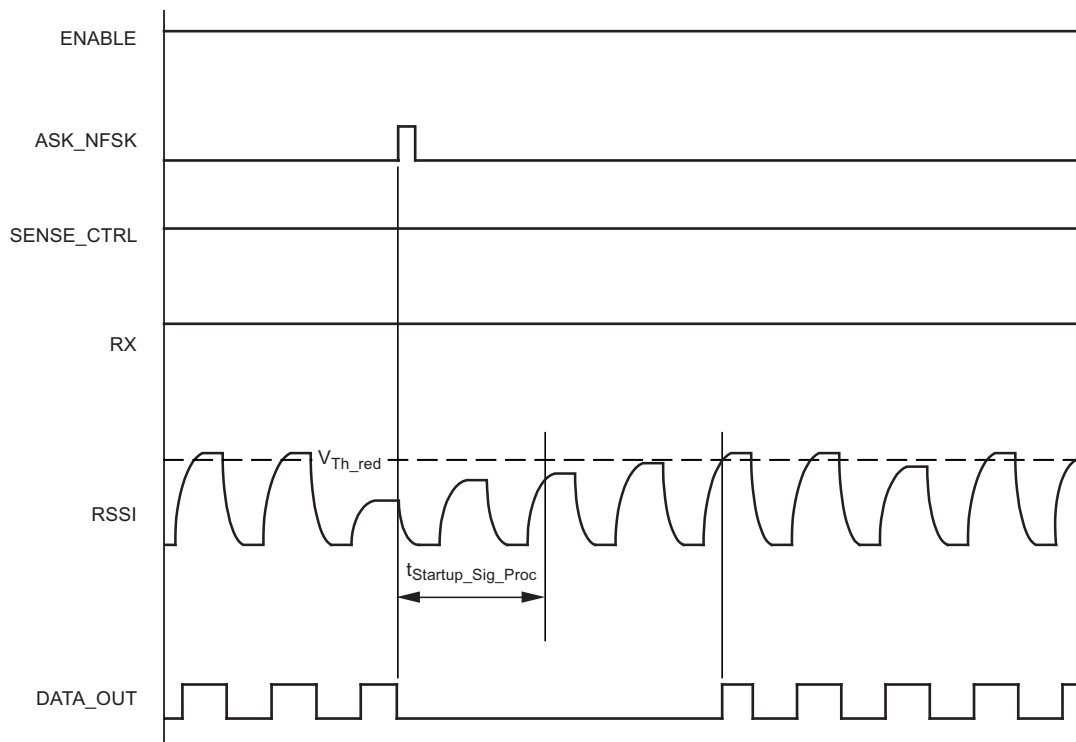
To operate with reduced sensitivity, pin SENSE\_CTRL must be set to high before the RX signal path will be enabled by setting pin RX to high (see [Figure 4-1 on page 16](#)). As long as the RSSI level is lower than  $V_{Th\_red}$  (defined by the external resistor  $R_{Sense}$ ) no data stream is available on pin DATA\_OUT (low level on pin DATA\_OUT). An internal RS flip-flop will be set to high the first time the RSSI voltage crosses  $V_{Th\_red}$ , and from then on the data stream will be available on pin DATA\_OUT. From then on the receiver also works with full sensitivity. This makes sure that a telegram will not be interrupted if the RSSI level varies during the transmission. The RS flip-flop can be set back, and thus the receiver switched back to reduced sensitivity, by generating a positive pulse on pin ASK\_NFSK (see [Figure 4-2 on page 17](#)). In FSK mode, operating with reduced sensitivity follows the same way.

**Figure 4-1. Reduced Sensitivity Active**



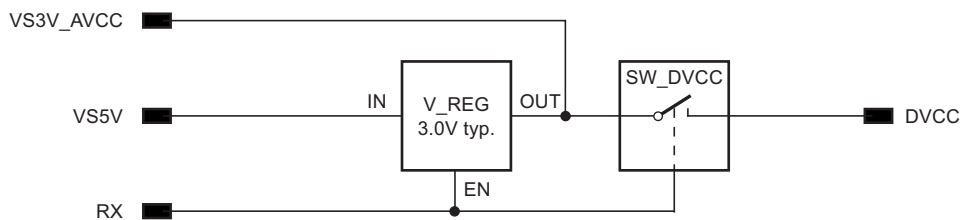


**Figure 4-2. Restart Reduced Sensitivity**



## 5. Power Supply

**Figure 5-1. Power Supply**



The supply voltage range of the Atmel® ATA8201/ATA8202 is 2.7V to 3.3V or 4.5V to 5.5V.

Pin VS3V\_AVCC is the supply voltage input for the range 2.7V to 3.3V, and is used in battery applications using a single lithium 3V cell. Pin VS5V is the voltage input for the range 4.5V to 5.5V (car applications) in this case the voltage regulator V\_REG regulates VS3V\_AVCC to typically 3.0V. If the voltage regulator is active, a blocking capacitor of 2.2µF has to be connected to VS3V\_AVCC (see [Figure 10-1 on page 25](#)).

DVCC is the internal operating voltage of the digital control logic and is fed via the switch SW\_DVCC by VS3V\_AVCC. DVCC must be blocked on pin DVCC with 68nF (see [Figure 9-1 on page 24](#) and [Figure 10-1 on page 25](#)).

Pin RX is the input to activate the RX signal processing and set the receiver to Active mode.

## 5.1 OFF Mode

A low level on pin RX and ENABLE will set the receiver to OFF mode (low power mode). In this mode, the crystal oscillator is shut down and no clock is available on pin CLK\_OUT. The receiver is not sensitive to a transmitter signal in this mode.

**Table 5-1. Standby Mode**

RX	ENABLE	Function
0	0	OFF mode

## 5.2 Standby Mode

The receiver activates the Standby mode if pin ENABLE is set to “1”.

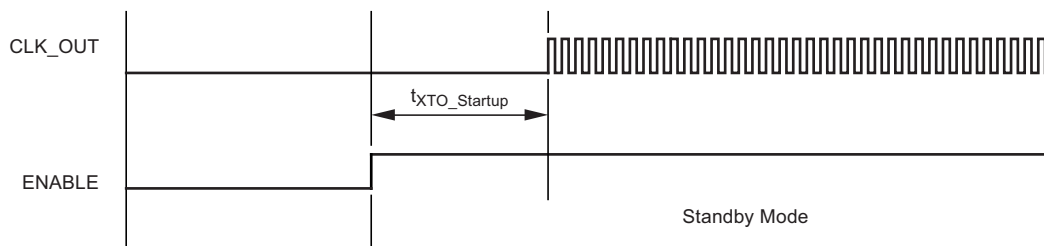
In Standby mode, the XTO is running and the clock on pin CLK\_OUT is available after the start-up time of the XTO has elapsed (dependent on pin CLK\_OUT\_CTRL0 and CLK\_OUT\_CTRL1). During Standby mode, the receiver is not sensitive to a transmitter signal.

In Standby mode, the RX signal path is disabled and the power consumption  $I_{\text{Standby}}$  is typically 50  $\mu\text{A}$  (CLK\_OUT output off, VS3V\_AVCC = VS5V = 3V). The exact value of this current is strongly dependent on the application and the exact operation mode, therefore check the section “[Electrical Characteristics: General](#)” on page 26 for the appropriate application case.

**Table 5-2. Standby Mode**

RX	ENABLE	Function
0	1	Standby mode

**Figure 5-2. Standby Mode (CLK\_OUT\_CTRL0 or CLK\_OUT\_CTRL1 = 1)**



## 5.3 Active Mode

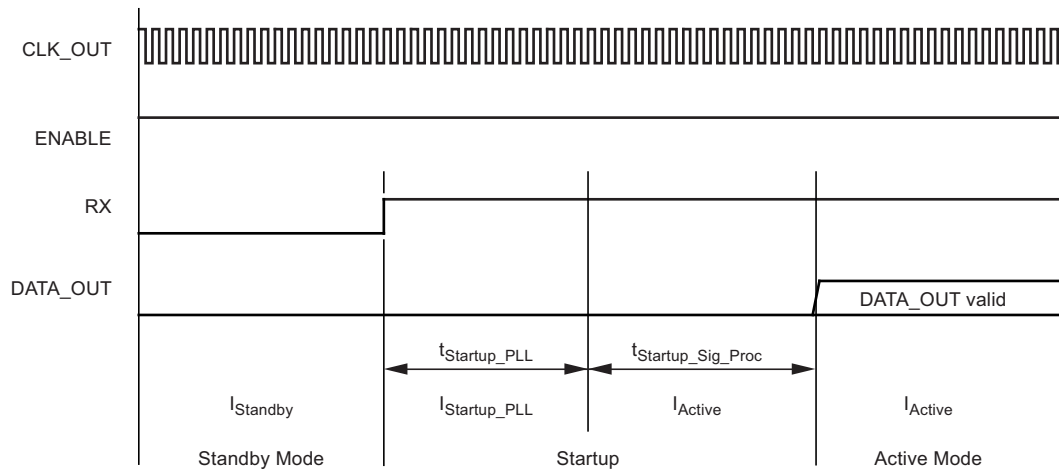
The Active mode is enabled by setting the level on pin RX to high. In Active mode, the RX signal path is enabled and if a valid signal is present it will be transferred to the connected microcontroller.

**Table 5-3. Active Mode**

RX	ENABLE	Function
1	1	Active mode

During  $T_{\text{Startup\_PLL}}$  the PLL is enabled and starts up. If the PLL is locked, the signal processing circuit starts up ( $T_{\text{Startup\_Sig\_Proc}}$ ). After the start-up time, all circuits are in stable condition and ready to receive. The duration of the start-up sequence depends on the selected bit rate range.

**Figure 5-3. Active Mode**



**Table 5-4. Start-up Time**

BR1	BR0	Atmel ATA8202 (433.92MHz)		Atmel ATA8201 (315MHz)	
		$T_{Startup\_PLL}$	$T_{Startup\_Sig\_Proc}$	$T_{Startup\_PLL}$	$T_{Startup\_Sig\_Proc}$
0	0	261 $\mu$ s	1096 $\mu$ s	269 $\mu$ s	1132 $\mu$ s
0	1		644 $\mu$ s		665 $\mu$ s
1	0		417 $\mu$ s		431 $\mu$ s
1	1		304 $\mu$ s		324 $\mu$ s

**Table 5-5. Modulation Scheme**

ASK_NFSK	RF <sub>IN</sub> at Pin LNA_IN	Level at Pin DATA_OUT
0	$f_{FSK\_H}$	1
	$f_{FSK\_L}$	0
1	$f_{ASK}$ on	1
	$f_{ASK}$ off	0

## 6. Bit Rate Ranges

Configuration of the bit rate ranges is carried out via the two pins BR0 and BR1. The microcontroller uses these two interface lines to set the corner frequencies of the band-pass data filter. Switching the bit rate ranges while the RF front end is in Active mode can be done on the fly and will not take longer than 100  $\mu$ s if done while remaining in either ASK or FSK mode. If the modulation scheme is changed at the same time, the switching time is ( $T_{Startup\_Sig\_Proc}$ , see [Figure 7-1 on page 22](#)). Each BR\_Range is defined by a minimum edge-to-edge time. To maintain full sensitivity of the receiver, edge-to-edge transition times of incoming data should not be less than the minimum for the selected BR\_Range.

**Table 6-1. BR Ranges ASK**

BR1	BR0	BR_Range	Recommended Bit Rate (Manchester) <sup>(1)</sup>	Minimum Edge-to-edge Time Period $T_{EE}$ of the Data Signal <sup>(2)</sup>	Edge-to-edge Time Period $T_{EE}$ of the Data Signal During the Start-up Period <sup>(3)</sup>
0	0	BR_Range0	1.0Kbit/s to 2.5Kbits/s	200 $\mu$ s	200 $\mu$ s to 500 $\mu$ s
0	1	BR_Range1	2.0Kbits/s to 5.0Kbits/s	100 $\mu$ s	100 $\mu$ s to 250 $\mu$ s
1	0	BR_Range2	4.0Kbits/s to 10.0Kbits/s	50 $\mu$ s	50 $\mu$ s to 125 $\mu$ s
1	1	BR_Range3	8.0Kbits/s to 10.0Kbits/s	50 $\mu$ s	50 $\mu$ s to 62.5 $\mu$ s

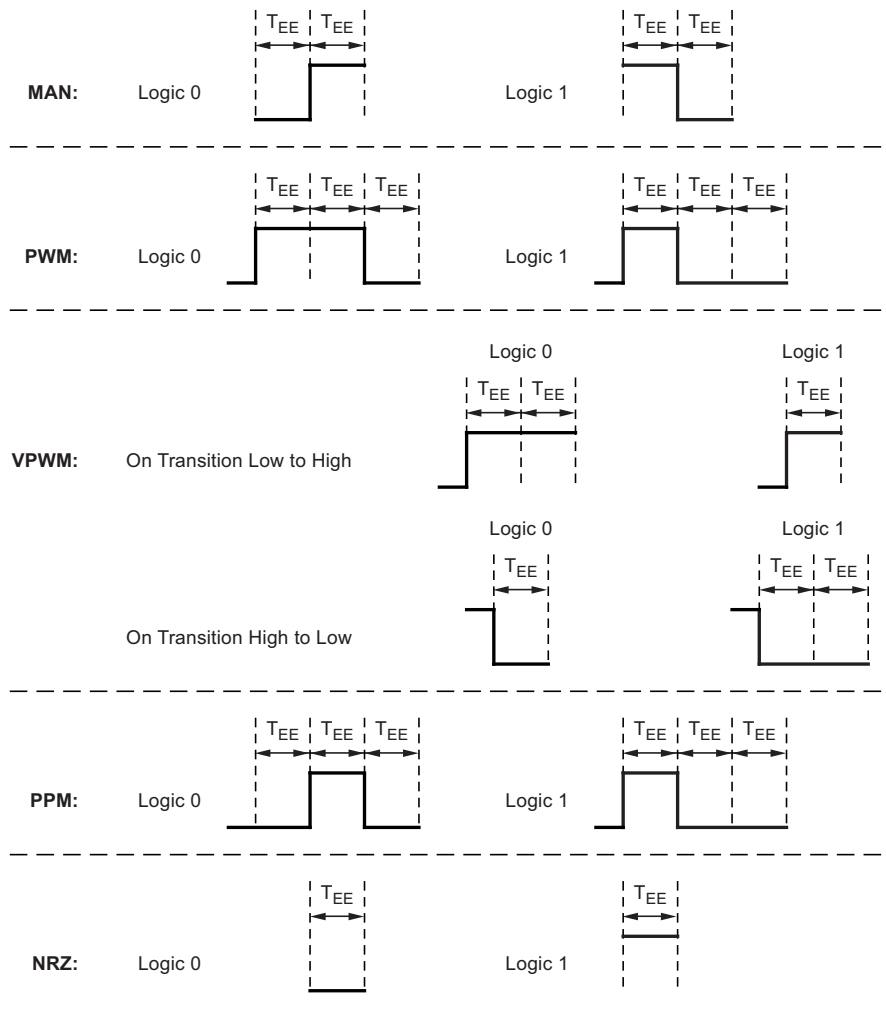
**Table 6-2. BR Ranges FSK**

BR1	BR0	BR_Range	Recommended Bit Rate (Manchester) <sup>(1)</sup>	Minimum Edge-to-edge Time Period $T_{EE}$ of the Data Signal <sup>(2)</sup>	Edge-to-edge Time Period $T_{EE}$ of the Data Signal During the Start-up Period <sup>(3)</sup>
0	0	BR_Range0	1.0Kbit/s to 2.5Kbits/s	200 $\mu$ s	200 $\mu$ s to 500 $\mu$ s
0	1	BR_Range1	2.0Kbits/s to 5.0Kbits/s	100 $\mu$ s	100 $\mu$ s to 250 $\mu$ s
1	0	BR_Range2	4.0Kbits/s to 10.0Kbits/s	50 $\mu$ s	50 $\mu$ s to 125 $\mu$ s
1	1	BR_Range3	8.0Kbits/s to 20.0Kbits/s	25 $\mu$ s	25 $\mu$ s to 62.5 $\mu$ s

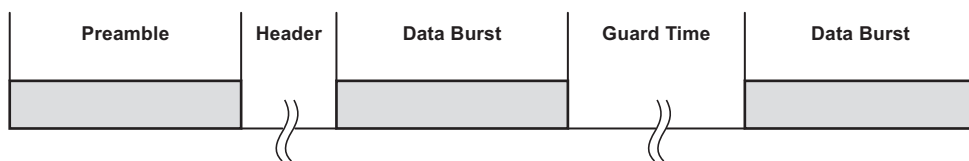
Note: If during the start-up period ( $T_{Startup\_PLL} + T_{Startup\_Sig\_Proc}$ ) there is no RF signal, the data filter settles to the noise floor, leading to noise on pin DATA\_OUT.

- Notes:
1. As can be seen, a bit stream of, for example, 2.5Kbits/s can be received in BR\_Range0 and BR\_Range1 (overlapping BR\_Ranges). To get the full sensitivity, always use the lowest possible BR\_Range (here, BR\_Range0). The advantage in the next higher BR\_Range (BR\_Range1) is the shorter start-up period, meaning lower current consumption during Polling mode. Thus, it is a decision between sensitivity and current consumption.
  2. The receiver is also capable of receiving non-Manchester-modulated signals, such as PWM, PPM, VPWM, NRZ. In ASK mode, the header and blanking periods occurring in Keeloq-like protocols (up to 52ms) are supported.
  3. To ensure an accurate settling of the data filter during the start-up period ( $T_{Startup\_PLL} + T_{Startup\_Sig\_Proc}$ ), the edge-to-edge time  $T_{EE}$  of the data signal (preamble) must be inside the given limits during this period.

**Figure 6-1. Examples of Supported Modulation Formats**



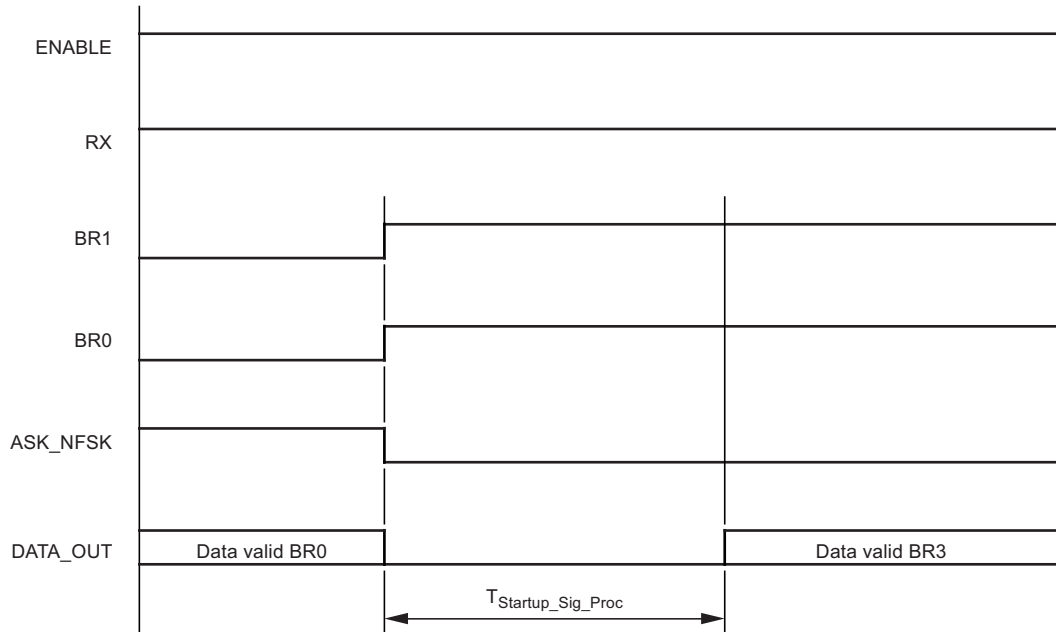
**Figure 6-2. Supported Header and Blanking Periods**



## 7. ASK\_NFSK

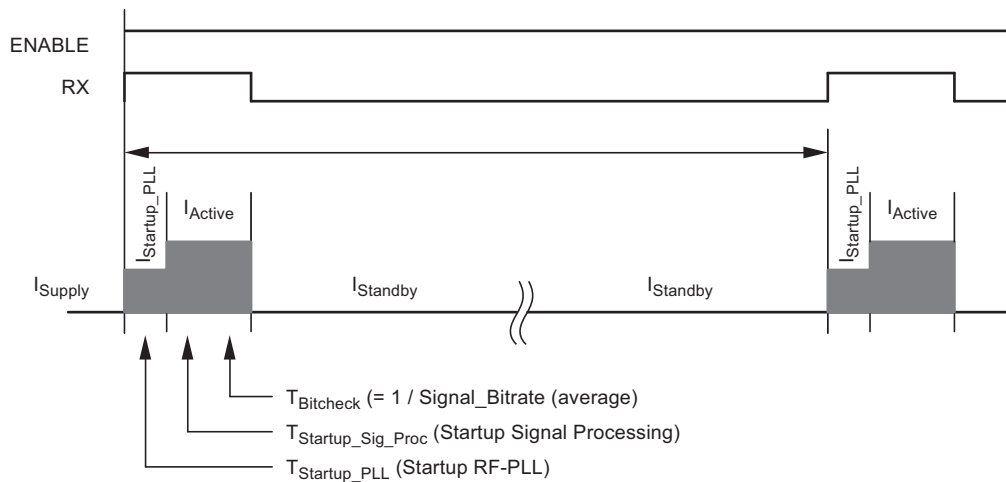
The ASK\_NFSK pin allows the microcontroller to rapidly switch the RF front end between demodulation modes. A logic 1 on this pin selects ASK mode, and a logic 0 FSK mode. The time to change modes ( $T_{Startup\_Sig\_Proc}$ ) depends on the bit rate range being selected (not current bit rate range) and is given in [Table 5-4 on page 19](#). This response time is specified for applications that require an ASK preamble followed by FSK data (for typical TPM applications). During  $T_{Startup\_Sig\_Proc}$ , the level on pin DATA\_OUT is low.

**Figure 7-1. ASK Preamble 2.4Kbits/s followed by FSK Data 9.6Kbits/s**



## 8. Polling Current Calculation

Figure 8-1. Polling Cycle



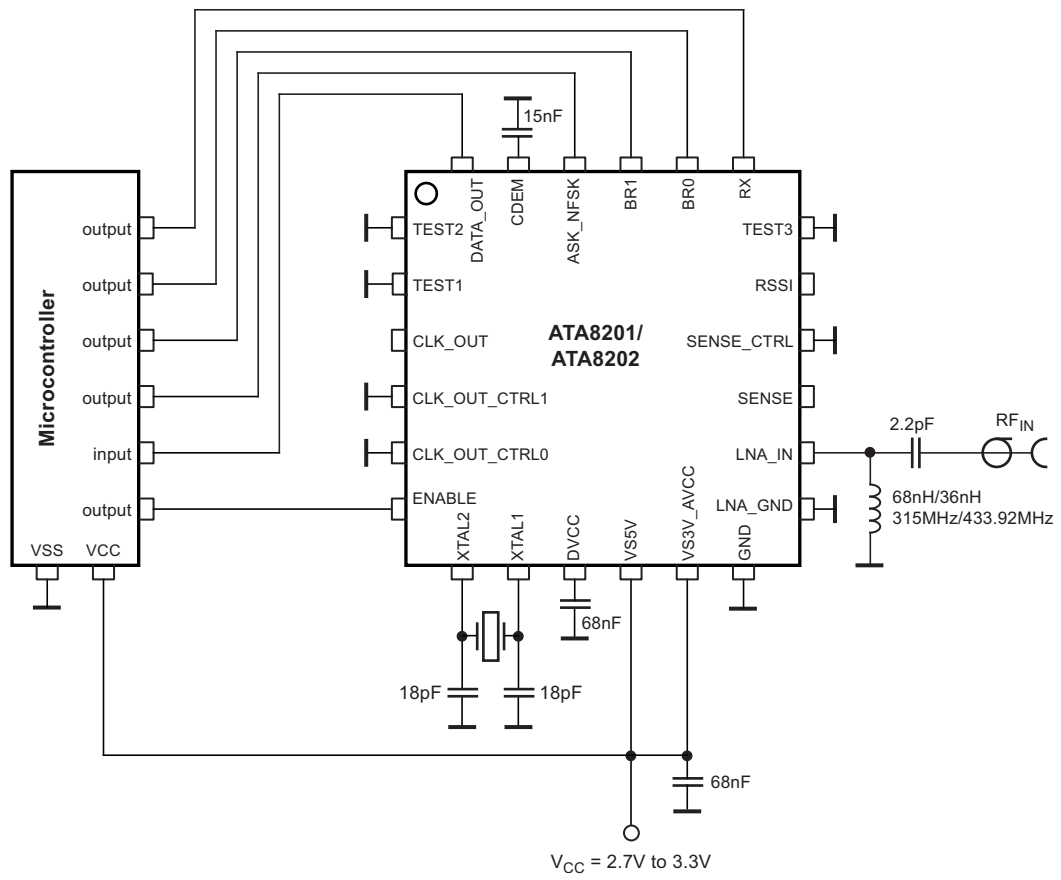
In an industrial or aftermarket RKE and TPM system, the average chip current in Polling mode,  $I_{\text{Polling}}$ , is an important parameter. The polling period must be controlled by the connected microcontroller via the pins ENABLE and RX. The polling current can be calculated as follows:

$$I_{\text{Polling}} = \left( \frac{T_{\text{Startup\_PLL}}}{T_{\text{Polling\_Period}}} \times I_{\text{Startup\_PLL}} + \left( \frac{T_{\text{Startup\_Sig\_Proc}}}{T_{\text{Polling\_Period}}} \times I_{\text{Active}} + \left( \frac{T_{\text{Bitcheck}}}{T_{\text{Polling\_Period}}} \times I_{\text{Active}} + \left( \frac{T_{\text{Polling\_Period}} - T_{\text{Startup\_PLL}} - T_{\text{Startup\_Sig\_Proc}} - T_{\text{Bitcheck}}}{T_{\text{Polling\_Period}}} \times I_{\text{Standby}} \right) \right) \right)$$

- $T_{\text{Startup\_PLL}}$ : depends on 315MHz/433.92MHz application.
  - $T_{\text{Startup\_Sig\_Proc}}$ : depends on 315MHz/433.92MHz application and the selected bit rate range.
  - $T_{\text{Bitcheck}}$ : depends on the signal bit rate ( $1 / \text{Signal\_Bit\_Rate}$ ).
  - $T_{\text{Polling\_Period}}$ : depends on the transmitter telegram (preburst).
  - $I_{\text{Startup\_PLL}}$ : depends on 3V or 5V application and the setting of pin CLK\_OUT.
  - $I_{\text{Active}}$ : depends on 3V or 5V application, ASK or FSK mode and the setting of pin CLK\_OUT.
  - $I_{\text{Standby}}$ : depends on 3V or 5V application and the setting of pin CLK\_OUT.
- Example:-
- 315-MHz application (ATA8201), bit rate: 9.6Kbits/s,  $T_{\text{Polling\_Period}} = 8\text{ms}$ 
    - >  $T_{\text{Startup\_PLL}} = 269\mu\text{s}$
    - >  $T_{\text{Startup\_Sig\_Proc}} = 324\mu\text{s}$  (Bit Rate Range 3)
    - >  $T_{\text{Bitcheck}} = 104\mu\text{s}$
  - 3V application; ASK mode, CLK\_OUT disabled
    - >  $I_{\text{Startup\_PLL}} = 4.5\text{mA}$
    - >  $I_{\text{Active}} = 6.5\text{mA}$
    - >  $I_{\text{Standby}} = 0.05\text{mA}$
    - >  $I_{\text{Polling}} = 0.545\text{mA}$

## 9. 3V Application

Figure 9-1. 3V Application

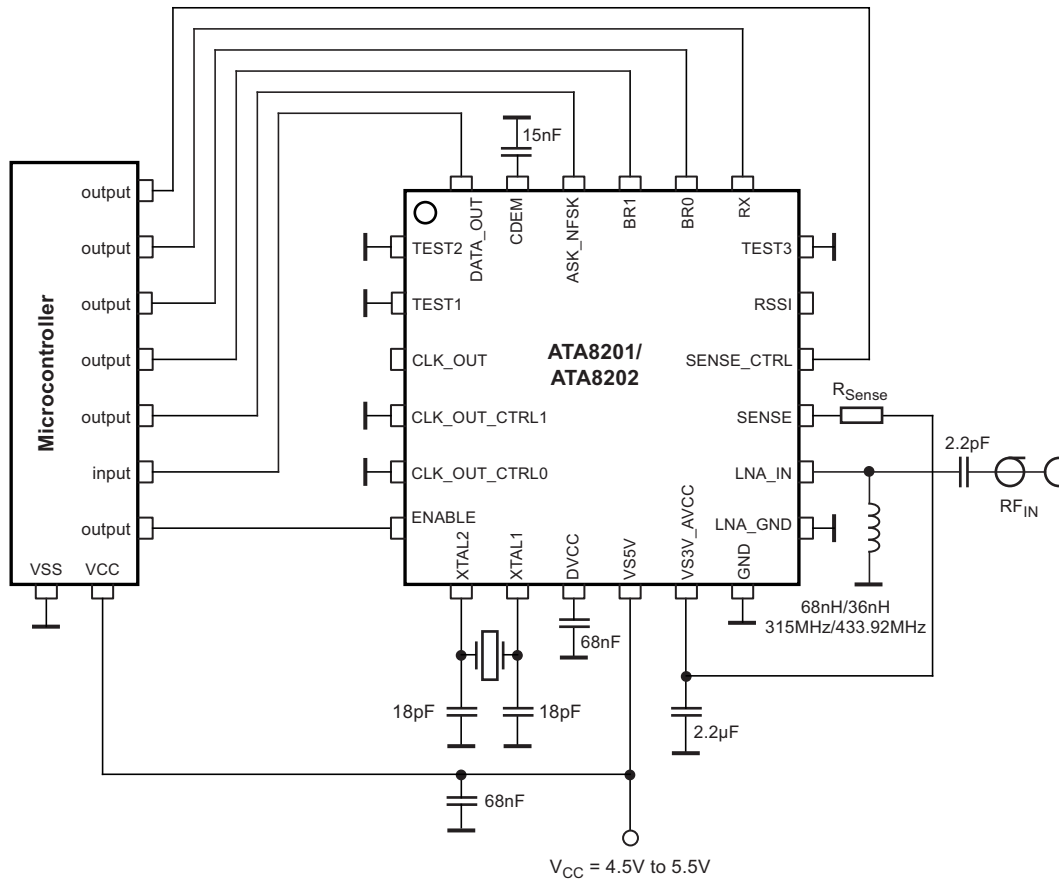


Note: Paddle (backplane) must be connected to GND



## 10. 5V Application

Figure 10-1. 5V Application with Reduced/Full Sensitivity



Note: Paddle (backplane) must be connected to GND

## 11. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
Junction temperature	$T_j$		+150	°C
Storage temperature	$T_{stg}$	-55	+125	°C
Ambient temperature	$T_{amb}$	-40	+85	°C
Supply voltage VS5V	$V_S$		+6	V
ESD (Human Body Model ESD S 5.1) every pin	HBM	-4	+4	kV
ESD (Machine Model JEDEC A115A) every pin	MM	-200	+200	V
ESD (Field Induced Charge Device Model ESD STM 5.3.1-1999) every pin	FCDM	-500	+500	V
Maximum input level, input matched to 50Ω	$P_{in\_max}$		0	dBm

## 12. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	$R_{thJA}$	35	K/W

## 13. Electrical Characteristics: General

All parameters refer to GND and are valid for  $T_{amb} = 25^\circ\text{C}$ ,  $V_{VS3V\_AVCC} = V_{VS5V} = 3\text{V}$ , and  $V_{VS5V} = 5\text{V}$ . Typical values are given at  $f_{RF} = 315\text{MHz}$  unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin <sup>(1)</sup>	Symbol	Min.	Typ.	Max.	Unit	Type*
1	OFF Mode								
1.1	Supply current in OFF mode	$V_{VS3V\_AVCC} = V_{VS5V} \leq 3\text{V}$ $V_{VS5V} = 5\text{V}$ CLK_OUT disabled	10, 11 10	$I_{SOFF}$			4 4	$\mu\text{A}$ $\mu\text{A}$	A A
2	Standby Mode								
2.1	Supply current Standby mode	XTO running $V_{VS3V\_AVCC} = V_{VS5V} \leq 3\text{V}$ CLK_OUT disabled	10, 11	$I_{Standby}$		50	100	$\mu\text{A}$	A
		XTO running $V_{VS5V} = 5\text{V}$ CLK_OUT disabled	10, 11	$I_{Standby}$		50	100	$\mu\text{A}$	A
2.2	System start-up time	XTO startup XTAL: $C_m = 5\text{fF}$ , $C_0 = 1.8\text{pF}$ , $R_m = 15\Omega$		$T_{XTO\_Startup}$		0.3		ms	A

\* Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in parenthesis were measured with RF\_IN matched to 50Ω according to Figure 2-1 on page 6 with component values as in Table 2-2 on page 7 (RF\_IN).

### 13. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for  $T_{amb} = 25^{\circ}\text{C}$ ,  $V_{VS3V\_AVCC} = V_{VS5V} = 3\text{V}$ , and  $V_{VS5V} = 5\text{V}$ . Typical values are given at  $f_{RF} = 315\text{MHz}$  unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin <sup>(1)</sup>	Symbol	Min.	Typ.	Max.	Unit	Type*	
2.3	Active mode start-up time	From Standby mode to Active mode BR_Range_3 Atmel ATA5745 Atmel ATA5746		$T_{Startup\_PLL} + T_{Startup\_Sig\_Proc}$			565 593	$\mu\text{s}$ $\mu\text{s}$	A	
<b>3 Active Mode</b>										
3.1	RF operating frequency range	Atmel ATA8201	14	$f_{RF}$	313		317	MHz	A	
		Atmel ATA8202	14	$f_{RF}$	433		435	MHz	A	
3.2	Supply current Active mode	$V_{VS3V\_AVCC} = V_{VS5V} = 3\text{V}$ ASK mode CLK_OUT disabled SENSE_CTRL = 0	10,11	$I_{Active}$		6.5		mA	A	
		$V_{VS3V\_AVCC} = V_{VS5V} = 3\text{V}$ FSK mode CLK_OUT disabled SENSE_CTRL = 0	10,11	$I_{Active}$		6.7		mA	A	
		$V_{VS5V} = 5\text{V}$ ASK mode CLK_OUT disabled SENSE_CTRL = 0	10	$I_{Active}$		6.7		mA	A	
		$V_{VS5V} = 5\text{V}$ FSK mode CLK_OUT disabled SENSE_CTRL = 0	10	$I_{Active}$		6.9		mA	A	
3.3	Supply current Polling mode	$V_{VS3V\_AVCC} = V_{VS5V} = 3\text{V}$ $T_{Polling\_Period} = 8\text{ms}$ BR_Range_3, ASK mode, CLK_OUT disabled Data rate = 9.6Kbits/s	10,11	$I_{Polling}$		545		$\mu\text{A}$	C	
3.4	Input sensitivity FSK $f_{RF} = 315\text{MHz}$	FSK deviation $f_{DEV} = \pm 38\text{kHz}$ BER = $10^{-3}$ $T_{amb} = 25^{\circ}\text{C}$								
		Bit rate 9.6Kbits/s BR2	(14)	$P_{REF\_FSK}$	-103	-105	-106.5	dBm	B	
		Bit rate 2.4Kbits/s BR0	(14)	$P_{REF\_FSK}$	-106	-108	-109.5	dBm	B	
		FSK deviation $\pm 18\text{kHz}$ to $\pm 50\text{kHz}$								
		Bit rate 9.6Kbits/s BR2	(14)	$P_{REF\_FSK}$	-101			dBm	B	
Bit rate 2.4Kbits/s BR0	(14)	$P_{REF\_FSK}$	-104			dBm	B			

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in parenthesis were measured with RF\_IN matched to 50 $\Omega$  according to Figure 2-1 on page 6 with component values as in Table 2-2 on page 7 (RF\_IN).

### 13. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for  $T_{amb} = 25^{\circ}\text{C}$ ,  $V_{VS3V\_AVCC} = V_{VS5V} = 3\text{V}$ , and  $V_{VS5V} = 5\text{V}$ . Typical values are given at  $f_{RF} = 315\text{MHz}$  unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin <sup>(1)</sup>	Symbol	Min.	Typ.	Max.	Unit	Type*	
3.5	Input sensitivity ASK $f_{RF} = 315\text{MHz}$	ASK 100% level of carrier, BER = $10^{-3}$ $T_{amb} = 25^{\circ}\text{C}$								
		Bit rate 9.6Kbits/s BR2	(14)	$P_{REF\_ASK}$	-109	-111	-112.5	dBm	B	
		Bit rate 2.4Kbits/s BR0	(14)	$P_{REF\_ASK}$	-112	-114	-115.5	dBm	B	
3.6	Sensitivity change at $f_{RF} = 433.92\text{MHz}$ compared to $f_{RF} = 315\text{MHz}$	$f_{RF} = 315\text{MHz}$ to $f_{RF} = 433.92\text{MHz}$ $P = P_{REF\_ASK} + \Delta P_{REF1}$ $P = P_{REF\_FSK} + \Delta P_{REF1}$	(14)	$\Delta P_{REF1}$		+1		dB	B	
3.7	Sensitivity change versus temperature, supply voltage and frequency offset	FSK $f_{DEV} = \pm 38\text{kHz}$ $\Delta f_{OFFSET} \leq \pm 160\text{kHz}$ ASK 100% $\Delta f_{OFFSET} \leq \pm 160\text{kHz}$ $P = P_{REF\_ASK} + \Delta P_{REF1} + \Delta P_{REF2}$ $P = P_{REF\_FSK} + \Delta P_{REF1} + \Delta P_{REF2}$	(14)	$\Delta P_{REF2}$	+4.5		-1.5		B	
3.8	Reduced sensitivity	$R_{Sense}$ connected from pin SENSE to pin VS3V_AVCC		$P_{Ref\_Red}$				dBm (peak level)		
		$R_{Sense} = 62\text{k}\Omega$ $f_{in} = 433.92\text{MHz}$				-76		dBm	C	
		$R_{Sense} = 82\text{k}\Omega$ $f_{in} = 433.92\text{MHz}$					-88		dBm	C
		$R_{Sense} = 62\text{k}\Omega$ $f_{in} = 315\text{MHz}$					-76		dBm	C
		$R_{Sense} = 82\text{k}\Omega$ $f_{in} = 315\text{MHz}$					-88		dBm	C
	Reduced sensitivity variation over full operating range	$R_{Sense} = 62\text{k}\Omega$ $R_{Sense} = 82\text{k}\Omega$ $P_{Red} = P_{Ref\_Red} + P_{\Delta Red}$			$\Delta P_{Red}$	-10		+10	dB	
3.9	Maximum frequency offset in FSK mode	Maximum frequency difference of $f_{RF}$ between receiver and transmitter in FSK mode ( $f_{RF}$ is the center frequency of the FSK signal with $f_{BIT} = 10\text{Kbits/s}$ , $f_{DEV} = \pm 38\text{kHz}$ )	(14)	$\Delta f_{OFFSET}$	-160		+160	kHz	B	

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in parenthesis were measured with RF\_IN matched to 50Ω according to Figure 2-1 on page 6 with component values as in Table 2-2 on page 7 (RF\_IN).

### 13. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for  $T_{amb} = 25^{\circ}\text{C}$ ,  $V_{VS3V\_AVCC} = V_{VS5V} = 3\text{V}$ , and  $V_{VS5V} = 5\text{V}$ . Typical values are given at  $f_{RF} = 315\text{MHz}$  unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin <sup>(1)</sup>	Symbol	Min.	Typ.	Max.	Unit	Type*
3.10	Supported FSK frequency deviation	With up to 2dB loss of sensitivity. Note that the tolerable frequency offset is 12kHz lower for $f_{DEV} = \pm 50\text{kHz}$ than for $f_{DEV} = \pm 38\text{kHz}$ , hence, $\Delta f_{OFFSET} \leq \pm 148\text{kHz}$	(14)	$f_{DEV}$	$\pm 18$	$\pm 38$	$\pm 50$	kHz	B
3.11	System noise figure	$f_{RF} = 315\text{MHz}$	(14)	NF		6.0	9	dB	B
		$f_{RF} = 433.92\text{MHz}$	(14)	NF		7.0	10	dB	B
3.12	Intermediate frequency	$f_{RF} = 433.92\text{MHz}$		$f_{IF}$		440		kHz	A
		$f_{RF} = 315\text{MHz}$		$f_{IF}$		440		kHz	A
3.13	System bandwidth	3dB bandwidth <b>This value is for information only!</b> Note that for crystal and system frequency offset calculations, $\Delta f_{OFFSET}$ must be used.	(14)	SBW		435		kHz	A
3.14	System out-band 3rd-order input intercept point	$\Delta f_{meas1} = 1.8\text{MHz}$ $\Delta f_{meas2} = 3.6\text{MHz}$ $f_{RF} = 315\text{MHz}$	(14)	IIP3		-24		dBm	C
		$f_{RF} = 433.92\text{MHz}$	(14)	IIP3		-23		dBm	C
3.15	System outband input 1-dB compression point	$\Delta f_{meas1} = 1\text{MHz}$ $f_{RF} = 315\text{MHz}$	(14)	I1dB <sub>BCP</sub>		-31	-36	dBm	C
		$f_{RF} = 433.92\text{MHz}$	(14)	I1dB <sub>BCP</sub>		-30	-35	dBm	C
3.16	LNA input impedance	$f_{RF} = 315\text{MHz}$	14	$Z_{in\_LNA}$		(72.4 - j298)		$\Omega$	C
		$f_{RF} = 433.92\text{MHz}$	14	$Z_{in\_LNA}$		(55 - j216)		$\Omega$	C
3.17	Maximum peak RF input level, ASK and FSK	BER < $10^{-3}$ , ASK: 100%	(14)	$P_{IN\_max}$		+5	-10	dBm	C
		FSK: $f_{DEV} = \pm 38\text{kHz}$	(14)	$P_{IN\_max}$		+5	-10	dBm	C
3.18	LO spurs at LNA_IN	$f < 1\text{GHz}$	(14)				-57	dBm	C
		$f > 1\text{GHz}$	(14)				-47	dBm	C
		$f_{LO} = 315.44\text{MHz}$ $2 \times f_{LO}$ $4 \times f_{LO}$	(14)			-90 -94 -68		dBm	C
		$f_{LO} = 434.36\text{MHz}$ $2 \times f_{LO}$ $4 \times f_{LO}$	(14)			-92 -88 -58		dBm	C
3.19	Image rejection	With the complete image band $f_{RF} = 315\text{MHz}$	(14)		24	30		dB	A
		$f_{RF} = 433.92\text{MHz}$	(14)		24	30		dB	A

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in parenthesis were measured with RF\_IN matched to 50 $\Omega$  according to Figure 2-1 on page 6 with component values as in Table 2-2 on page 7 (RF\_IN).

### 13. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for  $T_{amb} = 25^{\circ}\text{C}$ ,  $V_{VS3V\_AVCC} = V_{VS5V} = 3\text{V}$ , and  $V_{VS5V} = 5\text{V}$ . Typical values are given at  $f_{RF} = 315\text{MHz}$  unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin <sup>(1)</sup>	Symbol	Min.	Typ.	Max.	Unit	Type*
3.20	Useful signal to interferer ratio	Peak level of useful signal to peak level of interferer for BER < $10^{-3}$ with any modulation scheme of interferer							
		FSK BR_Ranges 0, 1, 2	(14)	$\text{SNR}_{\text{FSK0-2}}$		2	3	dB	B
		FSK BR_Range_3	(14)	$\text{SNR}_{\text{FSK3}}$		4	6	dB	B
		ASK ( $P_{RF} < P_{\text{RFIN\_High}}$ )	(14)	$\text{SNR}_{\text{ASK}}$		10	14	dB	B
3.21	RSSI output	Dynamic range	(14),17	$D_{\text{RSSI}}$		65		dB	A
		Lower level of range $f_{RF} = 315\text{MHz}$ $f_{RF} = 433.92\text{MHz}$	(14),17	$P_{\text{RFIN\_Low}}$		-110		dBm	A
		Upper level of range $f_{RF} = 315\text{MHz}$ $f_{RF} = 433.92\text{MHz}$	(14),17	$P_{\text{RFIN\_High}}$		-45		dBm	A
		Gain	(14),17			15		mV/dB	A
		Output voltage range	(14),17	$V_{\text{RSSI}}$	350		1675	mV	A
3.22	Output resistance RSSI pin		17	$R_{\text{RSSI}}$	8	10	12.5	k $\Omega$	C
3.23	Blocking	Sensitivity (BER = $10^{-3}$ ) is reduced by 3dB if a continuous wave blocking signal at $\pm\Delta f$ is $\Delta P_{\text{Block}}$ higher than the useful signal level (Bit rate = 10Kbits/s, FSK, $f_{\text{DEV}} \pm 38\text{kHz}$ , Manchester code, BR_Range2)							
		$f_{RF} = 315\text{MHz}$ $\Delta f \pm 1.5\text{MHz}$ $\Delta f \pm 2\text{MHz}$ $\Delta f \pm 3\text{MHz}$ $\Delta f \pm 10\text{MHz}$ $\Delta f \pm 20\text{MHz}$	(14)	$\Delta P_{\text{Block}}$		57.5 63.0 67.5 72.0 74.0		dBc	C
		$f_{RF} = 433.92\text{MHz}$ $\Delta f \pm 1.5\text{MHz}$ $\Delta f \pm 2\text{MHz}$ $\Delta f \pm 3\text{MHz}$ $\Delta f \pm 10\text{MHz}$ $\Delta f \pm 20\text{MHz}$	(14)	$\Delta P_{\text{Block}}$		56.5 62.0 66.5 71.0 73.0		dBc	C
3.24	CDEM	Capacitor connected to pin 23 (CDEM)	23		-5%	15	+5%	nF	D

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in parenthesis were measured with RF\_IN matched to 50 $\Omega$  according to Figure 2-1 on page 6 with component values as in Table 2-2 on page 7 (RF\_IN).

### 13. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for  $T_{amb} = 25^{\circ}\text{C}$ ,  $V_{VS3V\_AVCC} = V_{VS5V} = 3\text{V}$ , and  $V_{VS5V} = 5\text{V}$ . Typical values are given at  $f_{RF} = 315\text{MHz}$  unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin <sup>(1)</sup>	Symbol	Min.	Typ.	Max.	Unit	Type*		
4	XTO										
4.1	Transconductance XTO at start	At startup; after startup the amplitude is regulated to $V_{PPX\text{TAL}}$	7,8	$g_{m\_X\text{T}O}$		20		mS	B		
4.2	XTO start-up time	$C_0 \leq 2.2\text{pF}$ $C_m < 14\text{fF}$ $R_m \leq 120\Omega$	7,8	$T_{X\text{T}O\_Start\text{up}}$		300		$\mu\text{s}$	A		
4.3	Maximum $C_0$ of XTAL		7,8	$C_{0\text{max}}$			3.8	pF	D		
4.4	Pulling of LO frequency $f_{LO}$ due to XTO, $C_{L1}$ and $C_{L2}$ versus temperature and supply changes	$1.0\text{pF} \leq C_0 \leq 2.2\text{pF}$ $C_m = 4.0\text{fF}$ to $7.0\text{fF}$ $R_m \leq 120\Omega$	3	$\Delta f_{X\text{T}O}$	-5		+5	ppm	C		
4.5	Amplitude XTAL after startup	$C_m = 5\text{fF}$ , $C_0 = 1.8\text{pF}$ $R_m = 15\Omega$	7,8	$V_{PPX\text{TAL}}$		700		mVpp	C		
		$V(X\text{TAL}1)$ peak-to-peak value								$V_{PPX\text{TAL}}$	350
4.6	Maximum series resistance $R_m$ of XTAL at startup	$C_0 \leq 2.2\text{pF}$ , small signal start impedance, this value is important for crystal oscillator startup	7,8	$Z_{X\text{TAL}12\_START}$	-1400	-2000		$\Omega$	B		
4.7	Maximum series resistance $R_m$ of XTAL after startup	$C_0 \leq 2.2\text{pF}$ $C_m < 14\text{fF}$	7,8	$R_{m\_max}$		15	120	$\Omega$	B		
4.8	Nominal XTAL load resonant frequency	$f_{RF} = 433.92\text{MHz}$ $f_{RF} = 315\text{MHz}$	7,8	$f_{X\text{TAL}}$		13.57375 13.1433		MHz	D		
4.9	External CLK_OUT frequency	CLK_OUT_CTRL1 = 0 CLK_OUT_CTRL0 = 0 --> CLK_OUT disabled	3	$f_{CLK\_OUT}$			$f_{CLK}$ disabled (low level on pin CLK_OUT)		MHz	A	
		CLK_OUT_CTRL1 = 0 CLK_OUT_CTRL0 = 1 --> division ratio = 3									$f_{CLK} = \frac{f_{X\text{T}O}}{3}$
		CLK_OUT_CTRL1 = 1 CLK_OUT_CTRL0 = 0 --> division ratio = 6									$f_{CLK} = \frac{f_{X\text{T}O}}{6}$
		CLK_OUT_CTRL1 = 1 CLK_OUT_CTRL0 = 1 --> division ratio = 12									$f_{CLK} = \frac{f_{X\text{T}O}}{12}$

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in parenthesis were measured with RF\_IN matched to  $50\Omega$  according to Figure 2-1 on page 6 with component values as in Table 2-2 on page 7 ( $R_{F\text{IN}}$ ).

### 13. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for  $T_{amb} = 25^{\circ}\text{C}$ ,  $V_{VS3V\_AVCC} = V_{VS5V} = 3\text{V}$ , and  $V_{VS5V} = 5\text{V}$ . Typical values are given at  $f_{RF} = 315\text{MHz}$  unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin <sup>(1)</sup>	Symbol	Min.	Typ.	Max.	Unit	Type*
		$f_{RF} = 433.92\text{MHz}$ CLK_OUT division ratio = 3 = 6 = 12 CLK_OUT has nominal 50% duty cycle	3	$f_{CLK\_OUT}$		4.52458 2.26229 1.13114		MHz	D
		$f_{RF} = 315\text{MHz}$ CLK_OUT division ratio = 3 = 6 = 12 CLK_OUT has nominal 50% duty cycle	3	$f_{CLK\_OUT}$		4.3811 2.190 1.0952		MHz	D
4.10	DC voltage after startup	$V_{DC}$ (XTAL1, XTAL2) XTO running (Standby mode, Active mode)	7,8	$V_{DCXTO}$	-250	-45		mV	C
<b>5 Synthesizer</b>									
5.1	Spurs in Active mode	At $\pm f_{CLK\_OUT}$ CLK_OUT enabled (division ratio = 3) $f_{RF} = 315\text{MHz}$ $f_{RF} = 433.92\text{MHz}$		$SP_{RX}$		-75	-70	dBC	C
		at $\pm f_{XTO}$ $f_{RF} = 315\text{MHz}$ $f_{RF} = 433.92\text{MHz}$		$SP_{RX}$		-75	-70	dBC	A
5.2	Phase noise at 3 MHz Active mode	$f_{RF} = 315\text{MHz}$ $f_{RF} = 433.92\text{MHz}$		$L_{RX3M}$		-130	-127	dBC/Hz	A
5.3	Phase noise at 20 MHz Active mode	Noise floor		$L_{RX20M}$		-135	-132	dBC/Hz	B
<b>6 Microcontroller Interface</b>									
6.1	CLK_OUT output rise and fall time	$f_{CLK\_OUT} < 4.5\text{MHz}$ $C_L = 10\text{pF}$ $C_L = \text{Load capacitance on}$ pin CLK_OUT $2.7\text{V} \leq V_{VS5V} \leq 3.3\text{V}$ or $4.5\text{V} \leq V_{VS5V} \leq 5.5\text{V}$ 20% to 80% $V_{VS5V}$	3	$t_{rise}$ $t_{fall}$		20 20	30 30	ns ns	C
6.2	Internal equivalent capacitance	Used for current calculation	3	$C_{CLK\_OUT}$		8		pF	C

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in parenthesis were measured with RF\_IN matched to 50Ω according to Figure 2-1 on page 6 with component values as in Table 2-2 on page 7 (RF\_IN).



## 14. Electrical Characteristic: 3V Application

All parameters refer to GND and are valid for  $T_{amb} = 25^{\circ}\text{C}$ ,  $V_{VS3V\_AVCC} = V_{VS5V} = 3\text{V}$  and  $V_{VS5V} = 5\text{V}$ . Typical values are given at  $f_{RF} = 433.92\text{MHz}$  unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7	3V Application								
7.1	Supply current in OFF mode	$V_{VS3V\_AVCC} = V_{VS5V} \leq 3\text{V}$ CLK_OUT disabled	10, 11	$I_{SOFF}$			2	$\mu\text{A}$	A
7.2	Current in Standby mode (XTO is running)	$V_{VS3V\_AVCC} = V_{VS5V} \leq 3\text{V}$ external load C on pin CLK_OUT = 12pF CLK enabled (division ratio 3) CLK enabled (division ratio 6) CLK enabled (division ratio 12) CLK disabled	10, 11	$I_{Standby}$		420		$\mu\text{A}$	C
						290			C
						220			C
						50			A
7.3	Current during $T_{Startup\_PLL}$	$V_{VS3V\_AVCC} = V_{VS5V} \leq 3\text{V}$ CLK disabled	10, 11	$I_{Startup\_PLL}$		4.5		mA	C
7.4	Current in Active mode ASK	$V_{VS3V\_AVCC} = V_{VS5V} \leq 3\text{V}$ CLK disabled SENSE_CTRL = 0	10, 11	$I_{Active}$		6.5		mA	A
7.5	Current in Active mode FSK	$V_{VS3V\_AVCC} = V_{VS5V} \leq 3\text{V}$ CLK disabled SENSE_CTRL = 0	10, 11	$I_{Active}$		6.7		mA	A

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 15. Electrical Characteristics: 5V Application

All parameters refer to GND and are valid for  $T_{amb} = 25^{\circ}\text{C}$ ,  $V_{VS3V\_AVCC} = V_{VS5V} = 3\text{V}$  and  $V_{VS5V} = 5\text{V}$ . Typical values are given at  $f_{RF} = 433.92\text{MHz}$  unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8	5V Application								
8.1	Supply current in OFF mode	$V_{VS5V} = 5\text{V}$ CLK_OUT disabled	10	$I_{SOFF}$			2	$\mu\text{A}$	A
8.2	Current in Standby mode (XTO is running)	$V_{VS5V} \leq 5\text{V}$ external load C on pin CLK_OUT = 12pF CLK enabled	10	$I_{Standby}$		700		$\mu\text{A}$	C
		CLK enabled (division ratio 3)				490			C
		CLK enabled (division ratio 6)				370			C
		CLK enabled (division ratio 12) CLK disabled				50			A
8.3	Current during $T_{Startup\_PLL}$	$V_{VS5V} = 5\text{V}$ CLK disabled	10	$I_{Startup\_PLL}$		4.7		mA	C
8.4	Current in Active mode ASK	$V_{VS5V} = 5\text{V}$ CLK disabled SENSE_CTRL = 0	10	$I_{Active}$		6.7		mA	A
8.5	Current in Active mode FSK	$V_{VS5V} = 5\text{V}$ CLK disabled SENSE_CTRL = 0	10	$I_{Active}$		6.9		mA	A

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 16. Digital Timing Characteristics

All parameters refer to GND and are valid for  $T_{amb} = 25^{\circ}\text{C}$ ,  $V_{VS3V\_AVCC} = V_{VS5V} = 3\text{V}$ , and  $V_{VS5V} = 5\text{V}$ . Typical values are given at  $f_{RF} = 433.92\text{MHz}$  unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9	Basic Clock Cycle of the Digital Circuitry								
9.1	Basic clock cycle			$T_{DCLK}$	$16 / f_{XTO}$		$16 / f_{XTO}$	$\mu\text{s}$	A
9.2	Extended basic clock cycle	BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3		$T_{XDCLK}$	8 4 2 1 $\times T_{DCLK}$		8 4 2 1 $\times T_{DCLK}$	$\mu\text{s}$	A
10	Active Mode								
10.1	Startup PLL			$T_{Startup\_PLL}$			$15 \mu\text{s} + 208 \times T_{DCLK}$	$\mu\text{s}$	A
10.2	Startup signal processing	BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3		$T_{Startup\_Sig\_Proc}$	929.5 545.5 353.5 257.5 $\times T_{DCLK}$		929.5 545.5 353.5 257.5 $\times T_{DCLK}$		A
10.3	Bit rate range	ASK BR_Range = BR_Range0 BR_Range1 BR_Range2 BR_Range3 FSK BR_Range = BR_Range0 BR_Range1 BR_Range2 BR_Range3		BR_Range	1.0 2.0 4.0 8.0		2.5 5.0 10.0 10.0	Kbits/s	A
10.4	Minimum time period between edges at pin DATA_OUT	BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3	24	$T_{DATA\_OUT\_min}$	$10 \times T_{XDCLK}$			$\mu\text{s}$	A
10.5	Edge-to-edge time period of the data signal for full sensitivity in Active mode	BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3		$T_{DATA\_OUT}$	200 100 50 25		500 250 125 62.5	$\mu\text{s}$	B

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 17. Digital Port Characteristics

All parameters refer to GND and are valid for  $T_{amb} = 25^{\circ}\text{C}$ ,  $V_{VS3V\_AVCC} = V_{VS5V} = 3\text{V}$ , and  $V_{VS5V} = 5\text{V}$ . Typical values are given at  $f_{RF} = 433.92\text{MHz}$  unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
11	Digital Ports								
11.1	ENABLE input - Low level input voltage	$V_S = V_{VS3V\_AVCC} = V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} = 4.5\text{V to } 5.5\text{V}$	6	$V_{ll}$			$0.2 \times V_S$ $0.12 \times V_S$	V	A
	- High level input voltage	$V_S = V_{VS3V\_AVCC} = V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} = 4.5\text{V to } 5.5\text{V}$	6	$V_{lh}$	$0.8 \times V_S$			V	A
11.2	RX input - Low level input voltage	$V_S = V_{VS3V\_AVCC} = V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} = 4.5\text{V to } 5.5\text{V}$	19	$V_{ll}$			$0.2 \times V_S$ $0.12 \times V_S$	V	A
	- High level input voltage	$V_S = V_{VS3V\_AVCC} = V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} = 4.5\text{V to } 5.5\text{V}$	19	$V_{lh}$	$0.8 \times V_S$			V	A
11.3	BR0 input - Low level input voltage	$V_S = V_{VS3V\_AVCC} = V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} = 4.5\text{V to } 5.5\text{V}$	20	$V_{ll}$			$0.2 \times V_S$ $0.12 \times V_S$	V	A
	- High level input voltage	$V_S = V_{VS3V\_AVCC} = V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} = 4.5\text{V to } 5.5\text{V}$	20	$V_{lh}$	$0.8 \times V_S$			V	A
11.4	BR1 input - Low level input voltage	$V_S = V_{VS3V\_AVCC} = V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} = 4.5\text{V to } 5.5\text{V}$	21	$V_{ll}$			$0.2 \times V_S$ $0.12 \times V_S$	V	A
	- High level input voltage	$V_S = V_{VS3V\_AVCC} = V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} = 4.5\text{V to } 5.5\text{V}$	21	$V_{lh}$	$0.8 \times V_S$			V	A
11.5	ASK_NFSK input - Low level input voltage	$V_S = V_{VS3V\_AVCC} = V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} = 4.5\text{V to } 5.5\text{V}$	22	$V_{ll}$			$0.2 \times V_S$ $0.12 \times V_S$	V	A
	- High level input voltage	$V_S = V_{VS3V\_AVCC} = V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} = 4.5\text{V to } 5.5\text{V}$	22	$V_{lh}$	$0.8 \times V_S$			V	A

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 17. Digital Port Characteristics (Continued)

All parameters refer to GND and are valid for  $T_{amb} = 25^{\circ}\text{C}$ ,  $V_{VS3V\_AVCC} = V_{VS5V} = 3\text{V}$ , and  $V_{VS5V} = 5\text{V}$ . Typical values are given at  $f_{RF} = 433.92\text{MHz}$  unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
11.6	SENSE_CTRL input - Low level input voltage	$V_S = V_{VS3V\_AVCC} =$ $V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} =$ $4.5\text{V to } 5.5\text{V}$	16	$V_{ll}$			$0.2 \times V_S$ $0.12 \times V_S$	V	A
	- High level input voltage	$V_S = V_{VS3V\_AVCC} =$ $V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} =$ $4.5\text{V to } 5.5\text{V}$	16	$V_{lh}$	$0.8 \times V_S$			V	A
11.7	CLK_OUT_CTRL0 input - Low level input voltage	$V_S = V_{VS3V\_AVCC} =$ $V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} =$ $4.5\text{V to } 5.5\text{V}$	5	$V_{ll}$			$0.2 \times V_S$ $0.12 \times V_S$	V	A
	- High level input voltage	$V_S = V_{VS3V\_AVCC} =$ $V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} =$ $4.5\text{V to } 5.5\text{V}$	5	$V_{lh}$	$0.8 \times V_S$			V	A
11.8	CLK_OUT_CTRL1 input - Low level input voltage	$V_S = V_{VS3V\_AVCC} =$ $V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} =$ $4.5\text{V to } 5.5\text{V}$	4	$V_{ll}$			$0.2 \times V_S$ $0.12 \times V_S$	V	A
	- High level input voltage	$V_S = V_{VS3V\_AVCC} =$ $V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} =$ $4.5\text{V to } 5.5\text{V}$	4	$V_{lh}$	$0.8 \times V_S$			V	A
11.9	TEST1 input	TEST1 input must always be connected directly to GND	2		0		0	V	D
11.10	TEST2 output	TEST2 output must always be connected directly to GND	1		0		0	V	D
11.11	TEST3 input	TEST3 input must always be connected directly to GND	18		0		0	V	D

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 17. Digital Port Characteristics (Continued)

All parameters refer to GND and are valid for  $T_{amb} = 25^{\circ}\text{C}$ ,  $V_{VS3V\_AVCC} = V_{VS5V} = 3\text{V}$ , and  $V_{VS5V} = 5\text{V}$ . Typical values are given at  $f_{RF} = 433.92\text{MHz}$  unless otherwise specified. Details about current consumption, timing, and digital pin properties can be found in the specific sections of the “Electrical Characteristics”

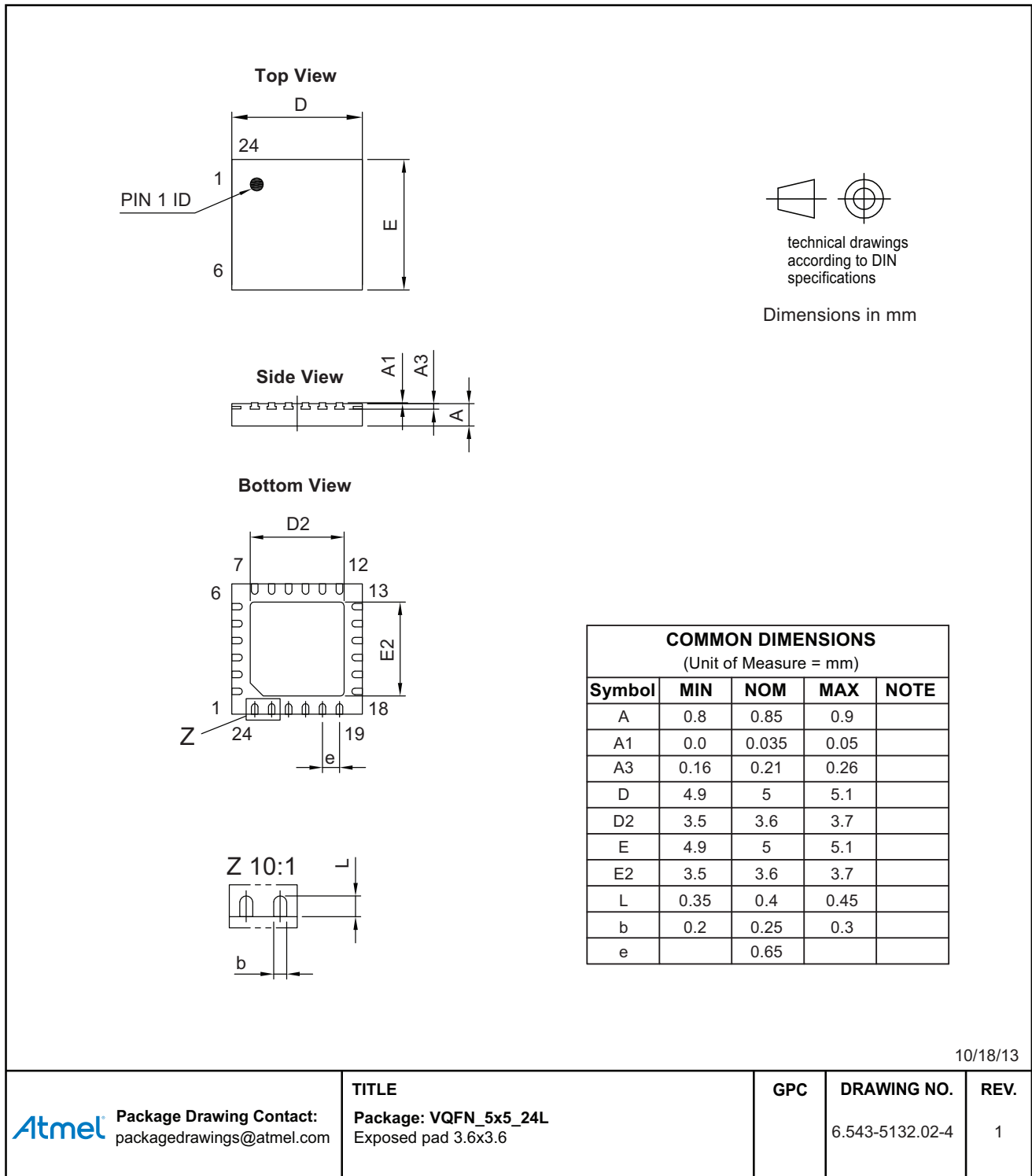
No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
11.12	DATA_OUT output - Saturation voltage low	$V_S = V_{VS3V\_AVCC} =$ $V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} =$ $4.5\text{V to } 5.5\text{V}$ $I_{DATA\_OUT} = 250\mu\text{A}$	24	$V_{ol}$		0.15	0.4	V	B
	- Saturation voltage high	$V_S = V_{VS3V\_AVCC} =$ $V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} =$ $4.5\text{V to } 5.5\text{V}$ $I_{DATA\_OUT} = -250\mu\text{A}$	24	$V_{oh}$	$V_{VS} - 0.4$	$V_{VS} -$ $0.15$		V	B
11.13	CLK_OUT output - Saturation voltage low	$V_S = V_{VS3V\_AVCC} =$ $V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} =$ $4.5\text{V to } 5.5\text{V}$ $I_{DATA\_OUT} = 100\mu\text{A}$	3	$V_{ol}$		0.15	0.4	V	B
	- Saturation voltage high	$V_S = V_{VS3V\_AVCC} =$ $V_{VS5V} = 2.7\text{V to } 3.3\text{V}$ $V_S = V_{VS5V} =$ $4.5\text{V to } 5.5\text{V}$ $I_{DATA\_OUT} = -100\mu\text{A}$	3	$V_{oh}$	$V_{VS} - 0.4$	$V_{VS} -$ $0.15$		V	B

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 18. Ordering Information

Extended Type Number	Package	MOQ	Remarks
ATA8202C-PXQW-1	QFN24	6000pcs	5mm × 5mm, Pb-free, 433.92MHz
ATA8201C-PXQW-1	QFN24	6000pcs	5mm × 5mm, Pb-free, 315MHz

## 19. Package Information



## 20. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4971G-INDCO-09/14	<ul style="list-style-type: none"><li>• Section 18 “Ordering Information” on page 39 updated</li><li>• Section 19 “Package Information” on page 39 updated</li></ul>
4971F-INDCO-07/14	<ul style="list-style-type: none"><li>• Put datasheet in the latest template</li></ul>
4971E-INDCO-12/12	<ul style="list-style-type: none"><li>• Section 18 “Ordering Information” on page 39 changed</li></ul>
4971D-INDCO-07/12	<ul style="list-style-type: none"><li>• Section 13 “Electrical Characteristics: General” on pages 26 to 32 changed</li><li>• Section 14 “Electrical Characteristic: 3V Application” on page 33 changed</li><li>• Section 15 “Electrical Characteristic: 5V Application” on page 34 changed</li><li>• Section 18 “Ordering Information” on page 39 changed</li></ul>
4971C-INDCO-04/09	<ul style="list-style-type: none"><li>• Put datasheet in the newest template</li><li>• Benefits on page 2 updated</li></ul>
4971B-INDCO-10/07	<ul style="list-style-type: none"><li>• Put datasheet in the newest template</li></ul>





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