



ATmega165A/PA/325A/PA/ 3250A/PA/645A/P/6450A/P

Silicon Errata and Data Sheet Clarification

Introduction

The ATmega165A/PA/325A/PA/3250A/PA/645A/P/6450A/P devices you have received conform functionally to the current device data sheet (www.microchip.com/mymicrochip/filehandler.aspx?ddocname=en598315), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATmega165A/PA/325A/PA/3250A/PA/645A/P/6450A/P devices.

Note:

- This document summarizes all the silicon errata issues from all silicon revisions, previous and current

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1. Silicon Issue Summary

- Erratum is not applicable.
- X** Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision				
		ATmega165A/PA			ATmega325A/PA ATmega3250A/PA	ATmega645A/P ATmega6450A/P
		Rev. I ⁽¹⁾	Rev. J	Rev. K	Rev. D ⁽¹⁾	Rev. B ⁽¹⁾
Timer	2.2.1 Interrupts may be lost when writing the timer registers in the asynchronous timer	X	X	X	X	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

- Erratum is not applicable.
- X Erratum is applicable.

2.2 Timer

2.2.1 Interrupts May Be Lost When Writing the Timer Registers in the Asynchronous Timer

The interrupt will be lost if writing a timer register that is a synchronous timer clock when the asynchronous Timer/Counter register (TCNTx) is 0x00.

Work Around

Always check that the asynchronous Timer/Counter register neither has the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

Affected Silicon Revisions

ATmega165A/PA		
Rev. I	Rev. J	Rev. K
X	X	X

ATmega325A/PA/3250A/PA
Rev. D
X

ATmega645A/P/6450A/P
Rev. B
X

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (www.microchip.com/mymicrochip/filehandler.aspx?ddocname=en598315).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Errata Section in Data Sheet is no Longer Valid

A clarification for the Errata section in the device data sheet has been made.

The errata content has been moved to a separate document, *ATmega165A/PA/325A/PA/3250A/PA/645A/P/6450A/P Silicon Errata and Data Sheet Clarifications* (this document).

See the *Silicon Errata Issues* section of this document for the latest errata.

3.2 Boot Loader

3.2.1 Boot Loader Parameters for ATmega165A/PA

A clarification has been made to list the *Boot loader parameters* and the *Read-While-Write limits* for ATmega165A/PA.

Table 3-1. Boot Size Configuration (ATmega165A/PA)⁽¹⁾

BOOTSZ1	BOOTSZ0	Boot Size	Pages	Application Flash Section	Boot Loader Flash Section	End Application Section	Boot Reset Address (Start Boot Loader Section)
1	1	128 words	2	0x0000 - 0x1F7F	0x1F80 - 0x1FFF	0x1F7F	0x1F80
1	0	256 words	4	0x0000 - 0x1EFF	0x1F00 - 0x1FFF	0x1EFF	0x1F00
0	1	512 words	8	0x0000 - 0x1DFF	0x1E00 - 0x1FFF	0x1DFF	0x1E00
0	0	1024 words	16	0x0000 - 0x1BFF	0x1C00 - 0x1FFF	0x1BFF	0x1C00

Note: The *Figure Memory sections* shows the different BOOTSZ Fuse configurations..

Table 3-2. Read-While-Write limit (ATmega165A/PA)⁽¹⁾

Section	Pages	Address
Read-While-Write (RWW) section	112	0x0000 - 0x1BFF
No Read-While-Write (NRWW) section	16	0x1C00 - 0x1FFF

Note: For details about these two sections, see *NRWW – No Read-While-Write Section* and *RWW – Read-While-Write Section*.

3.2.2 Boot Loader Parameters for ATmega325A/PA/3250A/PA

A clarification has been made to list the *Boot loader parameters* and the *Read-While-Write limits* for ATmega325A/PA/3250A/PA.

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Table 3-3. Boot Size configuration (ATmega325A/PA/3250A/PA)⁽¹⁾

BOOTSZ1	BOOTSZ0	Boot Size	Pages	Application Flash Section	Boot Loader Flash Section	End Application Section	Boot Reset Address (Start Boot Loader Section)
1	1	256 words	4	0x0000 - 0x3EFF	0x3F00 - 0x3FFF	0x3EFF	0x3F00
1	0	512 words	8	0x0000 - 0x3DFF	0x3E00 - 0x3FFF	0x3DFF	0x3E00
0	1	1024 words	16	0x0000 - 0x3BFF	0x3C00 - 0x3FFF	0x3BFF	0x3C00
0	0	2048 words	32	0x0000 - 0x37FF	0x3800 - 0x3FFF	0x37FF	0x3800

Note: The *Figure Memory sections* shows the different BOOTSZ Fuse configurations.

Table 3-4. Read-While-Write Limit (ATmega325A/PA/3250A/PA)⁽¹⁾

Section	Pages	Address
Read-While-Write (RWW) section	224	0x0000 - 0x37FF
No Read-While-Write (NRWW) section	32	0x3800 - 0x3FFF

Note: For details about these two sections, see *NRWW – No Read-While-Write Section* and *RWW – Read-While-Write Section*.

3.2.3 Boot Loader Parameters for ATmega645A/P/6450A/P

A clarification has been made to list the *Boot loader parameters* and the *Read-While-Write limits* for ATmega645A/P/6450A/P.

Table 3-5. Boot Size Configuration (ATmega645A/P/6450A/P)⁽¹⁾

BOOTSZ1	BOOTSZ0	Boot Size	Pages	Application Flash Section	Boot Loader Flash Section	End Application Section	Boot Reset Address (Start Boot Loader Section)
1	1	512 words	4	0x0000 - 0x7DFF	0x7E00 - 0x7FFF	0x7DFF	0x7E00
1	0	1024 words	8	0x0000 - 0x7BFF	0x7C00 - 0x7FFF	0x7BFF	0x7C00
0	1	2048 words	16	0x0000 - 0x77FF	0x7800 - 0x7FFF	0x77FF	0x7800
0	0	4096 words	32	0x0000 - 0x6FFF	0x7000 - 0x7FFF	0x6FFF	0x7000

Note: The *Figure Memory sections* shows the different BOOTSZ Fuse configurations.

Table 3-6. Read-While-Write Limit (ATmega645A/P/6450A/P)⁽¹⁾

Section	Pages	Address
Read-While-Write (RWW) section	224	0x0000 - 0x6FFF
No Read-While-Write (NRWW) section	32	0x7000 - 0x7FFF

Note: For details about these two sections, see *NRWW – No Read-While-Write Section* and *RWW – Read-While-Write Section*.

3.3 Power Management and Sleep Modes

3.3.1 Power Management and Sleep Modes

A clarification has been made to the *Active clock domains and wake-up sources in the different sleep modes* table to make the headings visible.

Table 10-1. Active Clock Domains and Wake-Up Sources in the Different Sleep Modes

Sleep Mode	Active Clock Domains					Oscillators		Wake-up Sources							Software BOD Disable
	clk _{CPU}	clk _{FLASH}	clk _{I/O}	clk _{ADC}	clk _{ASY}	Main Clock Source Enabled	Timer Osc Enabled	INT0 and Pin Change	USI Start Condition	LCD Controller	Timer2	SPM/ EEPROM Ready	ADC	Other I/O	
Idle			X	X	X	X	X ⁽²⁾	X	X	X	X	X	X	X	
ADC NRM				X	X	X	X ⁽²⁾	X ⁽³⁾	X	X ⁽²⁾	X ⁽²⁾	X	X		
Power-down								X ⁽³⁾	X						X
Power-save					X		X	X ⁽³⁾	X	X	X				X
Standby ⁽¹⁾						X		X ⁽³⁾	X						X

Notes:

1. Only recommended with external XTAL or resonator selected as clock source.
2. If Timer/Counter2 is running in asynchronous mode.
3. For INT0, only level interrupt.

3.4 Interrupts

3.4.1 Interrupt Vectors in ATmega165A/PA/325A/PA/3250A/PA/645A/P/6450A/P

A clarification for the source names of the **Interrupt Vectors** has been made to comply with the header file naming convention.

Table 3-7. Reset and Interrupt Vectors in ATmega165A/PA/325A/PA/645A/P

Vector No	Program Address ⁽²⁾	Source	Interrupts Definition
1	0x0000 ⁽¹⁾	RESET	External pin, Power-on Reset, Brown-out Reset, Watchdog System Reset and JTAG AVR Reset
2	0x0002	INT0	External Interrupt Request 0
3	0x0004	PCINT0	Pin Change Interrupt Request 0
4	0x0006	PCINT1	Pin Change Interrupt Request 1
5	0x0008	TIMER2_COMP	Timer/Counter2 Compare Match

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Vector No	Program Address ⁽²⁾	Source	Interrupts Definition
6	0x000A	TIMER2_OVF	Timer/Counter2 Overflow
7	0x000C	TIMER1_CAPT	Timer/Counter1 Capture Event
8	0x000E	TIMER1_COMPA	Timer/Counter1 Compare Match A
9	0x0010	TIMER1_COMPB	Timer/Counter1 Compare Match B
10	0x0012	TIMER1_OVF	Timer/Counter1 Overflow
11	0x0014	TIMER0_COMP	Timer/Counter0 Compare Match
12	0x0016	TIMER0_OVF	Timer/Counter0 Overflow
13	0x0018	SPI_STC	SPI Serial Transfer Complete
14	0x001A	USART0_RX	USART Receive complete
15	0x001C	USART0_UDRE	USART Data Register Empty
16	0x001E	USART0_TX	USART Transmit complete
17	0x0020	USI_START	USI Start Condition
18	0x0022	USI_OVERFLOW	USI Overflow
19	0x0024	ANALOG_COMP	Analog Comparator
20	0x0026	ADC	ADC Conversion complete
21	0x0028	EE_READY	EEPROM Ready
22	0x002A	SPM_READY	Store Program Memory Ready

Notes:

1. When the BOOTRST fuse is programmed, the device will jump to the boot loader address at Reset. See “*Boot Loader Support – Read-While-Write Self-Programming*”.
2. When setting the IVSEL bit in MCUCR, Interrupt Vectors will be moved to the start of the boot Flash section. The address of each Interrupt Vector will then be the address in this table added to the start address of the boot Flash section.

The table below shows Reset and Interrupt Vectors placement for the different BOOTRST and IVSEL settings combinations. If the program never enables an interrupt source, the Interrupt Vectors are not used, and regularly program code can be placed at these locations. This is also the case if the Reset Vector is in the Application section while the Interrupt Vectors are in the Boot section or vice versa.

Table 3-8. Reset and Interrupt Vectors Placement

BOOTRST ⁽¹⁾	IVSEL	Reset Address	Interrupt Vectors Start Address
1	0	0x000	0x002
1	1	0x000	Boot Reset Address + 0x0002
0	0	Boot Reset Address	0x002
0	1	Boot Reset Address	Boot Reset Address + 0x0002

Note: 1. For the BOOTRST Fuse, “1” means unprogrammed, while “0” means programmed.

The most typical and general program setup for the Reset and Interrupt Vector Addresses are:

Address	Labels	Code	Comments
0x0000		jmp	RESET ; Reset Handler
0x0002		jmp	INT0 ; IRQ0 Handler


```

0x0004      jmp      PCINT0      ; PCINT0 Handler
0x0006      jmp      PCINT1      ; PCINT1 Handler
0x0008      jmp      TIMER2_COMP ; Timer2 CompareA Handler
0x000A      jmp      TIMER2_OVF  ; Timer2 Overflow Handler
0x000C      jmp      TIMER1_CAPT ; Timer1 Capture Handler
0x000E      jmp      TIMER1_COMPA ; Timer1 CompareA Handler
0x0010      jmp      TIMER1_COMPB ; Timer1 CompareB Handler
0x0012      jmp      TIMER1_OVF  ; Timer1 Overflow Handler
0x0014      jmp      TIMER0_COMP ; Timer0 Compare Handler
0x0016      jmp      TIMER0_OVF  ; Timer0 Overflow Handler
0x0018      jmp      SPI_STC     ; SPI Transfer Complete Handler
0x001A      jmp      USART0_RX   ; USART RX Complete Handler
0x001C      jmp      USART0_UDRE ; USART UDR Empty Handler
0x0020      jmp      USI_START   ; USI Start Condition Handler
0x0022      jmp      USI_UDREOVERFLOW ; USI Overflow Handler
0x0024      jmp      ANALOG_COMP ; Analog Comparator Handler
0x0026      jmp      ADC         ; ADC Conversion Complete Handler
0x0028      jmp      EE_READY    ; EEPROM Ready Handler
0x002A      jmp      SPM_READY   ; SPM Ready Handler
;
0x0034      RESET:    ldi        r16,high(RAMEND) ; Main program start
0x0035      out        SPH,r16      ; Set Stack Pointer to top of RAM
0x0036      ldi        r16,low(RAMEND)
0x0037      out        SPL,r16
0x0038      sei                          ; Enable interrupts
0x0039      <instr> xxx
...         ...         ...         ...

```

When the BOOTRST Fuse is unprogrammed, the Boot section size is set to 2 KB, and the MCUCR.IVSEL is set before any interrupts are enabled, the most typical and general program setup for the Reset and Interrupt Vector Addresses are:

```

Address  Labels  Code  Comments
0x0000  RESET:    ldi    r16,high(RAMEND) ; Main program start
0x0001      out    SPH,r16      ; Set Stack Pointer to top of RAM
0x0002      ldi    r16,low(RAMEND)
0x0003      out    SPL,r16
0x0004      sei                          ; Enable interrupts
0x0005      <instr> xxx
;
.org 0x1C02
0x1C02      jmp    EXT_INT0      ; IRQ0 Handler
0x1C04      jmp    EXT_INT1      ; IRQ1 Handler
...         ...         ...         ;
0x1C32      jmp    SPM_RDY      ; SPM Ready Handler

```

When the BOOTRST Fuse is programmed and the Boot section size is set to 2 KB, the most typical and general program setup for the Reset and Interrupt Vector Addresses are:

```

Address  Labels  Code  Comments
.org 0x0002
0x0002      jmp    EXT_INT0      ; IRQ0 Handler
0x0004      jmp    EXT_INT1      ; IRQ1 Handler
...         ...         ...         ;
0x0032      jmp    SPM_RDY      ; SPM Ready Handler
;
.org 0x1C00
0x1C00  RESET:    ldi    r16,high(RAMEND) ; Main program start
0x1C01      out    SPH,r16      ; Set Stack Pointer to top of RAM
0x1C02      ldi    r16,low(RAMEND)
0x1C03      out    SPL,r16
0x1C04      sei                          ; Enable interrupts
0x1C05      <instr> xxx

```

When the BOOTRST Fuse is programmed, the Boot section size is set to 2 KB, and the MCUCR.IVSEL is set before any interrupts are enabled, the most typical and general program setup for the Reset and Interrupt Vector Addresses are:

```

Address  Labels  Code  Comments
;
.org 0x1C00
0x1C00      jmp    RESET      ; Reset handler

```

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```

0x1C02      jmp      EXT_INT0      ; IRQ0 Handler
0x1C04      jmp      EXT_INT1      ; IRQ1 Handler
...
0x1C32      jmp      SPM_RDY       ; SPM Ready Handler
;
0x1C34      RESET:    ldi      r16,high(RAMEND) ; Main program start
0x1C35      out      SPH,r16       ; Set Stack Pointer to top of RAM
0x1C36      ldi      r16,low(RAMEND)
0x1C37      out      SPL,r16
0x1C38      sei                          ; Enable interrupts
0x1C39      <instr> xxx
    
```

Table 3-9. Reset and Interrupt Vectors in ATmega3250A/PA/6450A/P

Vector No	Program Address ⁽²⁾	Source	Interrupts definition
1	0x0000 ⁽¹⁾	RESET	External pin, Power-on Reset, Brown-out Reset, Watchdog Reset and JTAG AVR Reset.
2	0x0002	INT0	External Interrupt Request 0
3	0x0004	PCINT0	Pin Change Interrupt Request 0
4	0x0006	PCINT1	Pin Change Interrupt Request 1
5	0x0008	TIMER2_COMP	Timer/Counter2 Compare Match
6	0x000A	TIMER2_OVF	Timer/Counter2 Overflow
7	0x000C	TIMER1_CAPT	Timer/Counter1 Capture Event
8	0x000E	TIMER1_COMPA	Timer/Counter1 Compare Match A
9	0x0010	TIMER1_COMPB	Timer/Counter1 Compare Match B
10	0x0012	TIMER1_OVF	Timer/Counter1 Overflow
11	0x0014	TIMER0_COMP	Timer/Counter0 Compare Match
12	0x0016	TIMER0_OVF	Timer/Counter0 Overflow
13	0x0018	SPI_STC	SPI Serial Transfer Complete
14	0x001A	USART0_RX	USART0 Receive complete
15	0x001C	USART0_UDRE	USART Data Register Empty
16	0x001E	USART0_TX	USART Transmit complete
17	0x0020	USI_START	USI Start condition
18	0x0022	USI_OVERFLOW	USI Overflow
19	0x0024	ANALOG_COMP	Analog Comparator
20	0x0026	ADC	ADC Conversion complete
21	0x0028	EE_READY	EEPROM Ready
22	0x002A	SPM_READY	Store Program Memory Ready
23	0x002C	NOT_USED	Reserved
24	0x002E	PCINT2	Pin Change Interrupt Request 2
25	0x0030	PCINT3	Pin Change Interrupt Request 3

Notes:

1. When the BOTRST fuse is programmed, the device will jump to the boot loader address at Reset. See “*Boot Loader Support – Read-While-Write Self-Programming*”.
2. When setting the IVSEL bit in MCUCR, Interrupt Vectors will be moved to the start of the boot Flash section. The address of each Interrupt Vector will then be the address in this table added to the start address of the boot Flash section.

The most typical and general program setup for the Reset and Interrupt Vector Addresses is:

Address	Labels	Code	Comments
0x0000		jmp RESET	; Reset Handler
0x0002		jmp INT0	; IRQ0 Handler
0x0004		jmp PCINT0	; PCINT0 Handler
0x0006		jmp PCINT1	; PCINT1 Handler
0x0008		jmp TIMER2_COMP	; Timer2 CompareA Handler
0x000A		jmp TIMER2_OVF	; Timer2 Overflow Handler
0x000C		jmp TIMER1_CAPT	; Timer1 Capture Handler
0x000E		jmp TIMER1_COMPA	; Timer1 CompareA Handler
0x0010		jmp TIMER1_COMPB	; Timer1 CompareB Handler
0x0012		jmp TIMER1_OVF	; Timer1 Overflow Handler
0x0014		jmp TIMER0_COMP	; Timer0 Compare Handler
0x0016		jmp TIMER0_OVF	; Timer0 Overflow Handler
0x0018		jmp SPI_STC	; SPI Transfer Complete Handler
0x001A		jmp USART0_RX	; USART RX Complete Handler
0x001C		jmp USART0_UDRE	; USART UDR Empty Handler
0x0020		jmp USI_START	; USI Start Condition Handler
0x0022		jmp USI_UDREOVERFLOW	; USI Overflow Handler
0x0024		jmp ANALOG_COMP	; Analog Comparator Handler
0x0026		jmp ADC	; ADC Conversion Complete Handler
0x0028		jmp EE_READY	; EEPROM Ready Handler
0x002A		jmp SPM_READY	; SPM Ready Handler
0x002C		jmp NOT_USED	; Reserved Handler
0x002E		jmp PCINT2	; PCINT2 Handler Handler
0x0030		jmp PCINT3	; PCINT3 Handler Handler
		;	
0x0034	RESET:	ldi r16,high(RAMEND)	; Main program start
0x0035		out SPH,r16	; Set Stack Pointer to top of RAM
0x0036		ldi r16,low(RAMEND)	
0x0037		out SPL,r16	
0x0038		sei	; Enable interrupts
0x0039		<instr> xxx	
...

3.5 Electrical Characteristics -TA = -40°C to 85°C

3.5.1 Analog Input Offset Voltage (TA = -40°C to 85°C)

A clarification has been made for the “Analog Comparator Input Offset Voltage”.

Table 3-10. TA = -40°C to 85°C, VCC = 1.8V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V _{IL}	Input low voltage, except XTAL1 pin	V _{CC} = 1.8-2.4V	-0.5		0.2V _{CC} ⁽¹⁾	V
		V _{CC} = 2.4-5.5V	-0.5		0.3V _{CC} ⁽¹⁾	
V _{IL1}	Input low voltage, XTAL1 pin	V _{CC} = 1.8-5.5V	-0.5		0.1V _{CC} ⁽¹⁾	
V _{IH}	Input high voltage, except XTAL1 and RESET pins	V _{CC} = 1.8-2.4V	0.7V _{CC} ⁽²⁾		V _{CC} + 0.5	
		V _{CC} = 2.4-5.5V	0.6V _{CC} ⁽²⁾		V _{CC} + 0.5	
V _{IH1}	Input high voltage, XTAL1 pin	V _{CC} = 1.8-2.4V	0.8V _{CC} ⁽²⁾		V _{CC} + 0.5	
		V _{CC} = 2.4-5.5V	0.7V _{CC} ⁽²⁾		V _{CC} + 0.5	
V _{IH2}	Input high voltage, RESET pin	V _{CC} = 1.8-5.5V	0.85V _{CC} ⁽²⁾		V _{CC} + 0.5	
V _{OL}	Output low voltage ⁽³⁾ , Port A, C, D, E, F, G, H, J	I _{OL} = 10 mA, V _{CC} = 5V I _{OL} = 5 mA, V _{CC} = 3V			0.9 0.6	
V _{OL1}	Output low voltage ⁽³⁾ , Port B	I _{OL} = 20 mA, V _{CC} = 5V I _{OL} = 10 mA, V _{CC} = 3V			0.9 0.6	
V _{OH}	Output high voltage ⁽⁴⁾ , Port A, C, D, E, F, G, H, J	I _{OH} = -10 mA, V _{CC} = 5V	4.2			
		I _{OH} = -5 mA, V _{CC} = 3V	2.3			
V _{OH1}	Output high voltage ⁽⁴⁾ , Port B	I _{OH} = -20 mA, V _{CC} = 5V	4.2			
		I _{OH} = -10 mA, V _{CC} = 3V	2.3			
I _{IL}	Input leakage current I/O Pin	V _{CC} = 5.5V, pin low (absolute value)			1	μA
I _{IH}	Input leakage current I/O Pin	V _{CC} = 5.5V, pin high (absolute value)			1	
R _{RST}	Reset pull-up resistor		20		100	kΩ
R _{PU}	I/O Pin pull-up resistor		20		100	kΩ
V _{ACIO}	Analog comparator input offset voltage	V _{CC} = 5V V _{in} = V _{CC} /2		< 10	40	mV
V _{ACIO}	Analog comparator input offset voltage	V_{CC} < 3.6V V_{in} < 0.5V		<15	60⁽⁵⁾	mV
V _{ACIO}	Analog comparator input offset voltage	V_{CC} > 3.6V V_{in} < 0.5V		<15	500⁽⁵⁾	mV
I _{ACLK}	Analog comparator	V _{CC} = 5V V _{in} = V _{CC} /2	-50		50	nA

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Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t _{ACID}	Analog comparator propagation delay	V _{CC} = 2.7V		750		ns
		V _{CC} = 4.0V		500		

Notes:

1. "Max" means the highest value where the pin is ensured to be read as low.
2. "Min" means the lowest value where the pin is ensured to be read as high.
3. Although each I/O port can sink more than the test conditions (20 mA at V_{CC} = 5V, 10 mA at V_{CC} = 3V for Port B and 10 mA at V_{CC} = 5V, 5 mA at V_{CC} = 3V for all other ports) under steady-state conditions (non-transient), observe the following:
 - TQFP and QFN/MLF Package:
 - i. For all ports, the sum of all I_{OL} may not exceed 400 mA.
 - ii. For ports A0 - A7, C4 - C7, and G2, the sum of all I_{OL} may not exceed 100 mA.
 - iii. For ports B0 - B7, E0 - E7, and G3 - G5, the sum of all I_{OL} may not exceed 100 mA.
 - iv. For ports D0 - D7, C0 - C3, and G0 - G1, the sum of all I_{OL} may not exceed 100 mA.
 - v. For ports F0 - F7, the sum of all I_{OL} may not exceed 100 mA.

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not ensured to sink current higher than the listed test condition.
4. Although each I/O port can source more than the test conditions (20 mA at V_{CC} = 5V, 10 mA at V_{CC} = 3V for Port B and 10 mA at V_{CC} = 5V, 5 mA at V_{CC} = 3V for all other ports) under steady-state conditions (non-transient), observe the following:
 - TQFP and QFN/MLF Package:
 - i. For all ports, the sum of all I_{OH} may not exceed 400 mA.
 - ii. For ports A0 - A7, C4 - C7, and G2, the sum of all I_{OH} may not exceed 100 mA.
 - iii. For ports B0 - B7, E0 - E7, and G3 - G5, the sum of all I_{OH} may not exceed 100 mA.
 - iv. For ports D0 - D7, C0 - C3, and G0 - G1, the sum of all I_{OH} may not exceed 100 mA.
 - v. For ports F0 - F7, the sum of all I_{OH} may not exceed 100 mA.

If I_{OH} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not ensured to source current higher than the listed test condition.
5. **These values are based on characterization. The maximum limit in production can, therefore, not be assured.**

3.5.2 Power-Down Specification Limit ($T_A = -40^{\circ}\text{C}$ to 85°C)

A clarification for the power-down specification limit has been made. This clarification has corrections that are impractical to mark in bold. The following tables in this section contain the most current information and notes.

Table 3-11. ATmega165A DC Characteristics. $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 1.8\text{V}$ to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current ⁽¹⁾	Active 1 MHz, $V_{CC} = 2\text{V}$		0.35	1.0	mA
		Active 4 MHz, $V_{CC} = 3\text{V}$		2.3	3.5	
		Active 8 MHz, $V_{CC} = 5\text{V}$		8.4	12.0	
		Idle 1 MHz, $V_{CC} = 2\text{V}$		0.1	0.45	
		Idle 4 MHz, $V_{CC} = 3\text{V}$		0.7	1.2	
		Idle 8 MHz, $V_{CC} = 5\text{V}$		3.0	5.5	
	Power-save mode ⁽²⁾	32.768 kHz TOSC enabled, $V_{CC} = 1.8\text{V}$		0.55		μA
		32.768 kHz TOSC enabled, $V_{CC} = 3\text{V}$		0.8		
	Power-down mode ⁽²⁾	WDT enabled, $V_{CC} = 3\text{V}$		6.0	15	
		WDT disabled, $V_{CC} = 3\text{V}$		0.2	3.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C . Maximum values are test limits in production.**

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Table 3-12. ATmega165PA DC Characteristics. $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 1.8\text{V}$ to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current ⁽¹⁾	Active 1 MHz, $V_{CC} = 2\text{V}$		0.35	0.44	mA
		Active 4 MHz, $V_{CC} = 3\text{V}$		2.3	2.5	
		Active 8 MHz, $V_{CC} = 5\text{V}$		8.4	9.5	
		Idle 1 MHz, $V_{CC} = 2\text{V}$		0.1	0.2	
		Idle 4 MHz, $V_{CC} = 3\text{V}$		0.7	0.8	
		Idle 8 MHz, $V_{CC} = 5\text{V}$		3.0	3.3	
	Power-save mode ⁽²⁾	32.768 kHz TOSC enabled, $V_{CC} = 1.8\text{V}$		0.55		μA
		32.768 kHz TOSC enabled, $V_{CC} = 3\text{V}$		0.8		
	Power-down mode ⁽²⁾	WDT enabled, $V_{CC} = 3\text{V}$		6.0	10.0	
		WDT disabled, $V_{CC} = 3\text{V}$		0.2	2.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C . Maximum values are test limits in production.**

Table 3-13. ATmega325A DC Characteristics. $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 1.8\text{V}$ to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current ⁽¹⁾	Active 1 MHz, $V_{CC} = 2\text{V}$		0.8	1.5	mA
		Active 4 MHz, $V_{CC} = 3\text{V}$		2.6	3.5	
		Active 8 MHz, $V_{CC} = 5\text{V}$		6.0	12.0	
		Idle 1 MHz, $V_{CC} = 2\text{V}$		0.2	0.45	
		Idle 4 MHz, $V_{CC} = 3\text{V}$		0.7	1.5	
		Idle 8 MHz, $V_{CC} = 5\text{V}$		1.8	5.5	
	Power-save mode ⁽²⁾	32.768 kHz TOSC enabled, $V_{CC} = 1.8\text{V}$		0.75		μA
		32.768 kHz TOSC enabled, $V_{CC} = 3\text{V}$		0.8		
	Power-down mode ⁽²⁾	WDT enabled, $V_{CC} = 3\text{V}$		7.5	15.0	
		WDT disabled, $V_{CC} = 3\text{V}$		0.3	3.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C . Maximum values are test limits in production.**

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Table 3-14. ATmega325PA DC Characteristics. $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 1.8\text{V}$ to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current ⁽¹⁾	Active 1 MHz, $V_{CC} = 2\text{V}$		0.37	0.55	mA
		Active 4 MHz, $V_{CC} = 3\text{V}$		2.4	2.9	
		Active 8 MHz, $V_{CC} = 5\text{V}$		5.3	11.0	
		Idle 1 MHz, $V_{CC} = 2\text{V}$		0.14	0.25	
		Idle 4 MHz, $V_{CC} = 3\text{V}$		0.6	0.9	
		Idle 8 MHz, $V_{CC} = 5\text{V}$		1.6	3.5	
	Power-save mode ⁽²⁾	32.768 kHz TOSC enabled, $V_{CC} = 1.8\text{V}$		0.75		μA
		32.768 kHz TOSC enabled, $V_{CC} = 3\text{V}$		0.8		
	Power-down mode ⁽²⁾	WDT enabled, $V_{CC} = 3\text{V}$		6.7	12.0	
		WDT disabled, $V_{CC} = 3\text{V}$		0.2	2.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C . Maximum values are test limits in production.**

Table 3-15. ATmega3250A DC Characteristics. $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 1.8\text{V}$ to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current ⁽¹⁾	Active 1 MHz, $V_{CC} = 2\text{V}$		0.8	1.5	mA
		Active 4 MHz, $V_{CC} = 3\text{V}$		2.6	3.5	
		Active 8 MHz, $V_{CC} = 5\text{V}$		6.0	12.0	
		Idle 1 MHz, $V_{CC} = 2\text{V}$		0.2	0.45	
		Idle 4 MHz, $V_{CC} = 3\text{V}$		0.7	1.5	
		Idle 8 MHz, $V_{CC} = 5\text{V}$		1.8	5.5	
	Power-save mode ⁽²⁾	32.768 kHz TOSC enabled, $V_{CC} = 1.8\text{V}$		0.75		μA
		32.768 kHz TOSC enabled, $V_{CC} = 3\text{V}$		0.8		
	Power-down mode ⁽²⁾	WDT enabled, $V_{CC} = 3\text{V}$		7.5	15.0	
		WDT disabled, $V_{CC} = 3\text{V}$		0.3	3.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C . Maximum values are test limits in production.**

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Table 3-16. ATmega3250PA DC Characteristics. $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 1.8\text{V}$ to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current ⁽¹⁾	Active 1 MHz, $V_{CC} = 2\text{V}$		0.37	0.55	mA
		Active 4 MHz, $V_{CC} = 3\text{V}$		2.4	2.9	
		Active 8 MHz, $V_{CC} = 5\text{V}$		5.3	11.0	
		Idle 1 MHz, $V_{CC} = 2\text{V}$		0.14	0.25	
		Idle 4 MHz, $V_{CC} = 3\text{V}$		0.6	0.9	
		Idle 8 MHz, $V_{CC} = 5\text{V}$		1.6	3.5	
	Power-save mode ⁽²⁾	32.768 kHz TOSC enabled, $V_{CC} = 1.8\text{V}$		0.75		μA
		32.768 kHz TOSC enabled, $V_{CC} = 3\text{V}$		0.8		
	Power-down mode ⁽²⁾	WDT enabled, $V_{CC} = 3\text{V}$		6.7	12.0	
		WDT disabled, $V_{CC} = 3\text{V}$		0.2	2.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C . Maximum values are test limits in production.**

Table 3-17. ATmega645A DC Characteristics. $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 1.8\text{V}$ to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current ⁽¹⁾	Active 1 MHz, $V_{CC} = 2\text{V}$		1.1	1.5	mA
		Active 4 MHz, $V_{CC} = 3\text{V}$		2.8	3.5	
		Active 8 MHz, $V_{CC} = 5\text{V}$		7.0	12.0	
		Idle 1 MHz, $V_{CC} = 2\text{V}$		0.3	0.45	
		Idle 4 MHz, $V_{CC} = 3\text{V}$		0.8	1.5	
		Idle 8 MHz, $V_{CC} = 5\text{V}$		2.5	5.5	
	Power-save mode ⁽²⁾	32.768 kHz TOSC enabled, $V_{CC} = 1.8\text{V}$		0.75		μA
		32.768 kHz TOSC enabled, $V_{CC} = 3\text{V}$		0.8		
	Power-down mode ⁽²⁾	WDT enabled, $V_{CC} = 3\text{V}$		7.0	15.0	
		WDT disabled, $V_{CC} = 3\text{V}$		0.25	3.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C . Maximum values are test limits in production.**

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Table 3-18. ATmega645P DC Characteristics. $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 1.8\text{V}$ to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current ⁽¹⁾	Active 1 MHz, $V_{CC} = 2\text{V}$		1.04	0.55	mA
		Active 4 MHz, $V_{CC} = 3\text{V}$		1.7	2.9	
		V_{CC} 8 MHz, $V_{CC} = 5\text{V}$		5.8	11.0	
		Idle 1 MHz, $V_{CC} = 2\text{V}$		0.25	0.25	
		Idle 4 MHz, $V_{CC} = 3\text{V}$		0.39	0.90	
		Idle 8 MHz, $V_{CC} = 5\text{V}$		1.6	3.50	
	Power-save mode ⁽²⁾	32.768 kHz TOSC enabled, $V_{CC} = 1.8\text{V}$		0.75		μA
		32.768 kHz TOSC enabled, $V_{CC} = 3\text{V}$		0.8		
	Power-down mode ⁽²⁾	WDT enabled, $V_{CC} = 3\text{V}$		7.0	10.0	
		WDT disabled, $V_{CC} = 3\text{V}$		0.25	2.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C . Maximum values are test limits in production.**

Table 3-19. ATmega6450A DC Characteristics. $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 1.8\text{V}$ to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current ⁽¹⁾	Active 1 MHz, $V_{CC} = 2\text{V}$		1.1	1.5	mA
		Active 4 MHz, $V_{CC} = 3\text{V}$		2.8	3.5	
		Active 8 MHz, $V_{CC} = 5\text{V}$		7.0	12.0	
		Idle 1 MHz, $V_{CC} = 2\text{V}$		0.3	0.45	
		Idle 4 MHz, $V_{CC} = 3\text{V}$		0.8	1.5	
		Idle 8 MHz, $V_{CC} = 5\text{V}$		2.5	5.5	
	Power-save mode ⁽²⁾	32.768 kHz TOSC enabled, $V_{CC} = 1.8\text{V}$		0.75		μA
		32.768 kHz TOSC enabled, $V_{CC} = 3\text{V}$		0.8		
	Power-down mode ⁽²⁾	WDT enabled, $V_{CC} = 3\text{V}$		7.0	15.0	
		WDT disabled, $V_{CC} = 3\text{V}$		0.25	3.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C . Maximum values are test limits in production.**

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Table 3-20. ATmega6450P DC Characteristics. $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 1.8\text{V}$ to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units	
I_{CC}	Power supply current ⁽¹⁾	Active 1 MHz, $V_{CC} = 2\text{V}$		1.04	0.55	mA	
		Active 4 MHz, $V_{CC} = 3\text{V}$		1.7	2.9		
		Active 8 MHz, $V_{CC} = 5\text{V}$		5.8	11.0		
		Idle 1 MHz, $V_{CC} = 2\text{V}$		0.25	0.25		
		Idle 4 MHz, $V_{CC} = 3\text{V}$		0.39	0.90		
		Idle 8 MHz, $V_{CC} = 5\text{V}$		1.6	3.50		
	Power-save mode ⁽²⁾	Power-save mode ⁽²⁾	32.768 kHz TOSC enabled, $V_{CC} = 1.8\text{V}$		0.75		μA
			32.768 kHz TOSC enabled, $V_{CC} = 3\text{V}$		0.8		
		Power-down mode ⁽²⁾	WDT enabled, $V_{CC} = 3\text{V}$		7.0	10.0	
			WDT disabled, $V_{CC} = 3\text{V}$		0.25	2.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

3.6 Electrical Characteristics -TA = -40°C to 105°C

3.6.1 Analog Input Offset Voltage (TA = -40°C to 105°C)

A clarification has been made for the “Analog Comparator Input Offset Voltage” in the following table.

Table 3-21. TA = -40°C to 105°C, VCC = 1.8V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V _{IL}	Input low voltage except XTAL1 and RESET pins	V _{CC} = 1.8-2.4V	-0.5		0.2V _{CC} ⁽¹⁾	V
		V _{CC} = 2.4-5.5V	-0.5		0.3V _{CC} ⁽¹⁾	
V _{IL1}	Input low voltage XTAL1 pins	V _{CC} = 1.8-5.5V	-0.5		0.1V _{CC} ⁽¹⁾	
V _{IL2}	Input low voltage, $\overline{\text{RESET}}$ pins	V _{CC} = 1.8-5.5V	-0.5		0.1V _{CC} ⁽¹⁾	
V _{IH}	Input high voltage except XTAL1 and $\overline{\text{RESET}}$ pins	V _{CC} = 1.8-2.4V	0.7V _{CC} ⁽²⁾		V _{CC} + 0.5	
		V _{CC} = 2.4-5.5V	0.6V _{CC} ⁽²⁾		V _{CC} + 0.5	
V _{IH1}	Input high voltage, XTAL1 pin	V _{CC} = 1.8-2.4V	0.8V _{CC} ⁽²⁾		V _{CC} + 0.5	
		V _{CC} = 2.4-5.5V	0.7V _{CC} ⁽²⁾		V _{CC} + 0.5	
V _{IH2}	Input high voltage, $\overline{\text{RESET}}$ pins	V _{CC} = 1.8-5.5V	0.9V _{CC} ⁽²⁾		V _{CC} + 0.5	
V _{OL}	Output low voltage ⁽³⁾ , Port A, C, D, E, F, G	I _{OL} = 10 mA, V _{CC} = 5V			0.7/1.0 ⁽⁵⁾	
		I _{OL} = 5 mA, V _{CC} = 3V			0.5/0.7 ⁽⁵⁾	
V _{OL1}	Output low voltage ⁽³⁾ , Port B	I _{OL} = 20 mA, V _{CC} = 5V			0.7/1.0 ⁽⁵⁾	
		I _{OL} = 10 mA, V _{CC} = 3V			0.5/0.7 ⁽⁵⁾	
V _{OH}	Output high voltage ⁽⁴⁾ , Port A, C, D, E, F, G	I _{OH} = -10 mA, V _{CC} = 5V	4.2			
		I _{OH} = -5 mA, V _{CC} = 3V	2.3			
V _{OH1}	Output high voltage ⁽⁴⁾ , Port B	I _{OH} = -20 mA, V _{CC} = 5V	4.2			
		I _{OH} = -10 mA, V _{CC} = 3V	2.3			
I _{IL}	Input leakage current I/O Pin	V _{CC} = 5.5V, pin low (absolute value)			1	μA
I _{IH}	Input leakage current I/O Pin	V _{CC} = 5.5V, pin high (absolute value)			1	
R _{RST}	Reset pull-up resistor		20		60	kΩ
R _{PU}	I/O Pin pull-up resistor		20		50	
V _{ACIO}	Analog comparator input offset voltage	V _{CC} = 5V V _{in} = V _{CC} /2		< 10	40	mV
V _{ACIO}	Analog comparator input offset voltage	V_{CC} < 3.6V V_{in} < 0.5V		<15	60⁽⁶⁾	mV
V _{ACIO}	Analog comparator input offset voltage	V_{CC} > 3.6V V_{in} < 0.5V		<15	500⁽⁶⁾	mV
I _{ACLK}	Analog comparator	V _{CC} = 5V V _{in} = V _{CC} /2	-50		50	nA

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.....continued						
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t _{ACID}	Analog comparator propagation delay	V _{CC} = 2.7V		750		ns
		V _{CC} = 4.0V		500		

Notes:

1. "Max" means the highest value where the pin is ensured to be read as low.
2. "Min" means the lowest value where the pin is ensured to be read as high.
3. Although each I/O port can sink more than the test conditions (20 mA at V_{CC} = 5V, 10 mA at V_{CC} = 3V for Port B and 10 mA at V_{CC} = 5V, 5 mA at V_{CC} = 3V for all other ports) under steady-state conditions (non-transient), the following must be observed.
 - TQFP and QFN/MLF Package:
 - i. For all ports, the sum of all I_{OL} may not exceed 400 mA.
 - ii. For ports A0 - A7, C4 - C7, and G2, the sum of all I_{OL} may not exceed 100 mA.
 - iii. For ports B0 - B7, E0 - E7, and G3 - G5, the sum of all I_{OL} may not exceed 100 mA.
 - iv. For ports D0 - D7, C0 - C3, and G0 - G1, the sum of all I_{OL} may not exceed 100 mA.
 - v. For ports F0 - F7, the sum of all I_{OL} may not exceed 100 mA.

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not ensured to sink current higher than the listed test condition.
4. Although each I/O port can source more than the test conditions (20 mA at V_{CC} = 5V, 10 mA at V_{CC} = 3V for Port B and 10 mA at V_{CC} = 5V, 5 mA at V_{CC} = 3V for all other ports) under steady-state conditions (non-transient), observe the following:
 - TQFP and QFN/MLF Package:
 - i. For all ports, the sum of all I_{OH} may not exceed 400 mA.
 - ii. For ports A0 - A7, C4 - C7, and G2, the sum of all I_{OH} may not exceed 100 mA.
 - iii. For ports B0 - B7, E0 - E7, and G3 - G5, the sum of all I_{OH} may not exceed 100 mA.
 - iv. For ports D0 - D7, C0 - C3, and G0 - G1, the sum of all I_{OH} may not exceed 100 mA.
 - v. For ports F0 - F7, the sum of all I_{OH} may not exceed 100 mA.

If I_{OH} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not ensured to source current higher than the listed test condition.
5. Largest value for ATmega325PA and ATmega3250PA.
6. **These values are based on characterization. The maximum limit in production can, therefore, not be assured.**

3.6.2 Power-Down Specification Limit ($T_A = -40^{\circ}\text{C}$ to 105°C)

A clarification for the power-down specification limit has been made. This clarification has corrections that are impractical to mark in bold. The following tables in this section contain the most current information and notes.

Table 3-22. Current Consumption ATmega165PA $T_A = -40^{\circ}\text{C}$ to 105°C , $V_{CC} = 1.8\text{V}$ to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current ⁽¹⁾	Active 1 MHz, $V_{CC} = 2\text{V}$		0.4	0.5	mA
		Active 4 MHz, $V_{CC} = 3\text{V}$		2.3	2.8	
		Active 8 MHz, $V_{CC} = 5\text{V}$		9	11	
		Idle 1 MHz, $V_{CC} = 2\text{V}$		0.1	0.2	mA
		Idle 4 MHz, $V_{CC} = 3\text{V}$		0.8	0.9	
		Idle 8 MHz, $V_{CC} = 5\text{V}$		3.1	3.3	
	Power-save mode ⁽²⁾	32.768 kHz TOSC enabled, $V_{CC} = 1.8\text{V}$		0.6	1.8	μA
		32.768 kHz TOSC enabled, $V_{CC} = 3\text{V}$		0.9	3	
	Power-down mode ⁽²⁾	WDT enabled, $V_{CC} = 3\text{V}$		7	11	
		WDT disabled, $V_{CC} = 3\text{V}$		0.2	2.5	

Note:

1. **Maximum and Typical values for 25°C . Maximum values are test limits in production.**

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Table 3-23. Current Consumption ATmega325A $T_A = -40^{\circ}\text{C}$ to 105°C , $V_{CC} = 1.8\text{V}$ to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units	
I_{CC}	Power supply current ⁽¹⁾	Active 1 MHz, $V_{CC} = 2\text{V}$		0.35	0.55	mA	
		Active 4 MHz, $V_{CC} = 3\text{V}$		1.65	2.9		
		Active 8 MHz, $V_{CC} = 5\text{V}$		5.7	11		
		Idle 1 MHz, $V_{CC} = 2\text{V}$		0.1	0.2		
		Idle 4 MHz, $V_{CC} = 3\text{V}$		0.4	0.90		
		Idle 8 MHz, $V_{CC} = 5\text{V}$		1.65	3.5		
	Power-save mode ⁽²⁾	32.768 kHz TOSC enabled, $V_{CC} = 1.8\text{V}$					μA
		32.768 kHz TOSC enabled, $V_{CC} = 3\text{V}$			3		
	Power-down mode ⁽²⁾	WDT enabled, $V_{CC} = 3\text{V}$			12	15	
		WDT disabled, $V_{CC} = 3\text{V}$			4.7	5	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

Table 3-24. Current Consumption ATmega325PA $T_A = -40^{\circ}\text{C}$ to 105°C , $V_{CC} = 1.8\text{V}$ to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units	
I_{CC}	Power supply current ⁽¹⁾	Active 1 MHz, $V_{CC} = 2\text{V}$		0.35	0.55	mA	
		Active 4 MHz, $V_{CC} = 3\text{V}$		1.65	2.9		
		Active 8 MHz, $V_{CC} = 5\text{V}$		5.7	11		
		Idle 1 MHz, $V_{CC} = 2\text{V}$		0.1	0.2		
		Idle 4 MHz, $V_{CC} = 3\text{V}$		0.4	0.90		
		Idle 8 Hz, $V_{CC} = 5\text{V}$		1.65	3.5		
	Power-save mode ⁽²⁾	32.768 kHz TOSC enabled, $V_{CC} = 1.8\text{V}$					μA
		32.768 kHz TOSC enabled, $V_{CC} = 3\text{V}$			3		
	Power-down mode ⁽²⁾	WDT enabled, $V_{CC} = 3\text{V}$			12	15	
		WDT disabled, $V_{CC} = 3\text{V}$			4.7	5	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

ATmega165A/PA/325A/PA/3250A/PA/645A...

Data Sheet Clarifications

Table 3-25. Current Consumption ATmega3250A $T_A = -40^{\circ}\text{C}$ to 105°C , $V_{CC} = 1.8\text{V}$ to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units	
I_{CC}	Power supply current ⁽¹⁾	Active 1 MHz, $V_{CC} = 2\text{V}$		0.35	0.55	mA	
		Active 4 MHz, $V_{CC} = 3\text{V}$		1.65	2.9		
		Active 8 MHz, $V_{CC} = 5\text{V}$		5.7	11		
		Idle 1 MHz, $V_{CC} = 2\text{V}$		0.1	0.2		
		Idle 4 MHz, $V_{CC} = 3\text{V}$		0.4	0.90		
		Idle 8 MHz, $V_{CC} = 5\text{V}$		1.65	3.5		
	Power-save mode ⁽²⁾	32.768 kHz TOSC enabled, $V_{CC} = 1.8\text{V}$					μA
		32.768 kHz TOSC enabled, $V_{CC} = 3\text{V}$			3		
	Power-down mode ⁽²⁾	WDT enabled, $V_{CC} = 3\text{V}$			12	15	
		WDT disabled, $V_{CC} = 3\text{V}$			4.7	5	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C . Maximum values are test limits in production.**

Table 3-26. Current Consumption ATmega3250PA $T_A = -40^{\circ}\text{C}$ to 105°C , $V_{CC} = 1.8\text{V}$ to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units	
I_{CC}	Power supply current ⁽¹⁾	Active 1 MHz, $V_{CC} = 2\text{V}$		0.35	0.55	mA	
		Active 4 MHz, $V_{CC} = 3\text{V}$		1.65	2.9		
		Active 8 MHz, $V_{CC} = 5\text{V}$		5.7	11		
		Idle 1 MHz, $V_{CC} = 2\text{V}$		0.1	0.2		
		Idle 4 MHz, $V_{CC} = 3\text{V}$		0.4	0.90		
		Idle 8 MHz, $V_{CC} = 5\text{V}$		1.65	3.5		
	Power-save mode ⁽²⁾	32.768 kHz TOSC enabled, $V_{CC} = 1.8\text{V}$					μA
		32.768 kHz TOSC enabled, $V_{CC} = 3\text{V}$			3		
	Power-down mode ⁽²⁾	WDT enabled, $V_{CC} = 3\text{V}$			12	15	
		WDT disabled, $V_{CC} = 3\text{V}$			4.7	5	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C . Maximum values are test limits in production.**

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc Rev.	Date	Comments
A	02/2023	<p>Initial document release.</p> <ul style="list-style-type: none"> Content moved from the data sheet and restructured to the new document template Updated the die revision list to reflect die revisions in production <p>Silicon Errata added:</p> <ul style="list-style-type: none"> Timer: 2.2.1. Interrupts May Be Lost When Writing the Timer Registers in the Asynchronous Timer <p>Data Sheet Clarifications added:</p> <ul style="list-style-type: none"> Errata section in data sheet is no longer valid Boot Loader <ul style="list-style-type: none"> 3.2.1. Boot Loader Parameters for ATmega165A/PA 3.2.2. Boot Loader Parameters for ATmega325A/PA/3250A/PA 3.2.3. Boot Loader Parameters for ATmega645A/P/6450A/P Power Management and Sleep Modes: 3.3.1. Power Management and Sleep Modes Interrupt Vectors: 3.4.1. Interrupt Vectors in ATmega165A/PA/325A/PA/3250A/PA/645A/P/6450A/P Electrical Characteristics – TA = -40°C to 85°C: <ul style="list-style-type: none"> 3.5.1. Analog Input Offset Voltage (TA = -40°C to 85°C) 3.5.2. Power-Down Specification Limit (TA = -40°C to 85°C) Electrical Characteristics – TA = -40°C to 105°C: <ul style="list-style-type: none"> 3.6.1. Analog Input Offset Voltage (TA = -40°C to 105°C) 3.6.2. Power-Down Specification Limit (TA = -40°C to 105°C)

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