
PL360-EK User Guide

Introduction

PL360-EK is an evaluation kit for the PL360 modem for Power Line Communication (PLC) from Microchip Technology Inc. PL360 is a multi-protocol device implementing a very flexible architecture, which allows implementation of standard and customized PLC solutions.

PL360 has been conceived to be bundled with an external Microchip MCU, which controls the PL360 PLC modem.

PL360MB is PLC multi-purpose modem board based on the PL360 transceiver and on the SAM4CMS16C ARM[®] Cortex™ M4 microcontroller. This development board provides a full featured platform to develop a complete communications system over PLC technology and to demonstrate the high accuracy single phase energy metering functions of ATSAM4CMS16C device. Microchip provides coupling reference designs for different load options, targeting common configurations in standard frequency bands complying with existing regulations (CENELEC, FCC and ARIB).

Contents

- Welcome letter introducing the evaluation kit and its contents
- Boards:
 - Two PL360MBv1 modem boards
 - Two PLCOUP007v2.5 coupling boards (CENELEC A-Band)
 - Two PLCOUP006v2 coupling boards (FCC frequency band)
- Cables:
 - Two micro A/B-type USB cables
 - Two power cord cables IEC320-C8
- Jumpers:
 - Two jumpers with pitch 5.08 mm
 - Two jumpers with pitch 2.54 mm

Features

- PL360 is a compact and highly efficient device for a wide range of Smart Grid applications such as smart metering (smart meters and data concentrators), lighting, industrial/home automation, home and building energy management systems, solar energy and Plug-in Hybrid Electric Vehicle (PHEV) charging stations, among others
- PL360 used as G3-PLC or PRIME device includes enhanced features such as additional robust modes and frequency band extension (up to 472 kHz)
- PL360MB board mounts a PL360 transceiver and a SAM4CMS16C ARM Cortex M4 microcontroller. This development board provides a full featured platform to develop a complete communications system based on PLC technology, and lets designers evaluate the accuracy of single phase energy metering SoC and develop code for smart energy applications. PL360MB board provides support for:

- PLC band characterization
- Noise level measurement
- PLC and metrology sensitivity level measurement
- Maximum reachable distance
- Power consumption
- Check PLC performance in different bands (CENELEC, FCC, ARIB) setting different PLC coupling boards (provided with this evaluation kit)
- Evaluate the high accuracy of single phase energy metering measurements with CT, shunt or Rogowski coil sensors
- Opto Port Interface compliant with ANSI C12.20 protocol
- Metering Pulses output pins (Wh, VAh, VAh)
- Battery-backed Real-Time Clock (RTC)
- Power fail detection
- On board Relay Driver circuitry
- PL360MB board can be supplied with 100/115/230 V_{AC} 50-60 Hz power input
- PL360MB board includes a JTAG interface for MCU debugging and programming purposes and two debugging UARTs. And also it provides battery backup and a slow crystal oscillator to support SAM4CMS16C embedded RTC and low power modes. Several wake-up conditions are available, such as mains crossover detection, voltage rails recovery condition, anti-tampering sources (TMP0 pad) and Force Wake-up (FWUP) pin

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1. Evaluation Kit Specifications

1.1 Safety Recommendations

These development boards must be only used by expert technicians. PL360MB is directly powered from mains grid, so hazardous voltage (100/115/230V_{AC}) is present on the board. To avoid user access to dangerous parts, PL360MB must always be used within its enclosure. All required connectors and configuration jumpers are easily accessible without electrical shock risk due to provided galvanic isolation.



Note that in case of performing metrology measurements, board may lose galvanic isolation, so convenient caution must be taken into account.



A normal use of PL360MB + PLCOUPxxx boards do not require removing the enclosure cover. If this action is necessary, it must be performed by qualified staff after being sure that the mains connection has been previously removed. Be careful, as it is only for indoor use. PL360MB and PLCOUPxxx boards are not compliant with EN60950-1 safety standard out of the enclosure.

This development board does not have any switch on mains connection to switch it on or off.

Do not connect any probe to high voltage sections if the board is not isolated from the mains supply to avoid the damage of measurement instruments.

This board can be used with lithium coin batteries, which are highly contaminating products. Used batteries must always be recycled or safely treated and disposed.



Important: Microchip does not assume any responsibility for the consequences arising from any improper use of this board.

Boards' kits are intended for further engineering, development, demonstration, or evaluation purposes only. It is not a finished product, except as may be otherwise noted on the board/kit.

1.2 Electrical Specifications

This section shows the electrical characteristics of the kit's boards.

Table 1-1. Power Supply Requirements

Parameter	Condition	Min.	Typ.	Max.	Unit
AC Mains Voltage Range		100	115/230	250	V _{AC}
Mains Frequency			50/60		Hz

Parameter	Condition	Min.	Typ.	Max.	Unit
Maximum Input Current				200 ⁽¹⁾	mA
Isolation Voltage	AC/DC power supply and PLC coupling transformer			3000	V _{AC}

Note that the PL360MB can be supplied with 100V_{AC}, 115V_{AC} or 230V_{AC} by setting the proper jumpers (pitch = 5.08mm) in the voltage selector, J2, as depicted in the [Figure 3-13](#). By default, voltage jumper is set for 230V_{AC}. For more information about power supply, see section [Power Supply System](#).

Note:

1. This maximum input current is measured in the worst consumption conditions so that when the board is supplied with a minimum input voltage, 100V_{AC}, and it emits against very low impedance in FCC frequency band, the display is on and it is supplying an external board (400 mA at 12 V) through the DC jack, J15.

Table 1-2. Power Consumption

Parameter	Condition	Min.	Typ.	Max.	Unit
TX Power Consumption	FW: G3 CEN-A PHY TX Test Console Application. Low Impedance Load (2 Ohm LISN, see Figure C.1 of ITU-T G.9901). Measured on V _{DD} (12 Volts) DC/DC output.		2200 ⁽¹⁾	3620 ⁽¹⁾	mW
	FW: G3 CEN-A PHY TX Test Console Application. High Impedance Load (CISPR LISN, see Figure 5 of EN50065-1). Measured on V _{DD} (12 Volts) DC/DC output.		1490 ⁽¹⁾	3360 ⁽¹⁾	mW
RX Power Consumption	Measured on 3.3V LDO output		479 ⁽¹⁾	594 ⁽¹⁾	mW
Low power mode current consumption	-		<10 ⁽²⁾		µA

Notes:

1. These measurements were taken with a non-optimized FW from a power consumption point of view (PHY TX Test Console project included in the kit with a default configuration in TX mode and RX mode) and also affected by the architecture and efficiency of the power supplies. These measurements correspond to the whole PCBA design and not only to PL360 and SAM4CMS16C devices. All PCB peripherals are supplied, i.e. LCD display and PLCOUP007 coupling board emitting in CENELEC A-band. Refer to PL360 and SAM4CMS16C datasheets for an optimized power consumption measurement result.
2. Output current of a 3.6V battery.

2. Getting Started

2.1 Powering-Up the Boards

Unpack and inspect the kit carefully.

Figure 2-1. Unpacked PL360-EK



Two PL360MB boards with PLCOUP007 coupling boards are encapsulated with methacrylate enclosures and shipped in protective anti-static foam. Two coupling boards, PLCOUP006, are shipped in shielded bags.



The boards must not be subject to high electrostatic discharge. We recommend using a grounding strap or similar ESD protective device when handling the board in hostile ESD environments. Avoid touching the components' pins or any other metallic elements on the board.

Note: This kit does not provide any battery to check the date and time backup functions of the SAM4CMS16C device.

Take into account that the PL360-EK provides two coupling boards for CENELEC A-Band set over the PL360MB board (i.e.: PLCOUP007). In addition, the evaluation kit includes two additional coupling boards for FCC bands (i.e.: PLCOUP006).

Figure 2-2. PLCOUP007 Board Set Over a PL360MB Board

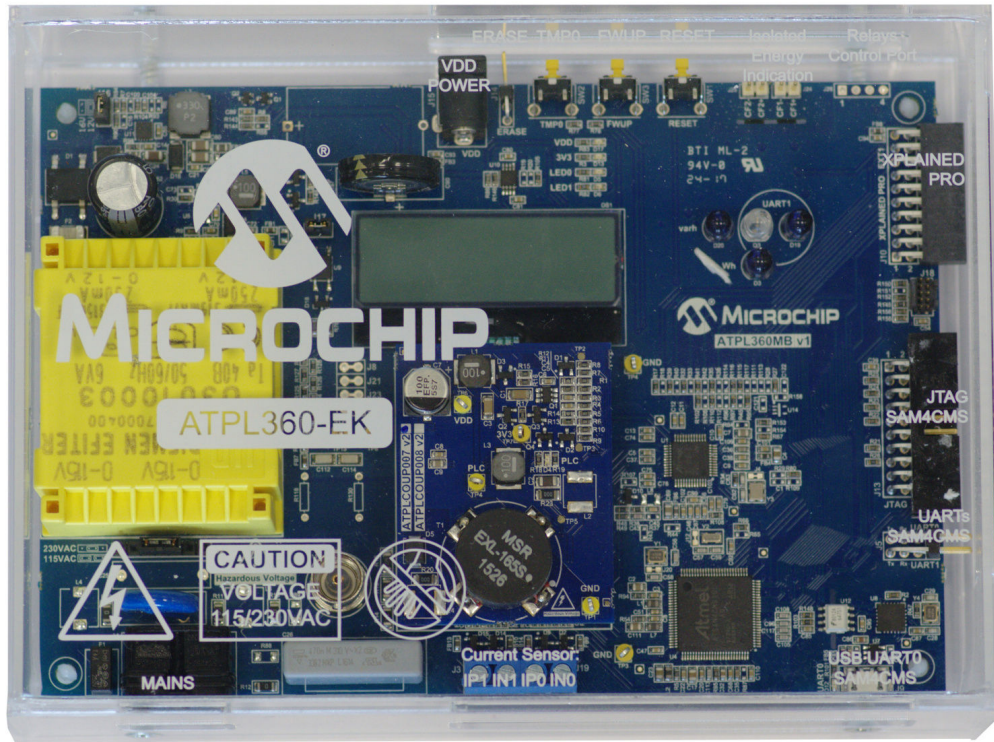


Figure 2-3. PLCOUP006 in a Shielded Bag



Prior to powering-up the boards, check your voltage level grid. By default, the board is configured to be supplied for 230V_{AC}. Otherwise change jumper J2 position, see [Figure 3-14](#).

Unpack the power cord cable and insert cable in the mains power connector. Plug the cable to an AC power plug. The board LCD will display a text and board's LEDs will show activity.



Important: Check your socket; the power cord provided for the kit is according to IEC320-C8, so it could be necessary to use an adapter.

2.2 Running Preloaded Firmware

The PL360-EK is delivered with a pre-programmed default application in SAM4CMS16 Flash memory: the G3-PLC PHY Tester for CENELEC A-Band.

Users can interface and control the PL360MB board by means of the PLC PHY Tester PC application. Using this PC tool, users can send and receive PLC messages using the PHY layer in the frequency band with the right coupling board according to the binary flashed in PL360MB board.

Please remember that the PLCOUP007 board only lets send and receive PLC messages in the CENELEC A-Band. Please change to the PLCOUP006 board in order to evaluate the FCC band.

2.3 Code and Technical Support

After boot up, designers can run sample code or their own application on the board's kit (please read corresponding firmware manual). Users can get technical support from the Microchip website.

Please note that the latest software code, documentation and support materials are available online. Follow instructions described in the welcome letter for more information.

For any technical support requests, please visit <http://support.microchip.com>.

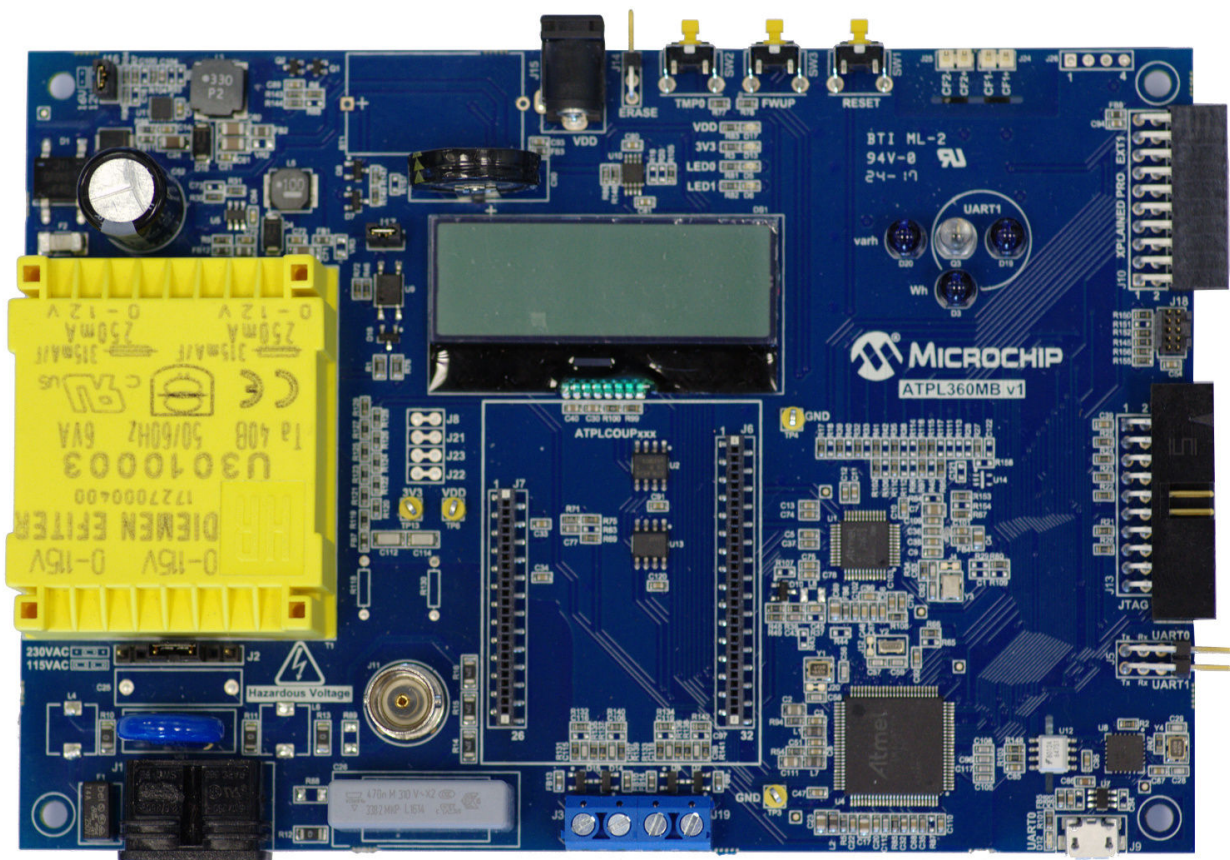
3. PL360MB Board

3.1 Overview

This section summarizes the PL360MB board design. It introduces system-level concepts, such as power supply, MCU, PLC coupling, memories, peripherals and interface board.

PL360MB is PLC multi-protocol modem board based on the PL360 transceiver and on SAM4CMS16C ARM Cortex M4 microcontroller. This development board provides a full featured platform to develop a complete communications system over PLC technology and to demonstrate the high accuracy single phase energy metering functions.

Figure 3-1. PL360MB Board



3.2 Features List

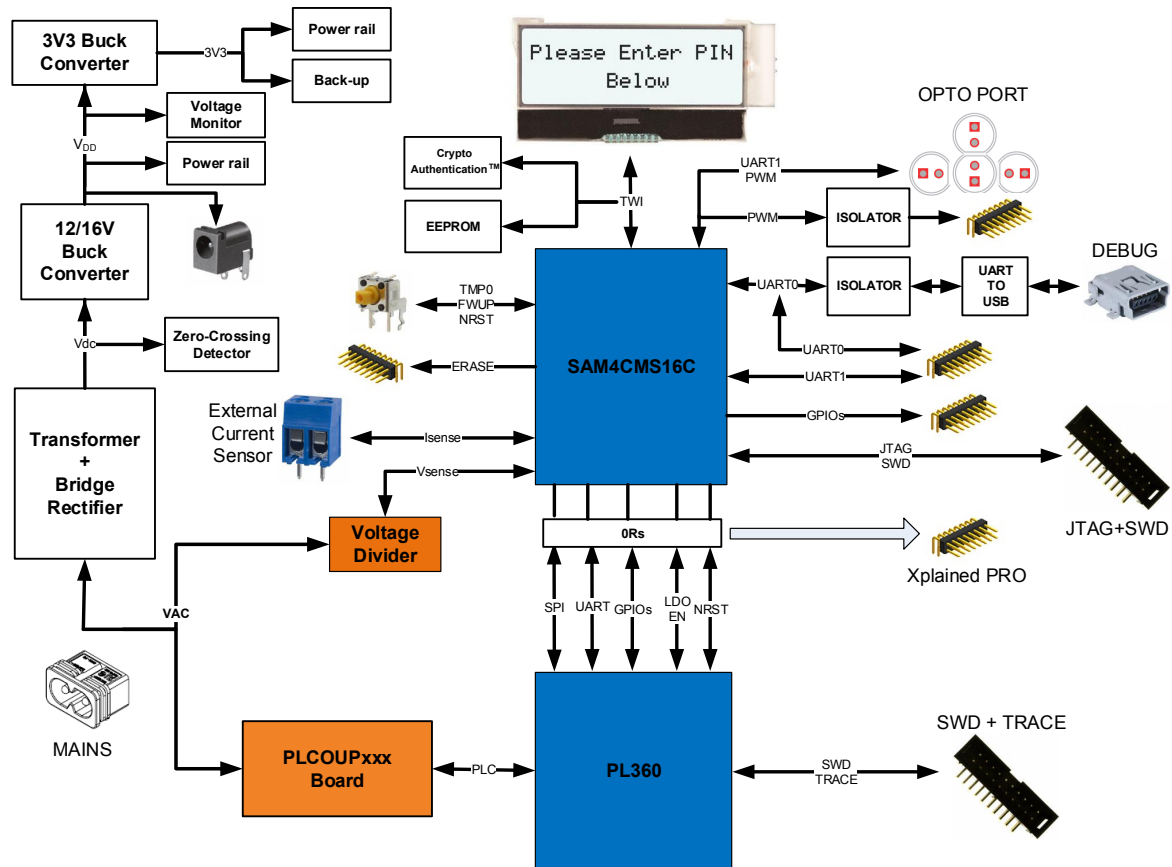
The PL360MB board includes the following features:

- PL360 PLC Transceiver:
 - Multi-protocol PLC modem:
 - G3-PLC, profiles CENELEC, FCC and ARIB
 - PRIME 1.3 and PRIME 1.4
 - 96 kB (up to 128 kB) of SRAM for program

- 96 kB (down to 64 kB) of SRAM for data
- One SPI peripheral to external MCU
- Zero-Cross Detection
- Embedded PLC Analog Front End (AFE)
- Low power consumption in transmission and reception
- Fuses burning circuit
- SAM4CMS16C MCU:
 - Master Core:
 - ARM Cortex[®]-M4 running at up to 120MHz
 - Memory Protection Unit (MPU)
 - DSP instruction set
 - Thumb[®]-2 instruction set
 - Instruction and Data Cache Controller with 2 Kbytes cache memory
 - 1024 Kbytes of Flash, 128 Kbytes of SRAM, 8 Kbytes of ROM
 - Coprocessor:
 - ARM Cortex-M4F running at up to 120 MHz
 - IEEE[®] 754 compliant, single precision Floating-Point Unit (FPU)
 - DSP instruction set
 - 16 Kbytes of embedded SRAM (SRAM1)
 - 8 Kbytes of embedded SRAM (SRAM2)
 - Cryptography
- Linear AC/DC 115/230 V_{AC} 50/60 Hz Power Supply
- Selectable 12/16 V_{DC} Power Supply for PLC Power Amplifier
- Back-Up Circuit with Battery
- Mains Zero-Crossing Detector Circuit
- Support to PLC Coupling Boards PLCOUPxxx
- Metrology:
 - Single phase measurements for voltage (between a voltage range of 85V-264V) and current (between a current range of 2-200A) with external Rogowski coils sensor, current transformer and shunt resistor
 - PWM optical energy indication
 - PWM isolated energy indication
 - Optical UART1
 - Relays control port connector
- Peripherals:
 - Liquid crystal display
 - Supply monitor
 - TWI 1Mbit EEPROM
 - CryptoAuthentication™ device
 - User LEDs
 - Force wake-up and tamper switch buttons
 - Reset button
 - Isolated UART0 over USB and non isolated UART0 & UART1 over CMOS levels

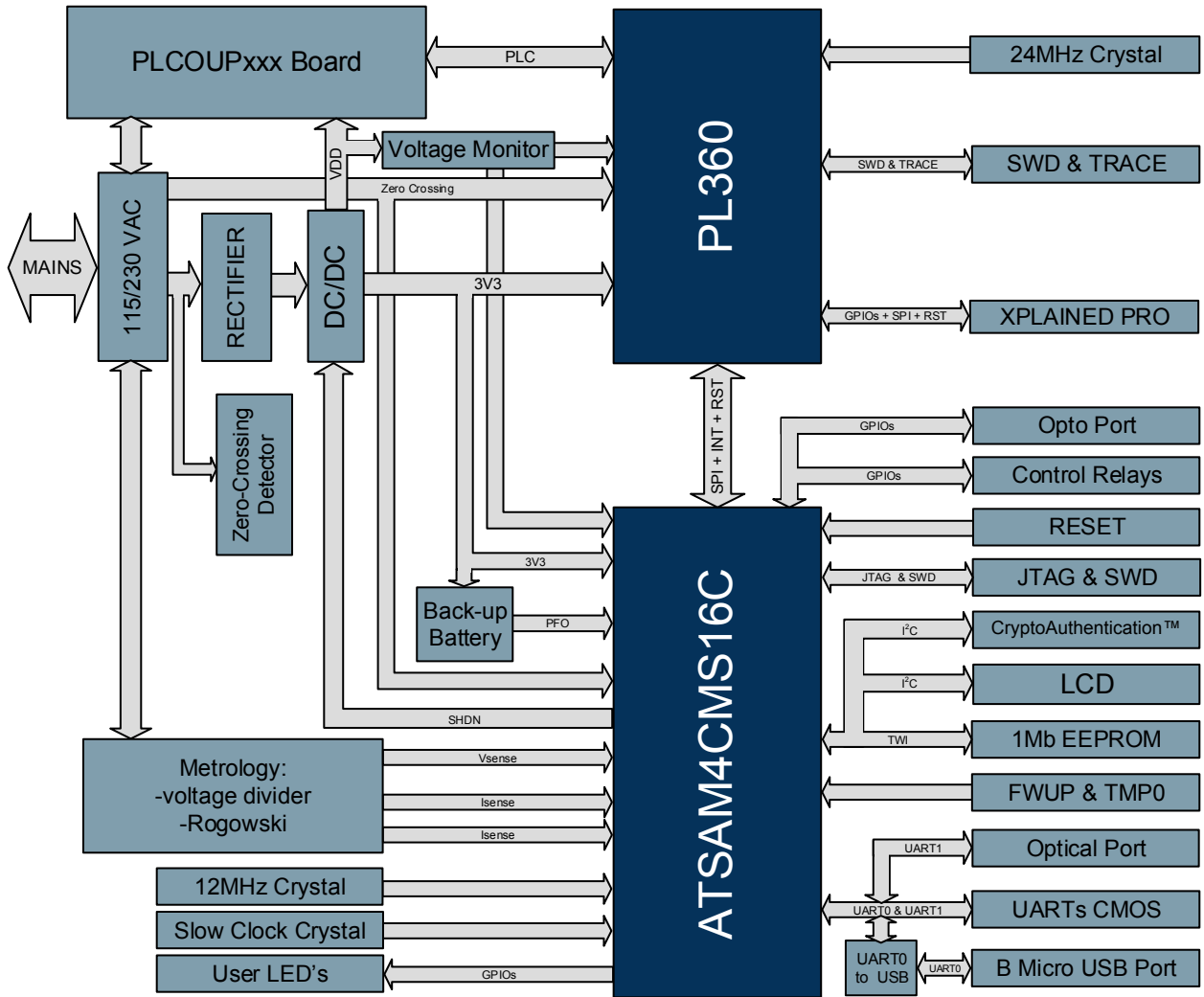
- Xplained PRO target connector
- JTAG debugging port

Figure 3-2. PL360MB Board Architecture



3.2.1 PL360MB Block Diagram

Figure 3-3. PL360MB Block Diagram

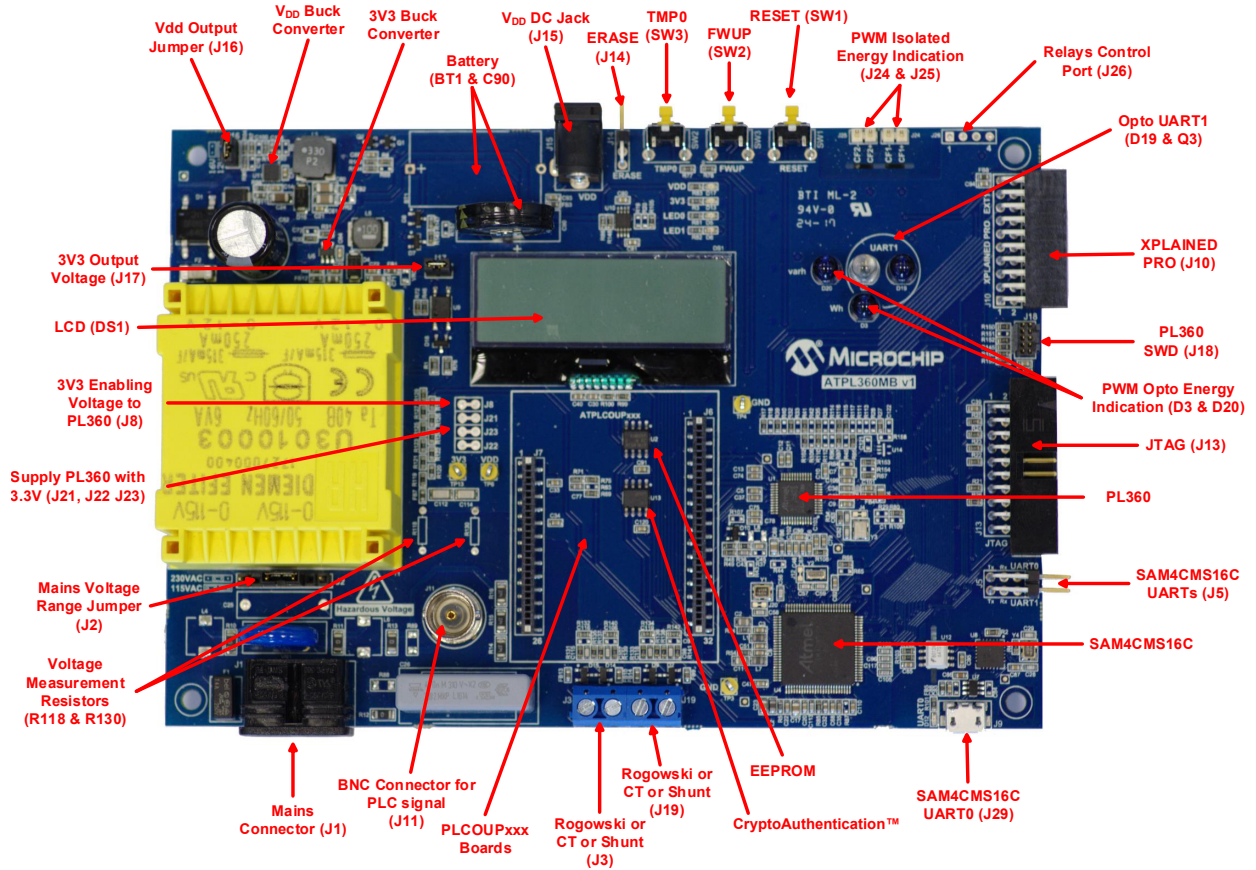


3.2.2 Interface Connection

PL360MB board includes hardware interfaces such as jumpers, buttons and connectors.

Following figure shows an overview of the connectors, jumpers and buttons of the PL360MB board.

Figure 3-4. PL360MB Connectors, Buttons and Jumpers Overview



3.2.2.1 Connectors

PL360MB board includes following connectors:

1. Mains connector, J1.

Table 3-1. Mains Connector, J1

Pin	Signal Name	Description
1	L	Line
2	N	Neutral

2. Dual triple row non-isolated UARTs connector, J5.

Table 3-2. UARTs Connector, J5

Pin	Signal Name	Description
1	UTXD0	Serial data output signal of UART0
2	URXD0	Serial data input signal of UART0
3	GND	Ground
4	UTXD1	Serial data output signal of UART1

Pin	Signal Name	Description
5	UTXD1	Serial data input signal of UART1
6	GND	Ground

3. Micro-B USB connector for the isolated UART0, J9.

Table 3-3. USB Device Connector, J9

Pin	Signal Name	Description
1	VBUS	5V power
2	D+	Data Plus
3	D-	Data Minus
4	ID	On the Go Identification
5	GND	Ground

4. Xplained PRO extension connector, J10.

Table 3-4. Xplained PRO Connector, J10

Pin	Mnemonic
1	ID
2	GND
3	ADC
4	ADC
5	GPIO
6	GPIO
7	GPIO
8	GPIO
9	IRQ
10	GPIO
11	TWD
12	TWCK
13	RXD
14	TXD
15	CS
16	MOSI
17	MISO
18	SCK

Pin	Mnemonic
19	GND
20	GND

5. BNC connector for PLC signal, J11.

Table 3-5. BNC Connector, J11

Pin	Signal Name	Description
1	PLC+	PLC Signal +
2	PLC-	PLC Signal -

6. JTAG/SWD 20-pin IDC connector for SAM4CMS16C, J13.

Table 3-6. JTAG/ICE Connector, J13

Pin	Mnemonic	Description
1	Vcc (3.3V power)	This is the target reference voltage. It is used to check if the target has power, to create the logic-level reference for the input comparators, and to control the output logic levels to the target. It is normally fed from V_{DD} on the target board and must not have a series resistor.
2	Vcc (opt) (3.3V power)	This pin is not connected in SAM-ICE. It is reserved for compatibility with other equipment. Connect to V_{DD} or leave open in target system.
3	TRST (TARGET RESET)	JTAG Reset (active-low output signal that resets the target). Output from SAM-ICE to the Reset signal on the target JTAG port. Typically connected to nTRST on the target CPU. This pin is normally pulled HIGH on the target to avoid unintentional resets when there is no connection.
4	GND	Ground.
5	TDI (TEST DATA INPUT)	JTAG data input of target CPU (serial data output line, sampled on the rising edge of the TCK signal). It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TDI on target CPU.
6	GND	Ground.
7	TMS (TEST MODE SELECT)	JTAG mode set input of target CPU. This pin should be pulled up on the target. Typically connected to TMS on target CPU. Output signal that sequences the target's JTAG state machine, sampled on the rising edge of the TCK signal.
8	GND	Ground.
9	TCK (TEST CLOCK)	JTAG clock signal to target CPU (output timing signal, for synchronizing test logic and control register access). It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TCK on target CPU.

Pin	Mnemonic	Description
10	GND	Ground.
11	RTCK	Input Return test clock signal from the target. Some targets must synchronize the JTAG inputs to internal clocks. To assist in meeting this requirement, a returned and retimed TCK can be used to dynamically control the TCK rate. SAM-ICE supports adaptive clocking which waits for TCK changes to be echoed correctly before making further changes. Connect to RTCK if available, otherwise to GND.
12	GND	Ground.
13	TDO (JTAG TEST DATA OUTPUT)	JTAG data output from target CPU (serial data input from the target). Typically connected to TDO on target CPU.
14	GND	Ground.
15	RESET	Active-low reset signal. Target CPU reset signal.
16	GND	Ground.
17	RFU	This pin is not connected in SAM-ICE.
18	GND	Ground.
19	RFU	This pin is not connected in SAM-ICE.
20	GND	Ground.

7. V_{DD} Output connector, J15.

Table 3-7. V_{DD} Output Connector, J15

Pin	Signal Name	Description
1	VDD	V_{DD} voltage
2	GND	Ground
3	-	-

8. PL360 SWD 10-pin connector for PL360 (for internal use only), J18.

Table 3-8. SW-DP Connector, J18

Pin	Mnemonic	Description
1	VCC	This is the target reference voltage.
2	SWDIO/TMS	Serial Wire Input / Output.
3	GND	Ground.
4	SWDCLK/TCK	Serial Wire Clock.
5	GND	Ground.
6	SWO/TDO	Trace Asynchronous Data Out from target CPU (serial data input from the target).

Pin	Mnemonic	Description
7	KEY	-
8	NC/TDI	Test Data Input. This pin is not connected.
9	GND Detect	Ground.
10	nRESET	Target CPU reset signal.

9. Input Current Sensor connector, J3 & J19.

Table 3-9. Input Current Sensor Connector, J3

Pin	Description
1	Differential input current sensor.
2	Differential input current sensor.

Table 3-10. Input Current Sensor Connector, J19

Pin	Description
1	Differential input current sensor.
2	Differential input current sensor.

10. PWM Isolated Energy Indication connector, J24 & J25.

Table 3-11. PWM Isolated Wh Connector, J24

Pin	Signal Name	Description
1	CF1+	Wh pulse.
2	CF1-	Wh pulse.

Table 3-12. PWM Isolated VARh Connector, J25

Pin	Signal Name	Description
1	CF2+	VARh pulse.
2	CF2-	VARh pulse.

11. Relay Control Port connector, J26.

Table 3-13. Relay Control Port Connector, J26

Pin	Mnemonic
1	PA26
2	PA19
3	PA18
4	GND

3.2.2.2 Jumper Configurations

The following table describes the functionality of the jumpers.

Table 3-14. Jumper Configuration

Jumper	Label	Default Setting	Function
J2	AC Voltage selection	230V _{AC} position	AC mains input voltage range selection ⁽¹⁾ .
J8	3V3_PL360	Closed	3V3 current measurement for PL360 device.
J14	ERASE	Open	SAM4CMS Flash memory code erase (closed = erase).
J16	V _{DD}	Closed	V _{DD} voltage selection, 12V (open = 16V).
J17	3V3	Closed	3V3 current measurement power rail.
J21	V _{DDIN}	Closed	V _{DDIN} current measurement for PL360 device.
J22	V _{DDIN_AN}	Closed	V _{DDIN_AN} current measurement for PL360 device.
J23	V _{DDIO}	Closed	V _{DDIO} current measurement for PL360 device.

Note:

- When mains is 230V_{AC} ±10% voltage range sets a single 5.08mm pitch jumper placed on the middle position of J2 header, see [Figure 3-13](#). When mains is 115V_{AC} ±10% voltage range set two 5.08mm pitch jumpers placed on J2 header, see [Figure 3-14](#).



Mains voltage range selection jumper must be always manipulated before connecting the board to the mains.

3.2.2.3 Test Points

Some test points (probes and pads) have been placed on the PL360MB board for the verification of important signals.

Table 3-15. Test Point Probes

Reference	Function
TP3, TP4	GND
TP6	VDD
TP13	3V3

Table 3-16. Test Point Pads

Reference	Function	Reference	Function
TP1	Line	TP25	SAM4CMS pin FWUP, SW3
TP2	Neutral	TP26	PL360 pin EMIT1
TP5	Input voltage scaled value (VP1) at ADC input	TP27	SAM4CMS pin TMP0, SW2

Reference	Function	Reference	Function
TP7	Zero cross signal, VZC	TP28	PL360 pin MISO/PA9
TP8	VDC	TP29	PL360 pin MOSI/PA8
TP9	24 MHz crystal oscillator Y3	TP30	PL360 pin EMIT2
TP10	PL360 pin PA2 (SW/TDO)	TP31	PL360 pin SPCK/PA7
TP11	PL360 pin PA5 (SWDCLK/TCK)	TP32	PL360 pin EMIT3
TP12	Supply monitor	TP33	PL360 pin TXRX0
TP14	SAM4CMS pin PB0 (TDI)	TP34	PL360 pin TXRX1
TP15	Input PLC signal (VIN) at ADC input	TP35	SAM4CMS pin PB3 (TCLK/RTCK)
TP16	Reset	TP36	Ground
TP17	SAM4CMS pin PA24 (TWD0)	TP37	Ground
TP18	SAM4CMS pin PA25 (TWCK0)	TP38	V _{DD}
TP19	SAM4CMS pin PB2 (TMS)	TP39	SAM4CMS pin PB1 (TDO)
TP20	SAM4CMS pin PA15, LED D5	TP40	3V3
TP21	SAM4CMS pin PA16, LED D6	TP41	3V3
TP22	PL360 pin EMIT0	TP42	PL360 pin NPCS0/PA6
TP23	PL360 pin PA4 (SWDIO/TMS)	TP43	Input voltage scaled value (VP1) at ADC input
TP24	PL360 pin AGC	TP44	Input voltage at VZC/PA12 pin

3.3 Mechanical and User Considerations

This development board is directly powered from the mains grid, so hazardous voltage is present on the board. To avoid user access to dangerous parts, PL360MB must always be used in its enclosure. Most of the required connectors and configuration jumpers are easily accessible without removing the enclosure cover.

PL360MB supply voltage is taken from the mains grid (100/115/230V_{AC}, 50-60Hz), J1 connector. Configure the mains voltage selection jumper, J2, according your voltage mains grid.



Mains voltage range selection jumper (J2) must be always manipulated before connecting the board to the mains.

PL360MB dimensions are 178mm x 124mm x 30mm (LxWxH) and the enclosure dimensions are 191mm x 140mm x 48mm (LxWxH). The operating temperature range is -10 to 85°C.

3.4 Hardware Description – System

3.4.1 SAM4CMS16C

The PL360MB is equipped with a SAM4CMS16C device.

The SAM4CM series represents a family of system-on-chip solutions for residential and polyphase metering applications. The devices offer up to class 0.2 metrology accuracy over a dynamic range of 3000:1 within the industrial temperature range and are compliant with ANSI C12.20-2002 and IEC62053-22 standards.

The SAM4CM family offers an unprecedented level of integration and flexibility with dual 32-bit ARM Cortex-M4 RISC processors running at a maximum speed of 120 MHz each, up to 2 Mbytes of embedded Flash, 304 Kbytes of SRAM and on-chip cache.

The peripheral set includes metrology-specific precision voltage reference, up to seven (7) simultaneously sampled Sigma-Delta ADC subsystems supporting three (3) voltage and four (4) current measurement channels (polyphase versions only), an extensive set of embedded cryptographic features, anti-tamper, Floating Point Unit (FPU), four USARTs, two UARTs, two TWIs, four SPIs, three 16-bit PWMs, two 3-channel general-purpose 16-bit timers, 6-channel 10-bit ADC, battery-backed RTC with <1 μ A consumption and a 38 x 6 segmented LCD controller.

Figure 3-5. SAM4CMS Microcontroller

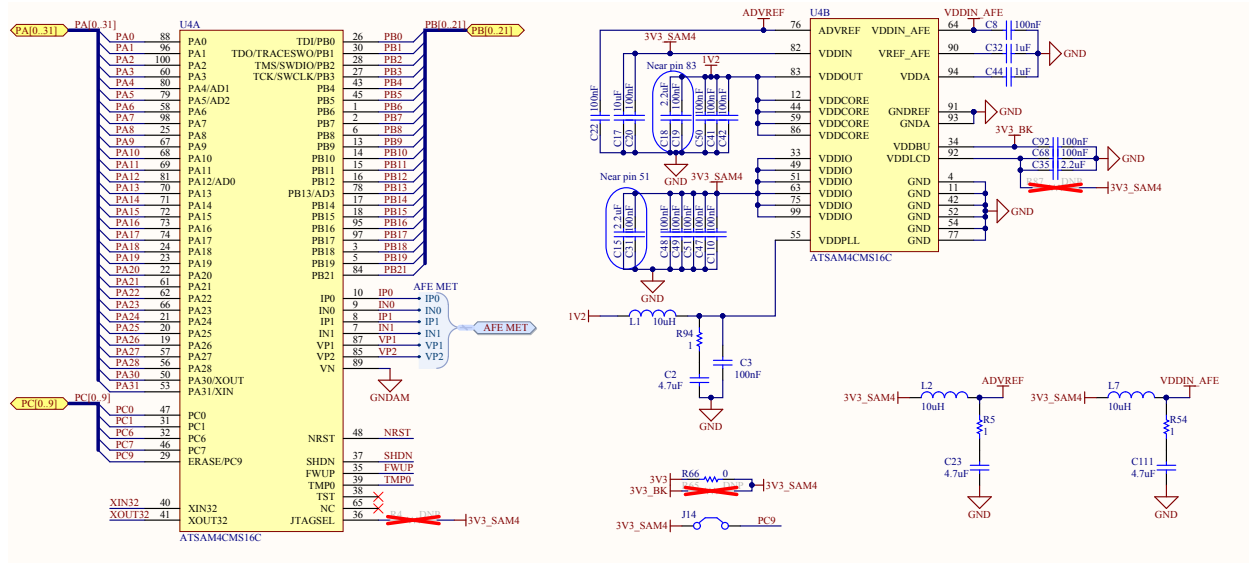


Table 3-17, Table 3-18 and Table 3-19 summarize the functionality of each input/output line of the SAM4CMS16C microcontroller in PL360MB board.

Table 3-17. Pinout of SAM4CMS16C PortA in PL360MB Board

I/O LINE	Function	I/O LINE	Function
PA0	-	PA16	User LED1
PA1	-	PA17	LCD RST
PA2	-	PA18	Relay Control
PA3	-	PA19	Relay Control

I/O LINE	Function	I/O LINE	Function
PA4	-	PA20	-
PA5	PL360 NPCS0	PA21	-
PA6	PL360 MISO	PA22	-
PA7	PL360 MOSI	PA23	-
PA8	PL360 SPCK	PA24	EEPROM TWD0
PA9	PL360 GPIO1	PA25	EEPROM TWCK0
PA10	PL360 GPIO0	PA26	Relay Control
PA11	-	PA27	-
PA12	-	PA28	-
PA13	-	PA30	XOUT
PA14	Power Fault	PA31	XIN/CLKIN
PA15	User LED0	-	-

Table 3-18. Pinout of SAM4CMS16C PortB in PL360MB Board

I/O LINE	Function	I/O LINE	Function
PB0	TDI	PB11	PL360 GPIO2
PB1	TDO	PB12	PL360 GPIO3
PB2	TMS	PB13	V _{DD} Supply Monitor
PB3	TCK	PB14	PL360 LDO_EN
PB4	UART0 RX	PB15	PL360 NRST
PB5	UART0 TX	PB16	-
PB6	-	PB17	-
PB7	-	PB18	-
PB8	-	PB19	-
PB9	-	PB21	-
PB10	VZC	-	-

Table 3-19. Pinout of SAM4CMS16C PortC in PL360MB Board

I/O LINE	Function	I/O LINE	Function
PC0	UART1 TX	PC7	PWM Energy Indication
PC1	UART1 RX	PC9	ERASE
PC6	PWM Energy Indication	-	-

3.4.2 PL360

The PL360MB is equipped with a PL360 device in the TQFP48 package.

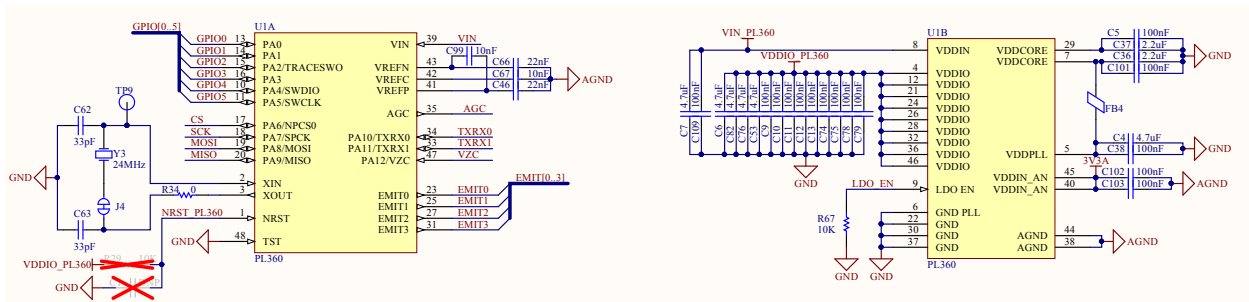
PL360 is a multi-protocol (G3-PLC, PRIME 1.3, PRIME 1.4) modem for Power Line Communication implementing a very flexible architecture, which allows implementation of standard and customized PLC solutions.

PL360 has been conceived to be bundled with an external Microchip MCU, which controls PL360 PLC modem.



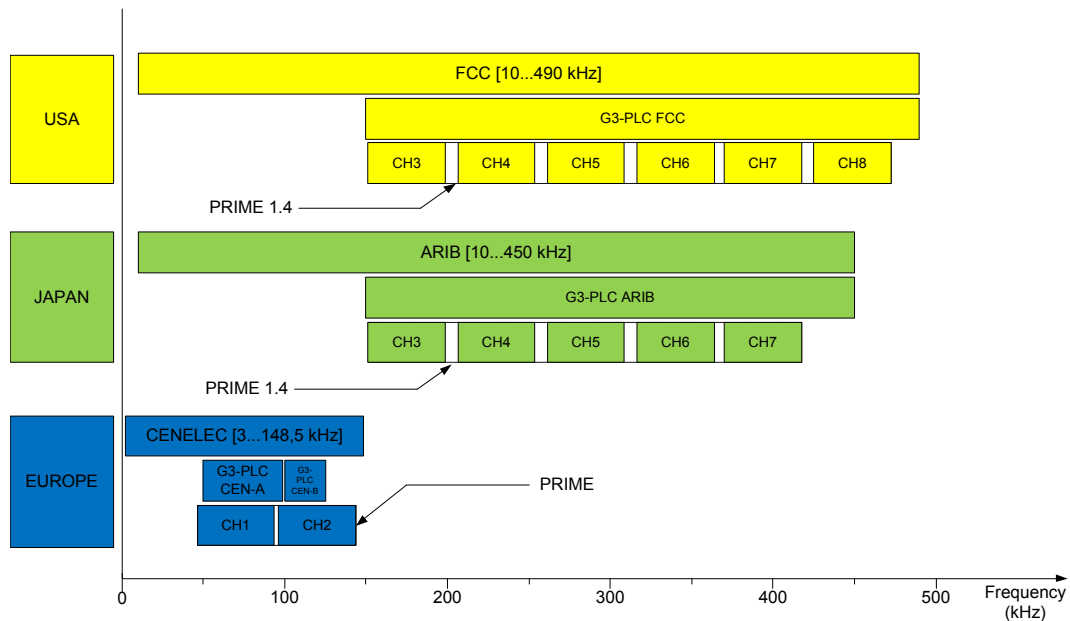
Important: At least one or two GPIOs from the PL360 device (e. g. PA3 and PA0) must be connected to the external MCU for the right firmware implementation per PLC standards (i.e. external interrupt for G3-PLC and carrier detect indication and external interrupt for PRIME). Check this point with the firmware implementation manual.

Figure 3-6. PL360 PLC Modem



Microchip provides highly efficient, reduced BOM reference designs for different coupling options, targeting common configurations in standard frequency bands complying with existing regulations (CENELEC, FCC & ARIB).

Figure 3-7. PLC Bands Supported by PL360



3.4.3 Clock Circuitry

Besides the embedded RC oscillators of SAM4CMS16C, three crystal oscillators are assembled on the PL360MB board to obtain a more precise and stable system clock reference:

- A 24 MHz clock signal generated for the PLC transceiver PL360
- A 12 MHz clock signal generated for the SAM4CMS16C
- A low power 32.768 kHz crystal oscillator for the SAM4CMS16C

Figure 3-8. 24 MHz Crystal Oscillator Scheme

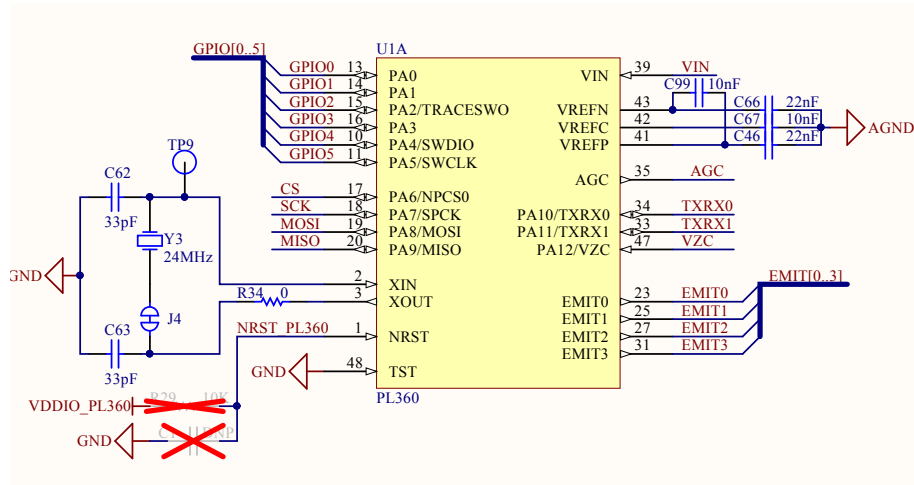
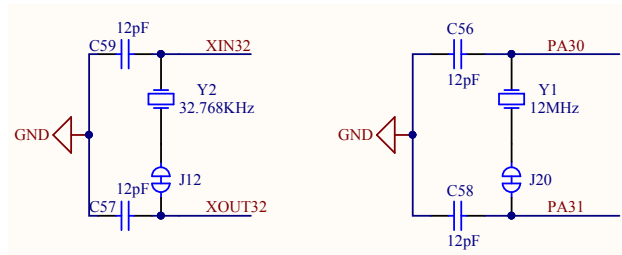


Figure 3-9. 12 MHz and 32.768 kHz Crystal Oscillator Scheme



3.4.4 Reset

The reset sources of the PL360MB board are:

- Power-on Reset function, embedded in the SAM4CMS device
- Push button reset. Every device, ATSAM4CMS16C and PL360, have a NRST pin: “NRST” for ATSAM4CMS16C and “NRST_360” for PL360. The user can manually reset the ATSAM4CMS16C, which manages the PL360 reset, by using a push button SW1. See section [Push Buttons](#).
- JTAG reset from an in-circuit emulator

3.4.5 PLC Coupling

The PL360MB evaluation board supports a set of PLC coupling boards, *PLCOUPxxx*, with the aim of easing the testing of different coupling reference designs while requiring only one PL360MB board. Furthermore, this functionality allows the same base board to cover several frequency bands by using the proper coupling board and firmware configuration. [Table 3-20](#) summarizes the main features of the available *PLCOUPxxx* boards.

Figure 3-10. Example of PLCOUPxxx Coupling Board Compatible with PL360MB

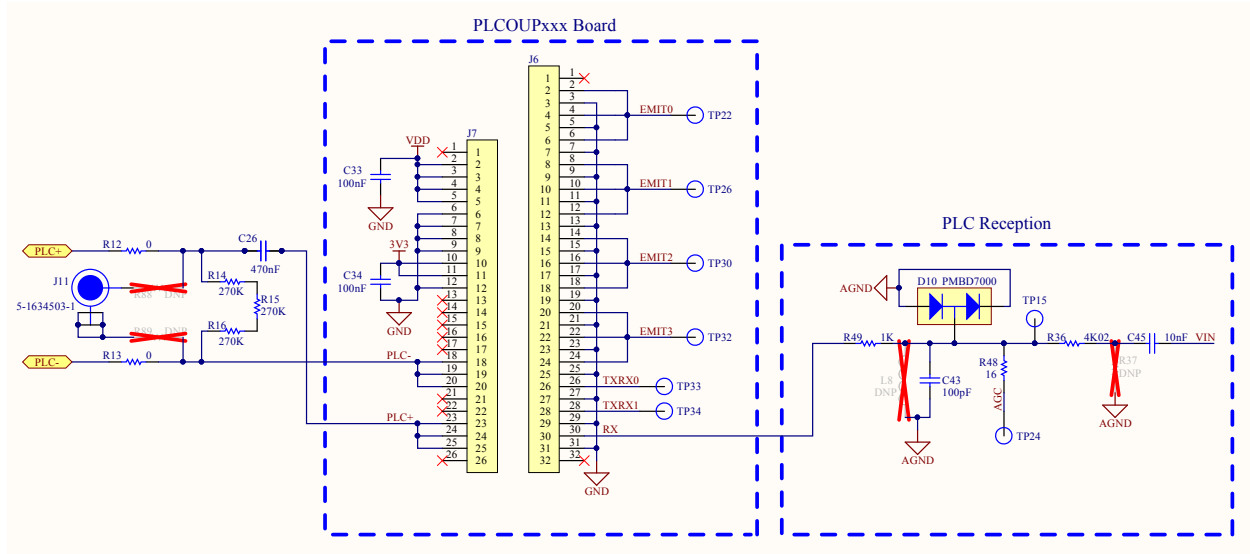


Table 3-20. Characteristics of PLCOUPxxx Boards

Board Name	Description	Frequency Band (kHz)	Branch	Electrical Isolation	PRIME Channel	G3-PLC Band	Applicable Regulation
PLCOUP002	G3 ARIB & PRIME ARIB (Channels 4 to 7) compliant	206 – 417	Double	Yes	4, 5, 6, 7	G3 ARIB	ARIB [STD-T84 Ver 1.0]
PLCOUP006	G3 FCC & PRIME FCC (Channels 3 to 8) and KN60 compliant	151 – 472	Double	Yes	3, 4, 5, 6, 7, 8	G3 FCC	FCC [part 15 – 91905]
PLCOUP007	G3 CEN-A & PRIME CEN-A compliant	35 – 91	Single	Yes	1	G3 CEN-A	CEN-A [EN50065]
PLCOUP008	Non-Isolated G3 CEN-A & PRIME CEN-A compliant	35 – 91	Single	No	1	G3 CEN-A	CEN-A [EN50065]
PLCOUP011	G3 CEN-A, G3 FCC, PRIME CEN-A & PRIME FCC (Channels 3 to 8) compliant	35 – 91 & 151 - 472	Double	Yes	1, 3, 4, 5, 6, 7, 8	G3 CEN-A & G3 FCC	CEN-A [EN50065]
PLCOUP012	Low cost with internal driver G3 CEN-B compliant	95 - 125	Single	Yes	2	G3 CEN-B	CEN-B [EN50065]
PLCOUP013	Ultra low cost with internal driver and non-Isolated G3 CEN-B compliant	95 - 125	Single	No	2	G3 CEN-B	CEN-B [EN50065]
PLCOUP014	G3 CEN-B compliant	95 - 125	Single	Yes	2	G3 CEN-B	CEN-B [EN50065]

As shown in [Figure 3-11](#), PL360MB has the possibility of disconnecting the PLC signal from the mains grid and connecting it to the BNC port, J11. This can be done by means of removing R12 and R13 and adding R88 and R89. This allows the possibility of using a dedicated communication channel for the PLC signal and eases the realization of certain PLC performance measurements.

Figure 3-11. PLC Coupling Schematic on PL360MB including headers for PLCOUPxxx boards



3.4.5.1 PLC Reception Circuit

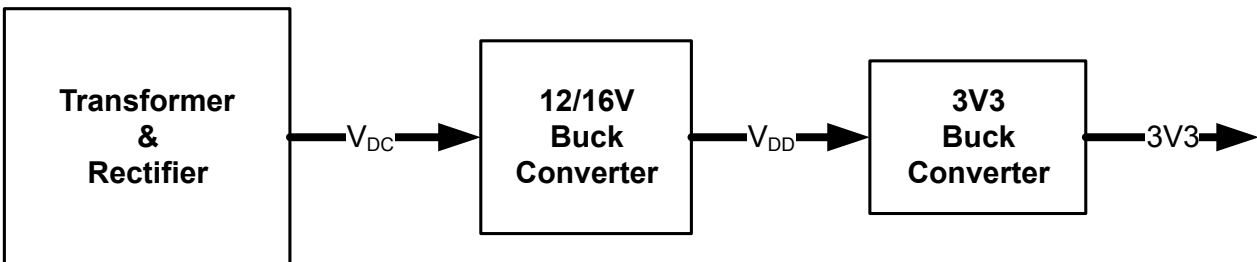
The PLC reception circuit used in PL360MB, see Figure 3-11, is the reference design of the reception stage described in the PL360 datasheet which is composed of:

- Single-pole low pass filter, R49 and C43
- Automatic Gain Control (AGC) circuit. A resistor, R48, used to attenuate the incoming PLC signal in case its amplitude is high enough to exceed the input dynamic range of the embedded ADC
- A resistor, R36, for impedance matching
- DC decoupling capacitor, C45

3.4.6 Power Supply System

To avoid on board self-generated disturbances within the PLC signal band (35 to 472 kHz), a linear (non-switched topology) AC/DC power supply schematic based on a power transformer plus full-wave rectifier is used to generate the unregulated DC voltage “V_{DC}” and two high frequency buck converters to get the power levels required. An F1 fuse and VR1 varistor are used as protective devices in the equipment input, and an F2 fuse protects the transformer output against overcurrent situations.

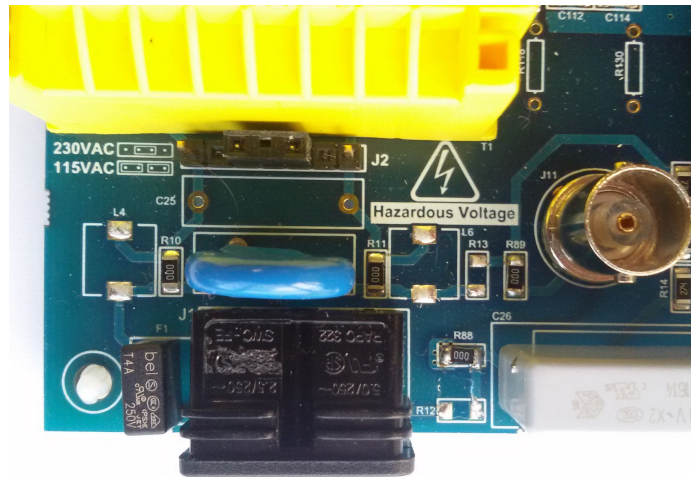
Figure 3-12. Linear AC/DC Power Supply Design



The mains rms input voltage range of PL360MB is selectable by means of jumpers on connector J2:

- 230VACrms ±10% mains voltage range: A jumper must be placed in the middle pins of connector J2, as shown in the following figure.

Figure 3-13. J2 Jumper Configuration for 230VACrms $\pm 10\%$



- 115VACrms $\pm 10\%$ mains voltage range: Two jumpers must be placed in connector J2. See following figure.

Figure 3-14. J2 Jumper Configuration for 115VACrms $\pm 10\%$

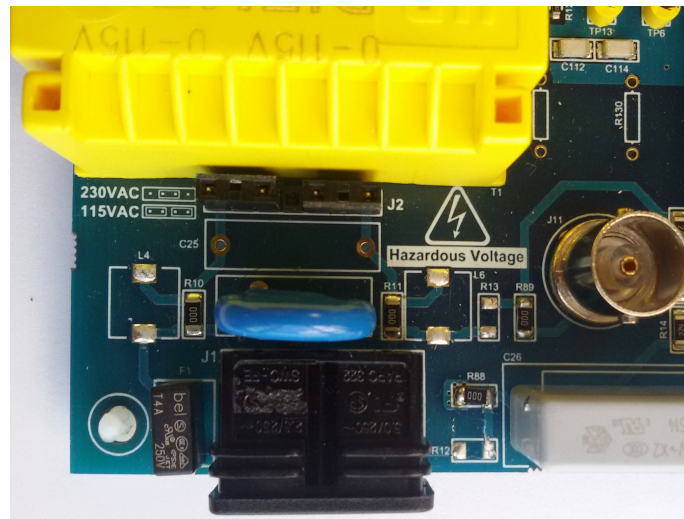
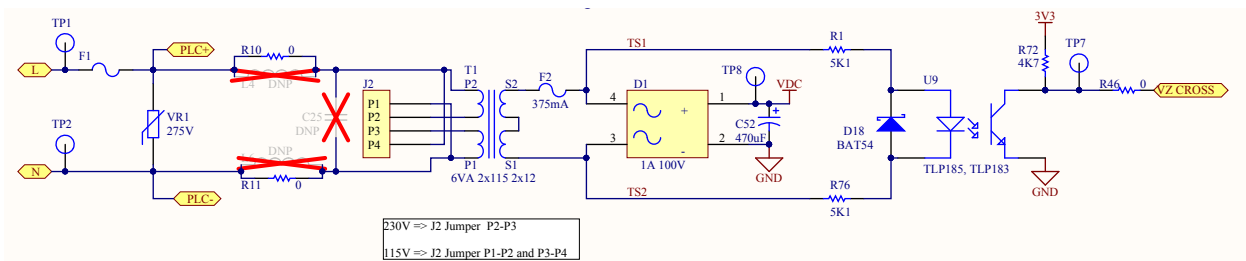


Figure 3-15. V_{DC} Voltage Design



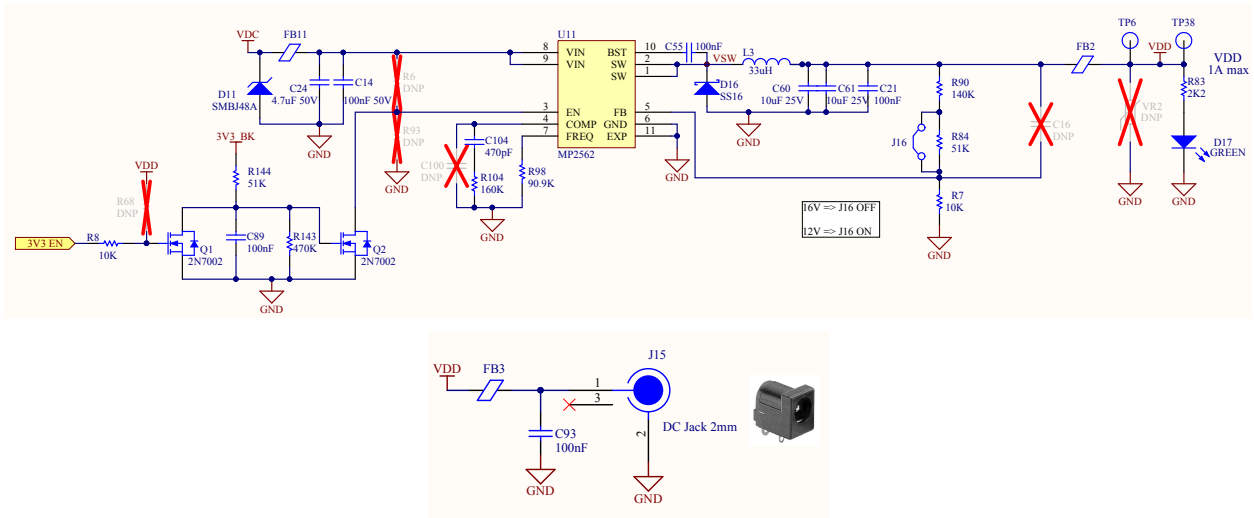
The “V_{DC}” voltage rail is used as input power of a high switching frequency buck converter to generate the regulated DC voltage “V_{DD}”, which is used to power the class-D amplifier of the PLC coupling circuit. The output level of the buck converter is selectable between 12V and 16V by means of jumper J16. Refer to sections [PLCOUP007 Board](#) and [PLCOUP006 Board](#) to see how the jumper J16 must be configured depending on the PLC coupling board being used.



Be careful with the V_{DD} voltage selected, because the PLC coupling driver board *PLCOUPxxx* could be damaged. Please check the features of these boards to select the operation voltage. Take into account that *PLCOUP006* and *PLCOUP007* boards use 12 volts.

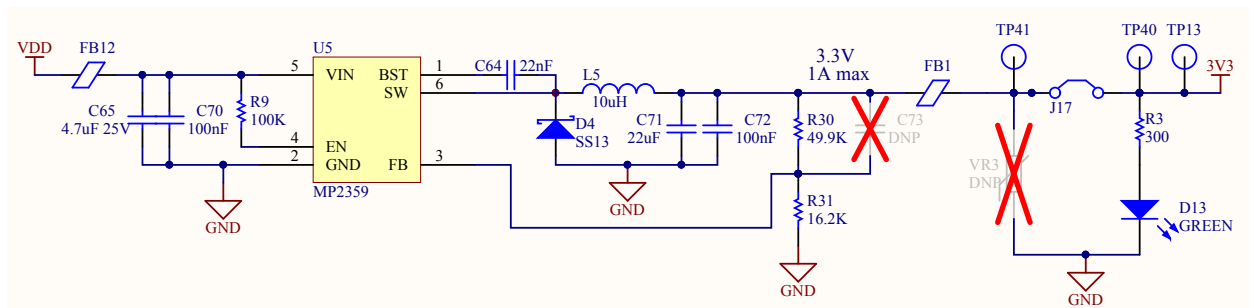
V_{DD} buck converter has a shutdown circuit enable which is controlled by the “3V3 EN” signal. This signal is an output pin of SAM4CMS16C, “SHDN”. This feature lets PL360MB boards enter in a low power mode. When PL360MB is supplied “3V3 EN” signal is in low value voltage as to not disable the V_{DD} buck converter. The DC Jack connector (J15) can be used to supply an external board to V_{DD} volts (400 mA at 12 V).

Figure 3-16. V_{DD} Buck Converter Design



A second buck converter with switching frequency above the highest PLC frequency band is also used to generate a regulated 3.3V voltage rail required by PL360 and the MCU. The current consumption from 3.3V voltage rail can be measured connecting an ammeter in the placeholder of jumper J17.

Figure 3-17. 3.3V Buck Converter Design



Other 1.2V voltage levels are generated by the embedded LDOs on SAM4CMS16C. For more detailed information about these LDOs, refer to [SAM4CM Series Datasheet](#).

There is a LED and a test point on each voltage rail to check whether all power supplies are operating properly.



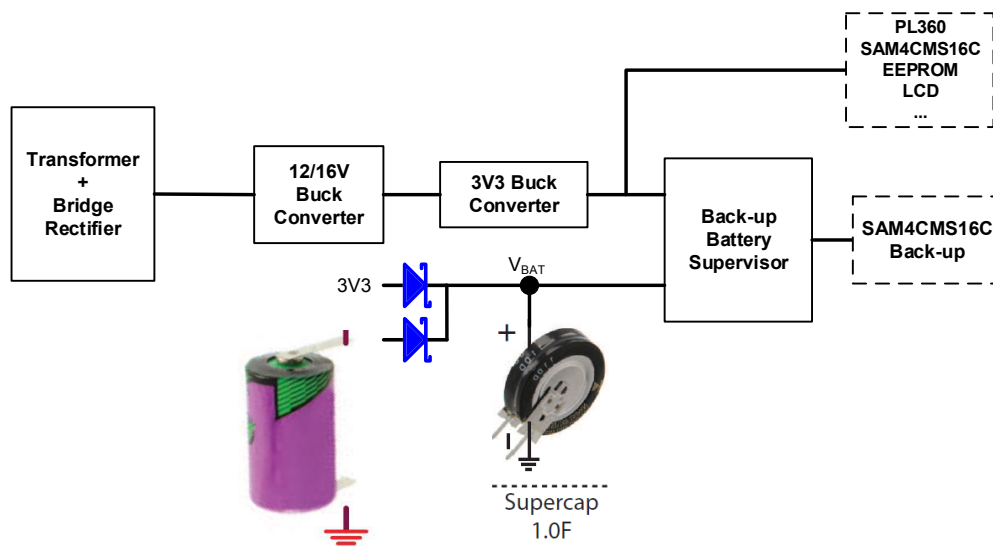
Tip: If choosing a different SMPS in your custom design, it is important to analyze its potential interference on the PLC frequency band.

3.4.6.1 Back-up

The purpose of Back-up mode is to achieve the lowest possible power consumption in a system that executes periodic wake-ups to perform tasks, but does not require fast start-up time.

PL360MB includes a back-up circuit with a battery (BT1) to maintain active RTC when the power supply of 3.3 volts shutdown and SAM4CMS enter in a low power mode. A voltage supervisor, U17, is also included.

Figure 3-18. Back-up Diagram

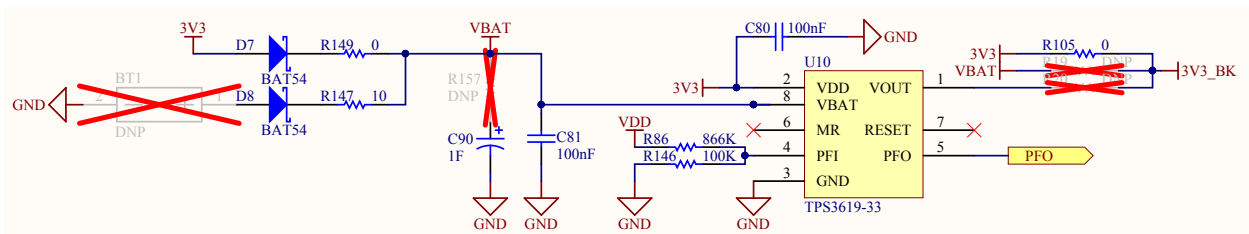


Note that there are three back-up resistor configurations:

1. Back-up mode disabled (default option) when R105 resistor is placed.
2. Back-up mode 1 (VBAT) enabled when R157 and R19 resistors are soldered (and R105 removed).
3. Back-up mode 2 (voltage supervisor) enabled when resistors R157 and R20 are soldered (and R105 removed).

In addition, even the VDDIO and VDDIN pins of the SAM4CMS16C microcontroller could be supplied removing R66 resistor and soldering R65 resistor.

Figure 3-19. Back-up Circuit





Important: By default, back-up components and configuration resistors such as battery BT1 and resistors R157, R19, R20 and R65 are not populated.

3.4.7 Zero-Crossing Detector Circuit

Phase identification is an important feature of devices that are connected to a Smart Grid network, such as smart meters. A typical implementation is based on measuring the time difference between a specific PLC frame reception and the last zero crossing event of the mains single-phase to which the device is connected.

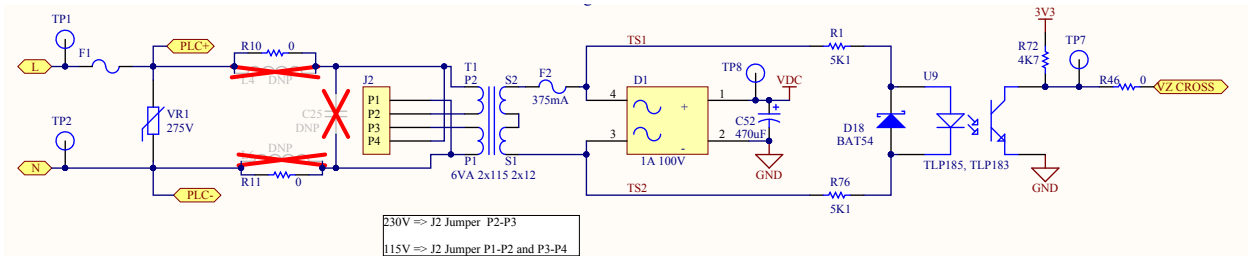


Important: The phase identification feature is mandatory for G3-PLC and PRIME1.4, but not PRIME1.3.

Zero-Crossing Detection Circuit shows the Zero-Crossing Detection circuit used in PL360MB board, which features detection of rising and falling edges of the mains voltage. The output signal of the detection circuit “VZ CROSS” is connected to VZ pin of PL360 and a synchronization algorithm is applied in order to obtain an accurate measurement of the time between PLC frame reception and zero crossing events.

The “VZ CROSS” signal is also connected to a GPIO pin of the SAM4CMS16C in order to also have information about zero crossing events on the microcontroller side.

Figure 3-20. Zero-Crossing Detection Circuit



It is important to note that for designs that do not require galvanic isolation, a simpler Zero-Crossing Detector such as a Zener diode can be used instead of the circuit previously shown.

3.4.8 Metrology

The Energy Metering Analog Front End peripheral (EMAFE) of SAM4CMS16C embeds four high-resolution Sigma-Delta Analog-to-Digital Converters followed by SINC decimation filters running at an output data rate of 16kS/s. The two current measurement channels feature a low noise programmable gain amplifier to accommodate any type of current sensor configured in any type of IEC/ANSI-C application. One of these channels is dedicated to neutral current measurement to implement anti-tamper functions.

The EMAFE also embeds a high-performance voltage reference and a die temperature sensor. The temperature characteristics of these functions are measured during manufacturing and stored in an internal read-only memory. A low-cost and efficient voltage reference temperature correction can then be implemented at the software level. The EMAFE has three types of acquisition channels:

- Voltage channel
- Current channels

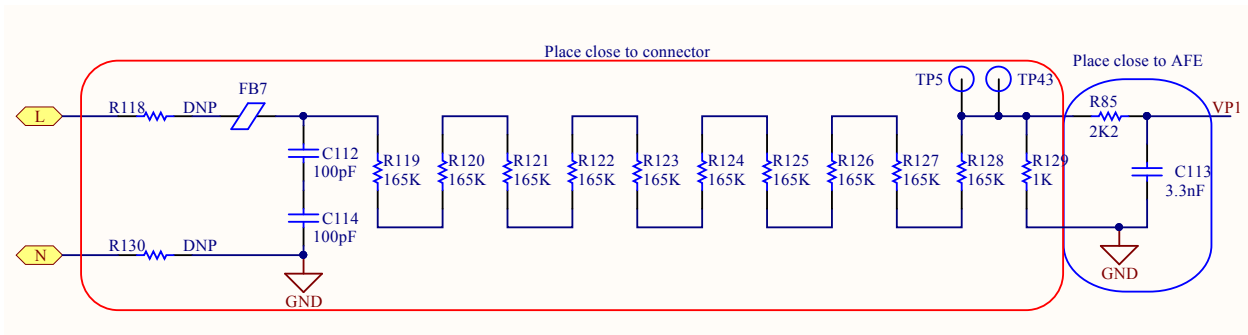
- Tamper and temperature channels

All these channels are built around the same Sigma-Delta A/D converter. The voltage reference of this converter is the VREF_AFE pin voltage referred to ground (GND pin). This reference voltage (with a typical output voltage of 1.144V) can be internally or externally sourced. The converter's sampling rate is EMAFE_CLK/4, typically 1.024 MHz. An external low-pass filter, typically a passive R-C network, is required at each ADC input to reject frequency images around this sampling frequency (anti-alias).

3.4.8.1 Mains Voltage Sense Input

Mains voltage is connected to the PL360MB board by two resistors, R118 and R130. Line voltage has a single-ended input referred to the neutral voltage (GND pin). This voltage is distributed to an ADC input through an 11-resistor (1%) divider with a ratio of 0.6057V : 1000V. An additional RC filter (R85/C113) limits the input bandwidth to approximately 16 kHz as shown in the following figure.

Figure 3-21. Mains Voltage Sense Input Schematic



Important: By default, R118 and R130 resistors are not populated, so mains voltage sense input is disabled.

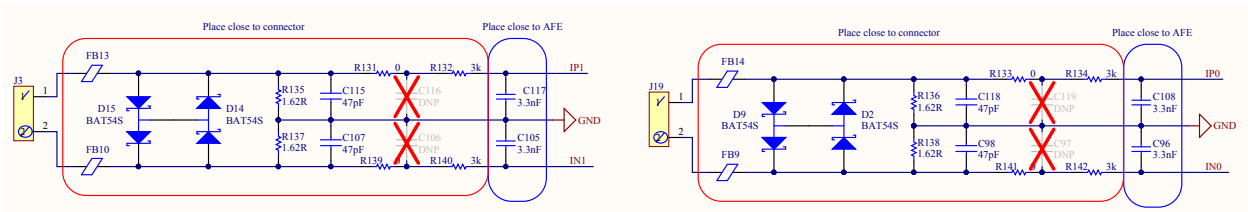


Note that if performing metrology voltage, the board loses galvanic isolation, so convenient caution must be taken into account.

3.4.8.2 Current Sensor Inputs

PL360MB board features two current sensor inputs for measuring the line and neutral currents. The current sensor used is connected to a 2-point connector (J3 & J19). These differential input lines are routed to an ADC through a configurable filter to accommodate various sensors (Current Transformer (CT), shunt or Rogowski coil). By default, all the inputs have the same layout and filter configuration. Their ground reference is GND node.

Figure 3-22. Current Filter Schematics





Important: By default, PL360MB board is configured to host a CT. The board is equipped with resistors R135, R136, R137 and R138 of 1.62 ohms to fit a 200A max current transformer with 20000:1 turn ratio. Firmware examples for the PL360MB board are configured to host a CT with a current ratio of 1:2000 (split core CT 1:2000 1Arms).



Important: Note that this kit does not provide CT, Rogowski coils, or shunt current sensors.

As previously mentioned, there are various current sensor types compatible with PL360MB board:

1. **CT**, e.g., Split Core CT 1:2000 1 Arms. To use a CT, the input network must provide a load (or burden) resistor and a first order low pass filter.



Info: The load resistor is sometimes integrated inside the CT.

For CT operation, the filters in [Figure 3-22](#) must be tuned with the following component values:

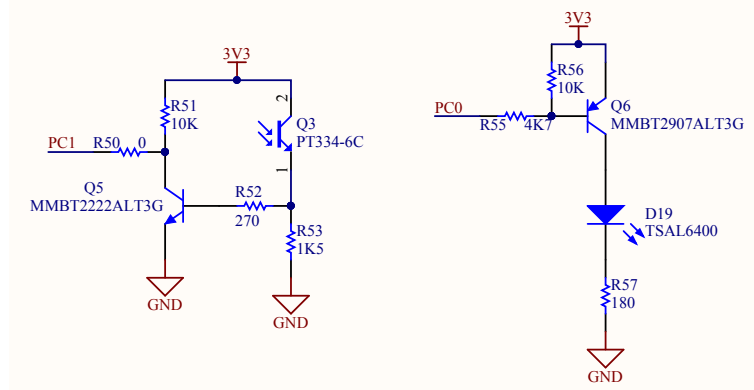
- R135, R136, R137 & R138 = Value depends on meter scale current and turn ratio
 - R131, R133, R139 & R141 = 0 Ω 100 ppm tempco
 - R132, R134, R140 & R142 = 3 k Ω , 1%, 100 ppm tempco
 - C98, C107, C115 & C118 = 47 pF / NP0
 - C97, C106, C116 & C119 = Do Not Populate
 - C96, C105, C108 & C117 = 3.3 nF / NP0
2. **Shunt Resistor**, e.g., 200A, 50mV Full Scale. To use a shunt resistor, the input network must only provide a first order low pass filter. So, for shunt operation, the filters in [Figure 3-22](#) must be tuned with the following component values:
 - R135, R136, R137 & R138 = Do Not Populate
 - R131, R133, R139 & R141 = 0 Ω 100 ppm tempco
 - R132, R134, R140 & R142 = 3 k Ω , 1%, 100 ppm tempco
 - C98, C107, C115 & C118 = 47 pF / NP0
 - C97, C106, C116 & C119 = Do Not Populate
 - C96, C105, C108 & C117 = 3.3 nF / NP0
 3. **Rogowski Coil**, e.g., RoCoil Series. To use a Rogowski coil sensor, the input network must provide a second order low pass filter. So, for Rogowski coil operation, the filters in [Figure 3-22](#) must be tuned with the following component values:
 - R135, R136, R137 & R138 = Do Not Populate
 - R131, R133, R139 & R141 = 100 Ω , 1%, 100 ppm tempco
 - R132, R134, R140 & R142 = 3 k Ω , 1%, 100 ppm tempco
 - C98, C107, C115 & C118 = 47 pF / NP0
 - C97, C106, C116 & C119 = 2.2 nF / NP0
 - C96, C105, C108 & C117 = 3.3 nF / NP0

3.4.8.3 Metrology Pulse Outputs, Opto-Port Interface and Relay Coil Command Interface

PL360MB includes several metrology interfaces:

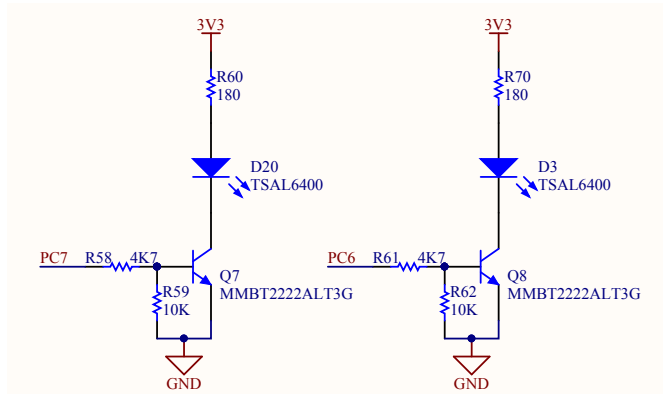
1. **Opto-Port for UART1.** The Opto-Port for UART1 is composed of an infrared emitting diode and a phototransistor to allow electrically isolated communications with an external optical probe. See following figure.

Figure 3-23. Opto-Port for UART1



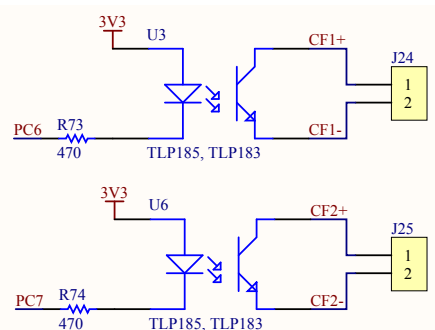
2. **Opto-Port for Pulse Output.** The user can measure the VARh and Wh pulses directly through LEDs D20 and D3 respectively with an external optical probe. See following figure.

Figure 3-24. Opto-Port for Pulse Output



3. **Isolated Pulse Output.** The user can measure the VARh and Wh pulses with isolation on connectors, J25 and J24 respectively, in differential mode. See following figure.

Figure 3-25. Isolated Pulse Output



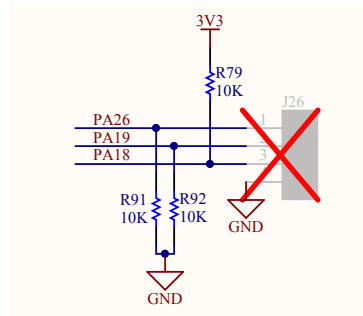
4. **Relays control port for external purposes.** The user can connect an external 3-phase latching relay and its power stage to the PL360MB board. For that, the following signal lines are routed to a 4-pin HE14 connector:

- J26, pin 1: COIL_ON_CM – ON Command, microcontroller request

- J26, pin 2: COIL_OFF_CMD – OFF Command, microcontroller request
- J26, pin 3: POSITION_RELAY – Relay Status
- J26, pin 4: GND – Digital Ground Reference

By default, COIL_ON_CM and COIL_OFF_CMD are pulled down to Ground through a 10 kΩ resistor and POSITION_RELAY is pulled up to 3.3 volts through a 10 kΩ resistor. See following figure.

Figure 3-26. Relay Control Port



3.5 Hardware Description – MCU Peripherals

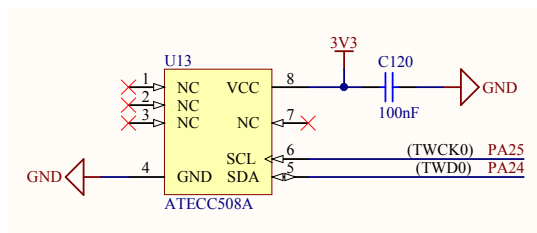
3.5.1 CryptoAuthentication

The ATECC508A is a member of the Microchip CryptoAuthentication library of crypto engine authentication devices with highly secure hardware-based key storage.

The ATECC508A integrates ECDH (Elliptic Curve Diffie Hellman) security protocol, an ultra-secure method to provide key agreement for encryption/decryption, along with ECDSA (Elliptic Curve Digital Signature Algorithm) sign-verify authentication for the Internet of Things (IoT) market.

Access to the device is made through a standard I²C Interface at speeds of up to 1Mb/s. The interface is compatible with standard Serial EEPROM I²C interface specifications.

Figure 3-27. CryptoAuthentication Schematic

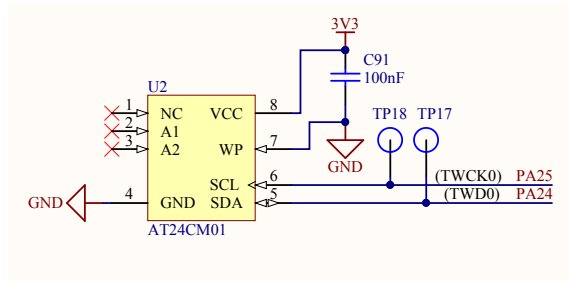


3.5.2 EEPROM

PL360MB mounts a serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) AT24CM01 device in an 8 JEDEC SOIC package.

AT24CM01 provides 1,048,576 bits of serial EEPROM organized as 131,072 words of 8 bits each. The 1-Mbit is internally organized as 512 pages of 256 bytes each. Random word addressing requires a 17-bit data word address. It is accessible through Two Wires Interface (TWI) and is I²C compatible.

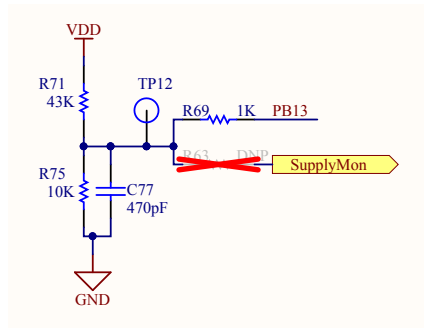
Figure 3-28. TWI EEPROM Schematic



3.5.3 Supply Monitor

Input pin PB13 of SAM4CMS16C is used to monitor the V_{DD} voltage rail through external voltage divisors. In addition, input pin PA4 of PL360 can be used to monitor the V_{DD} voltage rail.

Figure 3-29. Supply Monitor Circuit



The voltage monitor circuit allows the implementation of multiple applications such as:

- Detection of fault conditions
- Detection of low power mode entering conditions
- Detection of wake-up situations
- Measuring of PLC power amplifier voltage value

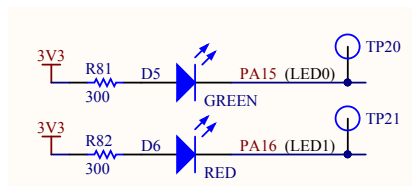
3.5.4 LEDs and Buttons

PL360MB is equipped with three user push buttons and five LEDs.

3.5.4.1 User LEDs

The PL360MB includes two general purpose LEDs, one green connected to PA15 (LED0) and one red connected to PA16 (LED1). Also this board disposes of three green LEDs connected to V_{DD} , 5 V and 3.3 V supplies for checking that these supplies are providing required voltage.

Figure 3-30. User LEDs



3.5.4.2 Push Buttons

The PL360MB board is equipped with three system push buttons. The push buttons consist of momentary push button switches mounted directly to the board. When any switch is depressed it will cause a low (zero) to appear at the associated input pin.

- NRST (Reset, perform system reset). Every device, ATSAM4CMS16C and PL360, have a NRST pin: “NRST” for ATSAM4CMS16C and “NRST_360” for PL360. Besides the reset conditions managed by the reset controller peripheral of the ATSAM4CMS16C, such as Power-on Reset and brown-out monitor, user can reset manually the ATSAM4CMS16C by using a push button SW1
- FWPU (Force Wake-Up). Wake-up from Back-up mode can be done through the Force Wake-up (FWUP) pin pushing the switch button SW3 (TMP0 button)
- TMP0 (Tamper). The anti-tamper input TMP0 is connected to switch SW2 (TMP0 button). This pin can also be used as a wake-up function.

Figure 3-31. Reset Button

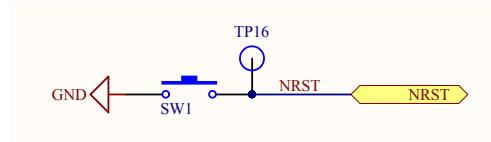
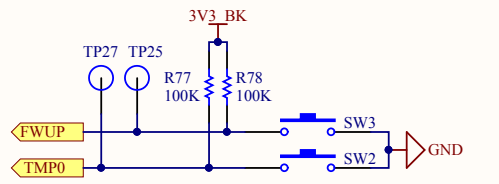


Figure 3-32. Tamper 0 & Force Wake-up Buttons

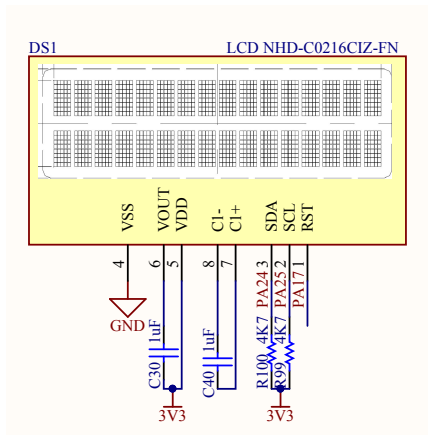


If wake-up and/or anti-tampering pins are used either as a wake-up or a fast start-up input, or as anti-tamper inputs, VDDIO must be supplied. Therefore the BT1 battery or C90 capacitor and circuitry respective must be populated.

3.5.5 Liquid Crystal Display

The PL360MB includes a Chip-on-Glass (COG), Liquid Crystal Display (LCD), DS1, model NHD-C0216CiZ-FN-FBW-3V of 2 lines x 16 characters, 5 x 8 dots with cursor with I²C interface and without LED backlight.

Figure 3-33. Display Schematic



3.5.6 Chip Erase

The 1x2 right angle pin-header J14 marked as “ERASE” is connected to the SAM4CMS16C chip erase pin (PC9) and 3.3 volts. This header can be used to re-initialize the Flash content (and some of its NVM bits) to an erased state (all bits read as logic level 1) by placing a jumper on the header and pressing the reset switch button. After a while, the erase jumper should be removed and the PCBA must be turned off

and turned on by disconnecting and connecting it again to the mains grid. See chapter “ERASE Pin” in the SAM4CMS16C datasheet for more information.

3.5.7 SAM4CMS JTAG Debug Port

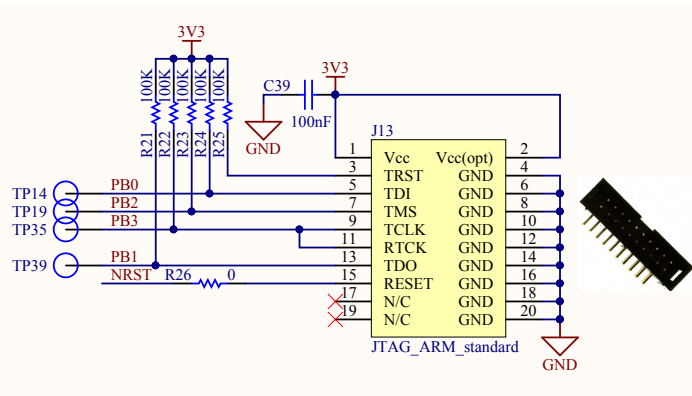
PL360MB board includes a JTAG interface port to provide debug level access to the system-on-chip. The JTAG port is a 20-pin, dual row, 0.1-inch male right angle connector (J13). This provides the required interface for in-circuit emulators such as the ARM® Multi-ICE and Atmel SAM-ICE™.



Important: Note that PL360-EK does not provide a [SAM-ICE JTAG](#) emulator probe to connect to the user’s host PC and the boards in order to download and debug the projects.

Please refer to the [SAM4CMS datasheet](#) for further description of the JTAG debug port.

Figure 3-34. JTAG/ICE Interface Schematic



Remember that the SAM4CMS16C JTAG connector is non-isolated. Please make use of proper isolation (i.e., USB isolator device) if debugging when the board is not galvanically isolated (metrology circuit measurements or using an *PLCOUPxxx* board which it is not isolated from mains).



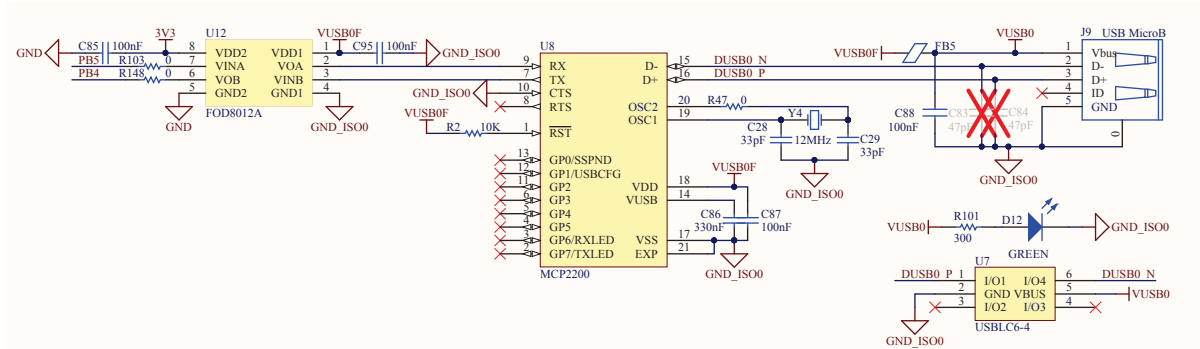
Important: If you are using USB isolators to connect the devices to the computer, take into account the possible noise that these isolators could be adding to the PLC network. Some of these USB isolators use frequencies of the FCC band that could affect the communications. For example, you can use the [UH401](#).

3.5.8 UART/USB Bridge Interface

UART0 of ATSAM4CMS16C is user accessible by means of micro USB type B connector (J9). A single chip bridge, MCP2200 device, is used to convert the UART signal to USB levels to ease PC connectivity (USB 2.0, full speed) for debugging purposes.

A high speed optocoupler provides isolation between the PCB signals and your PC. This lets you connect the USB cable when you are using metrology circuit or an *PLCOUPxxx* board not isolated from mains.

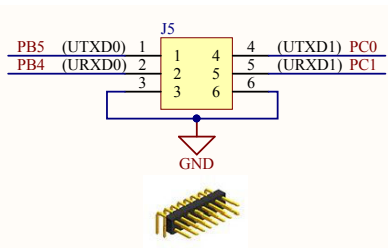
Figure 3-35. Debug UART over USB Circuit



Important: Check [weblink](#) to download the drivers according to your Operative System.

Furthermore, UART0 and UART1 as TTL level signals (3.3 V) are also available in a triple row male connector (J5). If this interface is used, USB port (J9) must remain unconnected to avoid collisions on UARTs signals.

Figure 3-36. Debug UARTs over 3.3 Volts Levels



This connector is not isolated from mains. Please make use of proper isolation (i.e.: USB isolator device) in case of debugging when the board is not galvanically isolated (metrology circuit measurements or using an *PLCOUPxxx* board which it is not isolated from mains).

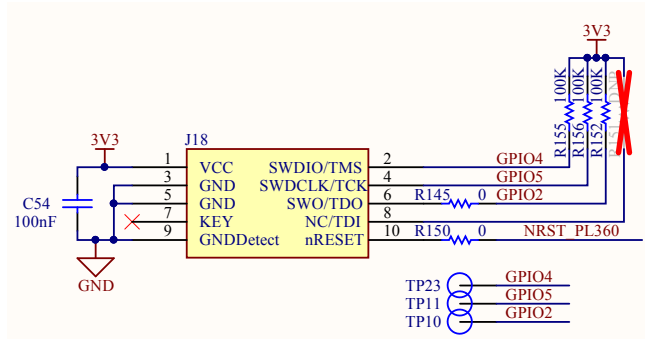
3.6 Hardware Description – PL360 Interface Ports

3.6.1 Serial Wire Debug Port

PL360MB board includes a Serial Wire Debug Port (SW-DP) used for internal debugging functions, such as downloading code and single-stepping through programs. It also embeds a serial wire trace. The SW-DP port is a 10-pin, dual row, 0.1-inch male connector (J18). This connector provides the required interface for in-circuit emulators. To use the ARM Multi-ICE and Atmel SAM-ICE a JTAG adapter for 20 to 10 pins is necessary, e.g., [this one](#).

Please refer to the [PL360 datasheet](#) for a further description of SW-DP debug port.

Figure 3-37. SWD & Trace Schematic



Remember that the SW-DP connector is non-isolated from mains. Please make use of proper isolation (i.e.: USB isolator device) in case of debugging when the board is not galvanically isolated (metrology circuit measurements or using an *PLCOUPxxx* board which it is not isolated from mains).



Important: If you are using USB isolators to connect the devices to the computer, take into account the possible noise that these isolators could be adding to the PLC network. Some of these USB isolators use frequencies of the FCC band that could affect the communications. For example, you can use the [UH401](#).

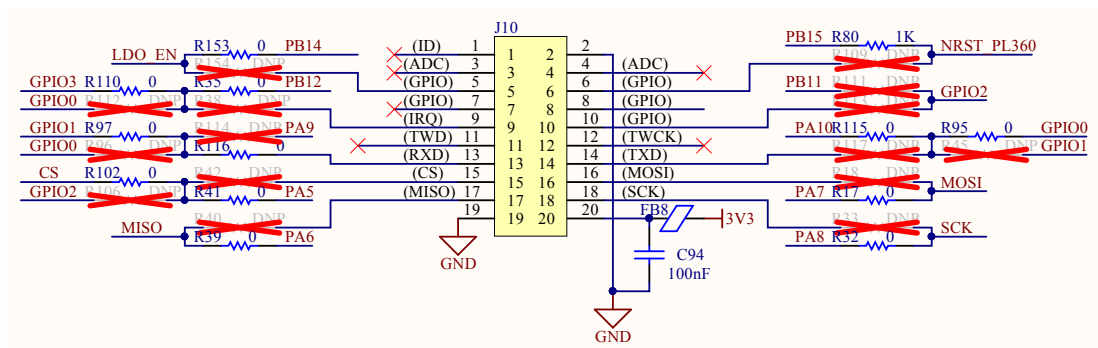
3.6.2 Xplained Pro Connector

Xplained Pro connector (J10) is Atmel's proprietary interface port intended to connect different [evaluation platforms](#) from AVR[®] and ARM microcontrollers.

This connector lets you manage PL360 with another MCU different from SAM4CMS. PL360MB Xplained Pro provides the following features:

- SPI
- UART
- I²C
- 2 ADC inputs
- 1 IRQ input
- 5 GPIOs

Figure 3-38. Extension Connector





Important: By default, output resistors to the connectors are not populated in the board.

3.7 PL360MB Schematics

This section contains the schematics for the PL360MBv1 board:

- Top Level Schematic, [Figure 3-39](#)
- Power Supply Schematic, [Figure 3-40](#)
- SAM4CMS16C Schematic, [Figure 3-41](#)
- Metrology AFE Schematic, [Figure 3-42](#)
- Metrology Opto and Relays Schematic, [Figure 3-43](#)
- Peripherals SAM4CMS Schematic, [Figure 3-44](#)
- PL360 Schematic, [Figure 3-45](#)
- Peripherals PL360 Schematic, [Figure 3-46](#)
- PLC Coupling Schematic, [Figure 3-47](#)

Figure 3-39. Top Level Schematic

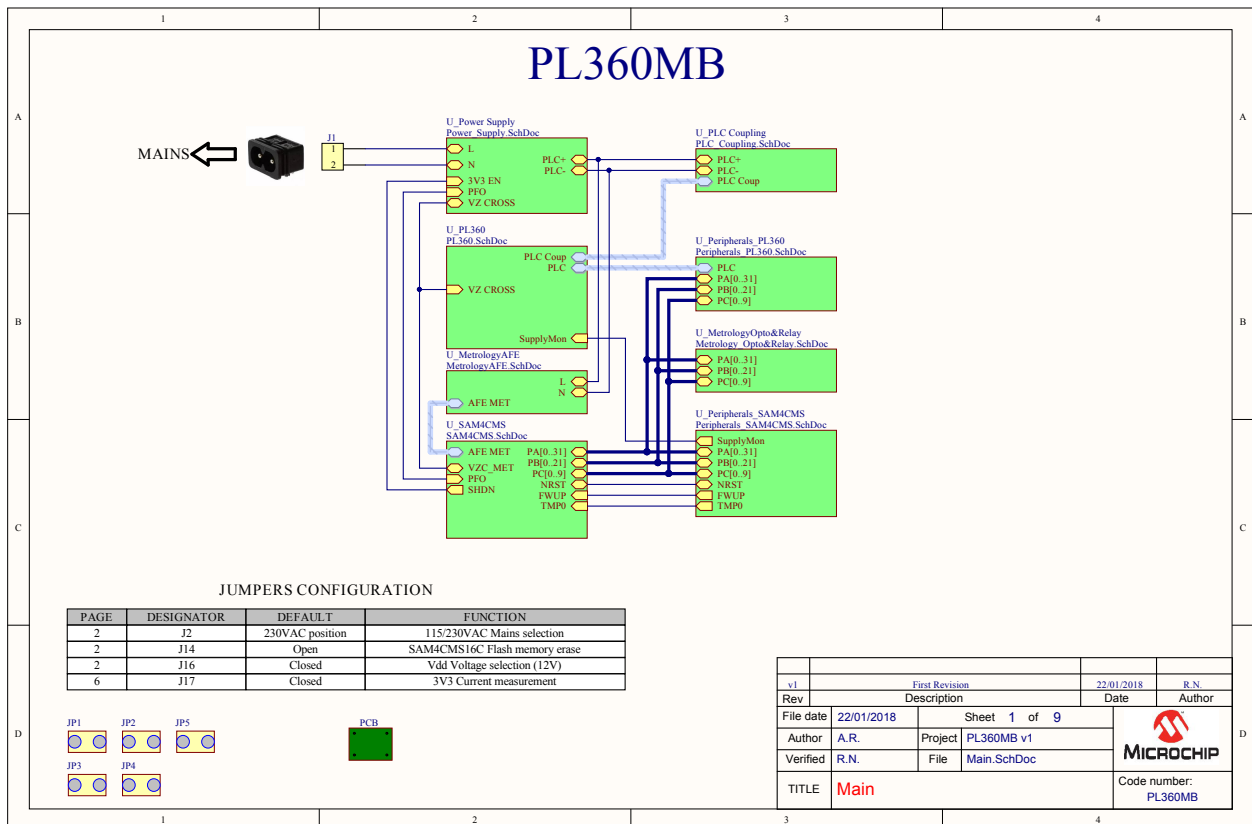
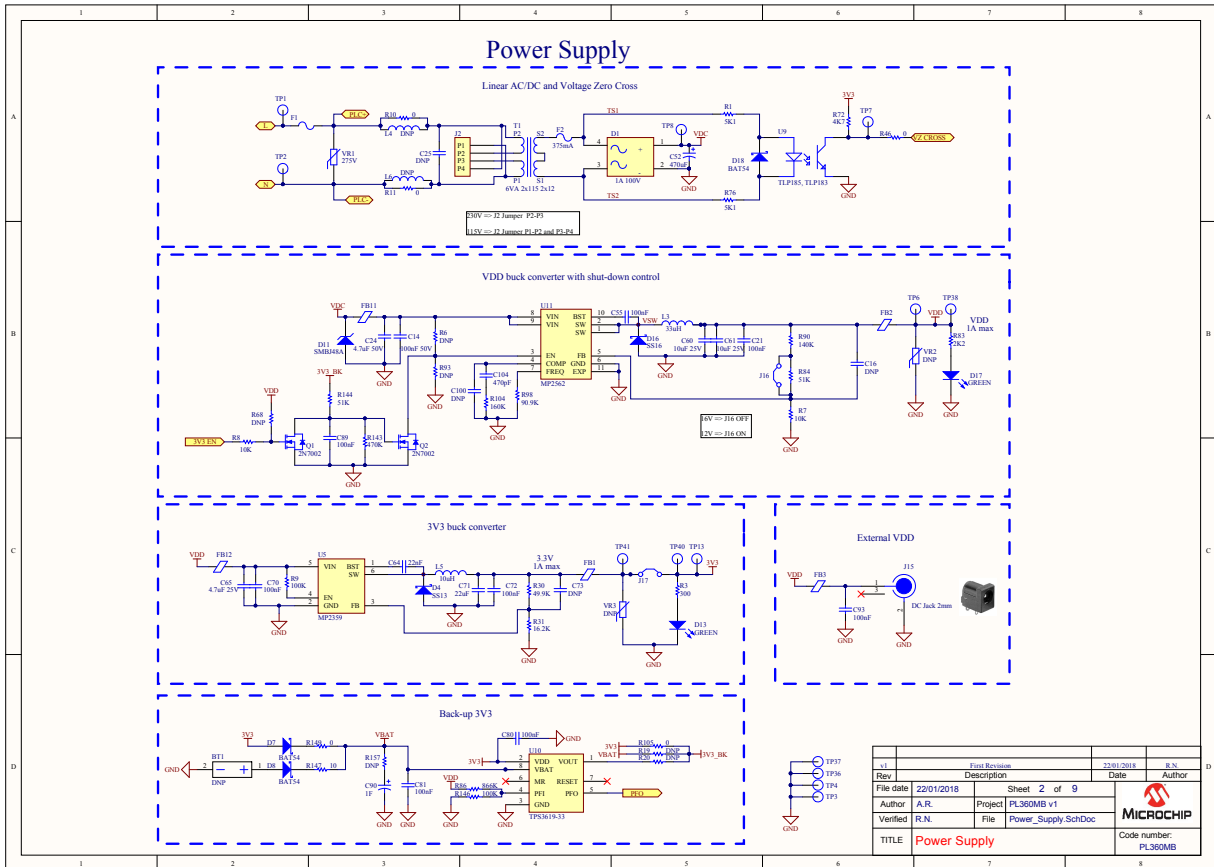


Figure 3-40. Power Supply Schematic



Rev		File date	Author	Project	File	Sheet	Date	R.N.
1		22/01/2018	A.R.L.	PL360MB v1	Power_Supply_SchDoc	2 of 9	22/01/2018	
2			R.N.					

TITLE	Power Supply	Code number:	PL360MB
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Figure 3-41. SAM4CMS16C Schematic

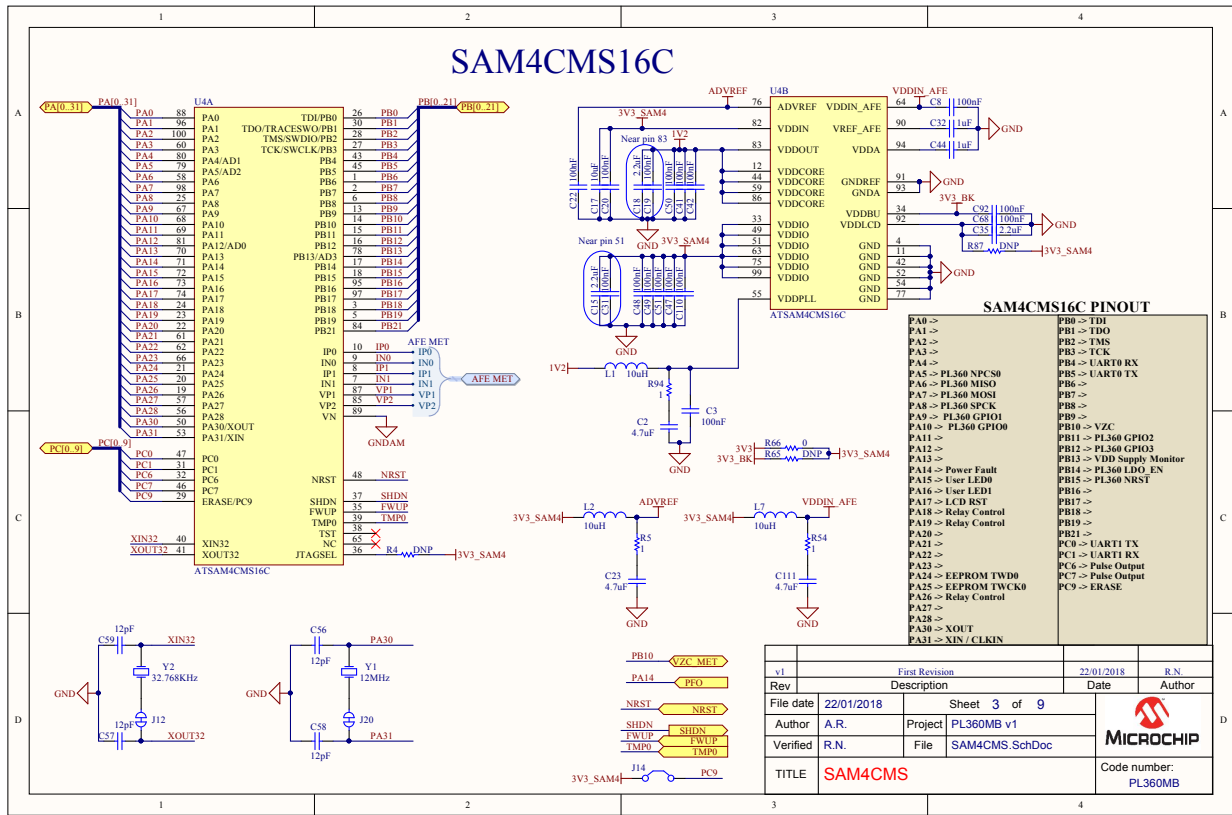


Figure 3-42. Metrology AFE Schematic

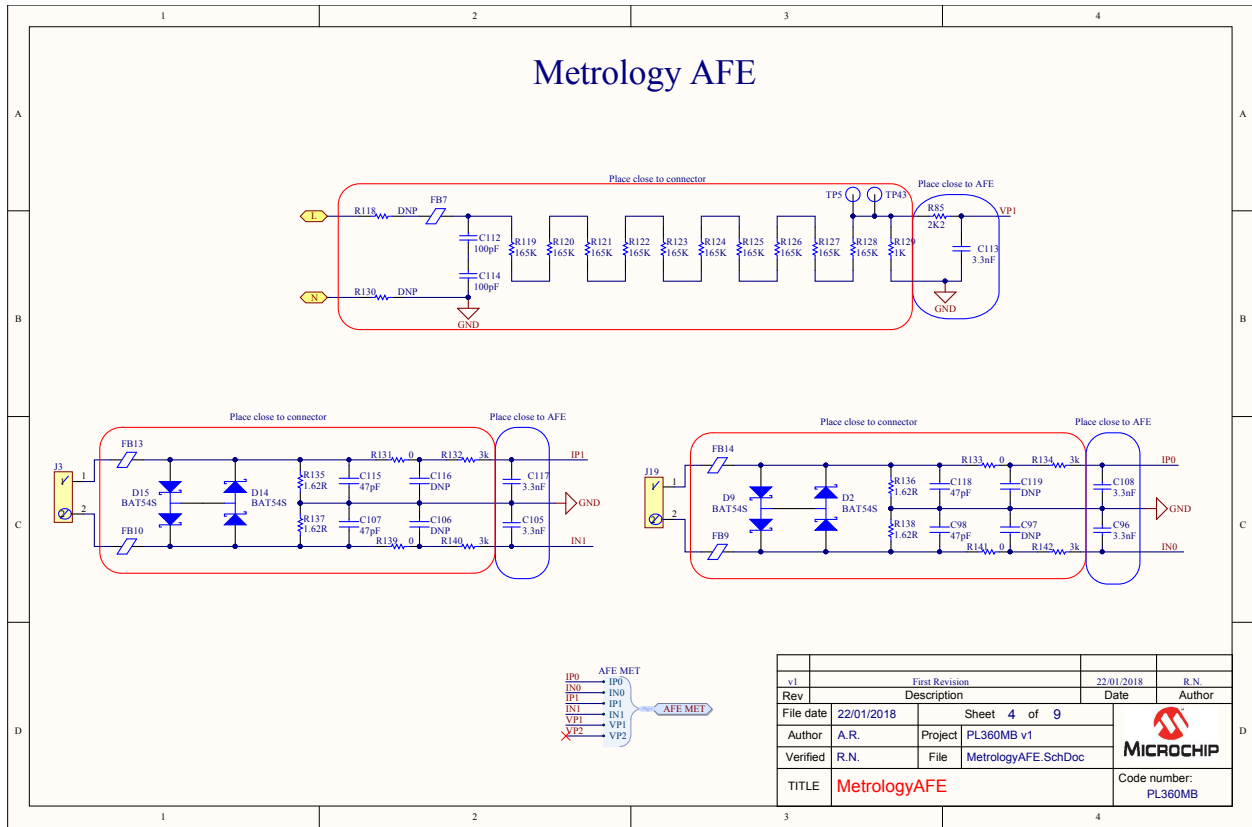


Figure 3-43. Metrology Opto and Relays Schematic

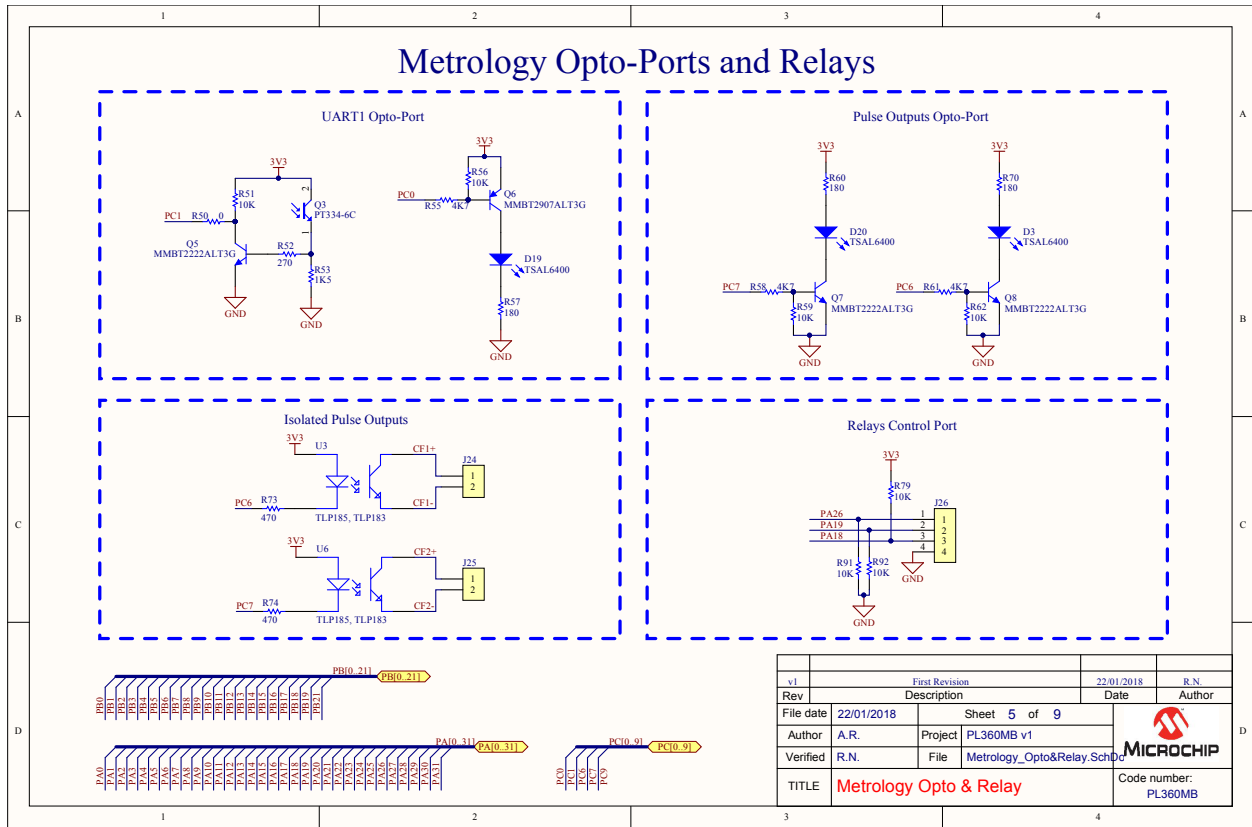


Figure 3-44. Peripherals SAM4CMS Schematic

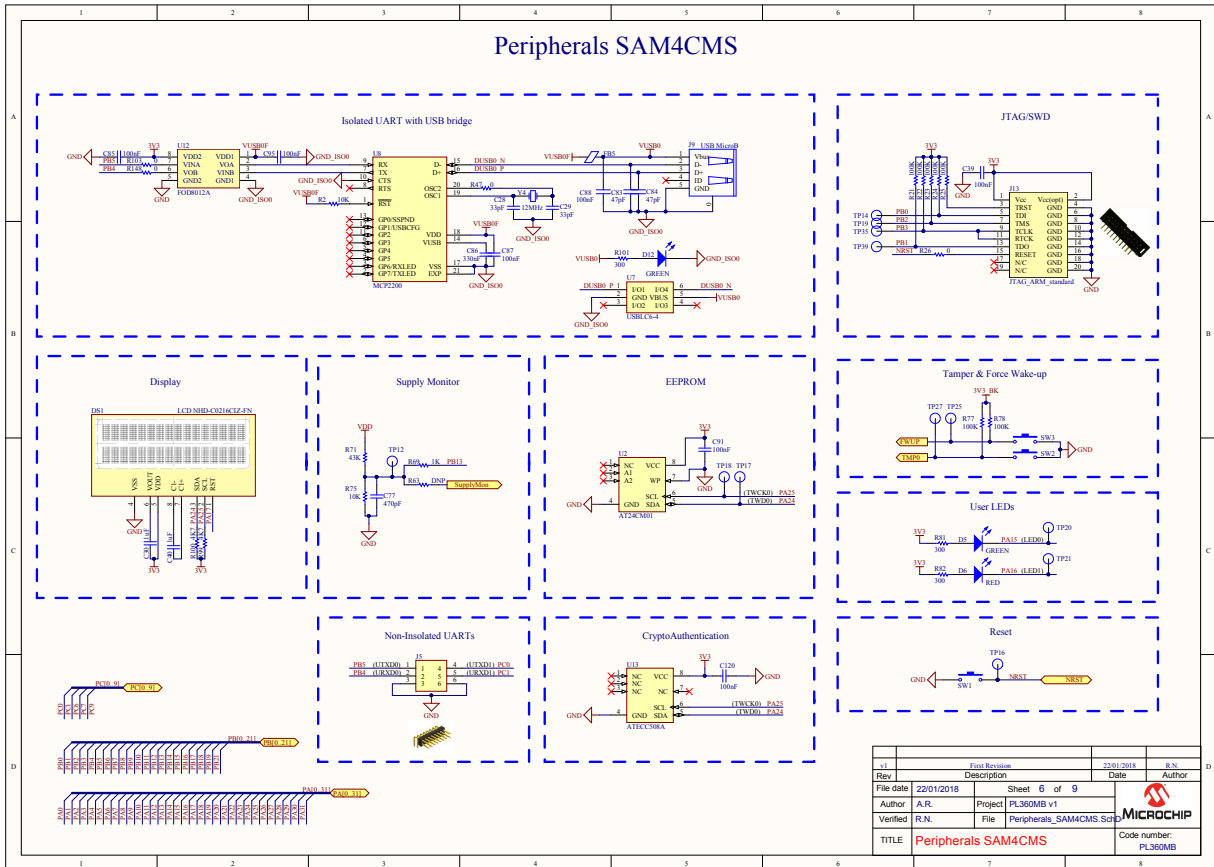


Figure 3-45. PL360 Schematic

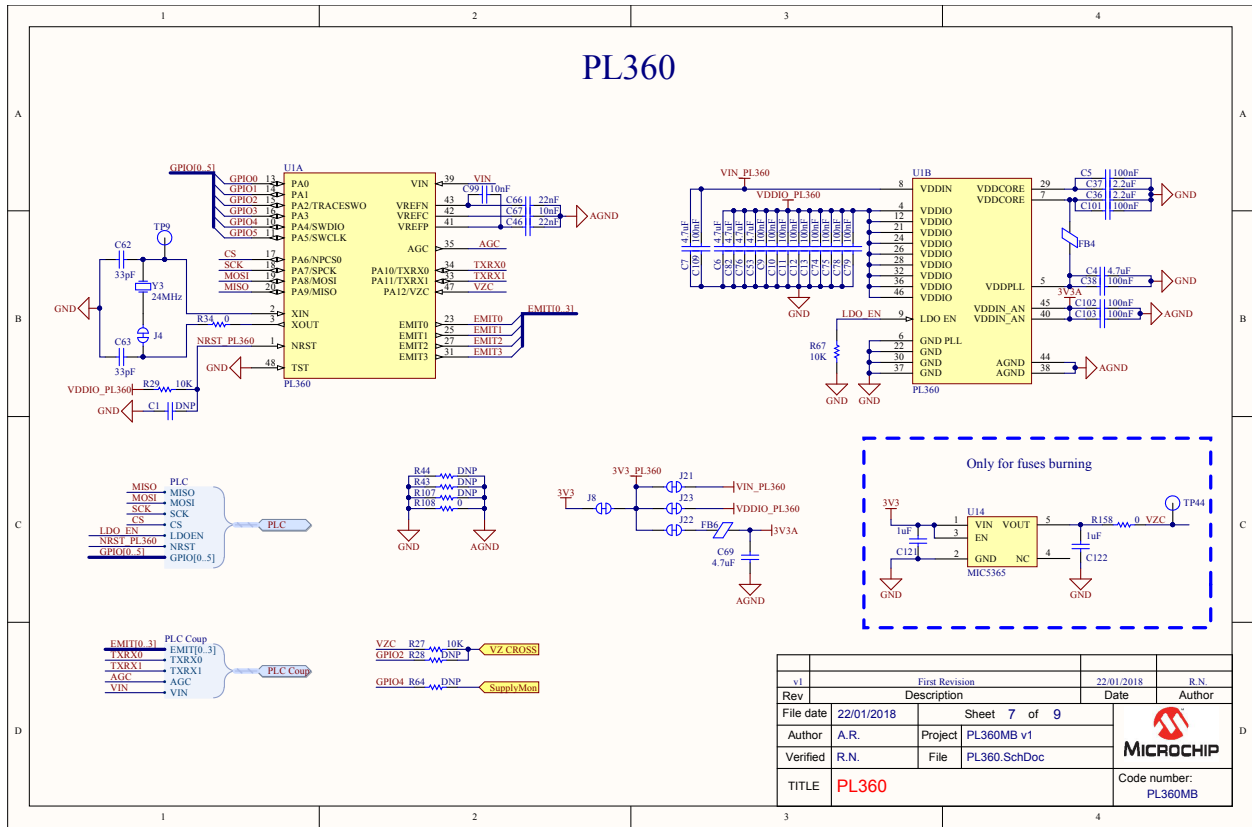
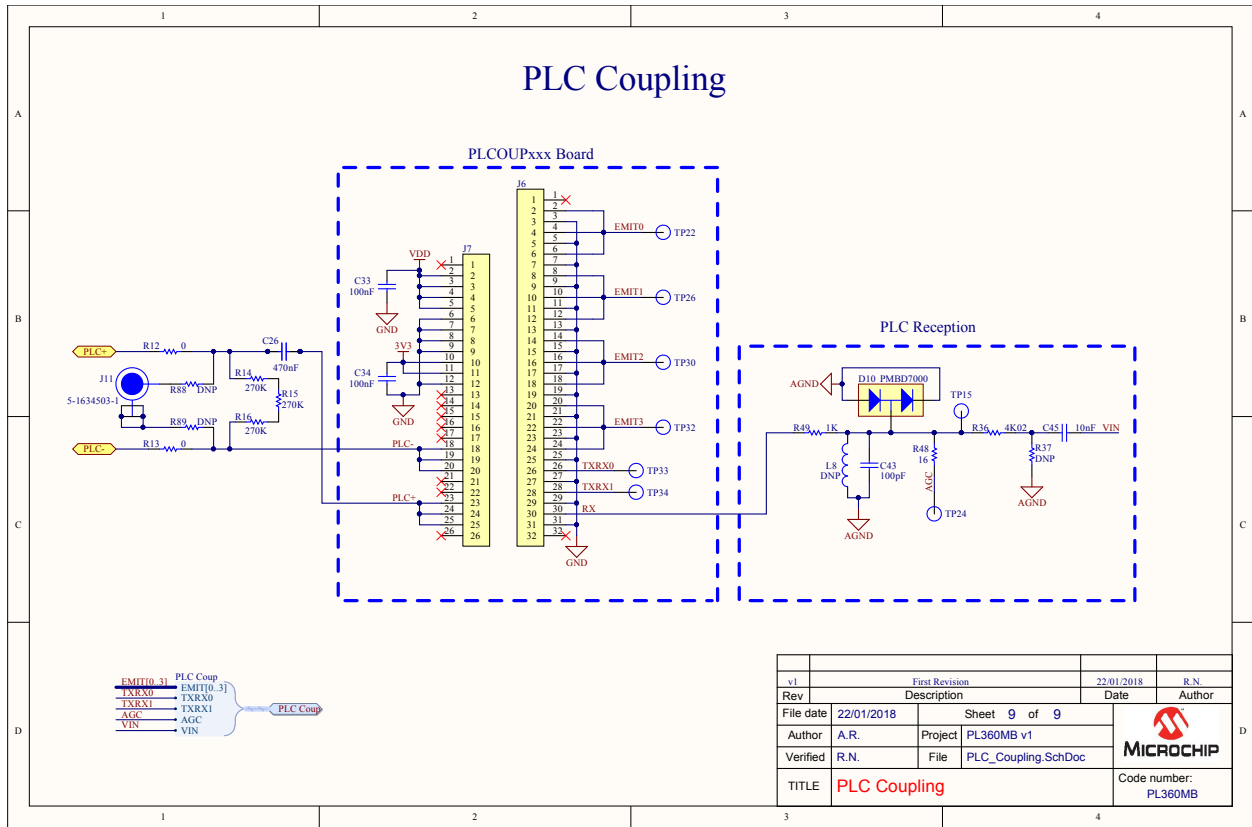


Figure 3-47. PLC Coupling Schematic



3.8 PL360MB Layout

This section contains the layout graphics for the PL360MBv1 board:

- Layer 1: Top Layer, [Figure 3-48](#)
- Layer 2: Mid Layer 1 (Ground), [Figure 3-49](#)
- Layer 3: Mid Layer 2 (Power Supplies), [Figure 3-50](#)
- Layer 4: Bottom Layer, [Figure 3-51](#)
- Top Components Placement, [Figure 3-52](#)
- Bottom Components Placement, [Figure 3-53](#)

Figure 3-48. PL360MBv1 Layout: Top Layer

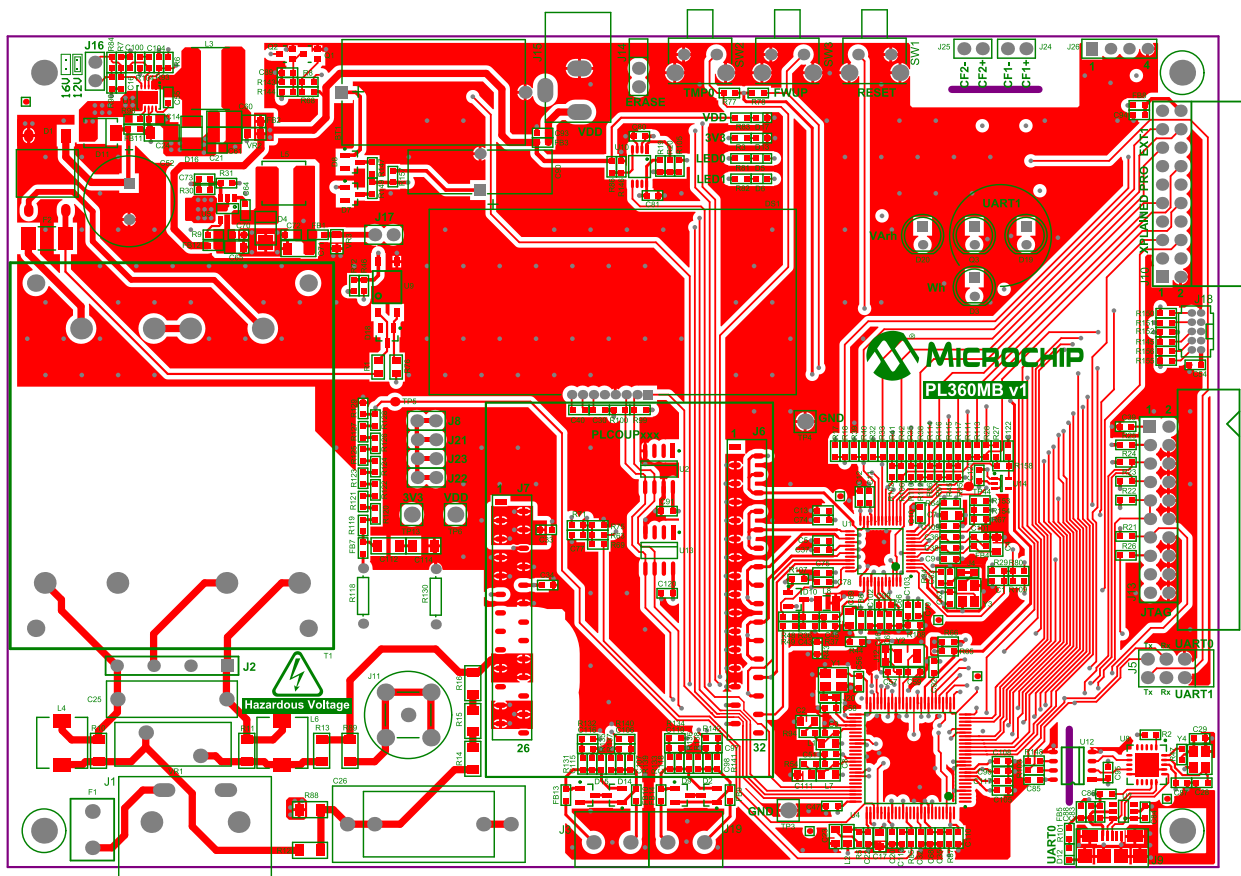


Figure 3-49. PL360MBv1 Layout: Mid Layer 1 (Ground)

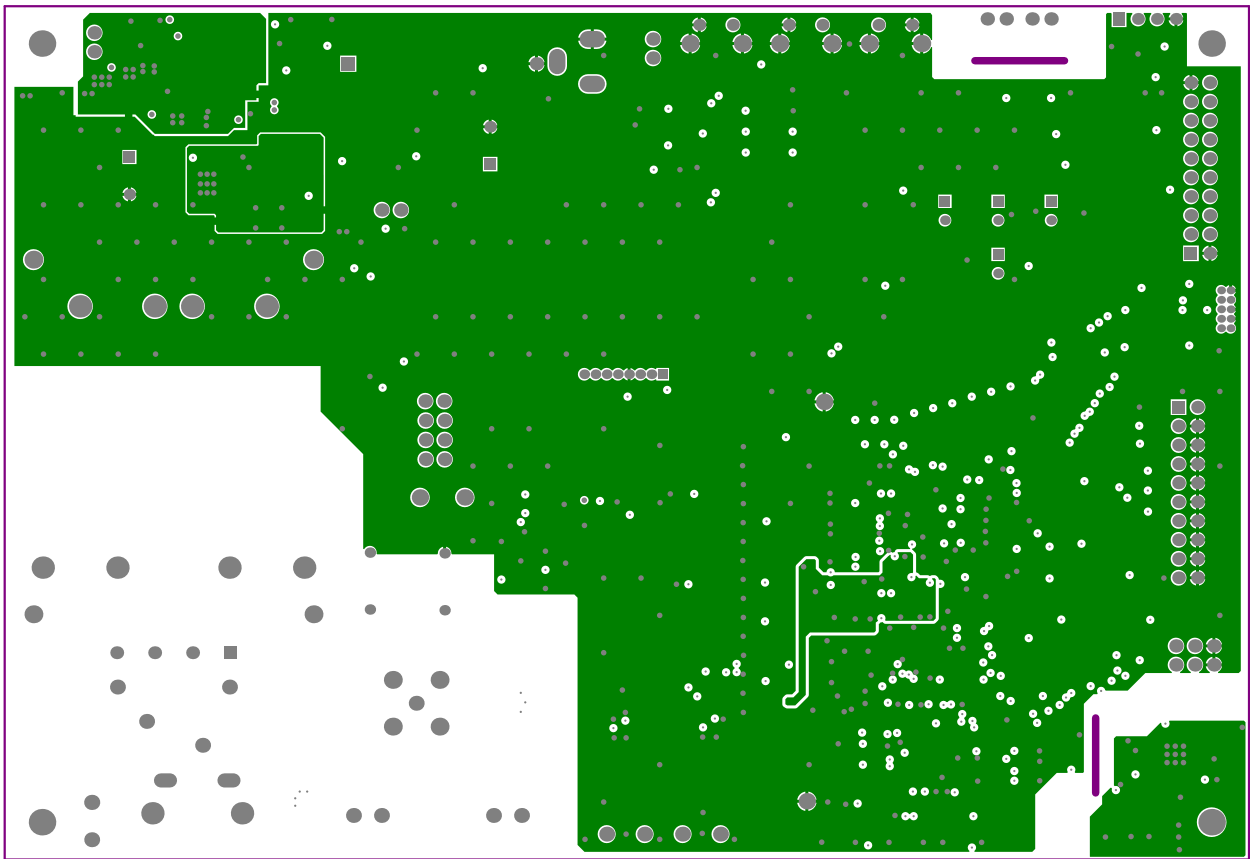


Figure 3-50. PL360MBv1 Layout: Mid Layer 2 (Power Supplies)

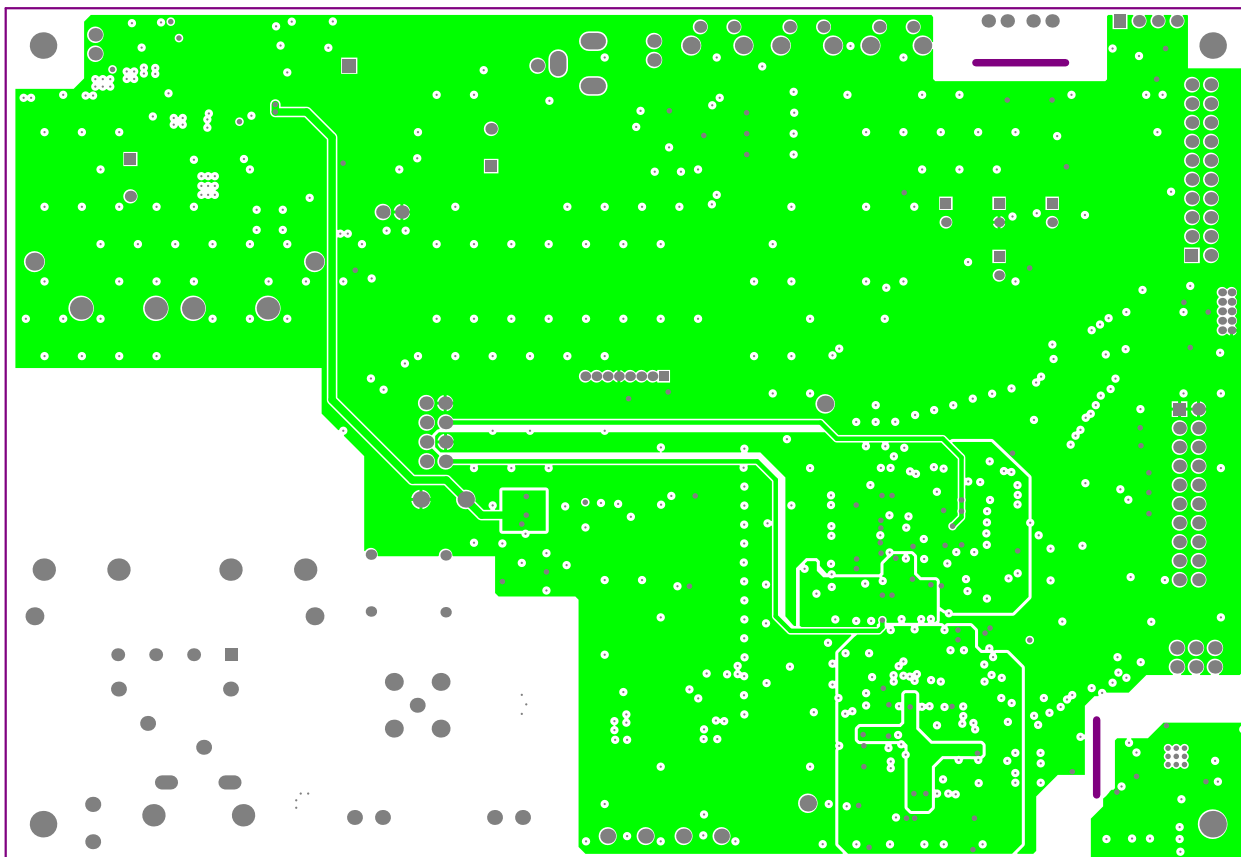


Figure 3-51. PL360MBv1 Layout: Bottom Layer

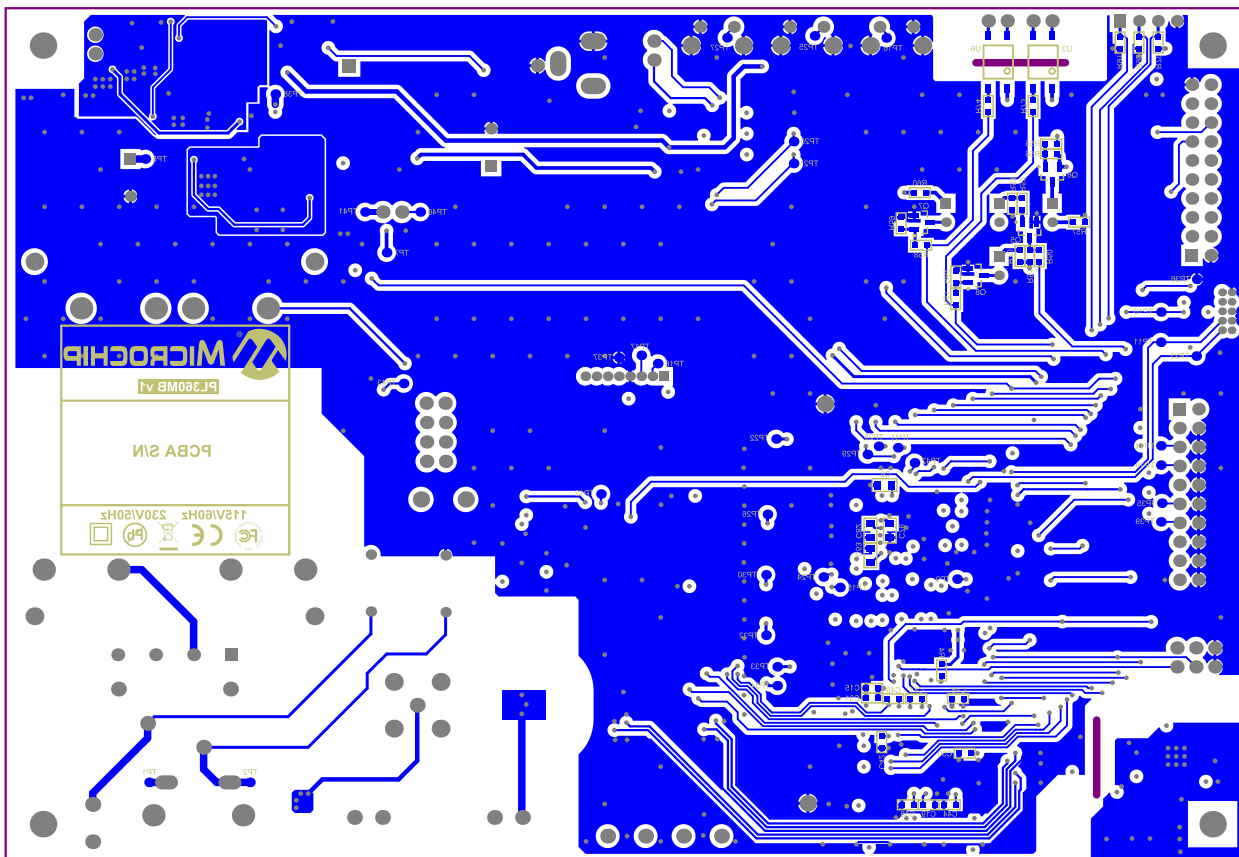


Figure 3-52. PL360MBv1 Layout: Top Components Placement

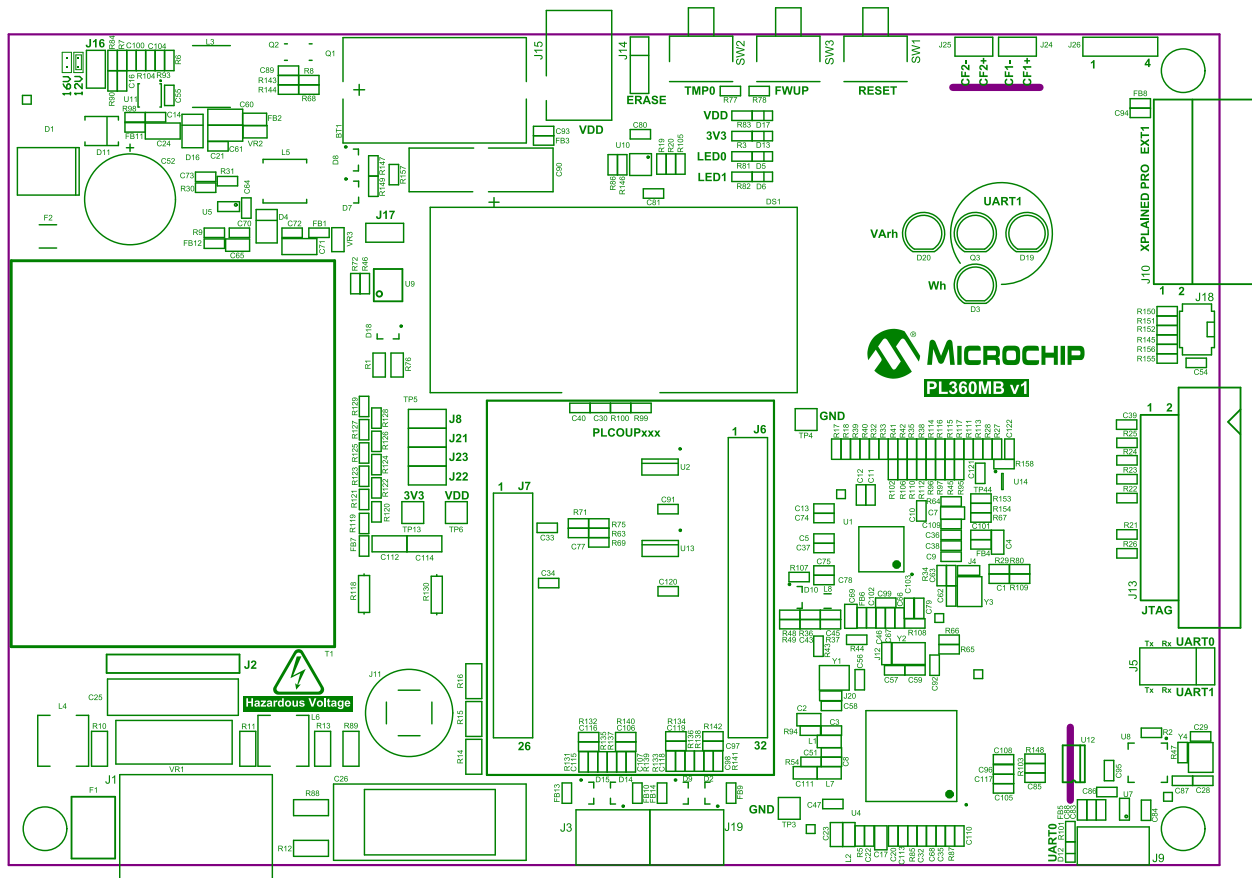
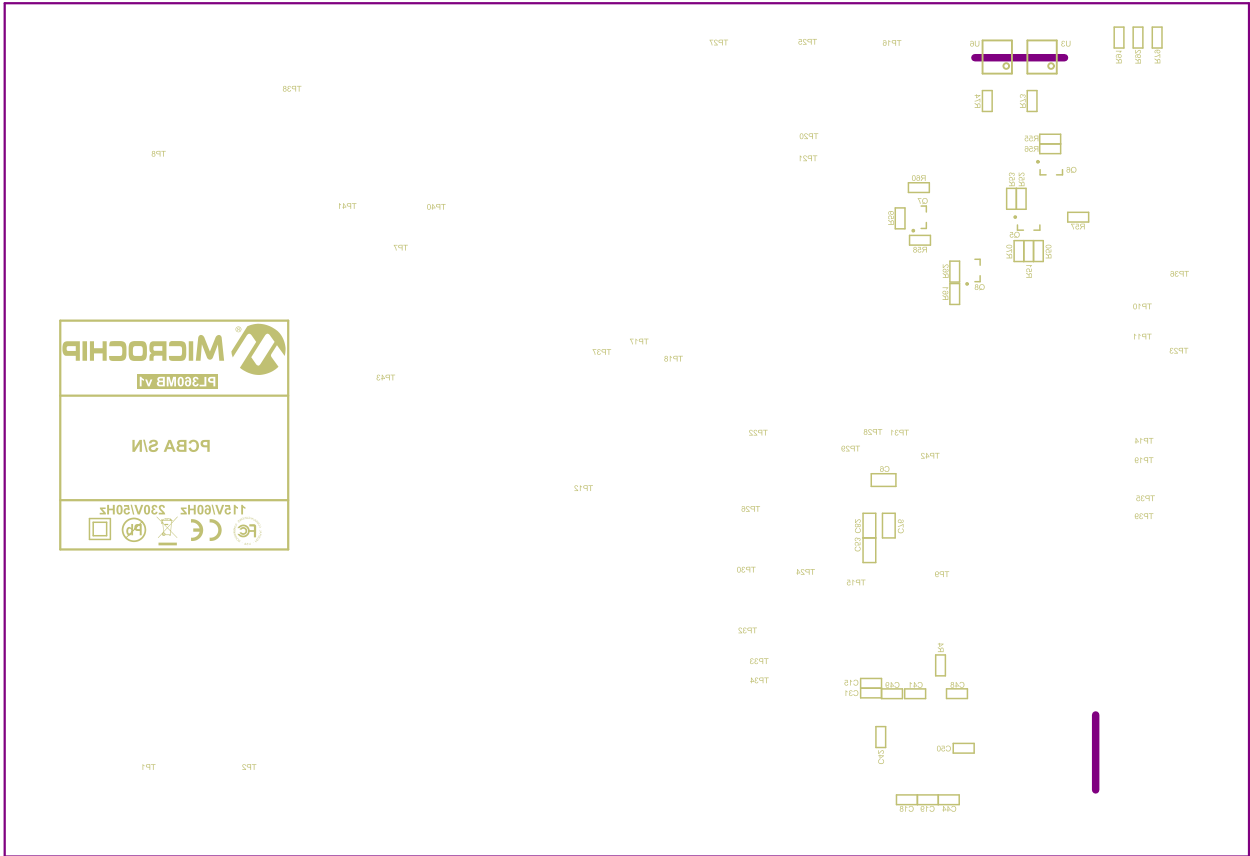


Figure 3-53. PL360MBv1 Layout: Bottom Components Placement



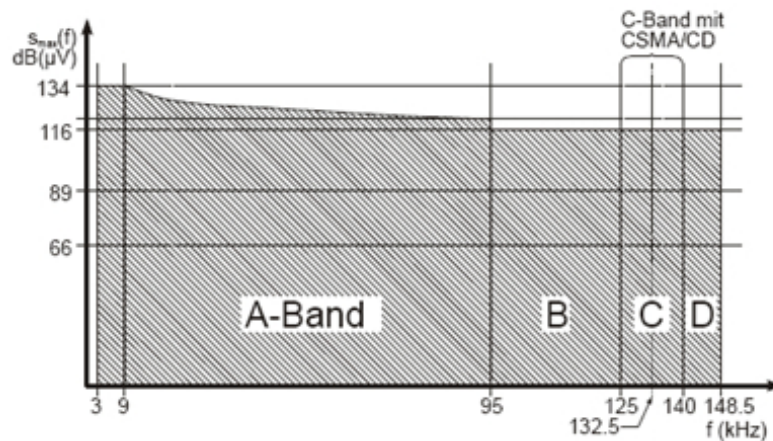
4. PLCOUP007 Board

4.1 Overview

PLCOUP007 is a PLC coupling board designed to communicate in CENELEC A-Band. PLCOUP007 mounts a single branch with galvanic isolation between mains and main board. The goal of this design is to provide to the customers a cost optimized-transmission board for CENELEC A-Band design. This coupling board fulfills requirements of both PRIME and G3-PLC protocols.

This board is set by default in the PL360MB board of the PL360-EK.

Figure 4-1. CENELEC Bands

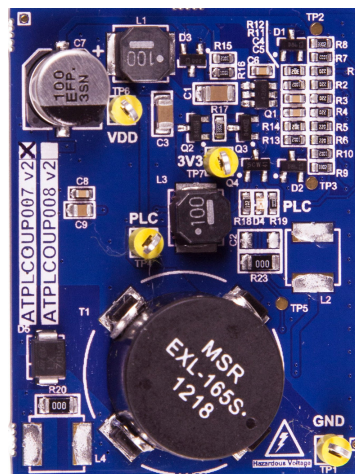


4.2 Features List

A PLCOUP007v2.5 board includes the following features:

- Suitable for both PRIME and G3-PLC protocols (CENELEC A-Band)
- Voltage isolation from mains with a transformer, MSR EXL-165S-LT, soldered in top layer board
- Low impedance design optimized

Figure 4-2. PLCOUP007v2.5 PLC Coupling Board (Top View)



4.3 Mechanical and User Considerations

The PLCOUP007 board is delivered with the PL360-EK. Board-to-board SMD connectors in bottom layer, J1 and J2, are used to connect the PLCOUP007 into connectors J6 and J7 of PL360MB board.

Hazardous voltage is present on the PLCOUP007 board. To avoid user access to dangerous parts, PLCOUP007 and PL360MB must always be used in its enclosure.

The board's dimensions are 51.5 mm x 39.5 mm x 18 mm (LxWxH) and the operating temperature range is -40 to 85°C.

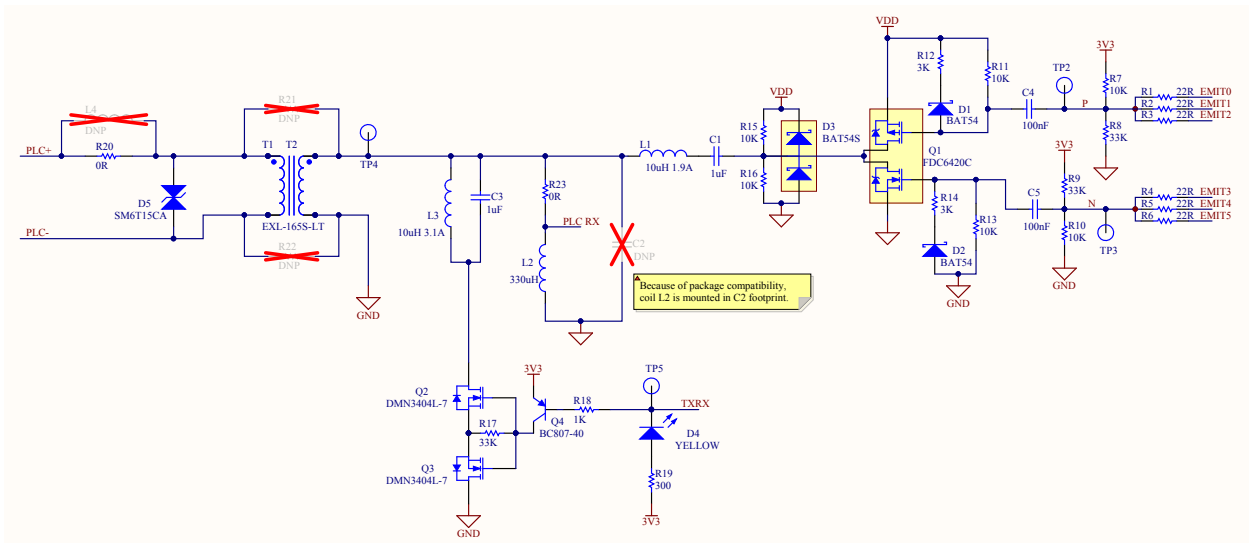
4.4 Hardware Description

The PLCOUP007 board is composed of a transmission branch whose filtering stage has a flat band pass response with typical field impedance. It involves a cost optimization in the BOM.

The PLCOUP007 board is equipped with four test points (V_{DD} volts, 3.3 volts, ground and PLC signal) and one orange LED for transmission indication.

The PLCOUP007 board could be transformed in an PLCOUP008 board (galvanically non-isolated board version), removing R20 resistor, removing T1 transformer, soldering two 0 ohms resistors in R21 and R22 and soldering a 15 μH coil in L4.

Figure 4-3. PLC Coupling Transmission Schematic

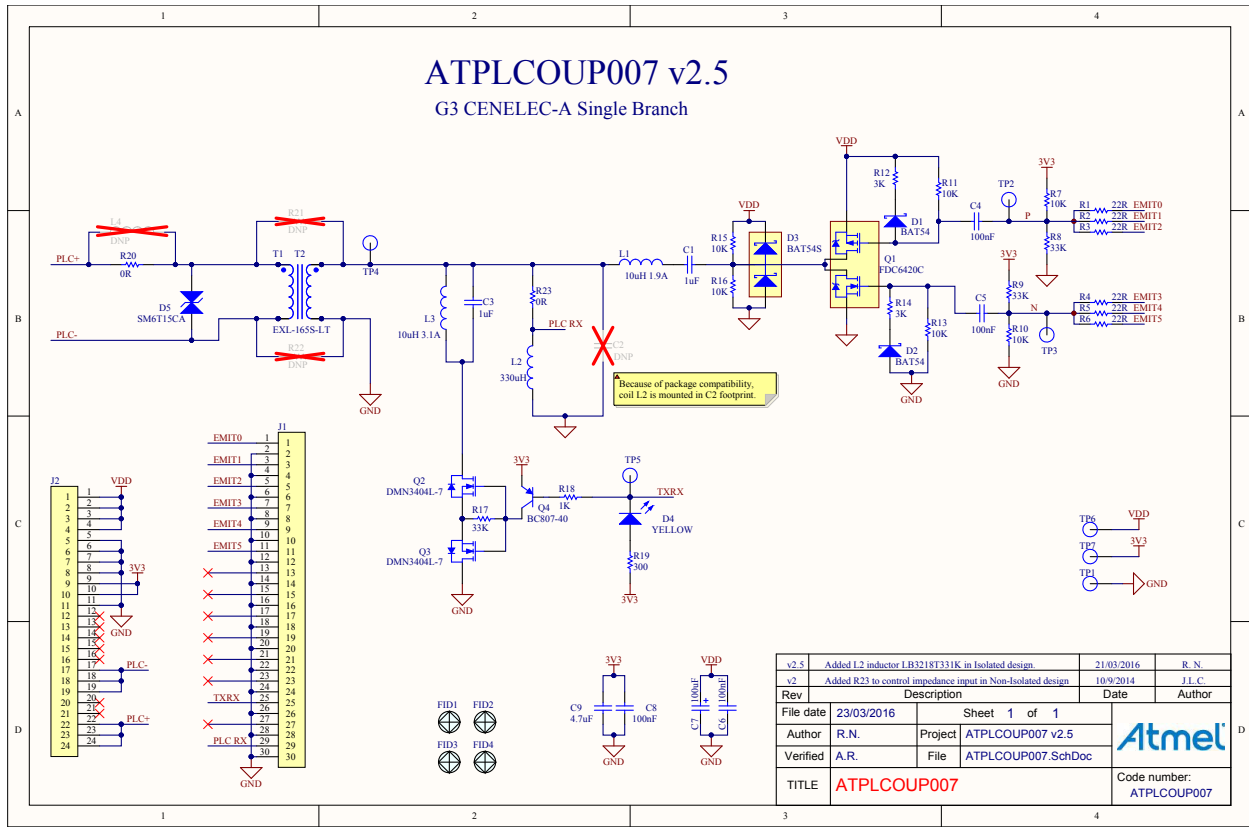


Take into account that, when PLCOUP007 board is set over PL360MB board, V_{DD} voltage must be 12 volts to maintain the high efficiency consumption; therefore, jumper in J16 must be set (see section [Power Supply System](#)).

4.5 PLCOUP007 Schematic

This section contains the PLC Coupling Transmission Schematic for the PLCOUP007v2.5 board.

Figure 4-4. PLC Coupling Transmission Schematic



4.6 PLCOUP007 Layout

This section contains the layout graphics for the PLCOUP007v2.5 board:

- Layer 1: Top Layer, [Figure 4-5](#)
- Layer 2: Bottom Layer, [Figure 4-6](#)
- Top Components Placement, [Figure 4-7](#)
- Bottom Components Placement, [Figure 4-8](#)

Figure 4-5. PLCOUP007v2.5 Top Layer

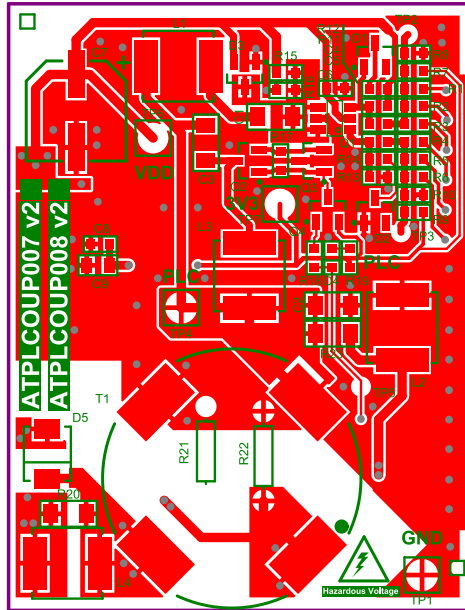


Figure 4-6. PLCOUP007v2.5 Bottom Layer

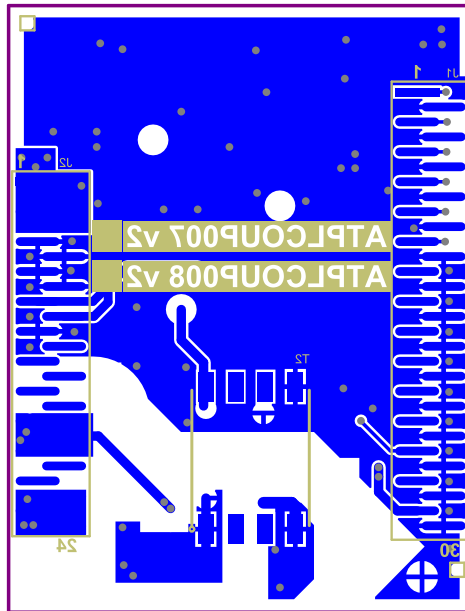


Figure 4-7. PLCOUP007v2.5 Top Components Placement

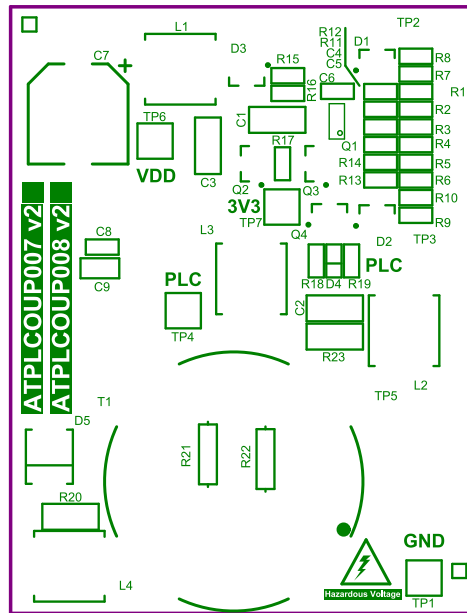
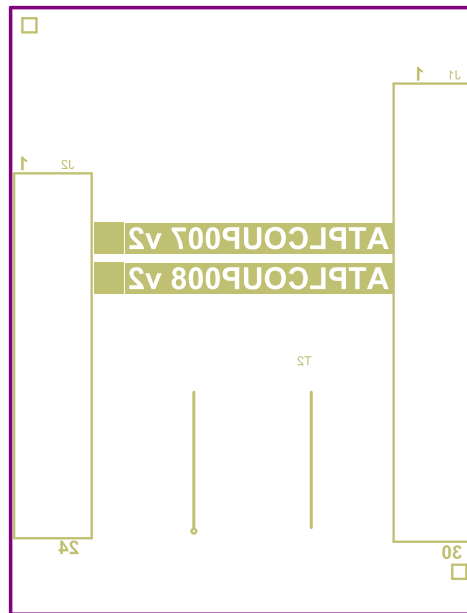


Figure 4-8. PLCOUP007v2.5 Bottom Components Placement

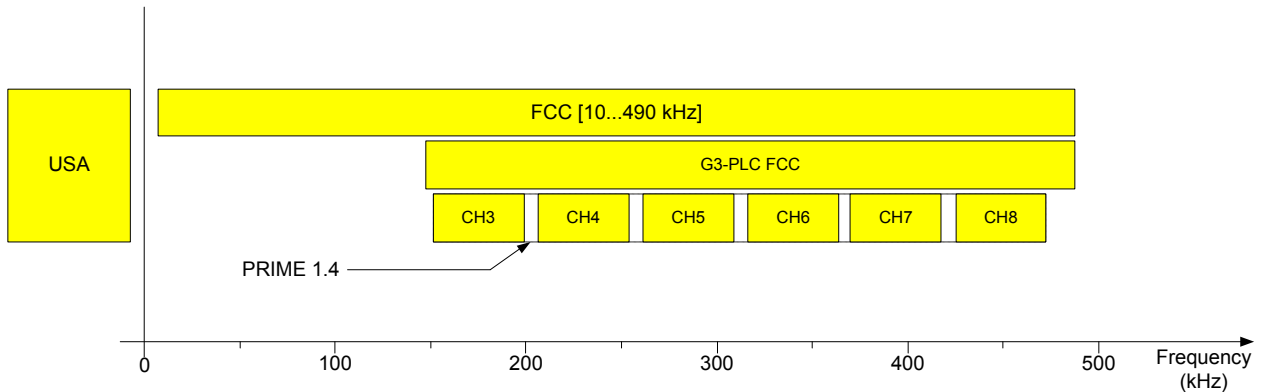


5. PLCOUP006 Board

5.1 Overview

PLCOUP006 is a PLC coupling board designed to communicate in FCC band, from 151 to 471 kHz. PLCOUP006 mounts a double branch with voltage isolation between mains and main board. The goal of this design is to provide to the customers with a full performance transmission board in FCC band.

Figure 5-1. FCC Band

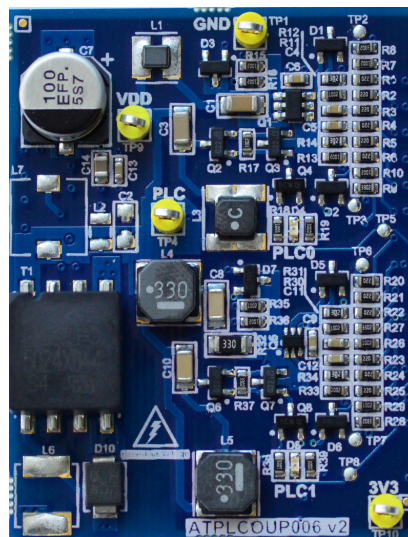


5.2 Features List

The PLCOUP006v2 board includes the following features:

- Specially designed to communicate in FCC frequency band (151.367 – 471.68 kHz)
- Voltage isolation from mains with a transformer, VAC T60403K5024X044, soldered in top layer board
- Double branch, each one for a range (low and high) of impedance optimized

Figure 5-2. PLCOUP006v2 PLC Coupling Board (Top View)



5.3 Mechanical and User Considerations

PLCOUP006 is delivered with the PL360-EK. Board-to-board SMD connectors in the bottom layer, J1 and J2, are used to connect the PLCOUP006 into connectors J6 and J7 of PL360MB board.

Hazardous voltage is present on the PLCOUP006 board. To avoid user access to dangerous parts, PLCOUP006 and PL360MB must always be used in its enclosure.

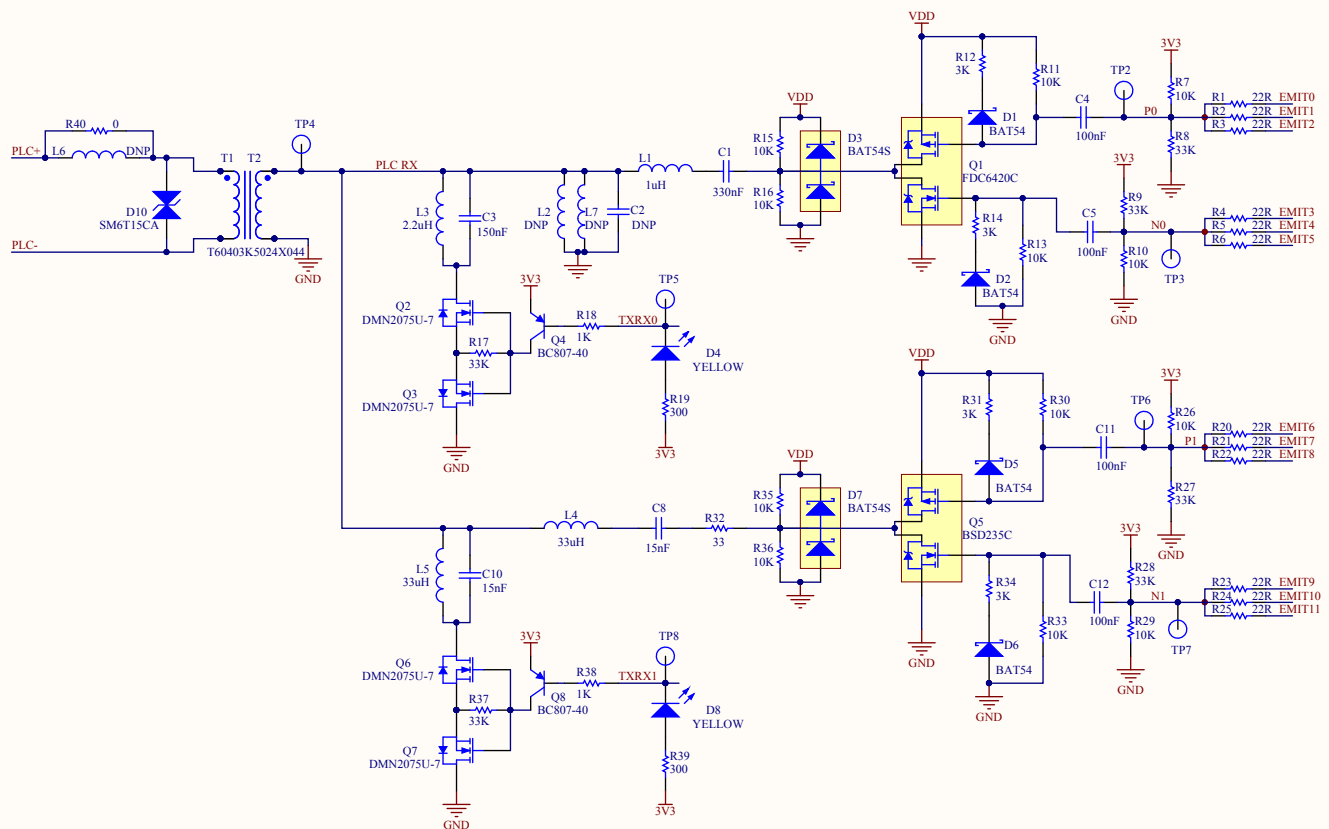
PLCOUP006 dimensions are 51.5 mm x 39.5 mm x 18 mm (LxWxH) and the operating temperature range is -40 to 85°C.

5.4 Hardware Description

PLCOUP006 board is a PLC coupling driver board with double branch design which only differ on the filtering stage. It has good performance in terms of transmitted channel power over a range of load impedance values complying with the FCC standard as the current carrier system.

PLCOUP006 is equipped with four test points (V_{DD} volts, 3.3 volts, ground and PLC signal) and two orange LEDs for transmission branch indication.

Figure 5-3. PLC Coupling Transmission Scheme

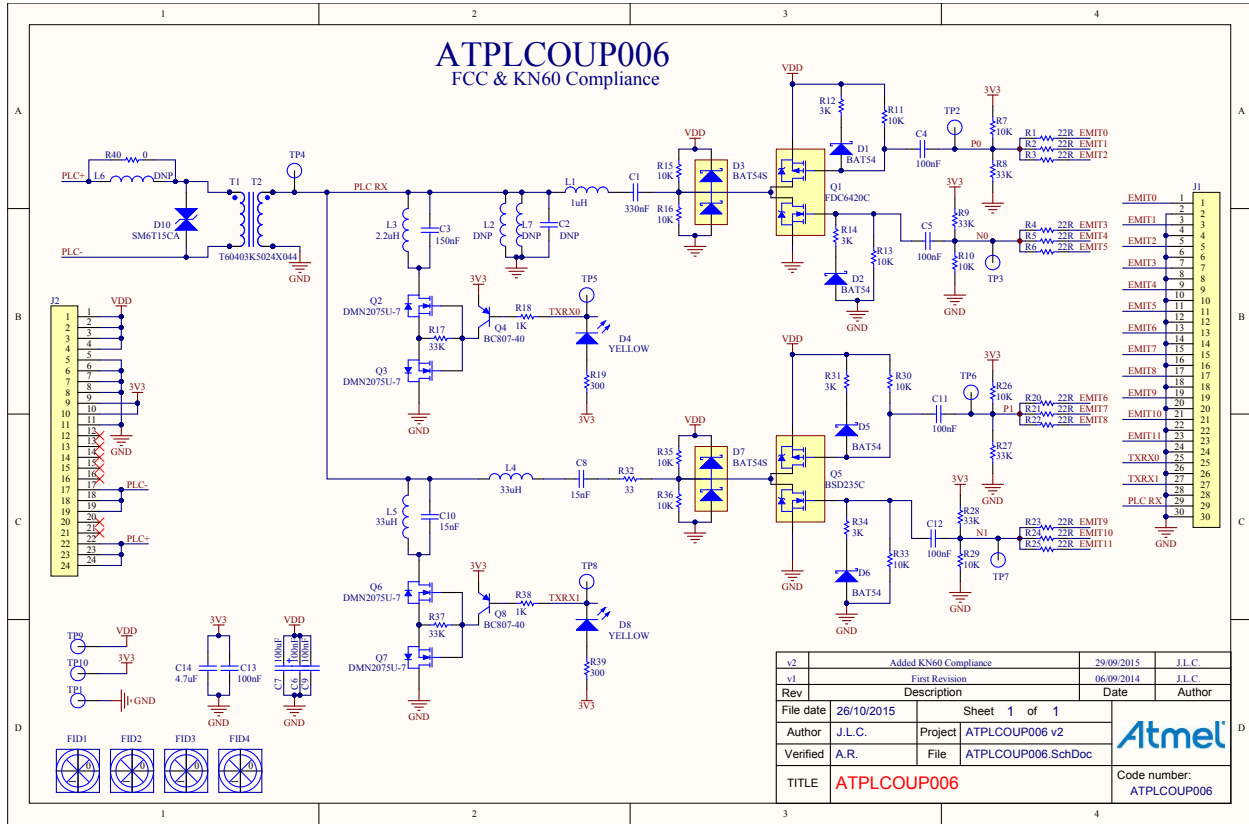


Take into account that, when PLCOUP006 is set over PL360MB, V_{DD} voltage must be 12 volts to avoid damaging the coupling board; therefore, the jumper in J16 must be set (see section [Power Supply System](#)).

5.5 PLCOUP006 Schematic

This section contains the PLC Coupling Transmission schematic for the PLCOUP006v2 board.

Figure 5-4. PLC Coupling Transmission Schematic



5.6 PLCOUP006 Layout

This section contains the layout graphics for the PLCOUP006v2 board:

- Layer 1: Top Layer, [Figure 5-5](#)
- Layer 2: Mid Layer 1 (Ground), [Figure 5-6](#)
- Layer 3: Mid Layer 2 (Power Supplies), [Figure 5-7](#)
- Layer 4: Bottom Layer, [Figure 5-8](#)
- Top Components Placement, [Figure 5-9](#)
- Bottom Components Placement, [Figure 5-10](#)

Figure 5-5. PLCOUP006v2 Top Layer

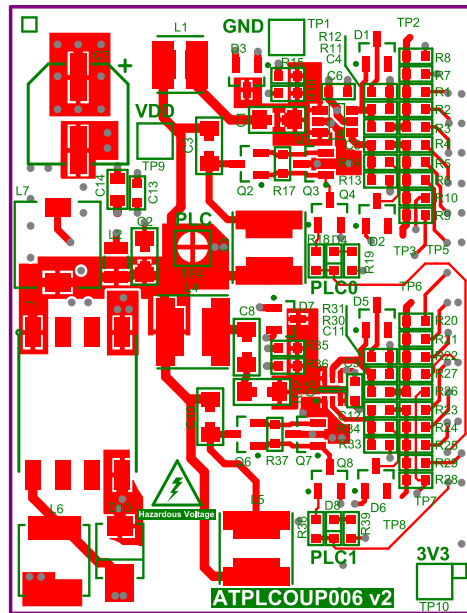


Figure 5-6. PLCOUP006v2 Mid Layer 1 (Ground)

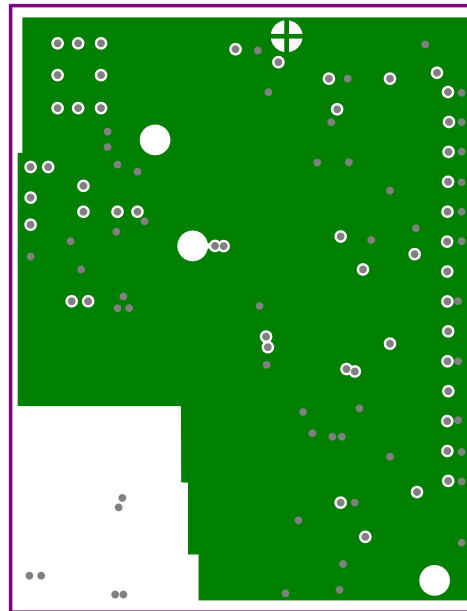


Figure 5-7. PLCOUP006v2 Mid Layer 2 (Power Supplies)

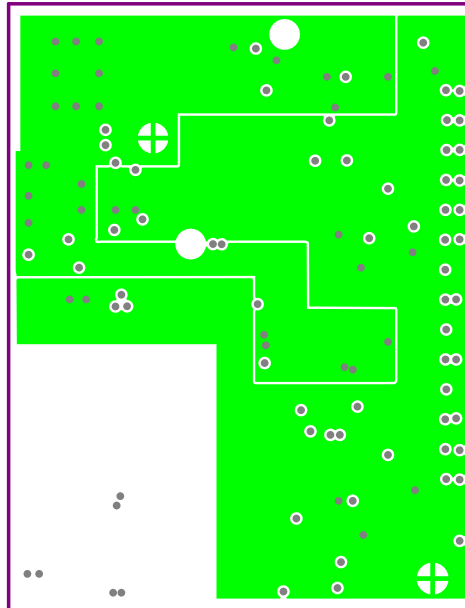


Figure 5-8. PLCOUP006v2 Bottom Layer

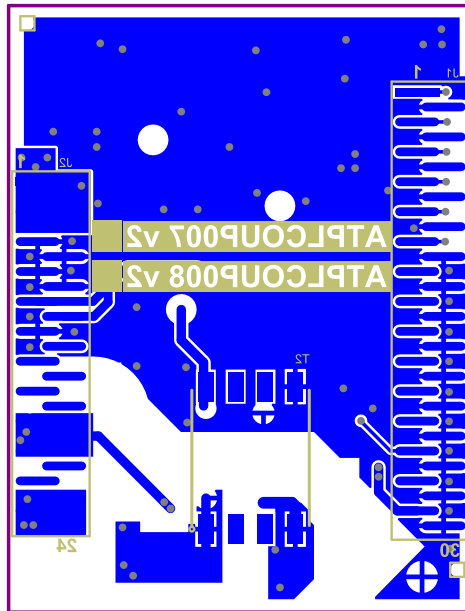


Figure 5-9. PLCOUP006v2 Top Components Placement

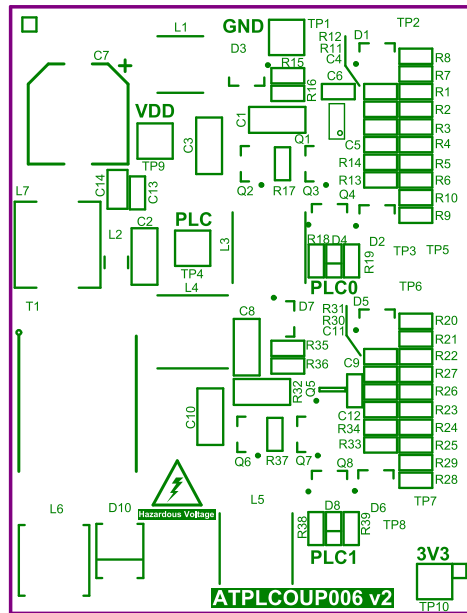
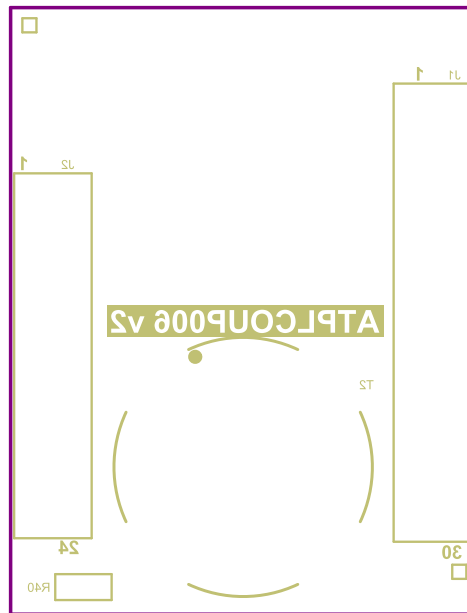


Figure 5-10. PLCOUP006v2 Bottom Components Placement



6. Compliance for Specific Standards

The development/evaluation tool is designed to be used for research and development in a laboratory environment. This development/evaluation tool is not intended to be a finished appliance, nor is it intended for incorporation into finished appliances that are made commercially available as single functional units to end users.

PL360MB and PLCOUP007 boards are a CE mark product which pass the EN60950-1 safety standard, EN50065-1, EN50065-2-3, EN50065-7 EMC standards. They also satisfy the Pb-Free and ROHS directive.

PL360MB and PLCOUP006 boards are a CE mark product which passes FCC part 15 sub part B for a current carrier system Class B device and KN60 compliance. They also satisfy the Pb-Free and ROHS directive.

7. References

- CENELEC, EN 50065-1. Signaling on low-voltage electrical installations in the frequency range 3 kHz to 148.5 kHz, 2002
- FCC Part 15 Subpart B, 2013
- [SAM4CM Series Datasheet, 2016](#)
- PL360 Datasheet, 2018

8. Revision History

8.1 Rev A - 02/2018

Document	Initial release.
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