# SAM4S-EK Development Board

# User Guide

11139A–ATARM–29-Nov-11

# Section 1
# Introduction

## 1.1 SAM4S Evaluation Kit

The SAM4S Evaluation Kit (SAM4S-EK) enables evaluation capabilities and code development of applications running on a SAM4S16 device.

## 1.2 User Guide

This guide focuses on the SAM4S-EK board as an evaluation platform. It is made up of 6 sections:

- Section 1 includes references, applicable documents, acronyms and abbreviations.
- Section 2 describes the kit contents, its main features and specifications.
- Section 3 provides board specifications.
- Section 4 describes the development environment.
- Section 5 provides instructions to power up the SAM4S-EK and describes how to use it.
- Section 6 describes the hardware resources, default jumper and switch settings, and connectors.
- Section 7 provides schematics.
- Section 8 describes the troubleshooting.

## 1.3 References and Applicable Documents

***Table 1-1.*** References and Applicable Documents

| Title | Comment |
|---|---|
| SAM4S Datasheet | http://www.atmel.com/dyn/resources/prod_documents/11100.pdf |

# Section 2

# Kit Contents

## 2.1 Deliverables

The Atmel® SAM4S-EK toolkit contains the following items:

- Board:
  - a SAM4S-EK board
  - a universal input AC/DC power supply with US, Europe and UK plug adapters
- Cables:
  - one USB cable
  - one serial RS232 cable
- A Welcome Letter

***Figure 2-1.*** Unpacked SAM4S-EK

Unpack and inspect the kit carefully. Contact your local Atmel distributor, should you have issues concerning the contents of the kit.

## 2.2 Electrostatic Warning

The SAM4S-EK board is shipped in a protective anti-static package. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the components or any other metallic element of the board.

# Section 3

# Power Up

## 3.1 Power up the Board

Unpack the board taking care to avoid electrostatic discharge. Unpack the power supply, select the right power plug adapter corresponding to that of your country, and insert it in the power supply.

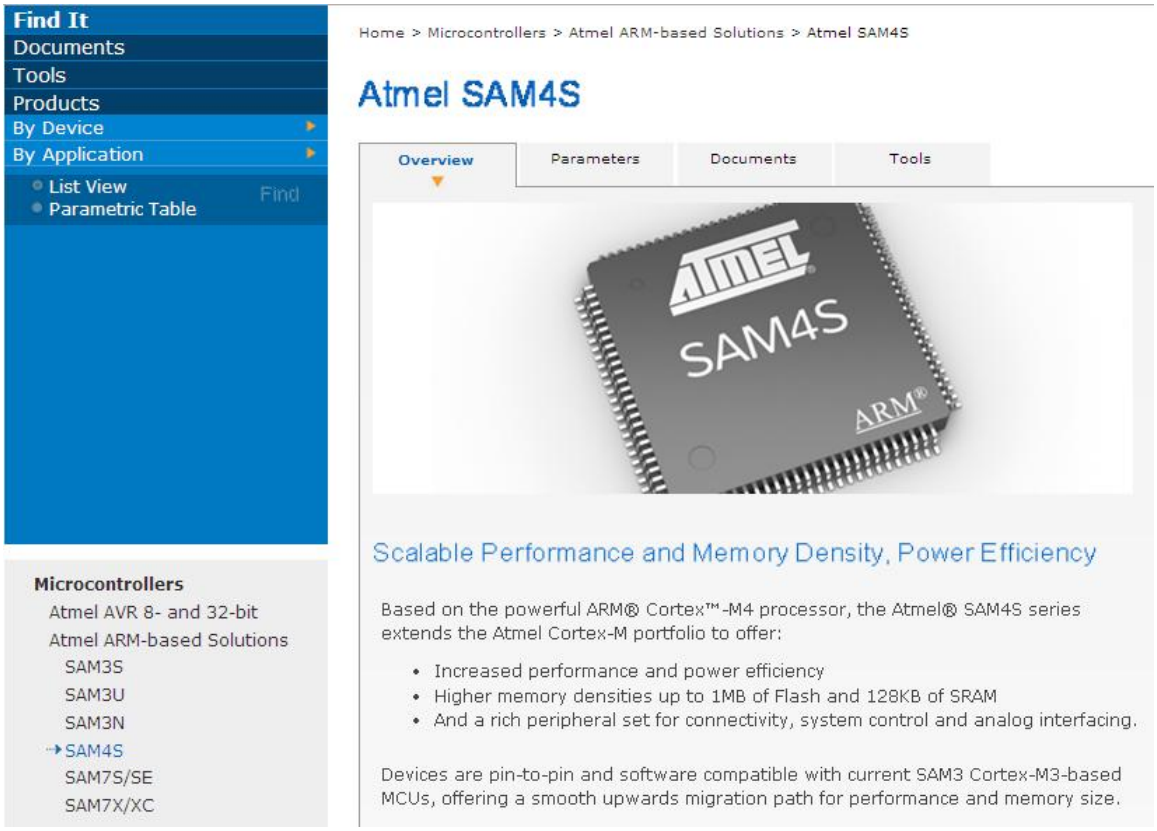
Connect the power supply DC connector to the board and plug the power supply to an AC power plug.

The board LCD should light up and display a welcome page. Then, click or touch icons displayed on the screen and enjoy the demo.

## 3.2 Sample Code and Technical Support

After boot up, you can run some sample code or your own application on the development kit. You can download sample code and get technical support from Atmel website http://www.atmel.com/dyn/products/tools.asp?category_id=163&family_id=605&subfamily_id=2404

***Figure 3-1.*** Atmel Website for AT91SAM Products



# Section 4

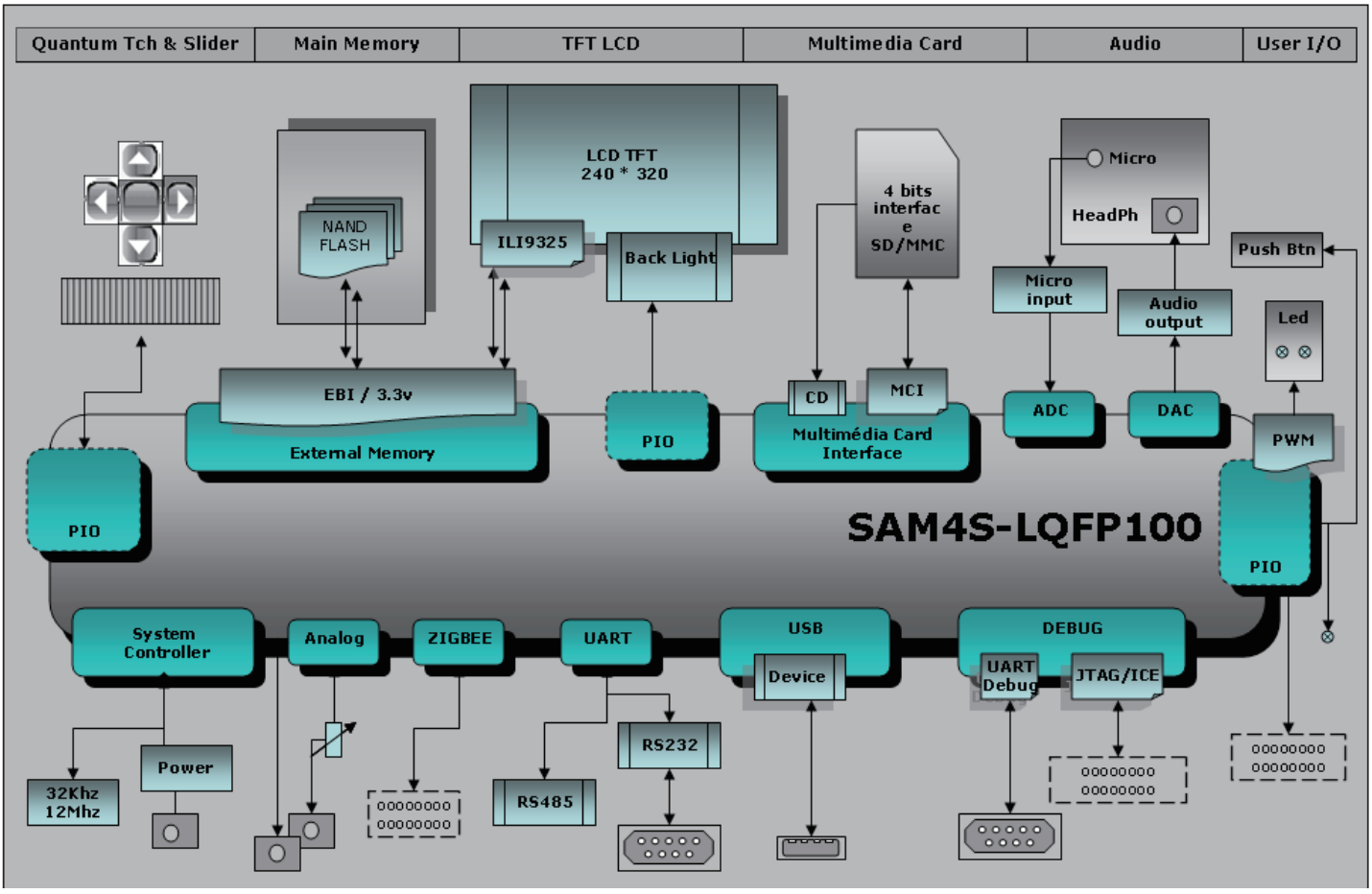
# Evaluation Kit Hardware

## 4.1 Board Overview

This section introduces the Atmel SAM4S Evaluation Kit design. It introduces system-level concepts, such as power distribution, memory, and interface assignments.

The SAM4S-EK board is based on the integration of an ARM® Cortex®-M3 processor with on-board NAND Flash and a set of popular peripherals. It is designed to provide a high performance processor evaluation solution with high flexibility for various kinds of applications.

***Figure 4-1.*** SAM4S-EK Block Diagram



## 4.2 Features List

Here is the list of the main board components and interfaces:

- SAM4S16 chip LQFP100 package with optional socket footprint
- 12 MHz crystal
- 32.768 KHz crystal
- Optional SMB connector for external system clock input
- NAND Flash
- 2.8 inch TFT color LCD display with touch panel and backlight
- UART port with level shifter circuit
- USART port with level shifter circuit multiplexed with RS485 port with level shifter circuit
- Microphone input and mono/stereo headphone jack output
- SD/MMC interface
- Reset button: NRST
- User buttons: Left and Right
- QTouch® buttons: Up, Down, Left, Right, Valid and Slider
- Full Speed USB device port
- JTAG/ICE port
- On-board power regulation
- Two user LEDs
- Power LED
- BNC connector for ADC input
- BNC connector for DAC output
- User potentiometer connected to the ADC input
- ZigBEE connector
- 2x32 bit PIO connection interfaces (PIOA, PIOC) and 1x16 bit PIO connection interface (PIOB)

## 4.3 Function Blocks

### 4.3.1 Processor

The SAM4S-EK is equipped with a SAM4S16 device in LQFP100 package.

### 4.3.2 Memory

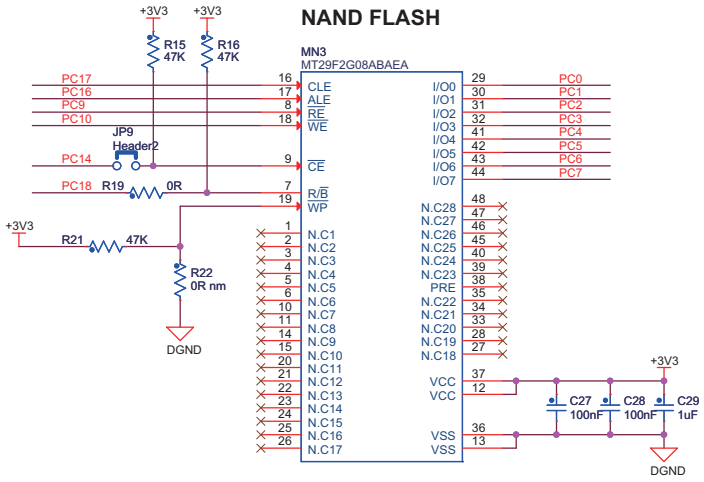
The SAM4S16 chip embeds:

- 1024 Kbytes of embedded Flash
- 128 Kbytes of embedded SRAM
- 16 Kbytes of ROM with embedded BootLoader routines (UART, USB) and In-Application Programming functions (IAP) routines.

The SAM4S features an External Bus Interface (EBI) that permits interfacing to a broad range of external memories and virtually to any parallel peripheral. The SAM4S-EK board is equipped with a memory device connected to the SAM4 EBI:

- One NAND Flash MT29F2G08ABAEA.

***Figure 4-2.*** NAND Flash




NCS0 chip select signal is used for NAND Flash chip selection. Furthermore, a dedicated jumper (JP9) can disconnect it from the on-board memories, thereby letting NCS0 free for other custom purpose.

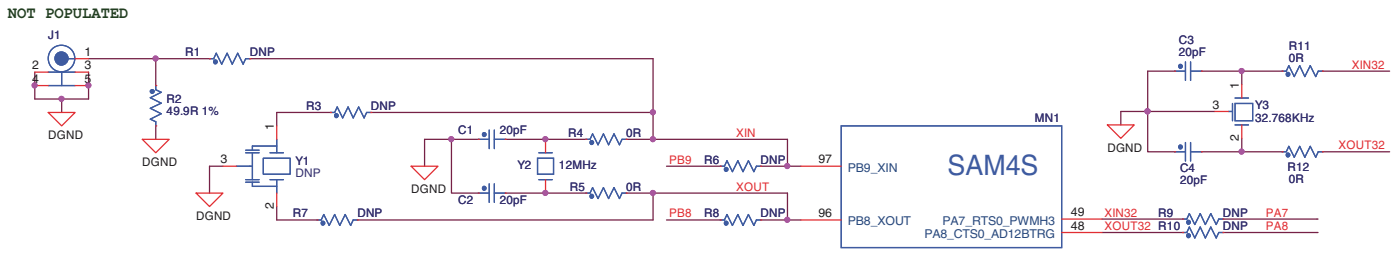
### 4.3.3 Clock Circuitry

The clock generator of a SAM4S microcontroller is made up of:

- A Low Power 32.768 Hz Slow Clock Oscillator with bypass mode.
- A 3 to 20 MHz Crystal Oscillator, which can be bypassed (12 MHz needed in case of USB).
- A factory programmed fast internal RC Oscillator. 3 output frequencies can be selected: 4 (default value), 8 or 12 MHz.
- A 60 to 130 MHz PLL (PLLB) providing a clock for the USB Full Speed Controller.
- A 60 to 130 MHz programmable PLL (PLLA), capable to provide the clock MCK to the processor and to the peripherals. The input frequency of PLLA is from 7.5 and 20 MHz.

The SAM4S-EK board is equipped with one 12 MHz crystal, optional Piezoelectric Ceramic Resonator 12 Mhz (Murata ref. CSTCE12M0G15L99-R0), one 32.768 Hz crystal and an external clock input connector (optional, not populated by default).

***Figure 4-3.*** External Clock Source



The SAM4S chip internally generates the following clocks:

- SLCK, the Slow Clock, which is the only permanent clock of the system
- MAINCK, the output of the Main Clock Oscillator selection: either a Crystal Oscillator or a 4/8/12 MHz Fast RC Oscillator
- PLLACK, the output of the Divider and 60 to 130 MHz programmable PLL (PLLA)
- PLLBCK, the output of the Divider and 60 to 130 MHz programmable PLL (PLLB)

### 4.3.4 Reset Circuitry

On-board NRST button BP1 provides an external reset control of the SAM4S.

The NRST pin is bidirectional. It is handled by the on-chip reset controller. It can be driven low to provide a reset signal out to the external components. Conversely, it can be asserted low from the outside to reset the microcontroller Core and the peripherals. The NRST pin integrates a permanent pull-up resistor of about 100 kOhm to VDDIO.

On the SAM4S-EK board, the NRST signal is connected to the LCD module and JTAG port.

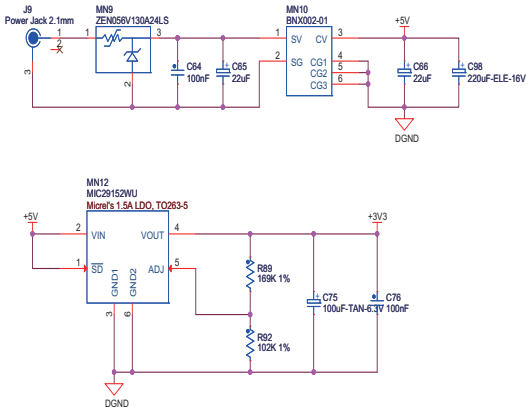
Note: At power-on, the NRST signal is asserted with a default duration of 2 clock cycles. That duration may not be sufficient to correctly reset any other system or board devices connected to that signal. First, in your custom application, you need to check for these devices' datasheets about reset duration requirements. Then, you need to set an appropriate configuration in the NRST Manager. This is done through the ERSTL field in the RSTC_MR register. The NRST duration is thereby configurable between 60 µs and 2 s, whether it is subsequently activated by a software reset or a user reset. Refer to the SAM4S datasheet for in depth information.

### 4.3.5 Power Supply and Management

The SAM4S-EK board is supplied with an external 5V DC block through input J9. It is protected by a PolyZen diode MN9 and an LC combinatory filter MN10. The PolyZen is used in the event of an incorrect power supply connection.

The adjustable LDO regulator MN12 is used for the 3.3V rail main supply. It powers all the 3.3V components on the board.

***Figure 4-4.*** Power Block




The SAM4S product series has different types of power supply pins:

- VDDIN pin:
  Power for the internal voltage regulator, ADC, DAC, and analog comparator power supplies.
  The voltage ranges from 1.8V to 3.6V.

- VDDIO pins:
  Power for the Peripherals I/O lines.
  The voltage ranges from 1.62V to 3.6V.
- VDDOUT pin:
  Output of the internal voltage regulator.
- VDDCORE pins:
  Power for the core, including the processor, embedded memories and peripherals.
  The voltage ranges from 1.62V to 1.95V.
- VDDPLL pin:
  Power for the PLL A, PLL B and 12 MHz oscillator.
  The voltage ranges from 1.62V to 1.95V.

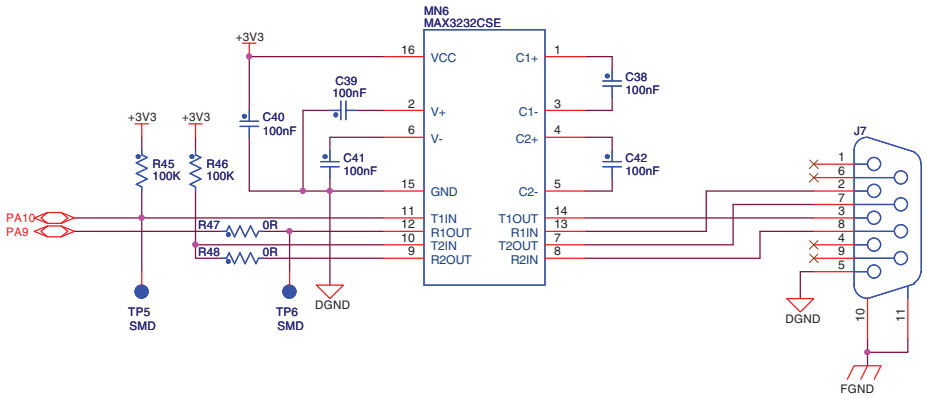
  ***Note:*** VDDPLL should be decoupled and filtered from VDDCORE.

### 4.3.6 UART

The Universal Asynchronous Receiver Transmitter features a two-pin UART that can be used for communication and trace purposes. It offers an ideal channel for in-situ programming solutions. This UART is associated with two PDC channels to reduce the processor time on packet handling.

This two-pin UART (TXD and RXD only) is buffered through an RS232 Transceiver MN6 and brought to the DB9 male connector J7.

***Figure 4-5.*** UART




### 4.3.7 USART

The Universal Synchronous/Asynchronous Receiver Transmitter (USART) provides one full duplex universal synchronous/asynchronous serial link. The data frame format is extensively configurable (data length, parity, number of stop bits) to support a broad range of serial communication standards. The USART is also associated with PDC channels for TX/RX data access.

***Note:*** For design optimization purposes, both transmitters have been implemented on the same PIO lines, that is PA21, 22, 23, 24 25.

To avoid any electrical conflict, the RS485 transceiver is isolated from the receiving line PA21.

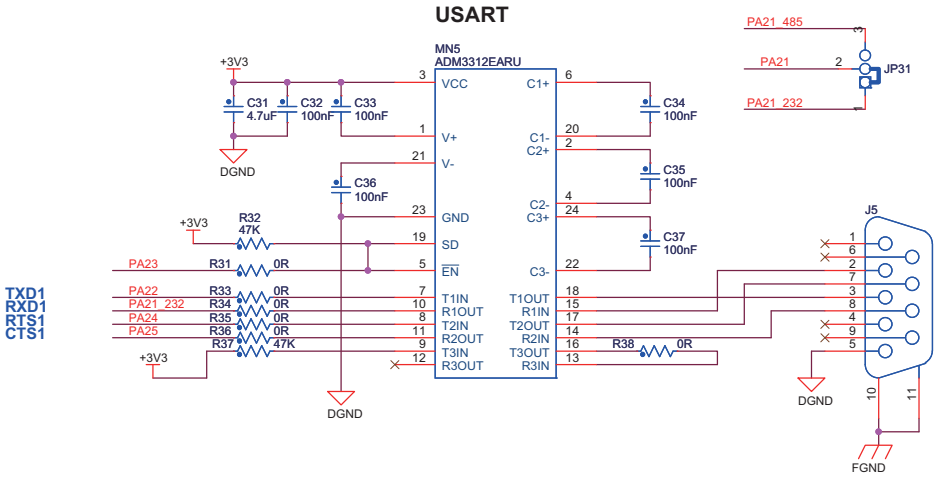
Should you need to implement an RS485 channel in place of the RS232, follow the procedure below:

1. make sure your software will permanently set PA23 to a high level - this will permanently disable the RS232 receiver.
2. solder a shunt resistor in place of R25 (a solder drop will do).

### 4.3.8 RS232

SAM4S-EK connects the USART1 bus (including TXD, RXD, RTS, CTS handshake signal controls and EN command) to the DB9 male connector J5 through the RS232 Transceiver MN5.

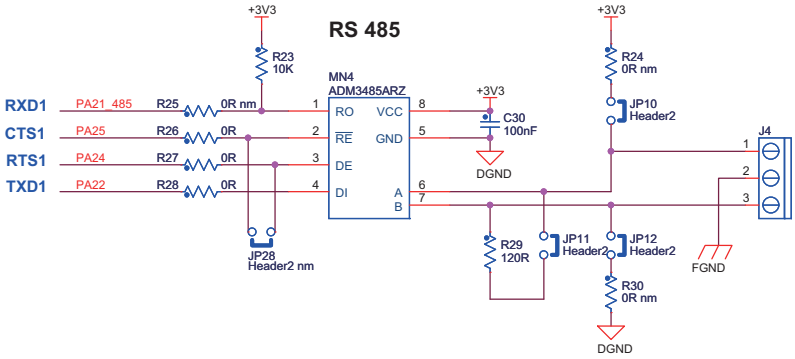
***Figure 4-6.*** USART




### 4.3.9 RS485

As noticed above, the USART1 is shared with the RS485 port, connected to the transceiver MN4, connected to the 3-point connector J4. The design includes selectable jumpers for RS485 bus termination resistors selection (JP10, JP11, JP12).

***Figure 4-7.*** RS485




### 4.3.10 Display Interface

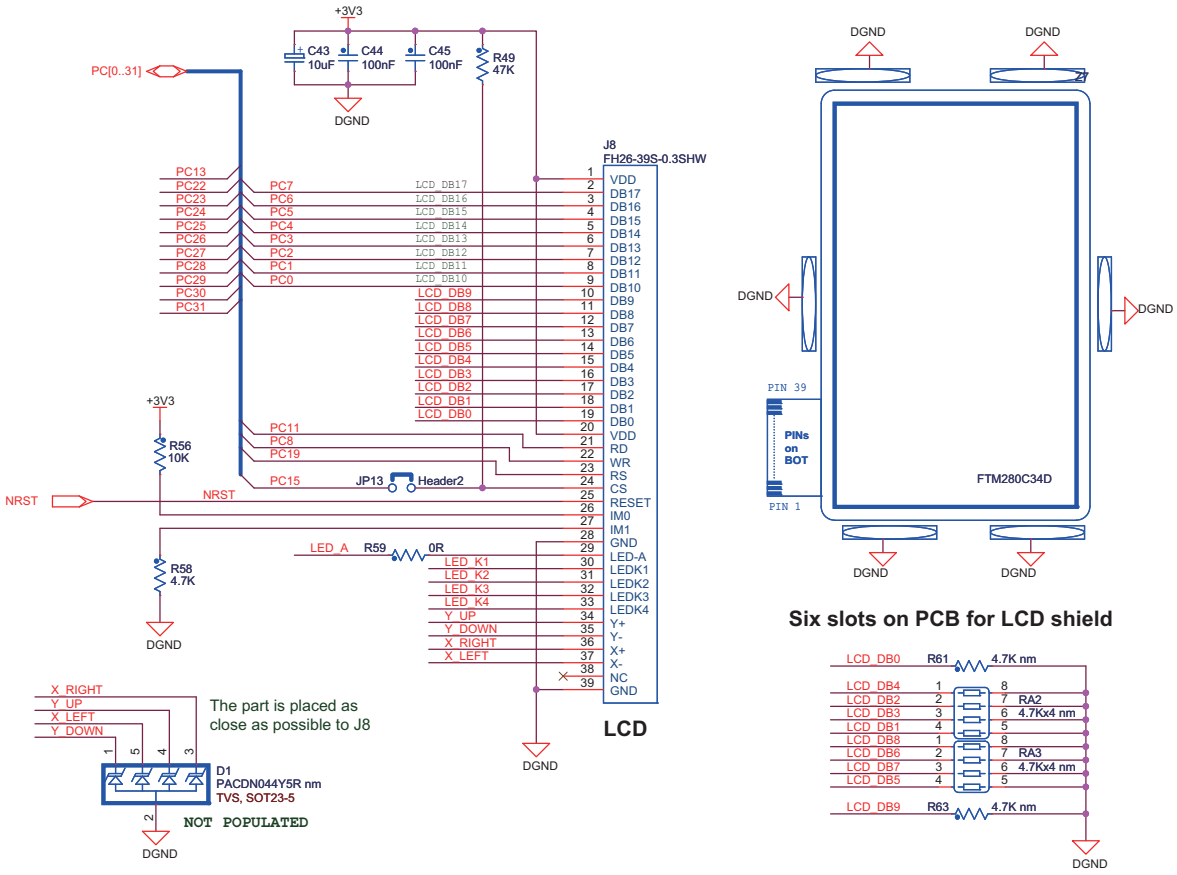
The SAM4S-EK carries a TFT Transmissive LCD module with touch panel, FTM280C34D. Its integrated driver IC is ILI9325. The LCD display area is 2.8 inches diagonally measured, with a native resolution of 240 x 320 dots.

### 4.3.11 LCD Module

The LCD module gets reset from the NRST signal. As explained, this NRST is shared with the JTAG port and the push-button BP1. The LCD chip select signal is connected to NCS1; the jumper JP13 can disconnect it so that this PIO line is available for other custom usage.

The SAM4S communicates with the LCD through PIOC where an 8-bit parallel “8080-like” protocol data bus has to be implemented by software.

***Figure 4-8.*** LCD Block

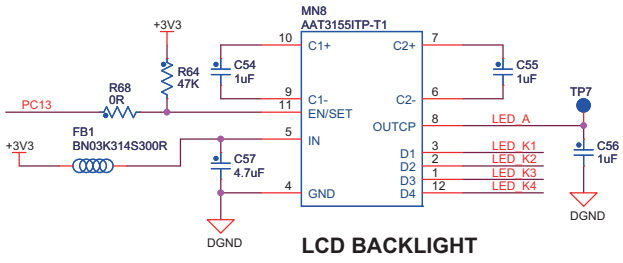



## 4.3.12 Backlight Control

The LCD backlight is made of four integrated white chip-LEDs arranged in parallel. These are driven by an AAT3155 charge pump, MN8.The AAT3155 is controlled by the SAM4S through a single PIO line PC13 interface; the 0 Ohm resistor R68 is mounted in series on this line, which permits to use it for other custom purposes. In that case, the pull-up resistor R64 maintains the charge pump permanently enabled by default.

On the anode drive line, a 0 Ohm resistor R59 is implemented in series for an optional current limitation.

***Figure 4-9.*** Backlight Control



### 4.3.13 Touch Screen Interface

The LCD module integrates a 4-wire touch panel controlled by MN7 (ADS7843) which is a slave device on the SAM4S SPI bus. The controller sends back the information about the X and Y positions, as well as a measurement for the pressure applied to the touch panel. The touch panel can be used with either a stylus or a finger.

The ADS7843 touch panel controller connects to the SPI0 interface via the NPCS0 control signal. Two interrupt signals are connected and provide events information back to the microcontroller: PenIrq and Busy.

***Note:*** PenIrq (PA16) is shared with ZigBEE signal IRQ0.
Busy (PA17) is shared with ZigBEE signal IRQ1.
Therefore, if using a ZigBEE interface in concurrence with the TouchScreen controller, take care not to have both drivers enabled at the same time on either PA16 or PA17.

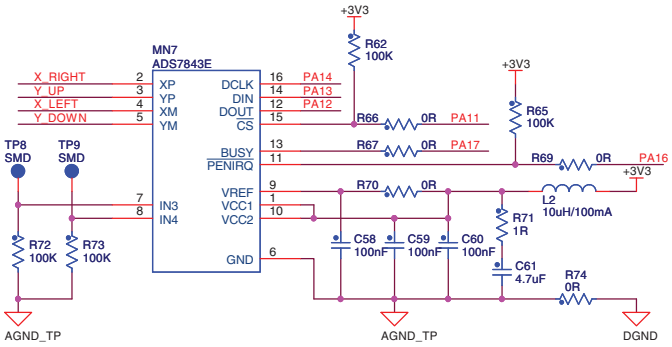
For that purpose, 0 Ohm resistors have been implemented on these PIO lines in order to disconnect either end driver from the other:

- On the touch panel controller side, R67 and R69.
- On ZigBEE side, R117 and R120.

for further information, refer to the "Schematics" section.

Touch ADC auxiliary inputs IN3/IN4 of the ADS7843 are connected to test point (TP8, TP9) for optional function extension.

***Figure 4-10.*** Touch Panel Control



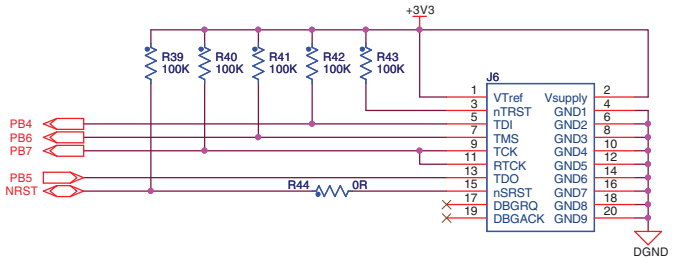

### 4.3.14 JTAG/ICE

A standard 20-pin JTAG/ICE connector is implemented on the SAM4S-EK for the connection of a compatible ARM JTAG emulator interface, such as the SAM-ICE from Segger.

***Notes:*** ***1.*** The NRST signal is connected to BP1 system button and is also used to reset the LCD module. The 0 ohm resistor R44 may be removed in order to isolate the JTAG port from this system reset signal.

***2.*** The TDO pin is in input mode with the pull-up resistor disabled when the Cortex M3 is not in debug mode. To avoid current consumption on VDDIO and/or VDDCORE due to floating input, the internal pull-up resistor corresponding to this PIO line must be enabled.

***Figure 4-11.*** JTAG Interface




### 4.3.15 Audio Interface

The SAM4S-EK board supports both audio recording and playback.

The audio volume can be adjusted using the potentiometer RV1, and the microphone amplifier gain can be adjusted via jumpers (fixed gain of 24 or 26 dB).

### 4.3.16 Microphone Input

The embedded microphone is connected to an audio pre-amplifier using the TS922 operational amplifier (MN11). The gain is set by using JP14 and JP15 jumpers; both must be set or removed at the same time.

By modifying the jumper positions, you can select each of the following gain values:

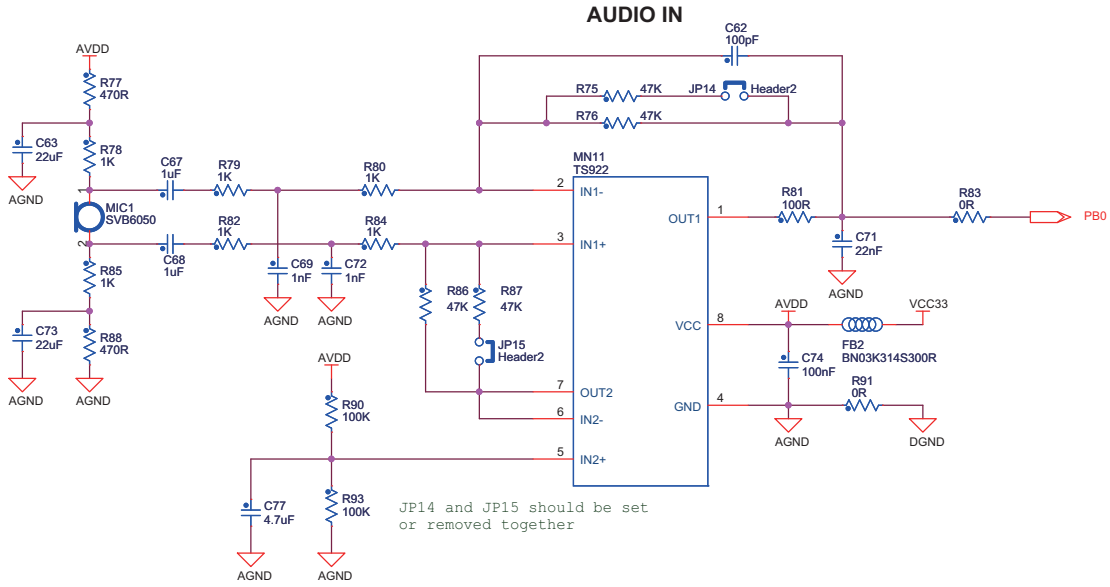
- 20 dB (default setting, both JP14 and JP15 are off)
- 26 dB (both JP14 and JP15 are on).

***Note:***

***3.*** The TB1 series 0 Ohm resistor is a reservation for future impedance adaptation facility. Under specific amplifier settings conditions, this enables the easy insertion of a capacitor or any other bipolar device on the audio path. On the other hand, R83 is a default 0 Ohm resistor that enables the disconnection of PB0 from the audio input path for custom usage.

***4.*** The audio pre-amplifier MN11 is powered by a dedicated low dropout regulator MIC5219-3.3 (MN14).

***Figure 4-12.*** Microphone Input

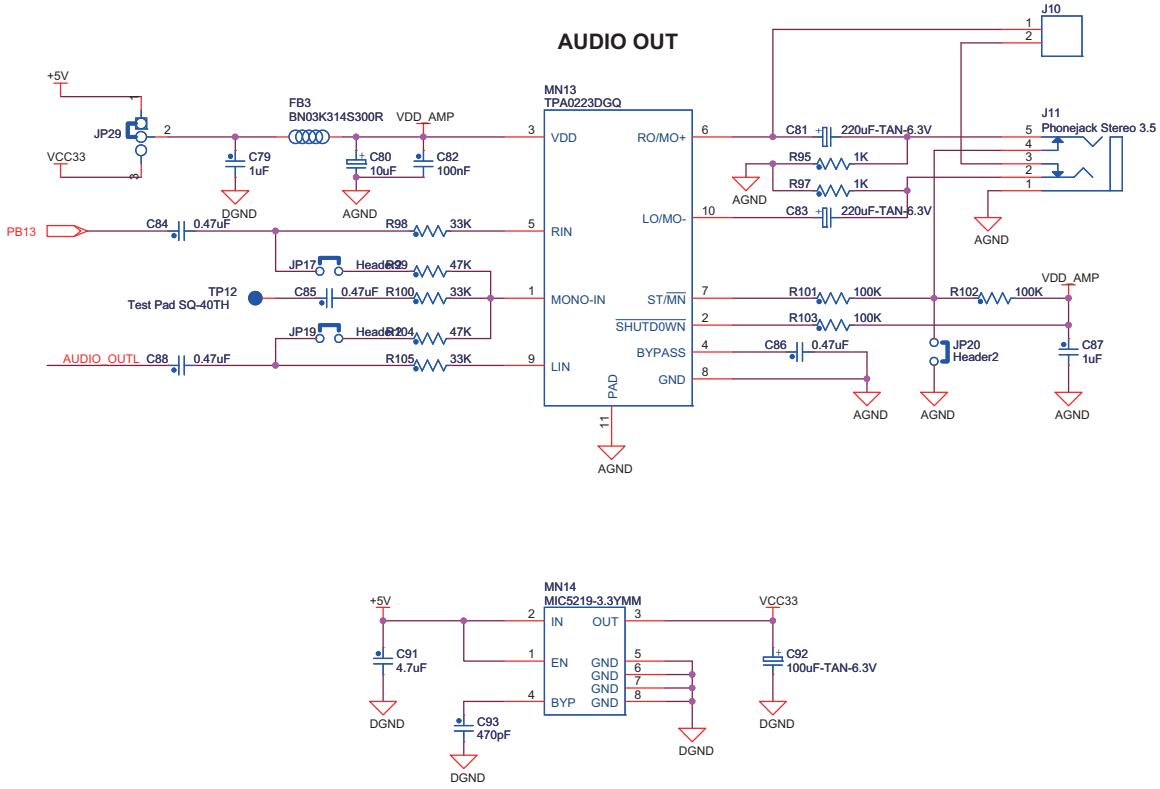



### 4.3.16.1 Headphone Output

The SAM4S-EK evaluation kit supports mono/stereo audio playback driven by a TPA0223 audio amplifier connected to two DAC channels of the microcontroller.

The TPA0223 is a 2W mono Bridge-Tied-Load (BTL) amplifier designed to drive speakers with as low as 4 Ohm impedance. The amplifier can be reconfigured on the fly to drive two stereo Single-Ended (SE) signals into head phones.

***Figure 4-13.*** Headphone Output



Using a readily available 1/8-in. (3,5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed, a 100-kOhm/1-kOhm divider pulls the ST/MN input low. When a jack plug is inserted, the 1-kOhm resistor is disconnected and the ST/MN input is pulled high. The mono speaker (J10 connector) is also physically disconnected from the RO/MO+ output so that no sound is heard from the speaker while the headphones are inserted.

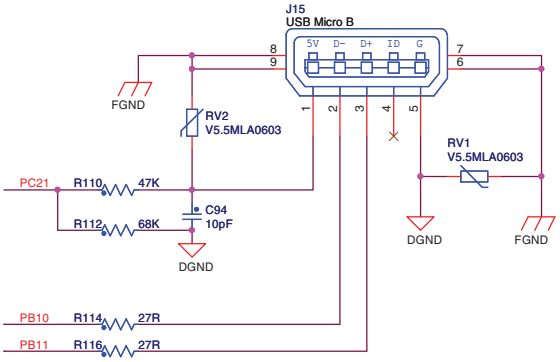
### 4.3.17 USB Device

The SAM4S UDP port is compliant with the Universal Serial Bus (USB) rev 2.0 Full Speed device specification. J15 is a micro B-type receptacle for USB device.

Both 27-Ohm resistors R114 and R116 build up a 90-Ohm differential impedance together with the (embedded) 6-Ohm output impedance of the SAM4S full speed channel drivers.

R110 and R112 build up a divider bridge from VBUS +5V to implement plug-in detection (5V level gets lowered to a PIO compatible 3.3V level) through PC21.

***Figure 4-14.*** USB



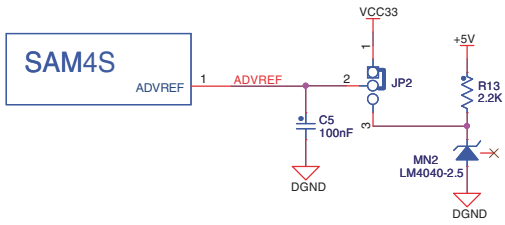

### 4.3.18 Analog Interface

#### 4.3.18.1 Analog Reference

The 3V voltage reference is based on an LM4040 (Precision Micropower Shunt Voltage Reference).

This ADVREF level can be set as 3V or 3.3V via the jumper JP2.

***Figure 4-15.*** Analog Vref



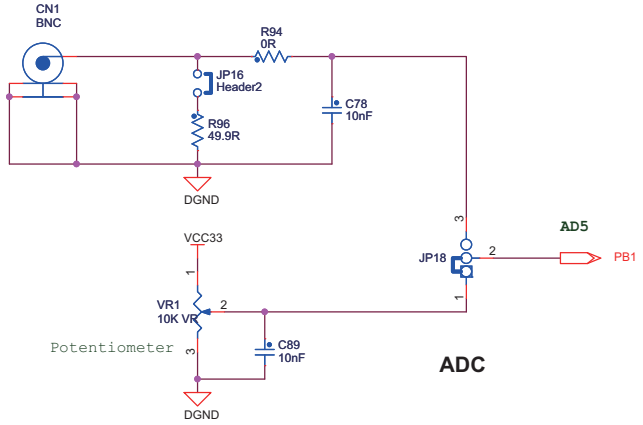
### 4.3.18.2 Analog Input

The BNC connector CN1 is connected to the ADC port PB1 as an external analog input. An on-board 50-Ohm resistor termination can be applied by closing jumper JP16. A low pass filter can be implemented for the BNC connector CN1 by replacing R94 and C78 with custom resistor and capacitor values, depending on your application requirements.

A 10-KOhm potentiometer (VR1) is also connected to this channel to implement an easy access to ADC programming and debugging (or implement an analog user control like display brightness, volume, etc.).

Either of these two functions can be selected by jumper JP18.

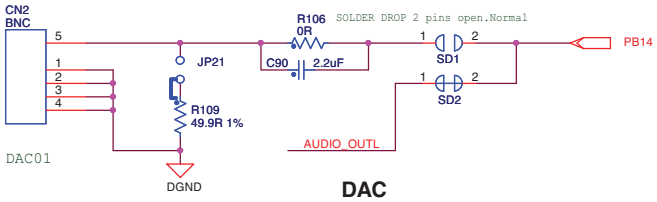
***Figure 4-16.*** ADC Input




### 4.3.18.3 Analog Output

The BNC connector CN2 is connected to the DAC port PB14 and provides an external analog output. An on-board 50-Ohm resistor termination can be enabled by closing jumper JP21. A filter can be implemented on this output channel by replacing R106 and C90 with appropriate resistor and capacitor values, depending on the application requirements.

***Figure 4-17.*** DAC Output



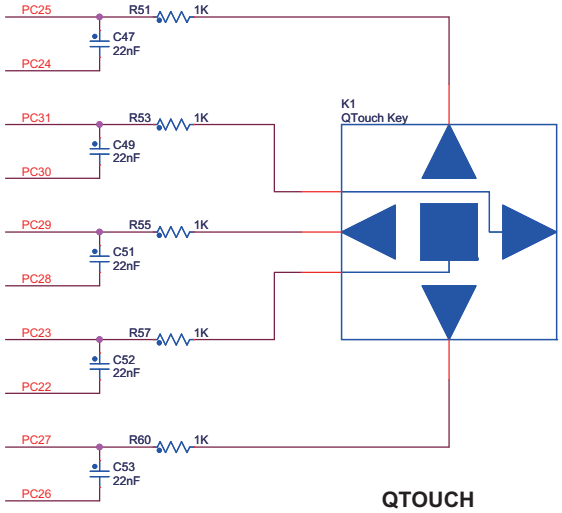

### 4.3.19 QTouch Elements

QTouch keys consist in a series of sensors formed by the association of a copper area and the capacitive effect of human fingers approaching it.

### 4.3.19.1 Keys

The SAM4S-EK implements five individual capacitive touch keys (UP, DOWN, RIGHT, LEFT and VALID) using five pairs of PIO.

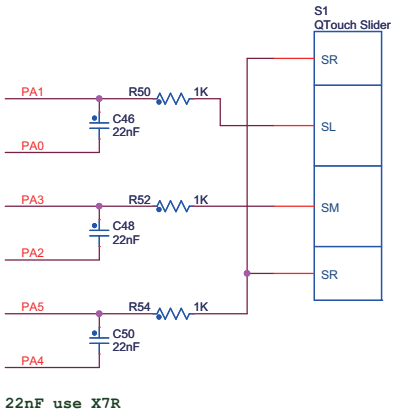
***Figure 4-18.*** QST Keys




### 4.3.19.2 Slider

A group of channels forms a Slider. A Slider is composed of three channels for a QTouch acquisition method using three pairs of PIO. Such a sensor is used to detect a linear finger displacement on a sensitive area. A typical implementation is volume control.

***Figure 4-19.*** QT_Slider

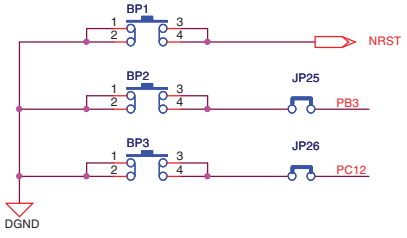



### 4.3.20 User Buttons

There are two mechanical user buttons on the SAM4S-EK, which are connected to PIO lines and defined to be "left" and "right" buttons by default.

In addition, a mechanical button controls the system reset, signal NRST.

***Figure 4-20.*** System Buttons

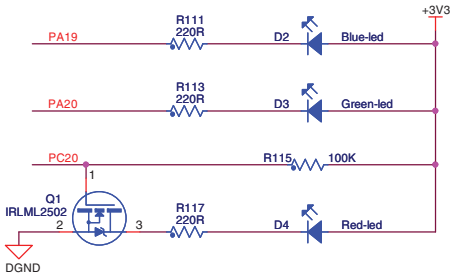


### 4.3.21 LEDs

There are three LEDs on the SAM4S-EK board:

- A blue LED (D2) and a green LED (D3), which are user defined and controlled by the GPIO.
- A red LED (D4), which is a power LED indicating that the 3.3V power rail is active. It is also controlled by the GPIO and can be treated as a user LED as well. The only difference with the two others is that it is controlled through a MOS transistor. By default, the PIO line is disabled; a pull-up resistor controls the MOS to light the LED when the power is ON).

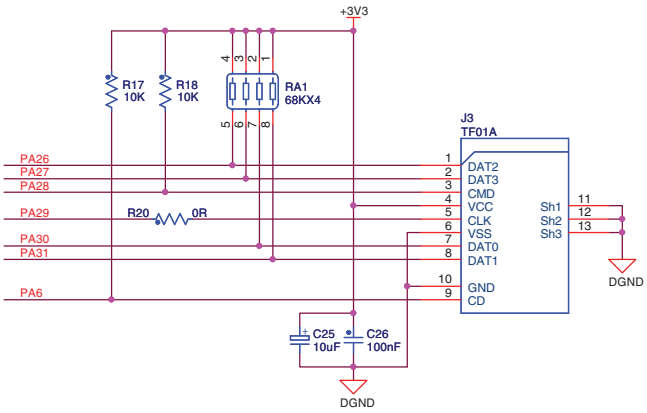
***Figure 4-21.*** LEDs




### 4.3.22 SD/MMC Card

The SAM4S EK has a high-speed 4-bit multimedia MMC interface, which is connected to a 4-bit SD/MMC micro card slot featuring a card detection switch.

***Figure 4-22.*** SD Card

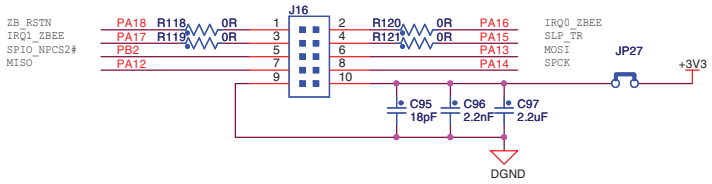



### 4.3.23 ZigBEE

SAM4S has a 10-pin male connector for the RZ600 ZigBEE module.

***Note:*** 0 Ohm resistors have been implemented in series with the PIO lines that are used elsewhere in the design, thereby enabling their individual disconnection, should a conflict occur in your application.

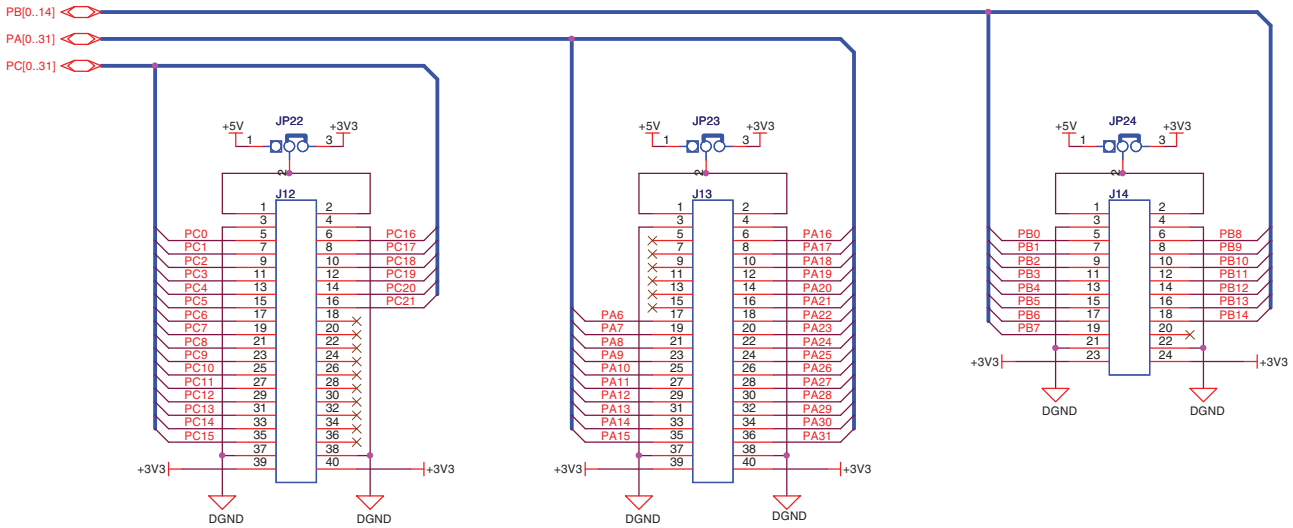
***Figure 4-23.*** ZigBEE Interface




### 4.3.24 PIO Expansion

The SAM4S product features three PIO controllers, PIOA, PIOB and PIOC, which are multiplexed with the I/O lines of the embedded peripherals. Each PIO Controller controls up to 32 lines (16 for PIOB). Expansion ports J12, J13 and J14 provide PIO lines access for customer defined usage.

***Figure 4-24.*** PIO Expansion




***Note:*** All PIO lines are available on these expansion connectors, except those that are used for the QTouch elements.

## 4.4 Configuration

This section describes the PIO usage, the jumpers, the test points and the solder drops of a SAM4S-EK board.

### 4.4.1 PIO Usage

***Table 4-1.*** **PIO Port A Pin Assignments and Signal Descriptions**

| No | I/O Line | Peripheral A | Peripheral B | Peripheral C | Extra Function | System Function | Comment | |
|---|---|---|---|---|---|---|---|---|
| 1 | PA0 | PWMH0 | TIOA0 | A17 | WKUP0 | | QTouch slider (left) SNS | |
| 2 | PA1 | PWMH1 | TIOB0 | A18 | WKUP1 | | QTouch slider (left) SNSK | |
| 3 | PA2 | PWMH2 | SCK0 | DATRG | WKUP2 | | QTouch slider (middle) SNS | |
| 4 | PA3 | TWD0 | NPCS3 | | | | QTouch slider (middle) SNSK | |
| 5 | PA4 | TWCK0 | TCLK0 | | WKUP3 | | QTouch slider (right) SNS | |
| 6 | PA5 | RXD0 | NPCS3 | | WKUP4 | | QTouch slider (right) SNSK | |
| 7 | PA6 | TXD0 | PCK0 | | | | MCI card detection | |
| 8 | PA7 | RTS0 | PWMH3 | | | XIN32 | CLK32KHz | |
| 9 | PA8 | CTS0 | AD12BTRG | | WKUP5 | XOUT32 | CLK32KHz | |
| 10 | PA9 | URXD0 | NPCS1 | PWMFI0 | WKUP6 | | UART receive data | |
| 11 | PA10 | UTXD0 | NPCS2 | | | | UART transmit data | |
| 12 | PA11 | NPCS0 | PWMH0 | | WKUP7 | | NPCS0# (TSC) | |
| 13 | PA12 | MISO | PWMH1 | | | | MISO_TSC | ZigBEE MISO |
| 14 | PA13 | MOSI | PWMH2 | | | | MOSI_TSC | ZigBEE MOSI |
| 15 | PA14 | SPCK | PWMH3 | | WKUP8 | | SPCK_TSC | ZigBEE CLK |
| 16 | PA15 | TF | TIOA1 | PWML3 | WKUP14 / PIO_DCEN1 | | ZigBEE SLPTR | |
| 17 | PA16 | TK | TIOB1 | PWML2 | WKUP15 / PIO_DCEN2 | | IRQ_TSC | ZigBEE IRQ0 |
| 18 | PA17 | TD | PCK1 | PWMH3 | AD0 | | BUSY_TSC | ZigBEE IRQ1 |
| 19 | PA18 | RD | PCK2 | A14 | AD1 | | ZigBEE RSTN | |
| 20 | PA19 | RK | PWML0 | A15 | AD2/ WKUP9 | | Blue LED (UserLED1) | |
| 21 | PA20 | RF | PWML1 | A16 | AD3/ WKUP10 | | Green LED (UserLED2) | |
| 22 | PA21 | RXD1 | PCK1 | | AD8 | | USART RXD | |
| 23 | PA22 | TXD1 | NPCS3 | NCS2 | AD9 | | USART TXD | |
| 24 | PA23 | SCK1 | PWMH0 | A19 | POI_DCCLK | | USART transceiver enable | |
| 25 | PA24 | RTS1 | PWMH1 | A20 | POI_DC0 | | USART RTS | |
| 26 | PA25 | CTS1 | PWMH2 | A23 | POI_DC1 | | USART CTS | |
| 27 | PA26 | DCD1 | TIOA2 | MCDA2 | POI_DC2 | | MCI data bit 2 | |
| 28 | PA27 | DTR1 | TIOB2 | MCDA3 | POI_DC3 | | MCI data bit 3 | |
| 29 | PA28 | DSR1 | TCLK1 | MCCDA | POI_DC4 | | MCI command | |

***Table 4-1.*** **PIO Port A Pin Assignments and Signal Descriptions** (Continued)

| No | I/O Line | Peripheral A | Peripheral B | Peripheral C | Extra Function | System Function | Comment |
|---|---|---|---|---|---|---|---|
| 30 | PA29 | RI1 | TCLK2 | MCCK | POI_DC5 | | MCI clock |
| 31 | PA30 | PWML2 | NPCS2 | MCDA0 | WKUP11 / POI_DC6 | | MCI data bit 0 |
| 32 | PA31 | NPCS1 | PCK2 | MCDA1 | POI_DC7 | | MCI data bit 1 |

***Table 4-2.*** **PIO Port B Pin Assignments and Signal Descriptions**

| No | I/O Line | Peripheral A | Peripheral B | Peripheral C | Extra Function | System Function | Comment |
|---|---|---|---|---|---|---|---|
| 1 | PB0 | PWMH0 | | | AD4 | | Microphone input |
| 2 | PB1 | PWMH1 | | | AD5 | | Analog input |
| 3 | PB2 | URXD1 | NPCS2 | | AD6 / WKUP12 | | ZigBee chip select |
| 4 | PB3 | UTXD1 | PCK2 | | AD7 | | User push-button 1 |
| 5 | PB4 | TWD1 | PWMH2 | | | TDI | JTAG data in |
| 6 | PB5 | TWCK1 | PWML0 | | WKUP13 | TDO/ TRACESWO | JTAG data out |
| 7 | PB6 | | | | | TMS/SWDIO | JTAG test mode select |
| 8 | PB7 | | | | | TCK/SWCLK | JTAG clock |
| 9 | PB8 | | | | | XOUT | CLK12MHz |
| 10 | PB9 | | | | | XIN | CLK12MHz |
| 11 | PB10 | | | | | DDM | USB DM |
| 12 | PB11 | | | | | DDP | USB DP |
| 13 | PB12 | PWML1 | | | | ERASE | Flash erase selector |
| 14 | PB13 | PWML2 | PCK0 | | DAC0 | | Audio Output R |
| 15 | PB14 | NPCS1 | PWMH3 | | DAC1 | | Audio Output L |

***Table 4-3.*** **PIO Port C Pin Assignments and Signal Descriptions**

| No | I/O Line | Peripheral A | Peripheral B | Peripheral C | Extra Function | System Function | Comments |
|---|---|---|---|---|---|---|---|
| 1 | PC0 | D0 | PWML0 | | | | EBI D0 |
| 2 | PC1 | D1 | PWML1 | | | | EBI D1 |
| 3 | PC2 | D2 | PWML2 | | | | EBI D2 |
| 4 | PC3 | D3 | PWML3 | | | | EBI D3 |
| 5 | PC4 | D4 | NPCS1 | | | | EBI D4 |
| 6 | PC5 | D5 | | | | | EBI D5 |
| 7 | PC6 | D6 | | | | | EBI D6 |
| 8 | PC7 | D7 | | | | | EBI D7 |
| 9 | PC8 | NWR0/NWE | | | | | TFT LCD write enable |
| 10 | PC9 | NANDOE | | | | | NAND Flash output enable |
| 11 | PC10 | NANDWE | | | | | NAND Flash write enable |
| 12 | PC11 | NRD | | | | | TFT LCD read enable |
| 13 | PC12 | NCS3 | | | AD12 | | User push-button 2 |
| 14 | PC13 | NWAIT | PWML0 | | AD10 | | LCD backlight control |
| 15 | PC14 | NCS0 | | | | | NAND Flash chip select |
| 16 | PC15 | NCS1 | PWML1 | | AD11 | | TFT LCD chip select |
| 17 | PC16 | A21/NANDALE | | | | | NAND Flash ALE |
| 18 | PC17 | A22/NANDCLE | | | | | NAND Flash CLE |
| 19 | PC18 | A0/NBS0 | PWMH0 | | | RDYBSY | NAND Flash RDY/BSY |
| 20 | PC19 | A1 | PWMH1 | | | | TFT LCD RegSel |
| 21 | PC20 | A2 | PWMH2 | | | | Red LED (Power) |
| 22 | PC21 | A3 | PWMH3 | | | | USB Vbus detection |
| 23 | PC22 | A4 | PWML3 | | | | QTouch valid button SNS |
| 24 | PC23 | A5 | TIOA3 | | | | QTouch valid button SNSK |
| 25 | PC24 | A6 | TIOB3 | | | | QTouch up button SNS |
| 26 | PC25 | A7 | TCLK3 | | | | QTouch up button SNSK |
| 27 | PC26 | A8 | TIOA4 | | | | QTouch down button SNS |
| 28 | PC27 | A9 | TIOB4 | | | | QTouch down button SNSK |
| 29 | PC28 | A10 | TCLK4 | | AD13 | | QTouch left button SNS |
| 30 | PC29 | A11 | TIOA5 | | AD14 | | QTouch left button SNSK |
| 31 | PC30 | A12 | TIOB5 | | | | QTouch right button SNS |
| 32 | PC31 | A13 | TCLK5 | | | | QTouch right button SNSK |

### 4.4.2 Jumpers

The SAM4S-EK board jumpers are essentially used for two main purposes: functional selection or current measurement. Details are given below.

***Table 4-4.*** **Jumpers Setting**

| Designation | Label | Default Setting | Feature |
|---|---|---|---|
| JP1 | JTAG | OPEN | Close to select the JTAG boundary scan of the SAM4S |
| JP2 | ADVREF | 1-2 | Analog reference voltage selection between 3.3V (close 1-2) and 2.5V (close 2-3) |
| JP3 | ERASE | OPEN | Close to reinitialize the Flash contents and some of its NVM bits. |
| JP4 | TEST | Not populated (OPEN) | Close for manufacturing test or fast programming mode |
| JP5 | VDDPLL | CLOSE | Access for current measurement on VDDPLL |
| JP6 | VDDIO | CLOSE | Access for current measurement on VDDIO |
| JP7 | VDDIN | CLOSE | Access for current measurement on VDDIN |
| JP8 | VDDCORE | CLOSE | Access for current measurement on VDDCORE |
| JP9 | CE FLASH | CLOSE | NCS0 enable NAND Flash chip select |
| JP10 | RS485 | OPEN | Maintain differential impedance for RS485 interface |
| JP11 | RS485 | CLOSE | Maintain impedance matching for RS485 interface |
| JP12 | RS485 | OPEN | Maintain differential impedance for RS485 interface |
| JP13 | CS | CLOSE | NCS1 chip select LCD |
| JP14 - JP15 | MIC GAIN0 | CLOSE (both) 20db<br>OPEN (both) 26db | Close both to lower gain stage on microphone input. |
| JP16 | ADC input | OPEN | Close for impedance matching on ADC BNC port |
| JP17 – JP19 | MIC Gain stage | | Close to mux RIN/LIN into MONO-IN path within audio PA |
| JP18 | SELECT ADC INP | 1-2<br>2-3 | ADC input potentiometer<br>ADC input BNC |
| JP20 | MONO/STEREO | CLOSE | Close to fix in mono speaker, no matter the stereo plug state |
| JP21 | DAC output | OPEN | Close for impedance matching on DAC BNC port |
| JP22 | PIO expansion J12 voltage supply | 2-3 | Set to 3.3V (position 1-2 sets to 5V) |
| JP23 | PIO expansion J13 voltage supply | 2-3 | Set to 3.3V (position 1-2 sets to 5V) |
| JP24 | PIO expansion J14 voltage supply | 2-3 | Set to 3.3V (position 1-2 sets to 5V) |
| JP25 | BP2 | CLOSE | Open to disconnect and free PB3 for custom usage |
| JP26 | BP3 | CLOSE | Open to disconnect and free PC12 for custom usage |
| JP27 | ZIGBEE | CLOSE | Power supply connection/disconnection for the ZigBEE module<br>May also be used as a current measurement point |

***Table 4-5.*** Audio Input Configuration

| JP17 | JP19 | MONO-STEREO INPUT |
|---|---|---|
| OFF | OFF | PIN test point (TP12) |
| OFF | ON | Left-in only |
| ON | OFF | Right-in only |
| ON | ON | Sum of Left-in and Right-in |

### 4.4.3 Test Points

Some test points have been placed on the SAM4S-EK board for the verification of important signals.

***Table 4-6.*** Test Points

| Designation | Part | Description |
|---|---|---|
| TP1 | Ring Hook | GND |
| TP2 | Ring Hook | GND |
| TP3 | Ring Hook | GND |
| TP4 | Ring Hook | GND |
| TP5 | Pad | UART TXD |
| TP6 | Pad | UART RXD |
| TP7 | Pad | LCD Backlight driver anode |
| TP8 | Pad | Aux ADC input for Touch Screen controller |
| TP9 | Pad | Aux ADC input for Touch Screen controller |
| TP10 | Ring Hook | +5V |
| TP11 | Ring Hook | +3V3 |
| TP12 | Pad | Optional Audio PA input |

### 4.4.4 Solder Drops

There are two solder drops designed on the SAM4S-EK for isolation.

***Table 4-7.*** Solder Drops

| Designation | Default Setting | Feature |
|---|---|---|
| SD1 | OPEN | Isolation of DAC output from shared channel (PB14) |
| SD2 | CLOSE | Connects PB14 to the AUDIO_OUTL channel |

### 4.4.5 Assigned PIO Lines, Disconnection Possibility

As pointed out in some previous interface description, 0 Ohm resistors have been inserted on the path of the receiver PIO lines of the SAM4S-EK. These are the PIO lines connected to an external driver on the board. The 0 Ohm resistors allow disconnecting each of these for custom usage (through PIO expansion connectors for example). This feature gives the user an added level of versatility for prototyping a system of his own. See the table below.

*Table 4-8.* **Disconnecting Possibility**

| Designation | Default Assignment | PIO |
|---|---|---|
| R19 | 0R | PC18, RDY/BSY on NAND Flash |
| R20 | 0R | PA29 |
| R22 | DNP | Optional write protection on NAND Flash |
| R25 | 0R | PA21 |
| R26 | 0R | PA25 |
| R27 | 0R | PA24 |
| R28 | 0R | PA22 |
| R31 | 0R | PA23 |
| R33 | 0R | PA22 |
| R34 | 0R | PA21 |
| R35 | 0R | PA24 |
| R36 | 0R | PA25 |
| R44 | 0R | NRST |
| R47 | 0R | PA9 |
| R48 | 0R | R2OUT/MN5 |
| R59 | 0R | LCD backlight LED anode |
| R66 | 0R | PA11 |
| R67 | 0R | PA5 |
| R68 | 0R | PC13 |
| R69 | 0R | PA4 |
| R70 | 0R | Vref TSC |
| R118 | 0R | PA3 ZB_RSTN |
| R119 | 0R | PA5 IRQ1_ZBEE |
| R120 | 0R | PA4 IRQ0_ZBEE |
| R121 | 0R | PA6 SLP_TR |

*Table 4-9.* Default Not Populated Parts

| Reference | Function |
|---|---|
| J1, R1 | External clock resource input |
| Y1, R3, R7 | Backup 12 MHz crystal |
| R6, R8 | Isolation on 12 MHZ clock source and GPIO expansion |
| R9, R10 | Isolation on 32 KHz clock source and GPIO expansion |
| R22 | Optional write protection NAND Flash |
| R23 | Optional pull-up for open drain output or equivalent device |
| R24, R30 | Differential impedance matching for RS485 cable |

***Table 4-9.*** Default Not Populated Parts

| Reference | Function |
|---|---|
| D1 | Optional ESD protection for LCD touch panel |
| R61, R63, RA2, RA3 | Optional data bus termination for LCD controller |
| JP4 | Test mode selection for the SAM chip |
| J2 | Optional QFP socket for the SAM4 chip |
| K1 | Virtual component for QTouch keys set - implemented as copper areas |
| S1 | Virtual component for QTouch slider set - implemented as copper areas |
| TPxx | Surface-mounted test points (copper area) |

## 4.5 Connectors

### 4.5.1 Power Supply Connector J9

The SAM4S-EK evaluation board can be powered from a 5VDC power supply connected to the external power supply jack J9. The positive pole is the center pin.

***Figure 4-25.*** Power Supply Connector J9

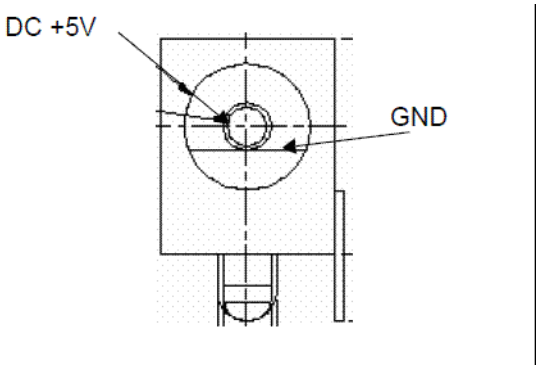



***Table 4-10.*** Power Supply Connector J9 Signal Descriptions

| Pin | Mnemonic | Signal Description |
|---|---|---|
| 1 | Center | +5vcc |
| 2 | Gnd | Ground reference |

### 4.5.2 USART Connector J5 With RTS/CTS Handshake Support

***Figure 4-26.*** Male RS232/USART Connector J5

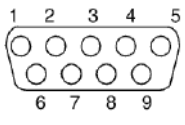


***Table 4-11.*** Serial COM1 Connector J5 Signal Descriptions

| Pin | Mnemonic | Signal Description |
|---|---|---|
| 1, 4, 6, 9 | NC | NO CONNECTION |
| 2 | TXD TRANSMITTED DATA | RS232 serial data output signal |
| 3 | RXD RECEIVED DATA | RS232 serial data input signal |
| 5 | GND | GROUND |
| 7 | RTS READY TO SEND | Active-positive RS232 input signal |
| 8 | CTS CLEAR TO SEND | Active-positive RS232 output signal |

### 4.5.3 UART Connector J7

Male RS232/UART connector J7

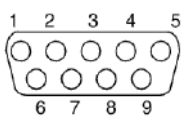



***Table 4-12.*** **Male RS232/UART Connector J7 Signal Descriptions**

| Pin | Mnemonic | Signal Description |
|---|---|---|
| 1, 4, 6, 7, 8, 9 | NC | NO CONNECTION |
| 2 | TXD TRANSMITTED DATA | RS232 serial data output signal |
| 3 | RXD RECEIVED DATA | RS232 serial data input signal |
| 5 | GND | GROUND |

### 4.5.4 USB Device Connector J15

***Figure 4-27.*** Micro-B USB Connector J15

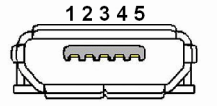



***Table 4-13.*** **Micro-B USB Connector J15 Signal Descriptions**

| Pin | Mnemonic | Signal Description |
|---|---|---|
| 1 | Vbus | 5v power |
| 2 | DM | Data - |
| 3 | DP | Data + |
| 4 | Gnd | Ground |
| 5 | Shield | Shield |

### 4.5.5 TFT LCD Connector J8

One 39-pin connector is available on the board to connect the LCD module, backlight and touch screen.

***Figure 4-28.*** LCD Connector J8

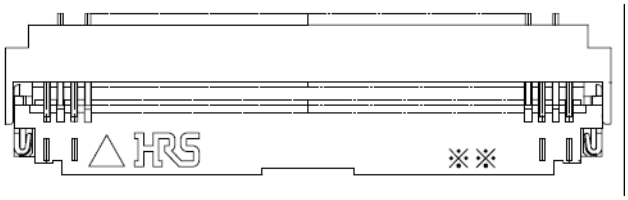



***Table 4-14.*** LCD Connector J8 Signal Descriptions

| Pin | Mnemonic | Pin | Mnemonic |
|---|---|---|---|
| 1 | 3V3 | 2 | LCD_DB17 (PC7) |
| 3 | LCD_DB16 (PC6) | 4 | LCD_DB15 (PC5) |
| 5 | LCD_DB14 (PC4) | 6 | LCD_DB13 (PC3) |
| 7 | LCD_DB12 (PC2) | 8 | LCD_DB11 (PC1) |
| 9 | LCD_DB10 (PC0) | 10 | LCD_DB09 (NC) |
| 11 | LCD_DB08 (NC) | 12 | LCD_DB07 |
| 13 | LCD_DB06 (NC) | 14 | LCD_DB05 (NC) |
| 15 | LCD_DB04 (NC) | 16 | LCD_DB03 (NC) |
| 17 | LCD_DB02 (NC) | 18 | LCD_DB01 (NC) |
| 19 | LCD_DB00 (NC) | 20 | 3V3 |
| 21 | RD (PC11) | 22 | WR (PC8) |
| 23 | RS (PC19) | 24 | CS (PC15) |
| 25 | RESET | 26 | IM0 |
| 27 | IM1 | 28 | GND |
| 29 | LED-A | 30 | LED-K1 |
| 31 | LED-K2 | 32 | LED-K3 |
| 33 | LED-K4 | 34 | Y UP |
| 35 | Y DOWN | 36 | X RIGHT |
| 37 | X LEFT | 38 | NC |
| 39 | GND | | |

### 4.5.6 JTAG Debugging Connector J6

This JTAG connector is a 20-way Insulation Displacement Connector (IDC) keyed box header (2.54 mm male) that mates with IDC sockets mounted on a ribbon cable. Its signal assignment is compatible with the SAM-ICE or any similar third-party interface.

***Figure 4-29.*** JTAG/ICE Connector J6

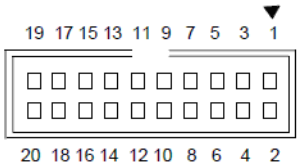



***Table 4-15.*** JTAG/ICE Connector J13 Signal Descriptions

| Pin | Mnemonic | Description |
|---|---|---|
| 1 | VTref. 3.3V power | This is the target reference voltage. It is used to check if the target has power, to create the logic-level reference for the input comparators and to control the output logic levels to the target. It is normally fed from Vdd on the target board and must not have a series resistor. |
| 2 | Vsupply. 3.3V power | This pin is not connected in SAM-ICE. It is reserved for compatibility with other equipment. Connect to Vdd or leave open in target system. |
| 3 | nTRST TARGET RESET — Active-low output signal that resets the target | JTAG Reset. Output from SAM-ICE to the Reset signal on the target JTAG port. Typically connected to nTRST on the target CPU. This pin is normally pulled HIGH on the target to avoid unintentional resets when there is no connection. |
| 4 | GND | Common ground |
| 5 | TDI TEST DATA INPUT — Serial data output line, sampled on the rising edge of the TCK signal | JTAG data input of target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TDI on target CPU. |
| 6 | GND | Common ground |
| 7 | TMS TEST MODE SELECT – | JTAG mode set input of target CPU. This pin should be pulled up on the target. Typically connected to TMS on target CPU. Output signal that sequences the target's JTAG state machine, sampled on the rising edge of the TCK signal. |
| 8 | GND | Common ground |
| 9 | TCK TEST CLOCK — Output timing signal, for synchronizing test logic and control register access | JTAG clock signal to target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TCK on target CPU. |
| 10 | GND | Common ground |
| 11 | RTCK<br>Input Return test clock signal from the target | Some targets must synchronize the JTAG inputs to internal clocks. To assist in meeting this requirement, a returned and retimed TCK can be used to dynamically control the TCK rate. SAM-ICE supports adaptive clocking which waits for TCK changes to be echoed correctly before making further changes. Connect to RTCK if available, otherwise to GND. |
| 12 | GND | Common ground |
| 13 | TDO JTAG TEST DATA OUTPUT — Serial data input from the target | JTAG data output from target CPU. Typically connected to TDO on target CPU. |
| 14 | GND | Common ground |

***Table 4-15.*** JTAG/ICE Connector J13 Signal Descriptions (Continued)

| Pin | Mnemonic | Description |
|---|---|---|
| 15 | nSRST RESET — | Active-low reset signal. Target CPU reset signal |
| 16 | GND | Common ground |
| 17 | RFU | This pin is not connected in SAM-ICE. |
| 18 | GND | Common ground |
| 19 | RFU | This pin is not connected in SAM-ICE. |
| 20 | GND | Common ground |

### 4.5.7 SD/MMC - MCI Connector J3

***Figure 4-30.*** SD/MMC Connector J3

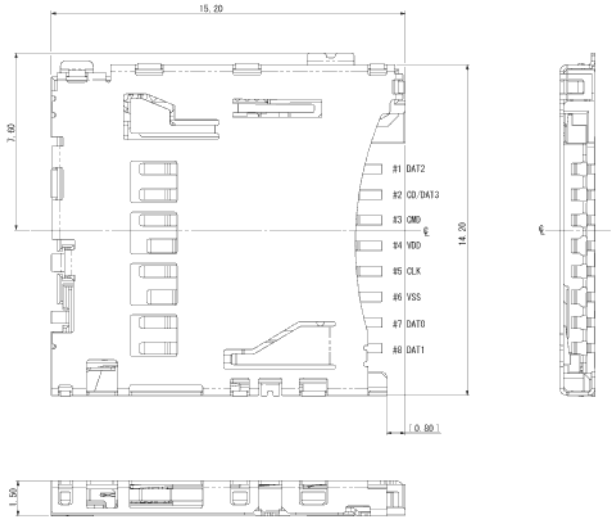



***Table 4-16.*** SD/MMC Connector J3 Signal Descriptions

| Pin | Mnemonic | Pin | Mnemonic |
|---|---|---|---|
| 1 | RSV/DAT3 | 2 | CDA |
| 3 | GND | 4 | VCC |
| 5 | CLK | 6 | GND |
| 7 | DAT0 | 8 | DAT1 |
| 9 | DAT2 | 10 | Card Detect |
| 11 | GND | 12 | |

### 4.5.8 Analog Connector CN1 & CN2

***Figure 4-31.*** Analog Input Connector CN1 and Analog Output CN2, Bottom View

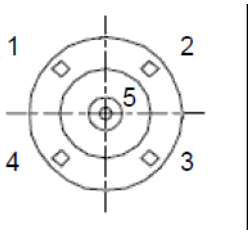



***Table 4-17.*** Analog Input, Output Connector CN1, CN2 Signal Descriptions

| Pin | Mnemonic |
|---|---|
| 1, 2, 3, 4 | GND |
| 5 | Analog input PB1 for CN1 and analog output PB13 for CN2 respectively |

### 4.5.9 RS485 Connector J14

***Figure 4-32.*** RS485 Connector J14

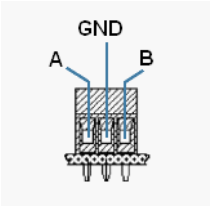



***Table 4-18.*** RS485 J14 Signal Descriptions

| Pin | Mnemonic |
|---|---|
| 1 | A - non-inverted RS485 signal A |
| 2 | Frame ground |
| 3 | B - non-inverted RS485 signal B |

### 4.5.10 Headphone Connector J11

***Figure 4-33.*** Headphone J11

***Table 4-19.*** Headphone J11 Signal Descriptions

| Pin | Mnemonic |
|---|---|
| 1 | AGND |
| 2 | Out left |
| 3 | |
| 4 | |
| 5 | Out Right |

### 4.5.11 ZigBEE Connector J16

***Figure 4-34.*** ZigBee Connector J16

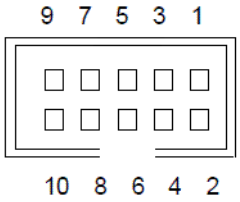



***Table 4-20.*** Connector J16 Signal Descriptions

| Function | Signal Name | Port | Pin | Pin | Port | Signal Name | Function | Option on Misc. Port Set by Zero Ohm Resistor or Solder Shunts |
|---|---|---|---|---|---|---|---|---|
| Reset | /RST | | 1 | 2 | | Misc. | | EEPROM for MAC address, CAP array settings and serial number<br>TST: test mode activation<br>CLKM: RF chip clock output |
| Interrupt Request | IRQ | | 3 | 4 | | SLP_TR | SLP_TR | |
| SPI chip select | /SEL | | 5 | 6 | | MOSI | SPI MOSI | |
| SPI MISO | MISO | | 7 | 8 | | SCLK | SPI CLK | |
| Power Supply | GND | GND | 9 | 10 | VCC | VCC | VCC | Voltage range: 1.8v to 5.5v, typically regulated to 3.3v |

### 4.5.12 PIO Expansion Port C Connector J12

***Figure 4-35.*** PIO Expansion Connector J12

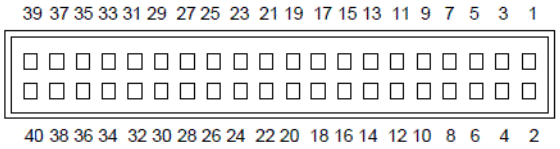



***Table 4-21.*** Connector J12 Signal Descriptions

| Pin | Mnemonic | Pin | Mnemonic |
|---|---|---|---|
| 1 | +5V or +3v3 | 2 | +5V or +3v3 |
| 3 | GND | 4 | GND |
| 5 | PC0 | 6 | PC16 |
| 7 | PC1 | 8 | PC17 |
| 9 | PC2 | 10 | PC18 |
| 11 | PC3 | 12 | PC19 |
| 13 | PC4 | 14 | PC20 |
| 15 | PC5 | 16 | PC21 |
| 17 | PC6 | 18 | NC |
| 19 | PC7 | 20 | NC |
| 21 | PC8 | 22 | NC |
| 23 | PC9 | 24 | NC |
| 25 | PC10 | 26 | NC |
| 27 | PC11 | 28 | NC |
| 29 | PC12 | 30 | NC |
| 31 | PC13 | 32 | NC |
| 33 | PC14 | 34 | NC |
| 35 | PC15 | 36 | NC |
| 37 | GND | 38 | GND |
| 39 | 3V3 | 40 | 3V3 |

### 4.5.13 PIO Expansion Port A Connector J13

***Figure 4-36.*** PIO Expansion Connector J13

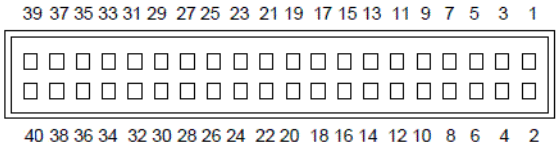



***Table 4-22.*** Connector J13 Signal Descriptions

| Pin | Mnemonic | Pin | Mnemonic |
|---|---|---|---|
| 1 | +5V or +3v3 | 2 | +5V or +3v3 |
| 3 | GND | 4 | GND |
| 5 | NC | 6 | PA16 |
| 7 | NC | 8 | PA17 |
| 9 | NC | 10 | PA18 |
| 11 | NC | 12 | PA19 |
| 13 | NC | 14 | PA20 |
| 15 | NC | 16 | PA21 |
| 17 | PA6 | 18 | PA22 |
| 19 | PA7 | 20 | PA23 |
| 21 | PA8 | 22 | PA24 |
| 23 | PA9 | 24 | PA25 |
| 25 | PA10 | 26 | PA26 |
| 27 | PA11 | 28 | PA27 |
| 29 | PA12 | 30 | PA28 |
| 31 | PA13 | 32 | PA29 |
| 33 | PA14 | 34 | PA30 |
| 35 | PA15 | 36 | PA31 |
| 37 | GND | 38 | GND |
| 39 | 3V3 | 40 | 3V3 |

# Section 5

# Schematics

## 5.1 Schematics

This section contains the following schematics:

- Block diagram
- General information
- Microcontroller
- NAND Flash, serial interface
- TFT LCD & Touch
- Audio & Power Supply
- USB, LEDs, push-buttons & ZigBEE

5 V Input
POWER SUPPLY
(3.3V)

MIC | AUDIO In (ADC)

PHONE JACK | AUDIO Out (DAC)

POT | ADC/ DAC

Sheet 6

POWER

PIO A, B, C

QTOUCH

LCD INTERFACE
2.8"
240x320
TFT

TOUCH SCREEN

Sheet 5

Board Configuration Sheet

Sheet 2

**ATMEL**
**Cortex-M4 ARM Processor**
**SAM4S (LQFP100)**

Sheet 3

PIO A, B, C

NAND F

HSMC

UART

USAR

USAR

ICE

Sheet 4

FS
DEVICE

ZIGBEE
INTERFA

LEDs, Bu

PIO A, B,
Extensio

Sheet 7

## REVISION HISTORY

| REV | DATA | NOTE |
|---|---|---|
| A | 2011.03 | ORIGINAL RELEASED |

## SCHEMATICS CONVENTIONS

| |
|---|
| (1) Resistance Unit: "K" is "Kohm", "R" is "Ohm? |
| (2) "nm" means the component is not populated by default |

## JUMPER and SOLDERDR

| PAGE | REFERENCE | DEFAULT | FU |
|---|---|---|---|
| 3 | JP1 | OPEN | Close |
| | JP2 | 1-2 | Analo |
| | JP3 | OPEN | Close |
| | JP4 | OPEN | Close |
| | JP5, JP6, JP7, JP8 | CLOSE | Acces |
| 4 | JP9 | CLOSE | Nand |
| | JP11 | CLOSE | RS485 |
| | JP10, JP12 | OPEN | RS485 |
| | JP31 | 1-2 | RS232 |
| 5 | JP13 | CLOSE | LCD |
| 6 | JP14, JP15 | OPEN | Sync |
| | JP17, JP19 | OPEN | Close |
| | JP16, JP21 | OPEN | Close |
| | JP18 | 1-2 | ADC i |
| | JP20 | OPEN | Close |
| | JP29 | 1-2 | AUDI |
| | JP30 | 1-2 | DAC |
| 7 | JP22, JP23, JP24 | 1-2 | DC vo |
| | JP25 | CLOSE | Button |
| | JP26 | CLOSE | Button |
| | JP27 | CLOSE | Powe |

## TABLE OF CONTENTS



## TEST POINT

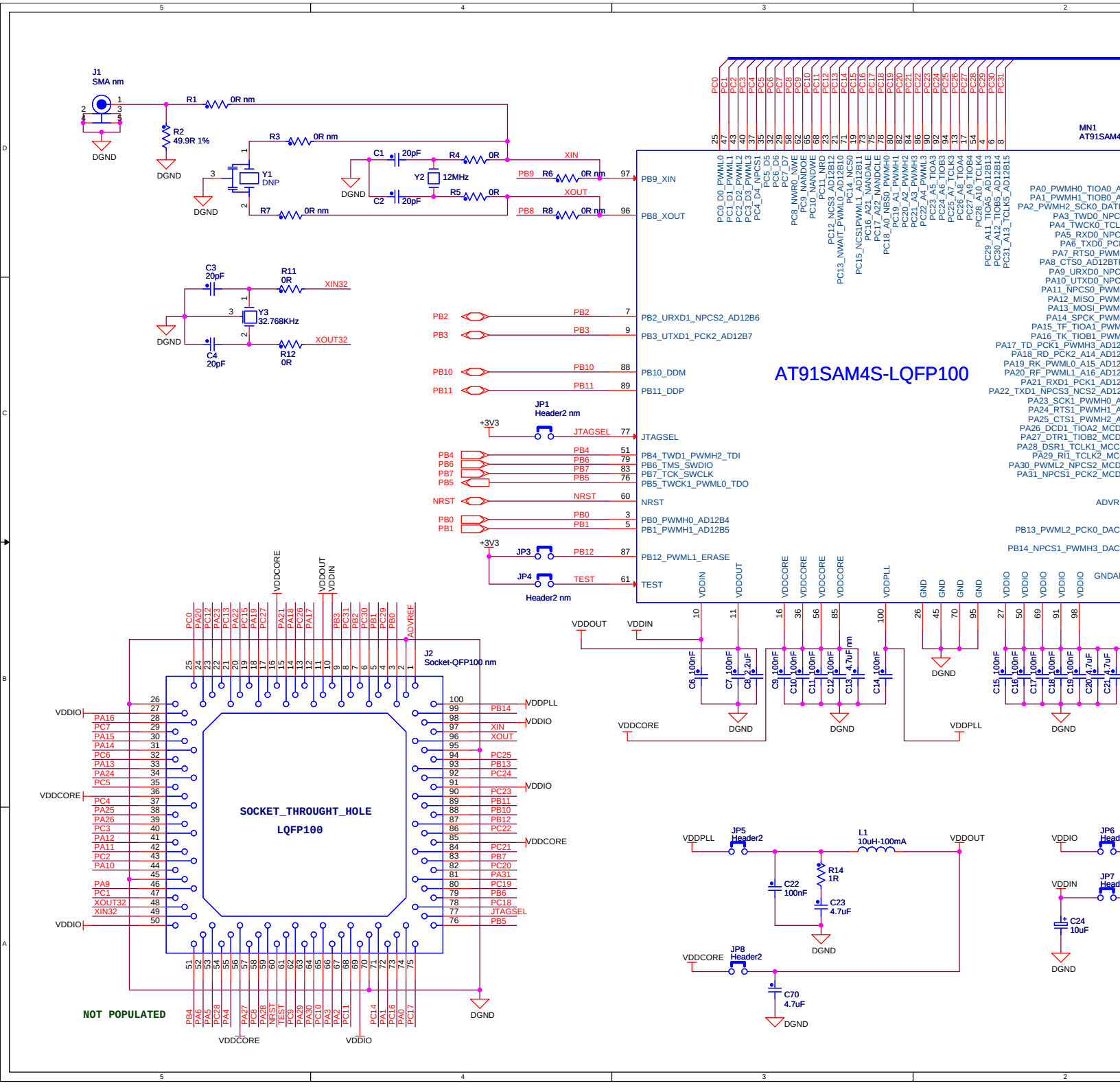
| PAGE | REFERENCE | FUNCTION |
|---|---|---|
| 3 | TP1, TP2, TP3, TP4 | GND |
| 4 | TP5 | UART TXD |
| | TP6 | UART RXD |
| 5 | TP7 | LCD backlight driver anode |
| | TP8, TP9 | Aux ADC input for TSC |
| 6 | TP12 | Optional audio PA input |

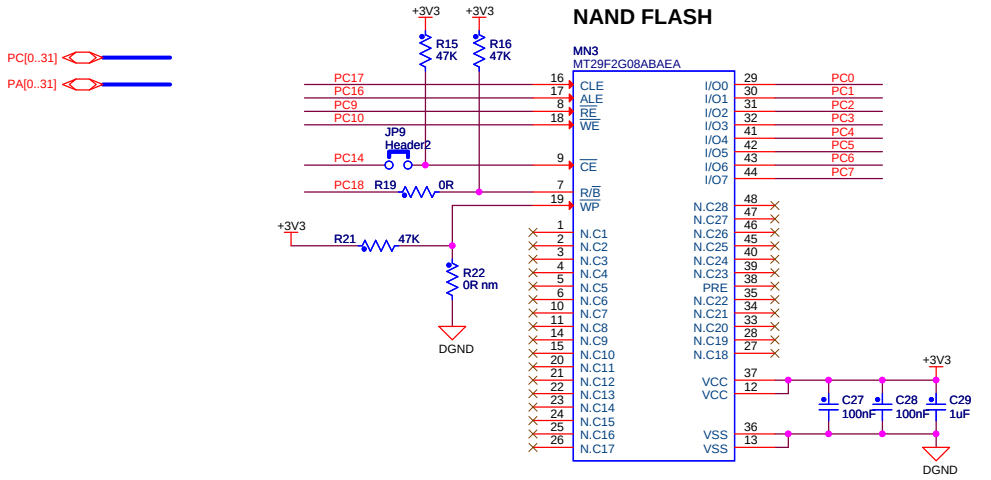
## PIO MUXING

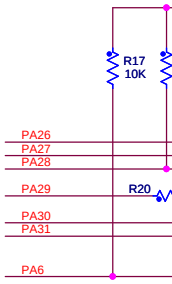
| PIOA | USAGE | PIOA | USAGE | PIOB | USAGE | PIOC | USAGE | PIOC | USAGE |
|---|---|---|---|---|---|---|---|---|---|
| PA0 | TSLIDR_SL_SNS | PA16 | TSC_IRQ/ZB_IRQ0 | PB0 | MIC INPUT | PC0 | D0 | PC16 | NAND_ALE |
| PA1 | TSLIDR_SL_SNSK | PA17 | TSC_BUSY/ZB_IRQ1 | PB1 | ANA INPUT | PC1 | D1 | PC17 | NAND_CLE |
| PA2 | TSLIDR_SM_SNS | PA18 | ZB_RSTN | PB2 | ZB_NPCS2 | PC2 | D2 | PC18 | NAND_RDYBSY |
| PA3 | TSLIDR_SM_SNSK | PA19 | LED_BLUE | PB3 | USER_PB1 | PC3 | D3 | PC19 | REGSEL_LCD |
| PA4 | TSLIDR_SR_SNS | PA20 | LED_GREEN | PB4 | JTAG | PC4 | D4 | PC20 | LED_RED(POWER) |
| PA5 | TSLIDR_SR_SNSK | PA21 | RXD1 | PB5 | JTAG | PC5 | D5 | PC21 | USB_CNX |
| PA6 | MCI_CD | PA22 | TXD1 | PB6 | JTAG | PC6 | D6 | PC22 | TVALID_SNS |
| PA7 | CLK_32K | PA23 | COM1EN | PB7 | JTAG | PC7 | D7 | PC23 | TVALID_SNSK |
| PA8 | CLK_32K | PA24 | RTS1 | PB8 | CLK_12M | PC8 | WR_LCD | PC24 | TUP_SNS |
| PA9 | RX_UART0 | PA25 | CTS1 | PB9 | CLK_12M | PC9 | NAND_OE | PC25 | TUP_SNSK |
| PA10 | TX_UART0 | PA26 | MCI | PB10 | USB_DDM | PC10 | NAND_WE | PC26 | TDWN_SNS |
| PA11 | TSC_CS | PA27 | MCI | PB11 | USB_DDP | PC11 | RD_LCD | PC27 | TDWN_SNSK |
| PA12 | MISO | PA28 | MCI | PB12 | ERASE | PC12 | USER_PB2 | PC28 | TLEFT_SNS |
| PA13 | MOSI | PA29 | MCI | PB13 | AUDIO OUT R | PC13 | EN_LCD | PC29 | TLEFT_SNSK |
| PA14 | SPCK | PA30 | MCI | PB14 | AUDIO OUT L | PC14 | NAND_NCS0 | PC30 | TRIGHT_SNS |
| PA15 | ZB_SLPTR | PA31 | MCI | | | PC15 | NSC1_LCD | PC31 | TRIGHT_SNSK |

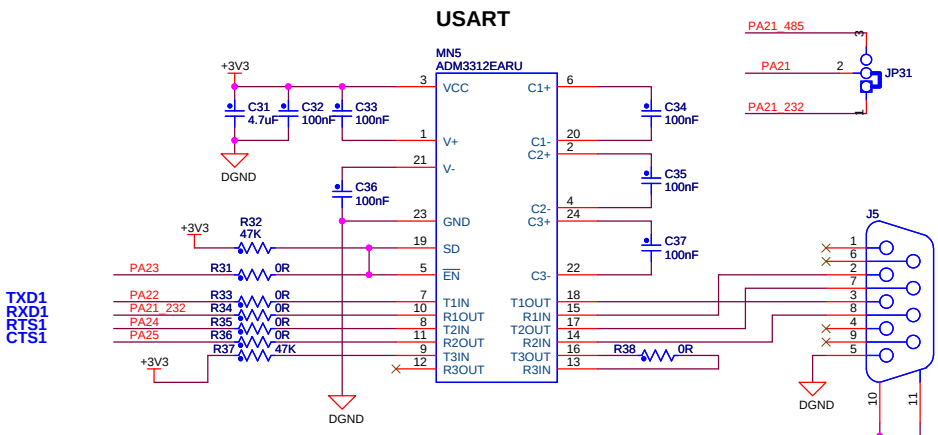
## DEFAULT NO PO

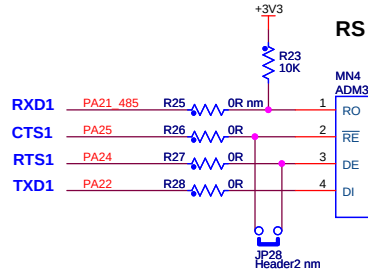
| PAGE | REFERENCE |
|---|---|
| 3 | J1, R1 |
| | Y1, R3, R7 |
| | R6, R8 |
| | R9, R10 |
| 4 | R22 |
| | R24, R30 |
| | R25 |
| 5 | D1 |
| | R61, R62, RA2, RA3 |

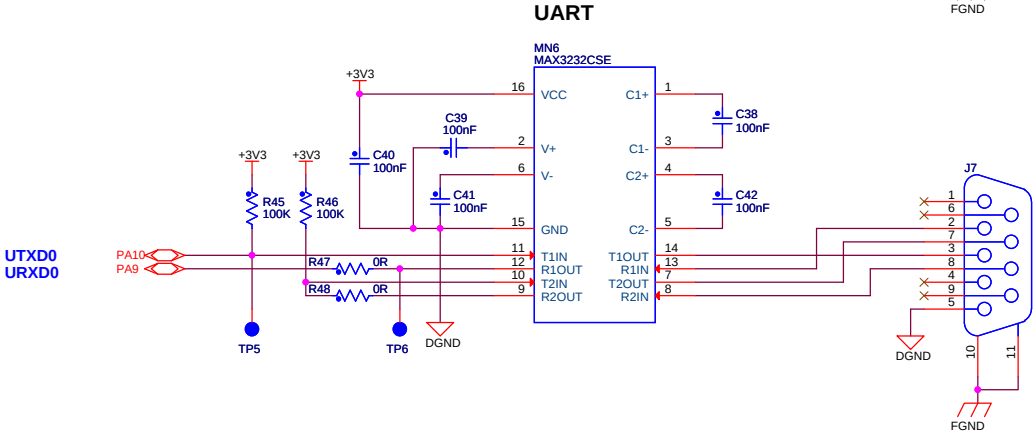

AT91SAM4S-LQFP100
SOCKET_THROUGHT_HOLE
LQFP100
NOT POPULATED
J1
SMA nm
J2
Socket-QFP100 nm
Y1
DNP
Y2
12MHz
Y3
32.768KHz
JP1
Header2 nm
JP3
JP4
JP5
Header2
JP6
JP7
JP8
Header2
L1
10uH-100mA
MN1
AT91SAM4
DGND
VDDCORE
VDDIO
VDDPLL
VDDOUT
VDDIN
XIN
XOUT
XIN32
XOUT32
NRST
JTAGSEL
TEST
ADVR

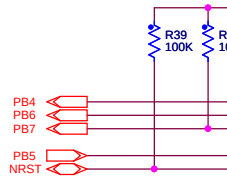

NAND FLASH
MN3
MT29F2G08ABAEA
PC[0..31]
PA[0..31]
+3V3
R15 47K
R16 47K
JP9 Header2
R19 0R
R21 47K
R22 0R nm
DGND
C27 100nF
C28 100nF
C29 1uF

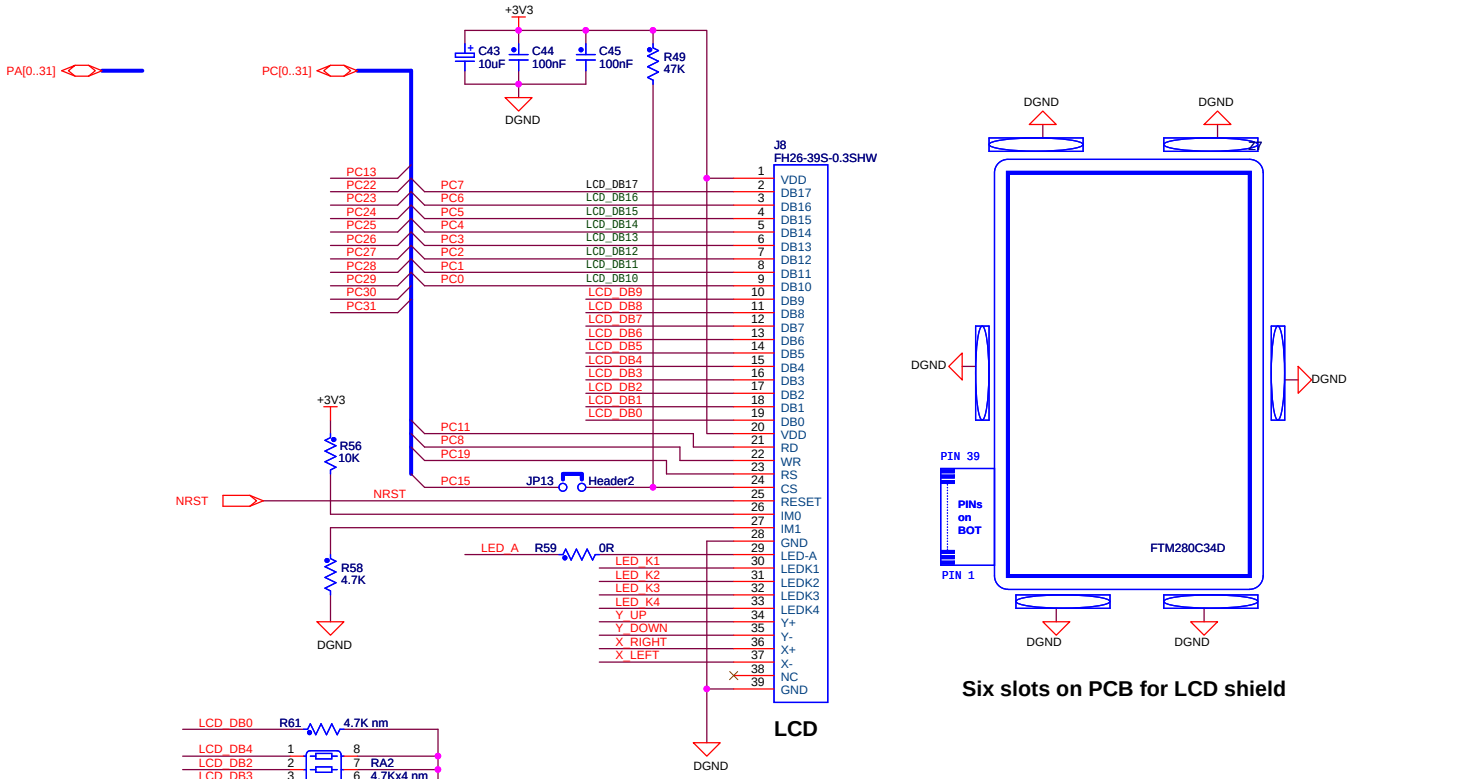

R17 10K
R20
PA26
PA27
PA28
PA29
PA30
PA31
PA6

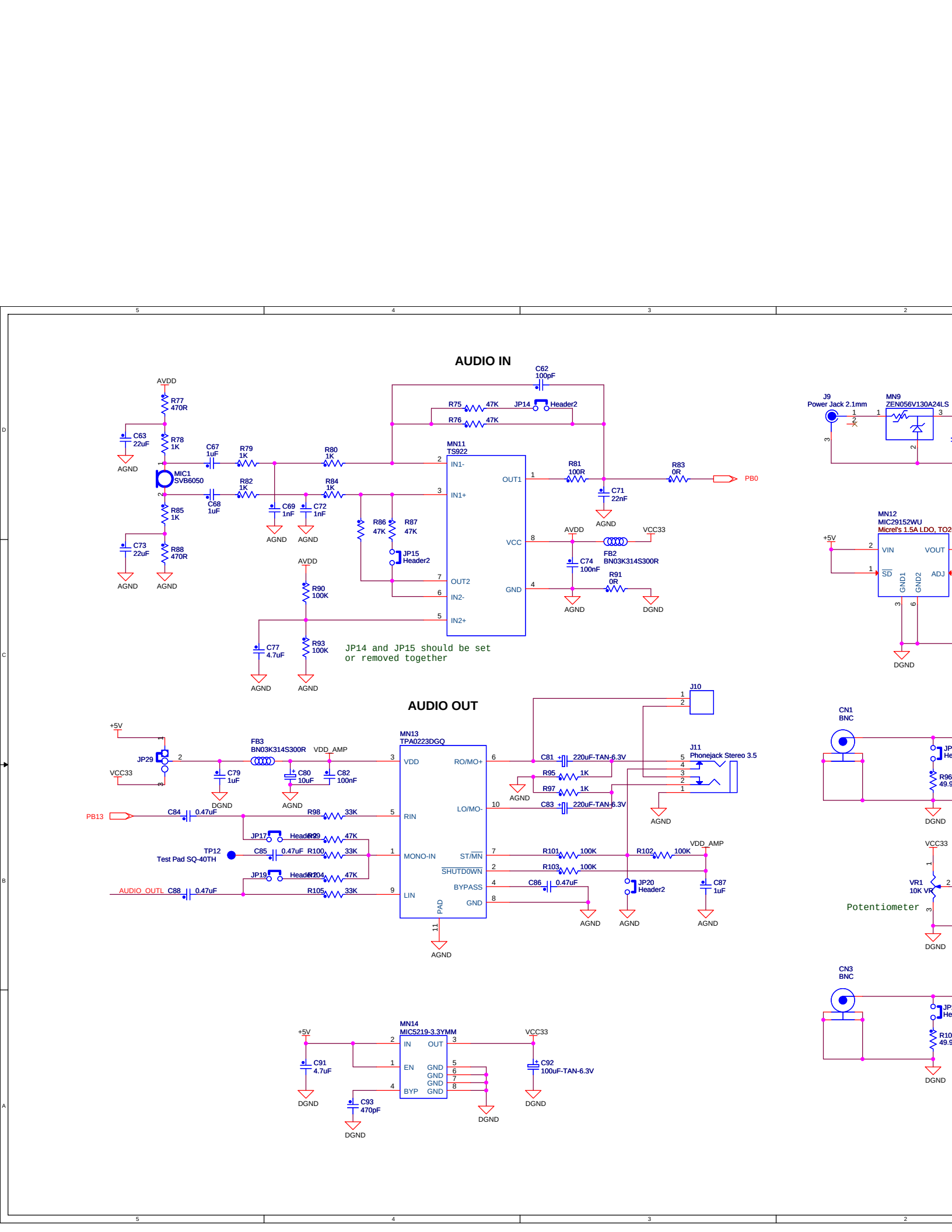

USART
MN5
ADM3312EARU
C31 4.7uF
C32 100nF
C33 100nF
C34 100nF
C35 100nF
C36 100nF
C37 100nF
R32 47K
R31 0R
R33 0R
R34 0R
R35 0R
R36 0R
R37 47K
R38 0R
PA21_485
PA21
PA21_232
JP31
J5
TXD1
RXD1
RTS1
CTS1
DGND
FGND

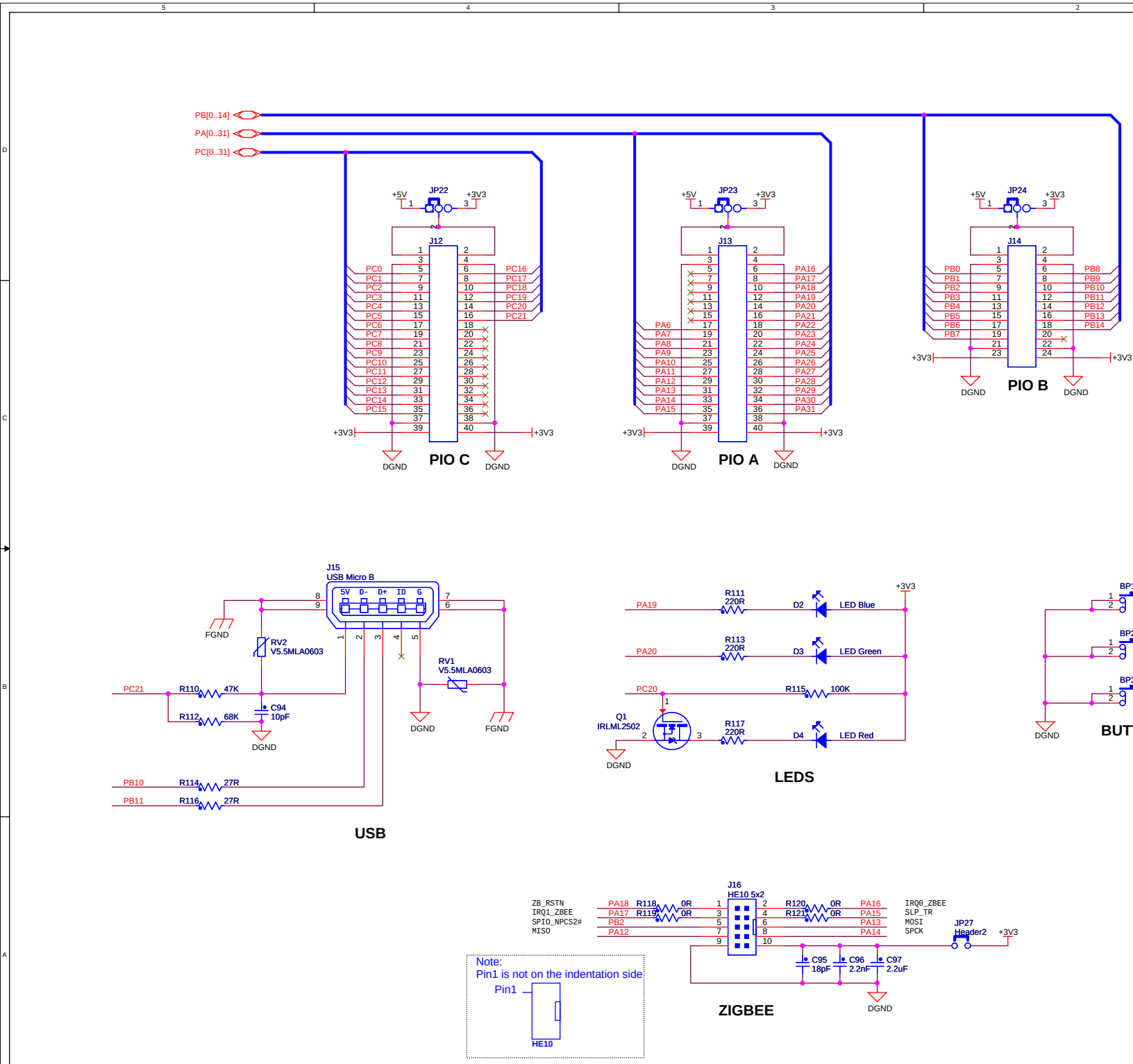

RS
MN4
ADM3
R23 10K
RXD1
CTS1
RTS1
TXD1
PA21_485
PA25
PA24
PA22
R25 0R nm
R26 0R
R27 0R
R28 0R
RO
RE
DE
DI
JP28 Header2 nm


UART
MN6
MAX3232CSE
C38 100nF
C39 100nF
C40 100nF
C41 100nF
C42 100nF
R45 100K
R46 100K
R47 0R
R48 0R
UTXD0
URXD0
PA10
PA9
TP5
TP6
J7
DGND
FGND


R39 100K
PB4
PB6
PB7
PB5
NRST


+3V3
C43 10uF
C44 100nF
C45 100nF
R49 47K
DGND
PA[0..31]
PC[0..31]
J8
FH26-39S-0.3SHW
VDD
DB17
DB16
DB15
DB14
DB13
DB12
DB11
DB10
DB9
DB8
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
VDD
RD
WR
RS
CS
RESET
IM0
IM1
GND
LED-A
LEDK1
LEDK2
LEDK3
LEDK4
Y+
Y-
X+
X-
NC
GND
LCD_DB17
LCD_DB16
LCD_DB15
LCD_DB14
LCD_DB13
LCD_DB12
LCD_DB11
LCD_DB10
LCD_DB9
LCD_DB8
LCD_DB7
LCD_DB6
LCD_DB5
LCD_DB4
LCD_DB3
LCD_DB2
LCD_DB1
LCD_DB0
PC13
PC22
PC23
PC24
PC25
PC26
PC27
PC28
PC29
PC30
PC31
PC7
PC6
PC5
PC4
PC3
PC2
PC1
PC0
PC11
PC8
PC19
PC15
JP13
Header2
NRST
R56 10K
R58 4.7K
LED_A
R59
0R
LED_K1
LED_K2
LED_K3
LED_K4
Y_UP
Y_DOWN
X_RIGHT
X_LEFT
LCD
LCD_DB0
R61
4.7K nm
RA2
4.7Kx4 nm
RA3
4.7Kx4 nm
R63
4.7K nm
X_RIGHT
Y_UP
X_LEFT
Y_DOWN
D1
PACDN044Y5R nm
TVS, SOT23-5
NOT POPULATED
The part is placed as close as possible to J8
DGND
DGND
DGND
DGND
DGND
DGND
DGND
PIN 39
PINs on BOT
PIN 1
FTM280C34D
Six slots on PCB for LCD shield
PC25
PC24
PC31
PC30
PC29
PC28
PC23
PC22
PC27
PC26
MN7
ADS7843E
XP
YP
XM
YM
DCLK
DIN
DOUT
CS
BUSY
PENIRQ
VREF
VCC1
VCC2
IN3
IN4
GND
PA14
PA13
PA12
PA11
PA17
PA16
R62 100K
R65 100K
R66 0R
R67 0R
R69 0R
R70 0R
L2 10uH-100mA
R71 1R
R74 0R
C58 100nF
C59 100nF
C60 100nF
C61 4.7uF
TP8
TP9
R72 100K
R73 100K
AGND_TP
AGND_TP
LCD TOUCH SCREEN
MN8
AAT3155ITP-T1
C1+
C1-
EN/SET
IN
GND
C2+
C2-
OUTCP
D1
D2
D3
D4
R64 47K
R68 0R
FB1
BN03K314S300R
C54 1uF
C55 1uF
C56 1uF
C57 4.7uF
LED_A
LED_K1
LED_K2
LED_K3
LED_K4
TP7
LCD BACKLIGHT


AUDIO IN
AVDD
R77 470R
C63 22uF
AGND
R78 1K
MIC1 SVB6050
C67 1uF
R79 1K
R80 1K
C62 100pF
R75 47K
JP14 Header2
R76 47K
MN11 TS922
IN1-
IN1+
OUT1
R81 100R
R83 0R
PB0
C71 22nF
R82 1K
R84 1K
C68 1uF
C69 1nF
C72 1nF
R85 1K
R88 470R
C73 22uF
R86 47K
R87 47K
JP15 Header2
VCC
GND
OUT2
IN2-
IN2+
C74 100nF
FB2 BN03K314S300R
VCC33
R91 0R
DGND
R90 100K
R93 100K
C77 4.7uF
JP14 and JP15 should be set
or removed together
AUDIO OUT
+5V
JP29
VCC33
FB3 BN03K314S300R
VDD_AMP
C79 1uF
C80 10uF
C82 100nF
MN13 TPA0223DGQ
VDD
RO/MO+
LO/MO-
RIN
MONO-IN
ST/MN
SHUTDOWN
BYPASS
LIN
GND
PAD
J10
J11 Phonejack Stereo 3.5
C81 220uF-TAN-6.3V
C83 220uF-TAN-6.3V
R95 1K
R97 1K
PB13
C84 0.47uF
R98 33K
JP17 Header2
R99 47K
TP12 Test Pad SQ-40TH
C85 0.47uF
R100 33K
JP19 Header2
R104 47K
AUDIO_OUTL
C88 0.47uF
R105 33K
R101 100K
R102 100K
R103 100K
C86 0.47uF
JP20 Header2
C87 1uF
MN14 MIC5219-3.3YMM
IN
OUT
EN
BYP
C91 4.7uF
C93 470pF
C92 100uF-TAN-6.3V
J9 Power Jack 2.1mm
MN9 ZEN056V130A24LS
MN12 MIC29152WU Micrel's 1.5A LDO, TO2
VIN
VOUT
SD
GND1
GND2
ADJ
CN1 BNC
CN3 BNC
VR1 10K VR
Potentiometer


PB[0..14]
PA[0..31]
PC[0..31]
JP22
JP23
JP24
J12
J13
J14
PIO C
PIO A
PIO B
+5V
+3V3
DGND
J15
USB Micro B
5V D- D+ ID G
FGND
RV2
V5.5MLA0603
RV1
V5.5MLA0603
PC21
R110 47K
R112 68K
C94 10pF
PB10 R114 27R
PB11 R116 27R
USB
PA19 R111 220R D2 LED Blue
PA20 R113 220R D3 LED Green
PC20 R115 100K
Q1 IRLML2502
R117 220R D4 LED Red
LEDS
BUT
J16
HE10 5x2
ZB_RSTN
IRQ1_ZBEE
SPI0_NPCS2#
MISO
PA18 R118 0R
PA17 R119 0R
PB2
PA12
R120 0R PA16
R121 0R PA15
PA13
PA14
IRQ0_ZBEE
SLP_TR
MOSI
SPCK
JP27 Header2
C95 18pF
C96 2.2nF
C97 2.2uF
ZIGBEE
Note:
Pin1 is not on the indentation side
Pin1
HE10

# Section 6

# Troubleshooting

## 6.1 Board Recovery

Closing JP3 and powering the board will assert ERASE and clear GPNVM bit 1, and thereby selects the boot from the ROM by default. The MCU will boot from the internal ROM to enable a SAM-BA connection through the UART. Connect the SAM4S-EK UART port (J3) to a PC COM port through an RS232 cross-over cable.

You can then run the SAM-BA application from that PC to program the internal Flash of the MCU as well as the GPNVM bit 1.

# Section 7

# Revision History

## 7.1 Revision History

*Table 7-1.*

| Document | Comments | Change Request Ref. |
|---|---|---|
| 11139A | Initial version. | |

## Headquarters

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